

June 23, 1964

G. F. DULIN

3,138,778

ELECTRONIC ACOUSTIC RECEIVER

Filed Feb. 15, 1962

3 Sheets-Sheet 1

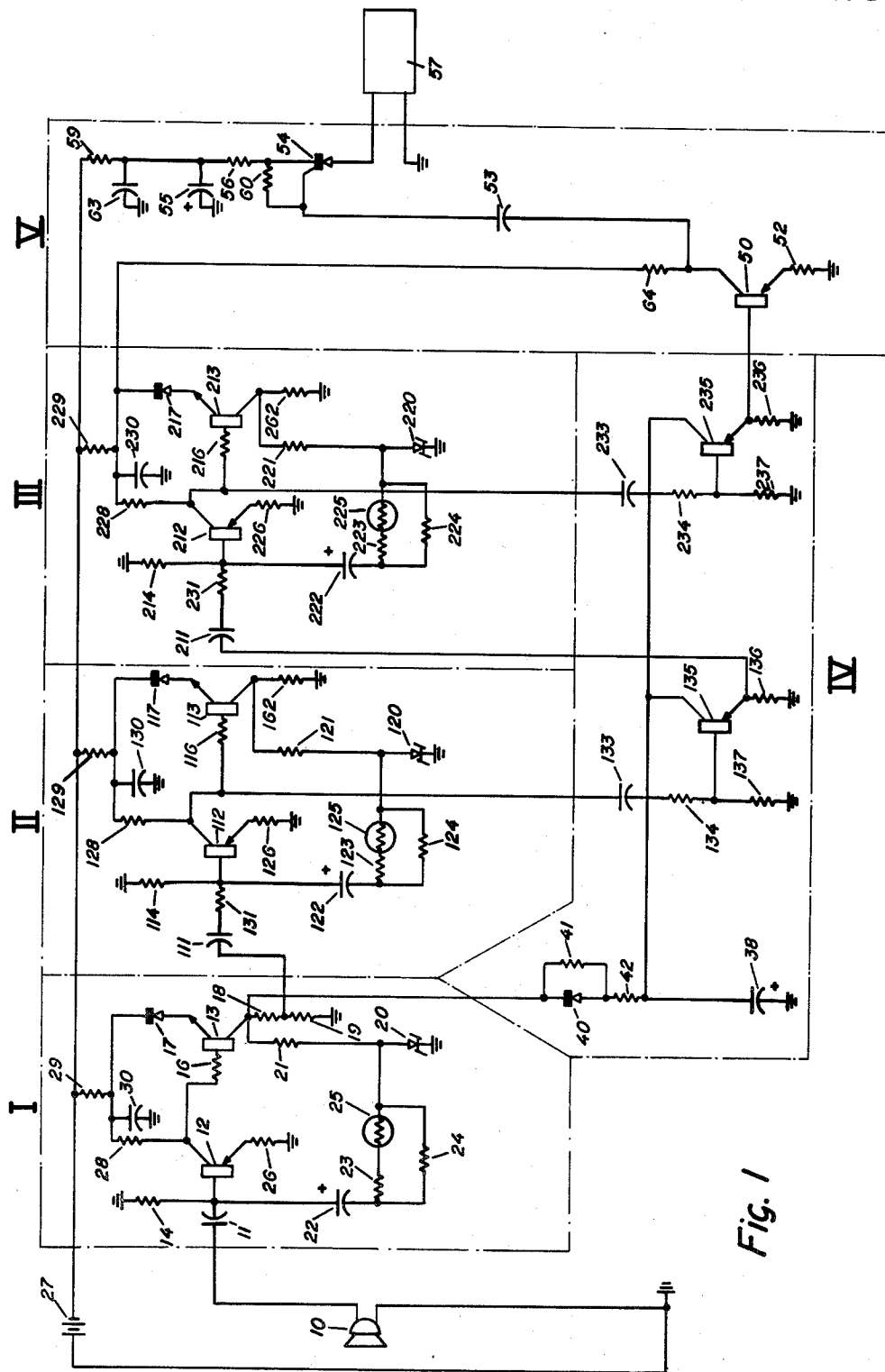


Fig. 1

June 23, 1964

G. F. DULIN

3,138,778

ELECTRONIC ACOUSTIC RECEIVER

Filed Feb. 15, 1962

3 Sheets-Sheet 2

Fig. 2

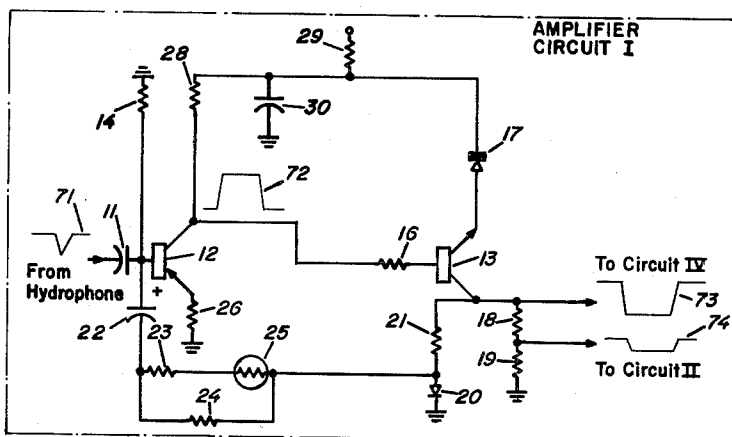


Fig. 3

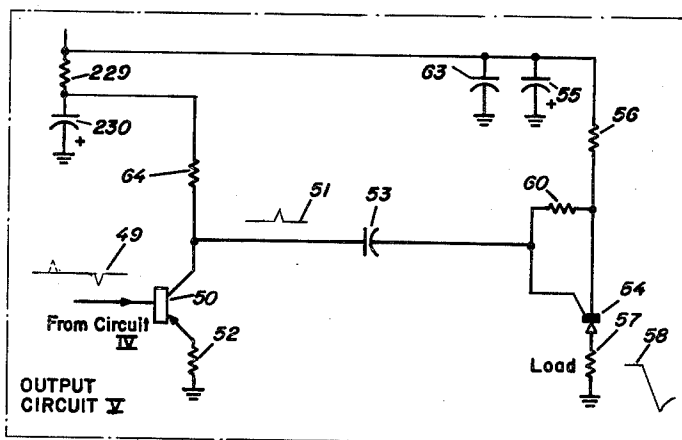
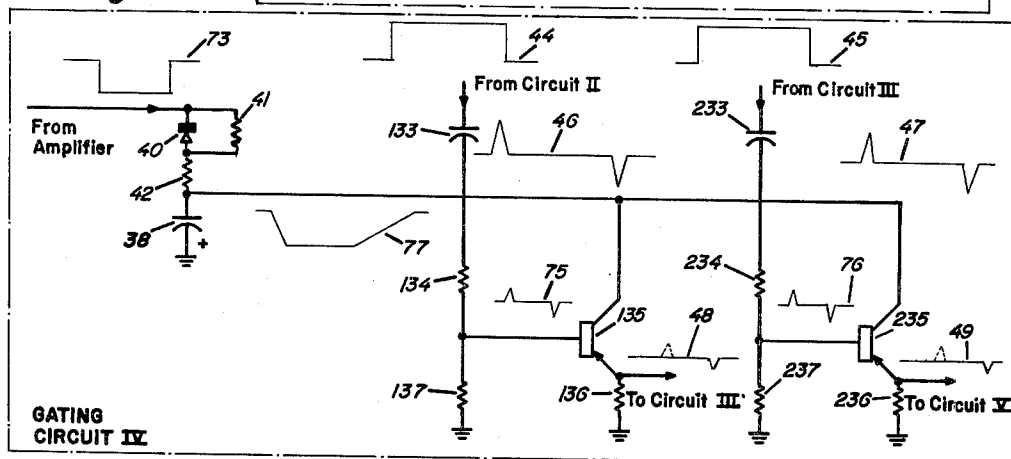


Fig. 4

June 23, 1964

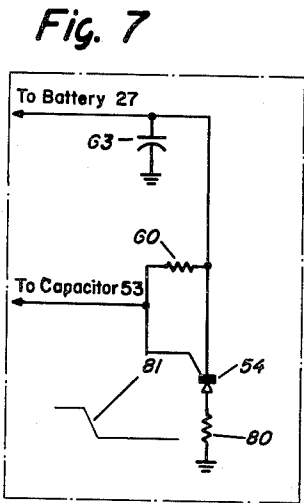
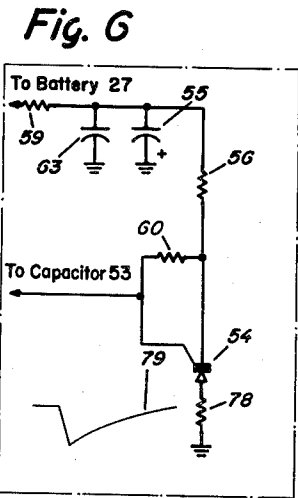
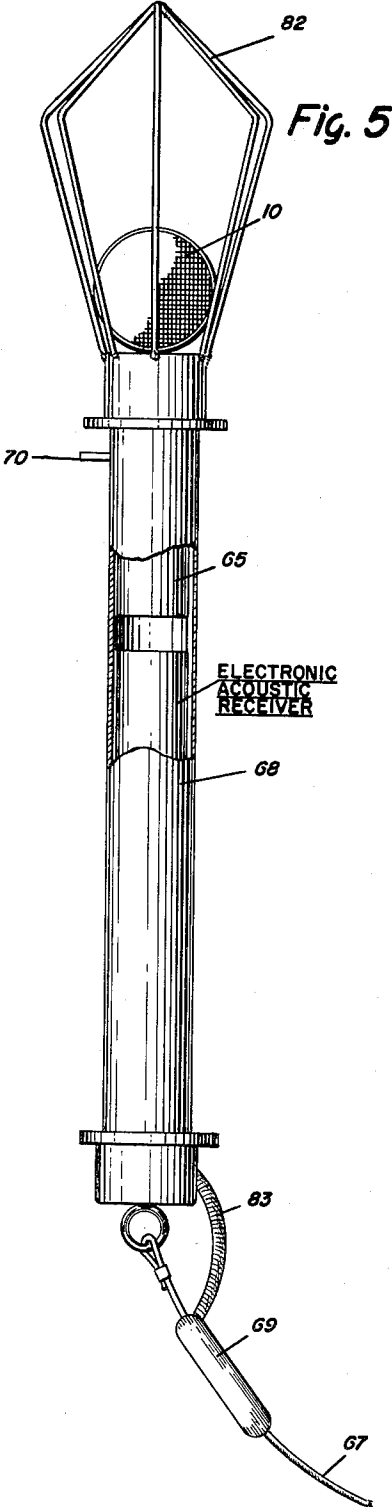
G. F. DULIN

3,138,778

ELECTRONIC ACOUSTIC RECEIVER

Filed Feb. 15, 1962

3 Sheets-Sheet 3



1

3,138,778

ELECTRONIC ACOUSTIC RECEIVER

Gerald F. Dulin, Palos Verdes Estates, Calif., assignor to Sea-Space Systems, Inc., a corporation of California
Filed Feb. 15, 1962, Ser. No. 173,550
5 Claims. (Cl. 340-15)

This invention relates generally to an acoustically actuated device and more specifically to an electronic acoustic receiver which receives time-coded sequential signals and which, upon determining that the received signals are properly coded, will detonate an explosive, start a motor, close a relay, turn on a radio transmitter, operate a valve or perform some other useful function.

This invention has been developed in response to a need for a remote-control actuation device which can be placed in an isolated location, such as in the depths of the open sea, and which upon receipt of an appropriately coded acoustic signal will generate an actuation impulse for operating an electrical load device. The receiver is thereby rendered capable of controlling multifarious mechanical or electrical operations in response to coded signals from a remote location. Obviously, such a device must be capable of rejecting spurious signals and must operate with a minimum amount of maintenance and maximum reliability.

It is therefore a primary object of this invention to provide an acoustic receiver for actuating a load device in response to acoustic signals, but only in response to such acoustic signals as are properly coded.

A further object of this invention is to provide an acoustic receiver which includes an amplifier circuit, a gating circuit, one or more time-delay circuits and means for providing an output pulse of an accurate, predetermined time duration for operating a load device.

An additional object of this invention is to provide an electronic acoustic receiver which includes an automatic lockout for preventing the reception of spuriously coded acoustic signals and for preventing reverberation pulses from falsely triggering the amplifier.

Another object of this invention is to provide an acoustic receiver which includes a dynamic signal regulating and standardizing unit for decreasing the current demand of the receiver and for maintaining the accurate timing of the amplifier even after the amplifier power supply, such as a galvanic battery, has suffered a decrease in potential from continued use. Thus the acoustic receiver equipped with this signal regulating and standardizing unit will be capable of operating over a greater period of time from a battery power-pack than it would be able to do if not so equipped.

It is a further object of this invention to provide a new and improved electronic acoustic receiver of simple and inexpensive construction for expendable use in activities such as the detonation of explosives under water.

The electronic acoustic receiver of the present invention is broadly speaking, an acoustically actuated device which includes an acoustic transducer to receive input acoustic signals and to provide an electric signal pulse representative thereof to an amplifier circuit. The amplifier circuit contains an automatic lockout for preventing the receipt of additional electric signal pulses during the amplification of the pulse already received and for a specified time thereafter. The amplifier circuit is connected to a gating circuit and to a time-delay circuit, both of which circuits receive the amplified pulse from the amplifier. The time-delay circuit contains means for prolonging the amplifier pulse at least until the end of said specific time whereupon said automatic lockout becomes temporarily inoperative and said prolonged pulse expires, resulting in a potential change in the time-delay circuit.

2

The gate circuit, which is connected to the time-delay circuit, contains a time-delay gate which opens momentarily in response to the expiration of said prolonged pulse. If an additional acoustic signal is received while the time-delay gate is open, it will be converted to an electric signal pulse by the transducer and be passed therefrom to the amplifier, from thence to the gating circuit and through the open time-delay gate. Connected to the time-delay gate is an output circuit for triggering the operation of a load device. The output circuit receives the electric signal pulse transmitted thereto through the open gate and energizes the load device.

The above-described receiver is capable of rejecting spurious acoustic signals so that the load device will be operated only when signals are received in the proper time sequence or code. For instance, in the event that a first acoustic signal is followed too quickly by a second acoustic signal, the receiver will not operate the load device in response thereto, because the automatic lockout will prevent the entry of the second signal into the amplifier. On the other hand if the second signal comes after the momentary opening and closing of the aforesaid time-delay gate operated by the expiration of the prolonged first pulse in the time-delay circuit, the receiver will again not operate the load device. If the gate has closed already, the second pulse cannot pass through it to energize the output circuit and load device. Thus it will be observed that unless the second pulse follows the first in the proper time sequence, the load device will remain inoperative.

In the basic receiver described above, there is an amplifier circuit and a single time-delay circuit operable to energize a load device in response to two properly timed acoustic signals. The timing feature allows the receiver to discriminate between spurious and authentic signals. In military applications of the receiver, the timing feature makes it more difficult for enemy agents to successfully operate the load device by creating random acoustic signals in the area where the receiver is located. Discrimination is made even more certain by utilizing one or more additional time-delay circuits in conjunction with the basic receiver described above. For instance, if one additional time-delay circuit were added to the basic receiver described above between the second time-delay circuit and the output circuit, a receiver would be obtained in which three properly timed acoustic signals would be needed to trigger the load device. In fact, such an arrangement is preferred by the inventor and it will therefore be described in detail as the preferred specific embodiment of the invention.

The load device may be almost any device susceptible to electrical control and/or actuation. For instance, the load device might be a relay, a blasting cap for opening a destructible link, a solenoid, an electric fuse for detonating explosives, a solenoid valve, a motor, a sonar pinging device, a radio transmitter, or the fusing arrangement of a solid propellant operated gas generator, to name a few of the many possibilities. Thus the term "load device" as used herein should be interpreted as broadly as the scope of the objects will permit.

Those who are skilled in the art will obtain sufficient understanding of how to make and use the invention by reading the following description in connection with the accompanying drawings in which:

FIGURE 1 is a schematic diagram of the invention showing the acoustic transducer, the combined circuit diagrams of FIGURES 2, 3 and 4, the battery power supply and the time-delay circuits, all of which taken together constitute a specific embodiment of the subject invention. This figure includes dash lines dividing and

identifying the sub-divisions of the over-all receiver circuit:

- I.—the amplifier circuit
- II.—the first time-delay circuit
- III.—the second time-delay circuit
- IV.—the gating circuit
- V.—the output circuit;

FIGURE 2 is a detailed schematic diagram of the amplifier circuit I, including symbolical representations of the pulses generated therein during the operation of the receiver;

FIGURE 3 is a detailed schematic diagram showing the gating circuit IV and symbolical representations of the pulses it receives and generates;

FIGURE 4 is a detailed schematic diagram of the output circuit V including symbolical representations of the pulses received by and generated in circuit V when properly coded signals have passed thereto through circuits I, II, III and IV;

FIGURE 5 is a partial section of a recoverable deep-sea temperature measuring and recording device employing the subject electronic acoustic receiver;

FIGURE 6 is a detailed schematic diagram of a portion of the output circuit, showing how the circuit can be modified so that it will reset itself and operate repeatedly;

FIGURE 7 is similar to FIGURE 6 and shows still another modification of the output circuit.

Amplifier circuit I will now be explained with reference to FIGURES 1 and 2 of the drawings, in which an acoustic transducer is shown figuratively in FIGURE 1 as a hydrophone 10 and is shown symbolically in FIGURE 2 as an input pulse wave form 71. Hydrophone 10 is located underwater. Its output is connected to the base of a p-n-p transistor 12 through a capacitor 11. The other hydrophone lead is grounded and connected to one side of the galvanic battery power supply 27. Capacitor 11 and the input impedance of transistor 12 constitute a high-pass filter for rejecting undesirable ambient noise from the hydrophone 10, noise which would otherwise gain admission to circuit I and interfere with its operation.

The transistor 12 and its companion n-p-n transistor 13 constitute a pair of complementary transistor stages. Transistor 12 is the first transistor stage. Its base is connected to ground through resistor 14. Its emitter is also grounded through resistor 26. The collector of p-n-p transistor 12 is coupled with the base of n-p-n transistor 13, the second transistor stage, through a resistor 16. The value of resistor 16 is selected to limit the current entering the base of transistor 13 to approximately 300 microamperes. The first-stage collector is also connected to the power supply 27 through a resistor 28 and a decoupling network including resistor 29 and capacitor 30. Battery 27 has an operating potential of -16 volts when new. The decoupling network prevents interaction between circuit I and other parts of the receiver as will become apparent from further reading.

Also connected to battery 27 through the same decoupling network mentioned above is a crystal diode 17. Diode 17 is also connected to the emitter of transistor 13. Its presence in the circuit will necessitate the generation of a higher potential in the circuit before transistor 13 will turn on. Therefore, the immunity of the amplifier from false triggering by extraneous noise pulses is enhanced. Furthermore, the diode 17 has an abrupt turn-on point. As a result, the timing of the operation of transistor 13 is rendered more accurate than it would be if diode 17 were omitted.

The collector of the second transistor stage, transistor 13, is connected to ground through resistors 18 and 19. These resistors constitute both the collector load of transistor 13 and a potential divider for the output from circuit I to circuit II. The resistors have a current dividing ratio of approximately 10 to 1, resistor 18 having the

larger value of the two. The output of circuit I to circuit II is taken from a point between resistors 18 and 19.

The collector of transistor 13 is in a positive feedback loop which contains capacitor 22 which constitutes an automatic lockout for preventing reverberation pulses from falsely triggering the amplifier and for closing the amplifier input to spuriously coded signals in which the signals are too close together in point of time. This loop interconnects the collector of transistor 13 with the base of transistor 12. In this portion of the loop are a resistor 21 and a resistor/thermistor network for controlling the discharge of capacitor 22. The network includes resistor 23, thermistor 25, and resistor 24. Thermistor 25 varies the charge time of capacitor in accordance with temperature. Therefore the network and the receiver may acclimate themselves to a broad range of temperature conditions.

Connected to the above-mentioned feedback loop, between resistor 21 and the resistor/thermistor network, is the Zener diode 20, which is grounded. Zener diode 20 serves as a dynamic signal regulating and standardizing unit for maintaining the accuracy of the output of transistor 13 to the feedback loop. The value of the resistor 21 is selected with special reference to the operating characteristics of Zener diode 20. The object of the selection is to cause Zener 20 to operate on the flattest portion of its E vs. I curve under those conditions which can be expected from the nature of the operating environment and power supply. This will result in the maintenance of a standardized output across the Zener regulator 20 which is not affected by the gradual deterioration of the battery 27 through continued use and consequent variation in the amplitude of the output pulses of the collector of transistor 13.

Finally, the collector of transistor 13 is also connected to the gate circuit IV. Thus the output of transistor 13 is divided between the feedback loop, the first time-delay circuit II and gate circuit IV.

From the above description, it should be apparent that amplifier circuit I is essentially a D.C.-coupled single-ended, saturating, asymmetrical, two-stage complementary transistor amplifier in which the transistors are normally biased to cut off (Class B), but in which the output of the second-stage transistor is returned to the input of the first transistor as a heavy positive feedback to enable the amplifier to produce a high-amplitude output pulse of long duration during regeneration. Not only will this amplifier amplify the input signal, but it will also serve the purpose of providing an output pulse of accurate time duration. It has an automatic lockout to prevent reverberation pulses from falsely triggering the receiver. In short, the amplifier circuit I may be characterized as a complementary, saturating amplifier with automatic lockout.

Time-delay circuits are provided to complete the circuitry needed for detecting properly coded signals. Time-delay circuits II and III, being the first and second time-delay circuits respectively, share many features in common with amplifier circuit I. In circuits II and III, the parts 111, 112, 113, 114, 116, 117, 120, 121, 122, 123, 124, 125, 126, 128, 129, and 130, as well as 211, 212, 213, 214, 216, 217, 220, 221, 222, 223, 224, 225, 226, 228, 229 and 230 respectively correspond in nature and function with parts 11, 12, 13, 14, 16, 17, 20, 21, 22, 23, 24, 25, 26, 28, 29 and 30 in circuit I, except as hereinafter distinguished.

Unlike circuit I, circuit II does not have its input connected to the hydrophone. Instead the input of circuit II is connected to the collector of transistor 13 in circuit I. Unlike either circuit I or circuit II, circuit III receives its input from gating circuit IV where it is connected to gate transistor 135 as will be more fully explained below. The outputs of circuits II and III are taken not from the collectors of their second transistor stages 113 and 213 as is the case in circuit I. Instead the outputs of

5

circuits II and III are both taken from the collectors of their first transistor stages 112 and 212. In circuits II and III, no potential divider network is needed or supplied. In lieu of resistors similar to resistors 18 and 19, in lieu of the output connection of circuit I located therein between resistors 18 and 19, and in lieu of the connection in circuit I between the collector of transistor 13 and the gating circuit IV, circuits II and III are provided with identical resistors 162 and 262 which connect the collectors of transistors 113 and 213 to ground. Furthermore, each of the circuits II and III are provided with identical resistors 131 and 231. They are means for isolating each delay circuit from its input circuit to the extent necessary to minimize undesirable interaction therebetween. Except for the above differences, the components and wiring of circuits I, II and III are identical. The difference in their function will be made clear in the description of their operation which follows the explanation of the gating and output circuits below.

The gate circuit IV will now be explained in detail with reference to FIGURES 1 and 3. The gate circuit includes a gate pulse capacitor 38. Capacitor 38 is connected to the collector of transistor 13. The flow path between the collector and capacitor includes crystal diode 40 across which the resistor 41 is wired in shunt. The flow path also includes a resistor 42 which is wired in series between diode 40 and gate pulse capacitor 38. The same side of the capacitor 38 which is connected to resistor 42 is also connected to the collectors of p-n-p gate transistors 135 and 235. The opposite side of capacitor 38 is grounded.

Gate pulse capacitor 38 constitutes a means for stretching an output pulse generated in circuit I. It also constitutes a means for prolonging the "pass" gate for gate transistors 135 and 235. Furthermore it serves as a power supply for the aforementioned transistors. The ability of capacitor 38 to perform these functions is a result of the arrangement of circuitry elements 40, 41 and 42 which will now be more fully explained. Because of the manner in which diode 40 is associated with the collector of transistor 13 and with capacitor 38, it is capable of passing current between them in one direction only. That direction is towards capacitor 38. Therefore, this capacitor has only three discharge paths. It may discharge through either or both of the gate transistors 135 and 235 if they happen to be in a conductive state when capacitor 38 discharges; and it may discharge through resistor 41 which is wired in shunt with diode 40. However, a high ohmic value is purposely selected for resistor 41, so that the major portion of the discharge current from the capacitor will pass through the collector-emitter flow paths of transistors 135 and 235, provided they are conducting. Otherwise, resistor 41 is the only discharge path available to this capacitor.

The gate transistors 135 and 235 constitute the principal components in a first time-delay gate and a second time-delay gate. The first time-delay gate includes a capacitor 133, resistors 134, 136 and 137 and transistor 135. The second time-delay gate includes the following parts, which are identical in nature to the parts of the first time-delay gate: 233, 234, 236, 237 and 235. The first and second time-delay gates are respectively associated with time-delay circuits II and III in a manner soon to be elucidated. It is worthwhile to note in anticipation of this fuller elucidation, however, that the relationships between the two time-delay gates and their respective associated time-delay circuits are identical, except that the output of the first gate is connected to the input of circuit III and the output of the second gate is connected to the final output circuit of the receiver circuit V.

More specifically, as previously explained, the outputs of time-delay circuits II and III are both located in the current path between the first and second transistor stages. The output of time-delay circuit II, for instance, is located

6

between the collector of transistor 112 and resistor 116. One side of capacitor 133 is connected to this point in circuit II. The other side of the capacitor is connected to resistor 134, which is in turn connected to the base of transistor 135. Also connected to the base of the transistor is one lead from resistor 137, whose other lead is grounded. The collector of transistor 135 is connected back to gate pulse capacitor 38 in the manner explained above. The emitter of this transistor is coupled to one lead of resistor 136, the other lead of this resistor being grounded. Parts 212, 216, 233, 234, 235, 236, 38 and 237 are connected together in the same manner as parts 112, 116, 133, 134, 135, 136, 38 and 137. Thus the input connections, internal wiring and power supply of the time-delay gates are identical. The distinction lies in their output connections. On the one hand, collector of gate transistor 135 is coupled with the input of time-delay circuit III. On the other hand, the collector of corresponding gate transistor 235 is coupled with transistor 50 in output circuit V.

Capacitor 133 and resistors 134 and 137, considered as a group, and capacitor 233 and resistors 234 and 237, considered as a corresponding, but separate group of circuitry components, constitute pulse differentiation units. From a functional point of view these units may be regarded as being capable of furnishing a short sharp pulse of current to the bases of the gate transistors 135 and 235 in response to changes in the potential of the output of the time-delay circuits. Whether such short pulses will be positive or negative in potential will of course depend upon whether the potential change in the time-delay circuits occurs in a positive or negative direction. The short differential pulses will be positive if the potential variations in the time-delay circuits are positive. They will be negative if the potential variations are negative.

As will become apparent from a description of the operation of the subject receiver, the outputs of the time-delay circuits are controlled-potential currents of extended duration, terminating in sharp drops in potential. The pulse differentiation units are provided for differentiating the aforesaid sharp drops in potential and for providing negative pulses to the bases of the gate transistors. Gate transistors 135 and 235, being of the p-n-p type, can be turned on momentarily by sharp negative pulses. Thus the pulse differentiation units 233, 234, 237 and 133, 134, 137 may accurately be denominated as means for rendering said gate transistors momentarily conductive in response to the termination of pulses within said time-delay circuits. It should also be clear that each gate transistor, and its companion pulse differentiation unit in combination, constitute the time-delay gates.

Output circuit V will now be explained in detail with reference to FIGURES 1 and 4. The purpose of the output circuit is to trigger the operation of the load device 57. In this embodiment the load device is a blasting cap for severing a destructible link in an anchoring system. The cap is illustrated figuratively in FIGURE 1 and symbolically as a resistance in FIGURE 4.

The power supply for the cap 57 is the large capacitor 55 whose discharge path is through the resistor 56 and through the silicon controlled switch 54. Resistor 56 serves as a current limiter for switch 54. Switch 54 is a standard semi-conductor unit, normally used as a rectifier. It has the ability to remain in an almost perfect condition of non-conduction until a prescribed trigger voltage is applied. It instantly becomes highly conductive and remains in that condition until the current flow diminishes to a very small flow. It is characterized by quite low leakage current and is capable of conducting a relatively heavy flow of current, at least several amperes. Together, capacitor 55, resistor 56 and switch 54 are capable of providing the cap 57 with a current of several amperes for at least a few milliseconds.

Switch 54 is operated by p-n-p transistor 50 and other auxiliary circuitry elements. Transistor 50 is connect-

ed by its base to the output of the gating circuit IV, or more particularly to the emitter of gate transistor 235. A resistor 52 interconnecting the emitter of transistor 50 with ground, constitutes a voltage gain limiter for the transistor. Its presence helps insure against the generation of significant outputs by the transistor 50 in response to mere noise inputs. The collector of this transistor is connected through resistor 64 to the decoupling network 229, 230. Resistor 64 is the collector load. The collector is also connected to the control lead of switch 54 through condenser 53. This connection is the flow path through which transistor 50 controls the closing of switch 54.

Certain auxiliary circuitry elements are present in the output circuit. The capacitor 63 is connected to the conductor connecting capacitor 55 with the battery 27. It is a high-frequency by-pass for the prevention of the firing of switch 54 by spurious noise signals. The resistor 60 is connected between the control lead of switch 54 and a point between resistor 56 and said switch. The purpose of including resistor 60 in circuit V is to provide means for biasing switch 54 during standby periods to keep it in a non-conducting state.

The invention is employed, for example, in the recovery system for an oceanographic device 65, for taking sub-surface measurements of under-sea conditions such as temperature. For instance, there are various oceanographic reasons for charting the movements and locations of under-sea currents. One practical method of doing this is to take reasonably continuous underwater temperature measurements at various locations in the vicinity of the currents. The means employed can be a large number of temperature recording devices, such as the device shown in FIGURE 5. They may be moored in water-tight cannisters beneath the surface. They may be planted on a grid layout in the open ocean and may be allowed to remain underwater over a period of time. At the end of the period they would be raised from their underwater moorings so that the temperature data and measuring equipment might be recovered.

An underwater temperature measuring device of the character described would ordinarily include an anchor (not shown), an anchor cable 67 and a buoyant, water-proof cannister 68. The cannister is anchored underwater with the aid of the anchor and cable 67. Included in cable 67 is destructible link 69, employing the blasting cap 57 as the destruction element. That is, the link 69 within which cap 57 is located, is adapted to break in two upon the firing of cap 57, thus releasing the cannister 68 from its mooring and allowing it to rise to the surface.

Projecting from the cannister through water-tight connections are a temperature sensing device 70, hydrophone 10 and a water-proof cable 83 for electrically connecting the cap 57 in link 69 to the output circuit V in the manner shown in FIGURE 1. Within the cannister 68 are the valuable temperature recorder 65, the collected data and the above-described electronic acoustic receiver.

When it is desired to recall the recorder 65 to the surface, it is necessary only to project three time-coded acoustic signals into the water within a few miles of the receiver. The signals will be transmitted underwater to the hydrophone. As the first signal enters the hydrophone it generates a negative going pulse 71 which enters the amplifier circuit and momentarily biases transistor 12 to a conducting condition as shown in FIGURE 2. The collector of transistor 12 which normally operates at -15 volts with a fresh battery rises sharply in potential as that transistor begins to conduct. The collector potential will then continue to rise positively until transistor 12 is saturated, thus holding the collector voltage at approximately 0 volts. The positive going potential of transistor 12 is fed to the base of transistor 13 through resistor 16. As transistor 13 becomes conducting, its collector voltage drops sharply until a condition of saturation is reached. Then regeneration begins in the positive A.C. feedback

loop, which includes transistor 13, resistor 21, resistor/thermistor network 23, 24, 25, capacitor 22, transistor 12, resistor 16 and, again, transistor 13. Current flows in this positive feedback loop in the proper direction to keep transistor 12 turned on and saturated. Any spurious signals which enter the amplifier at this time will simply be absorbed into the feedback.

The charge path for capacitor 22 is through resistor 26 and through the base-emitter junction of transistor 12. This current will continue to flow until capacitor 22 is charged to the extent necessary to reduce its charging current to a very small value. When the desired extent of charging is obtained in the capacitor 22, transistor 12 will no longer be saturated because its base emitter current will have dropped to too low a value. Thus the collector voltage of transistor 12 will fall to a negative value and automatically turn off transistor 13.

When transistor 13 shuts off, regeneration ceases. The duration of regeneration depends of course upon the charging time constant of capacitor 22 and the collector voltage of transistor 13. The time constant is a constant value, since the value of capacitor 22 is fixed. The Zener diode 20 clips any excess voltage from the collector of transistor 13. Therefore the collector voltage will be a standard voltage every time regeneration occurs until the battery 27 deteriorates from age and/or use. Since the time constant and voltage are regular, the period of regeneration will be the same every time a signal 71 is received, at least until such time as the battery 27 is no longer fit for service.

The beginning, timed duration and timed expiration of regeneration are represented by a prolonged amplifier pulse 73. This pulse passes to the gate circuit and to the potential divider network which includes resistors 18 and 19. There pulse 73 is reduced in potential. The result is pulse 74, having the same duration but a lower potential than pulse 73. Pulse 74 is sent to circuit II where it enters its first stage of delay. No appreciable delay in the transmission of pulses 73 and 74 occurs in the amplifier. Therefore, capacitor 22 will be strongly charged positively as the pulses 73 and 74 expire. This is true because the charging of capacitor 22 controls the duration and timed expiration of these pulses.

Because capacitor 22 is now strongly charged positively it is able to lockout reverberation pulses, which might otherwise trigger the amplifier, by back-biasing the base-emitter junction of transistor 12. Thus transistor 12 is prevented from re-energizing until capacitor 22 has discharged sufficiently to allow another negative signal pulse 71 to enter the base of transistor 12. The automatic lockout persists for the length of time that it takes for capacitor 22 to slowly discharge through resistances 14, 23, 24, 18, 19, 21 and 25. Any spurious acoustic signals which enter the amplifier while capacitor 22 is discharging will be locked out. Only when capacitor 22 becomes sufficiently discharged so that transistor 12 ceases to be back-biased will any additional acoustic signals be able to trigger additional output pulses 73 and 74.

While the automatic lockout is in operation, the pulse 73 proceeds to the gating circuit, circuit IV. As shown in FIGURE 3, pulse 73 proceeds from amplifier circuit I through diode 40, resistor 41 and resistor 42 to the capacitor 38 which is charged thereby. Capacitor 38 immediately starts to discharge, creating a gate pulse 77 in the circuit which is connected to the collectors of gate transistors 135 and 235. These transistors are normally in a non-conducting state, because as will be explained below, the gate transistors become conductive only in response to the receipt of two additional properly coded acoustic signals through hydrophone 10. Therefore, since gate transistors 135 and 235 are closed and diode 40 conducts in one direction only, the charge on capacitor 38 merely leaks off gradually through resistances 41 and 42.

As the automatic lockout takes effect and at the same time pulse 73 is sent to gating circuit IV, pulse 74 enters

the first time-delay circuit, circuit II. As indicated above, the pulse 74 is produced in circuit I and is transmitted to circuit II where it enters through capacitor 111 and resistor 131 and biases transistor 112 into a conducting state. A positive potential is transmitted to the base of transistor 113 through resistor 116, causing transistor 113 to conduct. Regeneration occurs in the feedback loop which includes resistor 121, resistor/thermistor network 123, 124, 125, transistors 112 and 113, resistor 116 and capacitor 122. Regeneration continues until capacitor 122 becomes charged whereupon it no longer conducts. Thus regeneration comes to an end. The beginning, continuation and end of regeneration is characterized by pulse 44 in FIGURE 3. The time-delay circuit controls the duration of its regeneration in the same fashion as does circuit I. Thus pulse 44 will always be of the same duration, except after the battery deteriorates.

Pulse 44 is differentiated by capacitor 133 to differentiate pulse 46, which is reduced in amplitude to reduce differential pulse 75 by the potential divider network which includes resistors 134 and 137. Since the transistor 135, being a p-n-p transistor, is rendered conductive only by negative pulses, the positive portion of pulse 75 has no effect on the transistor. However, the negative portion of pulse 75 does momentarily bias transistor 135 to a conducting state. If the collector of transistor 135 is provided with a pulse at the instant transistor 135 is biased to a conducting state, the gate circuit IV will send a pulse to the second time-delay circuit III. Attention is called to the fact that the capacitor 38 is the power supply for the collector of transistor 135 and that capacitor derives its charge from the amplifier circuit I. Thus if a second acoustic signal enters the amplifier I at such a time that it charges capacitor 38 and causes it to discharge pulse 77 while 135 is momentarily in a conducting condition, transistor 135 will conduct and send negative pulse 48 to circuit III. The regeneration period in time-delay circuit is long enough to outlast the operation of the automatic lockout.

Pulse 48 is received and treated by circuit III in exactly the same fashion as pulse 74 was received and treated by circuit II. The pulse initiates a heavy positive A.C. feedback in the loop which includes transistors 212 and 213, resistors 216 and 221, resistor/thermistor network 223, 224, 225 and capacitor 222. The last-mentioned capacitor stops regeneration after a predetermined period. The beginning, continuation and end of regeneration is characterized by the pulse 45 in FIGURE 3.

Pulse 45 is differentiated, reduced and converted to reduced differential pulse 76 by resistors 234 and 237 and by capacitor 233. The negative component of this pulse momentarily biases p-n-p gate transistor 235 to a conductive state. A properly timed third acoustic signal will charge and discharge 38 at the correct time to send a pulse 77 to the collector of gate transistor 235 while it is in a conductive state. Therefore, it will conduct current and produce a negative pulse 49.

The output circuit V is connected to gating circuit IV, as shown in FIGURE 1, by a conductor between the emitter of transistor 235 and the base of transistor 50. As shown in FIGURE 4, transistor 50 accepts only negative signals 49 from transistor 235 and produces only positive output signals 51. When three properly coded signals are delivered to the amplifier, time-delay and gate circuits I, II, III and IV, they deliver a negative output pulse 49 to transistor 50 as explained above. Transistor 50 in turn produces a positive output signal 51 which is coupled through the capacitor 53 to the control lead of switch 54.

Switch 54 is normally maintained in a non-conducting condition by resistor 60. However, when transistor 50 delivers its positive signal to the control lead of switch 54, switch 54 conducts, discharging the capacitor 55 through the resistor 56. The current from capacitor 55 passes on through resistor 56, through switch 54 and from thence through the cap 57 which is detonated thereby.

Detonation of the cap destroys the link member 69, freeing the buoyant cannister 68 from its mooring and allowing it to rise to the surface, where it may be recovered.

The firing pulse for blasting cap 57 may be recognized as the pulse 58 in FIGURE 4. The explosion of the cap will break the circuit and cut off the pulse at some point in time after its inception and before it would normally expire if an explosion did not take place.

Attention is directed to the fact that the blasting cap 57 can be operated only once. Therefore, there is no need to provide means for the output circuit to reset itself in the above-described embodiment of the invention. However, the nature of the invention makes it useful in connection with load devices which do not become inoperative during and as a result of their use as a blasting cap or fuse does. Such a load device is represented in FIGURE 6 by the numeral 78. FIGURE 6 differs from FIGURE 4 in three respects only. First it shows only part of the output circuit of FIGURE 4. Second the load device 78 is substituted for the blasting cap 57. Thirdly, a resistor 59 is provided between capacitor 63 and battery 27, which is outside the figure, but shown in FIGURE 1. The portions of FIGURES 1 and 4 which have been omitted from FIGURES 6 and 7 are unchanged.

The only differences in the operation of FIGURE 4 and FIGURE 6 are as follows. After the capacitor 55 has discharged through switch 54, current would continue to flow in a FIGURE 4 type of output circuit, with the battery 27 providing the current needed to maintain switch 54 in a conductive condition. The last statement presupposes that the load device is now of the character which is capable of continued operation. Thus the load device 78 would be expected to operate continuously until the battery 27 was exhausted. However, the resistor 59 has sufficient resistance to prevent the flow of the minimum amount of current needed to keep switch 54 conducting. Therefore, the FIGURE 6 circuit will operate load device 78 for as long as capacitor 55 is discharging enough current to keep switch 54 conducting, but no longer. The potential vs. time profile of the output is represented by pulse 79. Clearly, the circuit contemplated by FIGURE 6 is of the type which is suitable for load devices which are to be operated intermittently for short periods of time.

It will be readily apparent to those skilled in the art that there are some applications of the subject electronic acoustic receiver in which the receiver would be employed to continuously operate a load device, such as a radio transmitter, for the life of the battery 27, once three properly coded signals had been received. FIGURE 7, in which a radio transmitter is symbolically represented as resistance 80, discloses an adaptation of the output circuit useful for such an application of the invention. The FIGURE 7 depicts the same portion of the output circuit as FIGURE 6. However, the FIGURE 7 circuit eliminates the need for capacitor 55, resistor 59 and resistor 56. The FIGURE 7 circuit relies upon the battery instead of the capacitor 55 for powering the transmitter 80. Therefore capacitor 55 and its current limiter, resistor 56 are not needed and have therefore been eliminated. Furthermore, it is contemplated that the FIGURE 7 circuit will begin to operate the transmitter 80 the first time switch 54 conducts and will continue to operate the transmitter holding switch 54 in a conducting condition until the battery is exhausted. Therefore, the resistor 59 is not used. The battery 27 provides both the holding current for switch 54 and the power for the transmitter 80 until exhausted. Pulse 81 illustrates the time vs. potential profile for this circuit.

Those skilled in the art will recognize that FIGURES 4, 6 and 7 represent only a few of many modifications which can be made in the output circuit without departing from the spirit of the invention. Other modifications will readily suggest themselves to persons skilled in the art. No invention or avoidance of the present invention

11

would reside in reversing the polarity of the circuitry elements or in providing more or fewer time-delay circuits than are shown in the above specific embodiment. There would be no departure from the invention in substituting vacuum tubes for the transistors and crystal diodes. Nor would any departure therefrom reside in exchanging a thyatron tube for the silicon switch 54. All the above modifications and any other modifications falling within the skill of the art are included in the present invention.

One of the features of the present invention is that the amplifier circuit includes a D.C. coupled complementary, symmetrical transistor amplifier biased in Class B relationship so that both stages are cut off. The complementary fashion in which the transistors are paired permits the use of D.C. coupling. The nature of the circuit is such that the stand-by current is decreased to a very minute value resulting in a corresponding increase in battery life where batteries are used as the power source.

When new, the batteries 27 would provide a larger potential than after several months of use. Consequently, the amplifier and time-delay circuits would ordinarily be expected to provide longer output pulses when the batteries were newly charged than they would after several months of use. By using the Zener diodes as dynamic shunt regulators which are not operable (thus do not consume current) except when output pulses are being generated by the amplifier and time-delay circuits I, II and III constant consumption of bleeder current as in conventional shunt regulation is avoided. Thus the output voltage of the transistors in said circuits is regulated with only intermittent drain on battery 27, the drain being limited to those periods during which a signal is actually being regenerated.

There are a number of advantages in the use of a heavy positive A.C. feedback. Very little input signal is required. Therefore the use of a pre-amplifier in the input stage is rendered unnecessary. Secondly, regeneration brings about the saturation of both transistor stages, enabling the amplifier to produce a high amplitude output pulse of long duration. Thirdly, the feedback sets up an automatic lockout which renders the amplifier inoperative for a considerable period of time after the first acoustic signal has been applied, a coupling capacitor being used to back-bias the amplifier input. These features result in the elimination of signal reflection problems. Such features also reduce power requirements and make the coding more secure by insuring that the recovery time will be lengthy in the event that a false signal is applied to the circuit.

It is clear that the endurance and signal discriminating qualities of the subject electronic acoustic receiver make it eminently serviceable in remote-control, self-powered undersea devices requiring some means of communication with the surface for recovery, adjustment or operational purposes. However, many applications of the invention to other environments and purposes could be immediately suggested by one skilled in the art without resort to inventive alterations of the subject matter. Therefore, while a particular embodiment of the invention has been shown and described the various details thereof should not be regarded as unduly limiting the appended claims which should be read so as to include therein all such variations and modifications which fall within the true spirit and scope of this invention.

Having thus described my invention, I claim:

1. A code operated electronic acoustic receiver comprising:

- (a) an acoustic transducer to produce electric signals in response to acoustic signals;
- (b) an amplifier circuit, means for conductively connecting said amplifier circuit to said transducer to receive said electric signals, means in said amplifier for producing an amplifier output including time-standardized amplifier pulses generated in said amplifier in response to said electric signals;

12

(c) an automatic lockout in said amplifier circuit to prevent said amplifier from receiving electric signals from said transducer during a predetermined lockout time interval subsequent to the receipt of a first electric signal;

(d) a time-delay circuit, means for conductively connecting said time-delay circuit with said amplifier circuit to receive a first standardized amplifier pulse generated in said amplifier in response to a first coded acoustic signal, means in said time-delay circuit for producing in response to said first standardized amplifier pulse a prolonged time-delay pulse of standard duration which survives said lockout time interval for a short time;

(e) a gating circuit, means for conductively connecting said gating circuit to said time-delay circuit to receive said prolonged time-delay pulse therefrom, means in said gating circuit to differentiate said prolonged pulse, and to produce a differential pulse in response to the expiration of said time-delay pulse, means for conductively connecting said gating circuit to said amplifier circuit to receive a second amplifier pulse generated in said amplifier in response to a second acoustic signal transmitted to said transducer in coded relationship with said first acoustic signal, means for converting said amplifier pulse to a gate pulse, said code relationship being an interval of time separation between said acoustic signals which causes the presence of said gate pulse in said gating circuit to coincide with the production of said differential pulse, and means in said gating circuit for producing output pulses only in response to the coincident presence therein of said differential and gate pulses;

(f) an output circuit including a load device, power supply means for said load device, means for connecting said output circuit to said gating circuit, and means responsive to said output pulse for connecting said load device with said power supply;

whereby said first and second coded acoustic signals are effective to operate said load device.

2. The electronic acoustical receiver of claim 1 wherein said amplifier circuit includes:

(a) a D.C. coupled complementary, symmetrical two-stage transistor amplifier biased so that both stages are cut off, said amplifier having a first stage transistor and a second stage transistor, said transistors being provided with base, collector and emitter electrodes;

(b) a feedback loop conductively connecting the collector of the second stage transistor to the base of said first stage transistor for supplying a positive A.C. feedback signal from the output of said amplifier to the input of said amplifier; and

(c) lockout means in said feedback loop to prevent a negative signal from entering the amplifier circuit for a predetermined period of time after the amplifier has produced an output pulse;

whereby said output pulse is extinguished after a predetermined period of current flow.

3. The electronic acoustical receiver of claim 2 wherein the lockout means includes a capacitor in the feedback loop and an associated resistor network connected thereto to control the discharge of said capacitor.

4. A code operated electronic receiver comprising a transducer, a power supply, an amplifier, a plurality of serially connected time-delay circuits, a gating circuit, and an output circuit, said circuits having input and outputs, the transducer and said circuits being connected with the power supply, the transducer also being connected to the input of the power supply, the transducer also being connected to the input of the amplifier, the output of the amplifier being connected to the input of a first of said time-delay circuits, the outputs of the first time-delay circuit and of the amplifier being connected

to the gating circuit, the gating circuit being connected to both the inputs and the outputs of all the remaining time-delay circuits, the gating circuit finally being connected to the input of the output circuit, the output of said output circuit being connected to a load device, whereby coded signals received by said transducer and converted in said amplifier to timed pulses are successively applied to the serially connected time-delay circuits by the gating circuit to actuate the load device, and wherein the amplifier includes:

- (a) a first and second transistor, each having a collector, an emitter and a base, the first of the transistors being of p-n-p type and the second of the transistors being of the n-p-n type; 10
- (b) means for conductively connecting the collector of the first transistor to the base of the second transistor and means for conductively connecting the collector of the second transistor with the base of the first transistor, the aforesaid means, the base collector path of the first transistor and the base collector path of the second transistor constituting a first feedback loop; 15
- (c) means for supplying current to the first feedback loop; 20
- (d) a first capacitance wired in series in the first feedback loop; 25
- (e) means for conductively connecting the transducer to said first feedback loop at a point between the first capacitance and the base of the first transistor; 30
- (f) a first Zener diode associated with the first feedback loop by a conductive connection to the collector of the second transistor, and
- (g) a resistor network in said first feedback loop between said first Zener diode connection and the 35

first capacitance for regulating the discharge of the first capacitance.

5. The code operated electronic receiver of claim 4 wherein at least one of said time-delay circuits includes:

- (a) a third and a fourth transistor, each having a collector, an emitter and a base, the third transistor being of the p-n-p type and the fourth transistor being of the n-p-n type;
- (b) means for conductively connecting the collector of the third transistor to the base of the fourth transistor and means for conductively connecting the collector of the fourth transistor with the base of the third transistor, the aforesaid means, the base collector path of the third transistor and the base collector path of the fourth transistor constituting a second feedback loop;
- (c) means for supplying current to the second feedback loop;
- (d) a second capacitance wired in series in second feedback loop;
- (e) means for conductively connecting the collector of the second transistor in the amplifier circuit to a point in the second feedback loop between the second capacitance and the base of the third transistor;
- (f) a second Zener diode associated with the second feedback loop by a conductive connection to the collector of the fourth transistor;
- (g) a resistor network in said feedback loop between said Zener diode connection and said capacitance for regulating the discharge of said capacitance.

References Cited in the file of this patent

UNITED STATES PATENTS

2,951,985	Hudson et al. -----	Sept. 6, 1960
3,027,837	Kendall -----	Apr. 3, 1962