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(54) **PIXEL CIRCUIT**

(57) A pixel circuit (200, 300, 400) integrable as part of a display (280), comprises a selection block (102) connected to a selection line (104) and to a data line (105) and configured to receive pixel data on said data line (105) upon assertion of said selection line (104); a driver-side pixel data storage element (108); and a driver block (110) connectable to a self-emitting pixel element (112) for driving said self-emitting pixel element (112), wherein an instantaneous brightness of said self-emitting pixel element (112) is controlled based on said driver-side pixel data storage element (108), said pixel circuit (200, 300, 400) further comprising an intermediate stor-

age block (202) comprising an intermediate pixel data storage element (208) and connected to said selection block (102), to said driver-side pixel data storage element (108), and to a latch line (204), wherein said pixel circuit (200, 300, 400) is configured so that the pixel data input on said data line (105) is transferred to said intermediate pixel data storage element (208) upon assertion of said selection line (104), and so that pixel data is transferred from said intermediate pixel data storage element (208) to said driver-side pixel data storage element (108) upon assertion of said latch line (204).

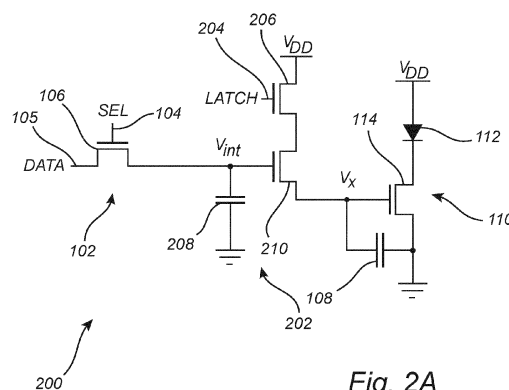


Fig. 2A

Description

Technical field

[0001] The present inventive concept relates to a pixel circuit, a display comprising a plurality of such pixel circuits, a method of controlling the display, a display controller configured to carry out the method, and to a non-transitory computer-readable storage medium having stored thereon instructions for implementing the method.

Background

[0002] Displays comprising self-emitting pixel elements, such as AMOLED and AMLED displays find wide application.

[0003] In most such displays, pixel data is refreshed, i.e., a new frame is written, through a scanning procedure wherein the new pixel data is written to the display sequentially line by line, e.g., from top to bottom of the display.

[0004] In most displays, this is unproblematic, since neighboring lines are refreshed immediately before or after their neighboring lines, so that any artefacts from the scanning procedure is not perceivable by the human eye.

[0005] However, there are instances where this may be problematic. For example, when tiling several display modules next to each other, the last row of one module may be located immediately next to the first row of another module. Therefore, these neighboring lines will be updated with a time difference corresponding to a full frame or sub-frame interval. This can cause undesired visual artifacts.

[0006] Thus, there is a need for improvement in this area.

Summary

[0007] An objective of the present inventive concept is to provide a pixel circuit allowing for a display with less temporal visual artefacts.

[0008] According to a first aspect, there is provided a pixel circuit integrable as part of a display, said pixel circuit comprising a selection block connected to a selection line and to a data line and configured to receive pixel data on said data line upon assertion of said selection line; a driver-side pixel data storage element; and a driver block connectable to a self-emitting pixel element for driving said self-emitting pixel element, wherein an instantaneous brightness of said self-emitting pixel element is controlled based on said driver-side pixel data storage element, said pixel circuit further comprising an intermediate storage block comprising an intermediate pixel data storage element and connected to said selection block, to said driver-side pixel data storage element, and to a latch line, wherein said pixel circuit is configured so that the pixel data input on said data line is transferred to said

intermediate pixel data storage element upon assertion of said selection line, and so that pixel data is transferred from said intermediate pixel data storage element to said driver-side pixel data storage element upon assertion of said latch line.

[0009] A pixel may be associated with or comprise a single self-emitting pixel element. In another case, a pixel may comprise several sub-pixels, each associated with or comprising a respective self-emitting pixel element. For example, the respective self-emitting pixel element of each sub-pixel may emit a different primary color. For example, there may be one sub-pixel for each of the colors red, green, and blue.

[0010] With "pixel circuit" should be understood the circuitry associated with the driving of a specific pixel or sub-pixel. Typically, a single pixel circuit may be associated with a single pixel or sub-pixel and each pixel or sub-pixel may be associated with a single pixel circuit.

[0011] With "pixel data" should be understood data indicating an intended instantaneous brightness of the self-emitting pixel element. For example, and typically, the pixel data may be either an analog or a digital voltage. In the case of an analog voltage, increasing voltage may indicate a higher instantaneous brightness level of the self-emitting pixel element. In the case of a digital voltage, the digital voltage may indicate whether the self-emitting pixel element should be turned on or off. In this case, the self-emitting pixel element may be arranged to repeatedly turn on and off, e.g., through pulse width modulation (PWM).

[0012] The present inventive concept stems from a realization that the arranging of an intermediate pixel data storage element allows simultaneous visual updating of all pixels of a display, instead of visual updating through scanning through the display lines. While the pixel data may still be written into the respective intermediate storage block through a scanning procedure employing the data and selection lines, the updated pixel data will only become visible and active in the respective pixel upon assertion of the latch line. By arranging for all pixel circuits in a display to be connected to a same, i.e., global latch line, and asserting that latch line, all pixels of the display may be simultaneously updated. Hereby, visual artefacts from the scanning may be eliminated.

[0013] The present inventive concept may find further use for 3D applications, wherein the 3D effect is created using a 2D display, such as a TV, and glasses that alternately block the light for either the left or the right eye and where therefore instantaneous updating of a whole display may be required, so the correct eye gets the correct image.

[0014] According to an embodiment, the intermediate storage block comprises a latch transistor controlled by the latch line. This is a particularly simple way of implementing the intermediate storage block.

[0015] According to an embodiment, the intermediate storage block further comprises a forwarding transistor, wherein the latch transistor is connected to a supply volt-

age and to the forwarding transistor and the forwarding transistor is controlled by the intermediate pixel data storage element and further is connected to said driver-side pixel data storage element. Hereby, the forwarding transistor may be configured as a source-follower. This is a particularly beneficial way of implementing the intermediate storage block in case of the pixel data being an analog voltage.

[0016] According to an embodiment, the latch transistor is connected to said intermediate pixel data storage element and to the driver-side pixel data storage element. This is a particularly simple way of implementing the intermediate storage block in case of the pixel data being a digital voltage.

[0017] According to an embodiment, the driver-side pixel data storage element is connected to a logic gate, and said logic gate is connected to said driver block. This is a particularly robust way of implementing the intermediate storage block in case of the pixel data being a digital voltage.

[0018] According to an embodiment, the logic gate is a buffer or inverter.

[0019] According to an embodiment, the logic gate is a NOR gate or NAND gate connected to a reset line. This allows for both simultaneously updating digital data voltages for all pixels and resetting all pixels.

[0020] According to an embodiment, the selection block comprises a transistor controlled by said selection line and connected to said data line and to the intermediate pixel data storage element. This is a particularly simple way of implementing the selection block.

[0021] According to an embodiment, the driver block comprises a transistor connectable in series with the self-emitting pixel element and controlled by the driver-side pixel-data storage element. This is a particularly simple way of implementing the driver block.

[0022] According to an embodiment, said intermediate pixel data storage element and/or said driver-side pixel data storage element is a capacitor.

[0023] According to a second aspect, there is provided a display comprising a plurality of pixel circuits according to the first aspect.

[0024] This aspect may generally present the same or corresponding advantages as the former aspect.

[0025] According to a third aspect, there is provided a method of updating the display according to the second aspect, said method comprising performing a pixel data update procedure, said procedure comprising simultaneously asserting said selection line for each pixel circuit in a subset of pixel circuits of said plurality of pixel circuits while inputting pixel data on each respective data line of each pixel circuit of said subset of pixel circuits, wherein said pixel data update procedure is repeated, sequentially in time, for different subsets of said plurality of pixel circuits; and, thereafter, simultaneously, for each pixel circuit of said plurality of pixel circuits, asserting said latch line.

[0026] This aspect may generally present the same or

corresponding advantages as the former aspects.

[0027] According to an embodiment, each said subset corresponds to a row of pixels in said display.

[0028] According to a fourth aspect, there is provided a display controller configured to carry out the method according to the third aspect.

[0029] This aspect may generally present the same or corresponding advantages as the former aspects.

[0030] According to a fifth aspect, there is provided a non-transitory computer-readable storage medium having stored thereon instructions for implementing the method according to the third aspect, when executed on a device having processing capabilities.

[0031] This aspect may generally present the same or corresponding advantages as the former aspects.

Brief description of the drawings

[0032] The above, as well as additional objects, features and advantages of the present inventive concept, will be better understood through the following illustrative and non-limiting detailed description, with reference to the appended drawings. In the drawings like reference numerals will be used for like elements unless stated otherwise.

Fig. 1A shows, for comparison, a pixel circuit not according to the present inventive concept.

Fig. 1B shows a timing diagram for the pixel circuit of Fig. 1A.

Fig. 2A shows a pixel circuit.

Fig. 2B shows a timing diagram for the pixel circuit of Fig. 2A.

Fig. 2C shows a display comprised of pixels each associated with a respective pixel circuit.

Fig. 3 shows a further pixel circuit.

Fig. 4 shows a further pixel circuit.

Detailed description

[0033] Firstly, for comparison, Fig. 1A illustrates a pixel circuit 100 not according to the present inventive concept.

[0034] There is shown a pixel circuit 100, which may form part of a display comprised of self-emitting pixel elements, such as an AMOLED display or an AMLED display. The display may be an active matrix (AM) display.

[0035] The pixel circuit 100 comprises a selection block 102, a driver-side storage element 108, and a driver block 110, and is connectable to a self-emitting pixel-element 112, such as an LED, OLED, or μ LED.

[0036] The selection block 102 is connected to a selection line 104 and to a data line 105. In the shown implementation, the selection block comprises a selection transistor 106, where a gate terminal of the selection transistor 106 is connected to the selection line 104 and a source or drain terminal is connected to the data line 105. Thereby, the selection block 102 is configured to receive

pixel data on the data line 105 upon assertion of the selection line 104. The other source or drain terminal of the selection transistor 106 is connected to the node V_x .

[0037] The driver block 110 comprises a driver transistor 114 connectable in series with the self-emitting pixel element 112 between a supply voltage V_{DD} and ground. Further, the gate terminal of the driver transistor 114 is connected to the node V_x , and thus to the upper plate of the capacitor 108, so that the driver-side pixel-data storage element 108 controls the driver transistor 114.

[0038] The driver-side storage element 108 is in the example of Fig. 1A a capacitor 108. It is connected between the node V_x and ground, i.e., between a source or drain terminal of the selection transistor 106 opposite to the data line 105, and to the source terminal of the driver transistor 114, opposite to the self-emitting pixel element 112. In other embodiments, the driver-side storage element 108 may be connected to the drain terminal of the driver transistor 114.

[0039] Hereby, the driver block 110 is connectable to the self-emitting pixel element 112 for driving the self-emitting pixel element 112, wherein an instantaneous brightness of the self-emitting pixel element 112 is controlled based on said driver-side pixel data storage element 108.

[0040] In the example of Fig. 1A, the pixel circuit is a so-called 2T1C pixel circuit, comprising two transistors 106, 114 and one capacitor 108.

[0041] Fig. 1B shows a timing diagram for driving a display comprising a plurality of pixel circuits 100 of Fig. 1A.

[0042] As typical in a display, pixels may be organized in columns and rows. Data lines DATA1, DATA2, DATA3... may run vertically through the display, while selection lines SEL1, SEL2, SEL3... may run horizontally through the display. Thus, a specific selection line selects a corresponding line of pixels in the display, while the individual pixels of that line then may be addressed through the data lines.

[0043] Thus, pixel data may be refreshed by sequentially selecting each selection line, while applying a corresponding pixel data voltage to each data line. This is exemplified for a single data line DATA_i in Fig. 1B, corresponding to a specific column of pixels. The timing diagram is provided for the updating of pixel data of two consecutive frames (frame a and frame b). Schematically shown are voltages on selection lines SEL1, SEL2, ..., SEL N and on nodes V_{x1} , V_{x2} , ..., V_{xN} , i.e., the V_x node of the respective pixel circuit.

[0044] As can be seen, pixel data $d1_a$ is input on the DATA_i line while asserting the selection line SEL1. Hereby, $d1_a$ shows up on V_{x1} . The procedure is repeated with pixel data $d2_a$ while asserting the selection line SEL2, and so on.

[0045] In the pixel circuit asserting the selection line connected to the pixel in question, and inputting a pixel data voltage on the data line, will result in the data voltage

being provided to node V_x , thereby charging the driver-side pixel data storage element 108 capacitor and immediately being visible in the pixel, since, in the pixel circuit 100 of Fig. 1A, the instantaneous brightness of said self-emitting pixel element of the respective pixel is controlled based on the respective driver-side pixel data storage element. Through this non-simultaneous updating, image tearing may be visible.

[0046] Fig. 2A shows a pixel circuit 200. The pixel circuit 200 is particularly useful for analog pixel driving, but may also be used for digital driving. Similarly to Fig. 1A, there is shown a pixel circuit 200, which may form part of a display comprised of self-emitting pixel elements, such as an AMOLED display or an AMLED display. The display may be an active matrix (AM) display.

[0047] The pixel circuit 200 comprises a selection block 102, a driver-side storage element 108, and a driver block 110, and is connectable to a self-emitting pixel-element 112, such as an LED, OLED, or μ LED.

[0048] Furthermore, and in addition to the pixel circuit 100 of Fig. 1A, the pixel circuit 200 comprises an intermediate storage block 202, connected between the selection block 102 and the driver-block 110, as will be elaborated further upon below.

[0049] The selection block 102 is connected to a selection line SEL 104 and to a data line DATA 105. In the shown implementation, the selection block comprises a selection transistor 106, where a gate terminal of the selection transistor 106 is connected to the selection line 104, so that the selection transistor 106 is controlled by the selection line 104, and where a source or drain terminal of the selection transistor 106 is connected to the data line 105. Thereby, the selection block 102 is configured to receive pixel data on the data line 105 upon assertion of the selection line 104.

[0050] Instead of being connected directly to the node V_x (cf. Fig. 1A), the other source or drain terminal of the selection transistor 106 is connected at a node V_{int} to the intermediate storage block 202, and in particular to the intermediate pixel data storage element 208.

[0051] It should be noted that the present inventive concept is by no means limited to the selection block being comprised of a single selection transistor 106. Rather, other designs, for example, comprising several transistors and/or logic gates, etc., as known by the skilled person, are equally possible.

[0052] In the example of Fig. 2A, the driver block 110 comprises a driver transistor 114 connectable in series with the self-emitting pixel element 112 between a supply voltage V_{DD} and ground. Further, the gate terminal of the driver transistor 114 is connected to the node V_x .

[0053] The driver-side storage element 108 is in the example of Fig. 2A capacitor 108. It is connected between the node V_x and ground, i.e., between the intermediate storage block 202 and the source terminal of the driver transistor 114 opposite to the self-emitting pixel element 112.

[0054] Hereby, the driver block 110 is connectable to

the self-emitting pixel element 112 for driving the self-emitting pixel element 112, wherein an instantaneous brightness of the self-emitting pixel element 112 is controlled based on said driver-side pixel data storage element 108. Naturally, other pixel driving arrangements as known by the skilled person are equally possible.

[0055] As mentioned above, the intermediate storage block 202 is connected between the selection block 102 and the driver block 110. More specifically, the intermediate storage block 202 is connected at the node V_{int} to the selection block 102. Further, the intermediate storage block 202 is connected to the driver block 110 at the node V_x .

[0056] The intermediate storage block 202 comprises an intermediate pixel data storage element 208, a latch transistor 206 and a forwarding transistor 210.

[0057] In the example of Fig. 2A, the intermediate pixel data storage element is a capacitor 208. The intermediate pixel data storage element 208 is connected at the node V_{int} to the selection block 102, and to ground.

[0058] Hereby, since the selection block 102 is configured to receive pixel data on the data line 105 upon assertion of the selection line 104, upon assertion of the selection line 104, the voltage on the data line 105 will charge the intermediate pixel data storage element 208.

[0059] Further, the intermediate storage block 202 is connected to the driver-side pixel data storage element 108 at the node V_x , and to a latch line LATCH 204.

[0060] In the example of Fig. 2A, the intermediate storage block 202 comprises a latch transistor 206 connected at a gate terminal to the latch line 204, so that the latch line 204 controls the latch transistor 206. The latch transistor is at a drain terminal connected to the supply voltage V_{DD} and at its source terminal to a drain terminal of the forwarding transistor 210.

[0061] The gate terminal of the forwarding transistor 210 is connected to the selection block 102 and the intermediate pixel data storage element 208 through the node V_{int} . Hereby, the forwarding transistor 210 is controlled by the voltage present on the upper plates of the intermediate pixel data storage element 208. Thus, the forwarding transistor is configured as a source-follower.

[0062] At a source terminal opposite to the drain terminal connected to the latch transistor 204, the forwarding transistor 210 is connected to the driver-side pixel data storage element 108 through the node V_x .

[0063] Thus, through this arrangement, the pixel circuit is configured so that the pixel data input on said data line is transferred to said intermediate pixel data storage element upon assertion of the selection line 104, and so that pixel data is transferred from the intermediate pixel data storage element 208 to the driver-side pixel data storage element 108 upon assertion of the latch line 204. The skilled person could naturally contemplate other arrangement for configuring this functionality.

[0064] An example of operation of the pixel circuit 200 will now be exemplified with reference to the timing diagram of Fig. 2B for driving a display comprising a plurality

of pixel circuits 200 of Fig. 2A. In conjunction herewith, a method example of updating a display comprised of pixels each associated with a respective pixel circuit 200 will be disclosed. While exemplified herein for the pixel circuit 200 of Fig. 2A, the method example is equally valid, mutatis mutandis, for displays comprising the pixel circuits 300 of Fig. 3 (see below) or 400 of Fig. 4 (also see below).

[0065] Fig. 2C shows a display 280 comprised of pixels each associated with a respective pixel circuit 200. Just as explained above in conjunction with Fig. 1B, pixels may be organized in columns and rows. Data lines DATA1, DATA2, DATA3... DATAM may run vertically through the display, while selection lines SEL1, SEL2, SEL3... SELN may run horizontally through the display. Thus, a specific selection line selects a corresponding row of pixels in the display, while the individual pixels of that line then may be addressed through the data lines. Thus, such a row corresponds to a subset of pixels in the display. Furthermore, each pixel circuit 200 may be connected to a same latch line LATCH.

[0066] Through the respective intermediate pixel data storage blocks in each pixel circuit 200, the pixels may be sequentially updated with respective pixel data, such as a respective analog data voltage, i.e., the voltage on the internal node V_{int} (cf. Fig. 2A), at the upper plate of the intermediate pixel data storage element 208 in the pixel circuit may be refreshed like in the 2T1C pixel circuit of Fig. 1A. Thus, in a pixel data update procedure, pixel data may be refreshed by sequentially selecting each selection line, while applying a corresponding pixel data voltage to each data line.

[0067] However, furthermore, when all data stored in intermediate pixel data storage elements 208 of each pixel circuit has been refreshed, the global, i.e., common, LATCH line 204, common to each pixel circuit of the display may be activated, allowing the voltage stored in the intermediate pixel data storage element 208 to pass to the driver-side pixel data storage element 108 and driver block 110.

[0068] The method example may be implemented in a display controller 282, connected to each data line DATAi 105, each selection line SELj 104 and the single latch line LATCH 204. Further, there may be provided a non-transitory computer-readable storage medium having stored thereon instructions for implementing the method, when executed on a device having processing capabilities.

[0069] This is exemplified for a single data line DATAi in Fig. 2B, corresponding to a specific column of pixels. The timing diagram is provided for reading in new data of two consecutive frames (frame a and frame b). Schematically shown are voltages on selection lines SEL1, SEL2, ..., SEL N, on nodes V_{x1} , V_{x2} , ..., V_{xN} , i.e., the V_x node of the respective pixel circuit 200, and on nodes V_{int1} , V_{int2} , ..., V_{intN} i.e., the V_{int} node of the respective pixel circuit 200.

[0070] As can be seen, at 250, pixel data d1_a is input

on the DATA_i line while asserting the selection line SEL1. Hereby, d1_a shows up on V_{int1}. Simultaneously, other pixel data may be input on the other DATA lines (not shown in Fig. 2B), with all pixel circuits connected to the SEL1 line forming a subset of pixel circuits in the form of a row of the display. Thus, asserting the selection line SEL1 is asserted for each pixel circuit in the subset of pixel circuits of the plurality of pixel circuits formed by the row.

[0071] At 252, the procedure is repeated with pixel data d2_a while asserting the selection line SEL2 corresponding to a next row of the display, and so on.

[0072] In the pixel circuit asserting the selection line connected to the pixel in question, and inputting a pixel data voltage on the data line, will result in the pixel data being provided to the respective node V_{int}, thereby charging the intermediate pixel data storage element 208 capacitor. Thus, contrary to the situation with the pixel circuit 100, the pixel data thus input will not be immediately visible in the pixel. Instead, it is only stored in the intermediate pixel-data storage element 208, while the instantaneous brightness of the self-emitting pixel element of the respective pixel remains unchanged.

[0073] At 254 with all pixel data having been input for frame a, the common LATCH line may be asserted, i.e., simultaneously, for each pixel circuit of the plurality of pixel circuits, asserting said LATCH line. This results in a simultaneous updating of all pixels.

[0074] At 256, the above steps 250, 252, and 254 be repeated for the subsequent frame b.

[0075] Fig. 3 shows a pixel circuit suitable for employing digital pixel driving. Similarly to Figs 1A and 2A, there is shown a pixel circuit 300, which may form part of a display comprised of self-emitting pixel elements, such as an AMOLED display or an AMLED display. The display may be an active matrix (AM) display.

[0076] The pixel circuit 300 comprises a selection block 102, a driver-side storage element 108, and a driver block 110 and is connectable to a self-emitting pixel-element 112, such as an LED, OLED, or μ LED. Furthermore, just as in Fig. 2A, the pixel circuit 300 comprises an intermediate storage block 202, connected between the selection block 102 and the driver-block 110, as will be elaborated further upon below.

[0077] Just as in Figs 1A and 2A, the selection block 102 is connected to a selection line 104 and to a data line 105. In the shown implementation, the selection block comprises a selection transistor 106, where a gate terminal of the selection transistor 106 is connected to the selection line 104, so that the selection transistor 106 is controlled by the selection line 104, and where a source or drain terminal of the selection transistor 106 is connected to the data line 105. Thereby, the selection block 102 is configured to receive pixel data on the data line 105 upon assertion of the selection line 104. The other source or drain terminal of the selection transistor 106 is connected at a node V_{int} to the intermediate storage block 202, and in particular to the intermediate pixel data stor-

age element 208.

[0078] It should be noted that the present inventive concept is by no means limited to the selection block being comprised of a single selection transistor 106. Rather, other designs, for example, comprising several transistors and/or logic gates, etc, as known by the skilled person, are equally possible.

[0079] In the example of Fig. 3, just as in Figs 1A and 2A the driver block 110 comprises a driver transistor 114 connectable in series with the self-emitting pixel element 112 between a supply voltage V_{DD} and ground. Further, the gate terminal of the driver transistor 114 is connected to the inverter 302.

[0080] The driver-side storage element 108 is in the example of Fig. 3 a capacitor 108. It is connected between the node V_x and ground, i.e., between the intermediate storage block 202 and the source terminal of the driver transistor 114 opposite to the self-emitting pixel element 112.

[0081] Through the above, the driver block 110 is connectable to the self-emitting pixel element 112 for driving the self-emitting pixel element 112, wherein an instantaneous brightness of the self-emitting pixel element 112 is controlled based on said driver-side pixel data storage element 108. Naturally, other pixel driving arrangements as known by the skilled person are equally possible.

[0082] As mentioned above, just as in Figs 1A and 2A, the intermediate storage block 202 is connected between the selection block 102 and the driver block 110. More specifically, the intermediate storage block 202 is connected at the node V_{int} to the selection block 102. Further, the intermediate storage block 202 is connected to the driver block 110 at the node V_x.

[0083] In the pixel circuit 300 of Fig. 3, and differently from the pixel circuit 200 of Fig. 2A, the intermediate storage block 202 comprises an intermediate pixel data storage element 208 and a latch transistor 206.

[0084] In the example of Fig. 3, the intermediate pixel data storage element is a capacitor 208. The intermediate pixel data storage element 208 is connected at the node V_{int} to the selection block 102, and to ground.

[0085] Hereby, as in Figs 1A and 2A, since the selection block 102 is configured to receive pixel data on the data line 105 upon assertion of the selection line 104, upon assertion of the selection line 104, the voltage on the data line 105 will charge the intermediate pixel data storage element 208.

[0086] Further, the intermediate storage block 202 is connected to the driver-side pixel data storage element 108 at the node V_x, and to a latch line 204.

[0087] The latch transistor 206 is connected at its gate terminal to the latch line 204, so that the latch line 204 controls the latch transistor 206. Furthermore, the latch transistor 206 is at a source or drain terminal connected at the node V_{int} to the selection transistor 106 of the selection block 102 and to the upper plate of the intermediate pixel data storage element 208. At the other source or drain terminal, the latch transistor 206 is connected at

the node V_x to the upper plate of the driver-side pixel data storage element 108 and an inverter 302. The inverter 302 is further connected to the gate terminal of the driver transistor 114, so that the driver-side pixel-data storage element 108 controls the driver transistor 114 through the inverter 302.

[0088] The inverter 302 serves to keep the full signal swing at the driving block 110. This inverter could be replaced by another logic gate, such as, e.g., a buffer. Thus, generally, the driver-side pixel data storage element may be connected to a logic gate, and the logic gate may be connected to the driver block. Another example will be given below in conjunction with Fig. 4.

[0089] Thus, also through this arrangement, the pixel circuit is configured so that the pixel data input on the data line is transferred to the intermediate pixel data storage element upon assertion of the selection line 104, and so that pixel data is transferred from the intermediate pixel data storage element 208 to the driver-side pixel data storage element 108 upon assertion of the latch line 204. The skilled person could naturally contemplate other arrangement for configuring this functionality, as known in the art.

[0090] The pixel circuit 300 of Fig. 3 is suitable for use when the data voltage applied to the pixel is a digital voltage, e.g., when using PWM digital signals to set gray levels. The new data is read into the storage element like in the pixel circuit 200 of Fig. 2A, but the circuitry to allow passing the data when the latch signal is activated is different. Nevertheless, the principle as per the present inventive concept remains the same.

[0091] Fig. 4 shows a pixel circuit 400. The pixel circuit 400 is identical to the pixel circuit 300 of Fig. 3, with the exception that the inverter 302 of the pixel circuit 300 of Fig. 3 has been replaced with a NOR gate 402, which at an output is connected to the gate terminal of the driver transistor 114 of the driver block 110. Further, at one of its inputs, the NOR gate 402 is connected to the intermediate pixel data storage block 202 at the node V_x . Further, a second input of the NOR gate is connected to a reset line 406.

[0092] The inverter is replaced by another logic gate, more specifically the NOR gate, allowing both simultaneously updating digital data voltages for all pixels and resetting all pixels simultaneously.

[0093] Instead of a NOR gate, the use of a NAND gate is equally possible, in particular in the case of using PMOS transistors.

[0094] It should be noted that additional buffers, inverters, or other logical gates may be inserted in the schematics for digital driving (Figs 3 and 4) to improve signal integrity. When the latch line 204 is asserted, there will be charge redistribution between the two capacitances 108, 208 on either side of the latch transistor 206. With adequately designed capacitances, this may be manageable. Otherwise an additional buffer/inverter may be inserted, e.g. between the intermediate pixel data storage element capacitor 208 and the latch transistor 206.

[0095] In the above the inventive concept has mainly been described with reference to a limited number of examples. However, as is readily appreciated by a person skilled in the art, other examples than the ones disclosed above are equally possible within the scope of the inventive concept, as defined by the appended claims.

[0096] In particular, although this description discloses a limited number pixel circuits, it should be noted that many different embodiments are possible without going beyond the scope of the invention. For example, the scope of the present inventive concept is not limited to n-type transistor pixel circuits, but can also be applied to p-type or mixed (CMOS) transistor pixel circuits. Moreover, the present inventive concept is not limited to the disclosed relatively simple pixel circuits, but can also be applied to more complex pixel circuits, as contemplatable by the skilled person, within the scope of the claims.

Claims

1. A pixel circuit (200, 300, 400) integrable as part of a display (280), said pixel circuit (200, 300, 400) comprising:

a selection block (102) connected to a selection line (104) and to a data line (105) and configured to receive pixel data on said data line (105) upon assertion of said selection line (104);

a driver-side pixel data storage element (108); and

a driver block (110) connectable to a self-emitting pixel element (112) for driving said self-emitting pixel element (112), wherein an instantaneous brightness of said self-emitting pixel element (112) is controlled based on said driver-side pixel data storage element (108),

said pixel circuit (200, 300, 400) being **characterized by** further comprising:

an intermediate storage block (202) comprising an intermediate pixel data storage element (208) and connected to said selection block (102), to said driver-side pixel data storage element (108), and to a latch line (204), wherein said pixel circuit (200, 300, 400) is configured so that the pixel data input on said data line (105) is transferred to said intermediate pixel data storage element (208) upon assertion of said selection line (104), and so that pixel data is transferred from said intermediate pixel data storage element (208) to said driver-side pixel data storage element (108) upon assertion of said latch line (204).

2. The pixel circuit of claim 1, wherein said intermediate storage block (202) comprises a latch transistor (206) controlled by said latch line (204).
3. The pixel circuit of claim 2, wherein said intermediate

storage block (202) further comprises a forwarding transistor (210), wherein said latch transistor (206) is connected to a supply voltage and to said forwarding transistor (210) and said forwarding transistor (210) is controlled by said intermediate pixel data storage element (208) and further is connected to said driver-side pixel data storage element (108).

4. The pixel circuit of claim 2, wherein said latch transistor (206) is connected to said intermediate pixel data storage element (208) and to said driver-side pixel data storage element (108). 10
5. The pixel circuit of claim 4, wherein said driver-side pixel data storage element (108) is connected to a logic gate (302, 402), and said logic gate (302, 402) is connected to said driver block (110). 15
6. The pixel circuit of claim 4, wherein said logic gate (302) is a buffer or inverter. 20
7. The pixel circuit of claim 4, wherein said logic gate (402) is a NOR gate or NAND gate connected to a reset line. 25
8. The pixel circuit of any one of claims 1-7, wherein said selection block (102) comprises a selection transistor (106) controlled by said selection line (104) and connected to said data line (105) and to said intermediate pixel data storage element (208). 30
9. The pixel circuit of any one of claims 1-8, wherein said driver block (110) comprises a driver transistor (114) connectable in series with said self-emitting pixel element (112) and controlled by said driver-side pixel-data storage element (108). 35
10. The pixel circuit of any one of claims 1-9, wherein said intermediate pixel data storage element (208) and/or said driver-side pixel data storage element (108) is a capacitor. 40
11. A display (280) comprising a plurality of pixel circuits (200, 300, 400) according to any one of claims 1-10. 45
12. A method of updating the display according to claim 11, said method comprising:

performing a pixel data update procedure, said procedure comprising simultaneously asserting (250) said selection line for each pixel circuit in a subset of pixel circuits of said plurality of pixel circuits while inputting pixel data on each respective data line of each pixel circuit of said subset of pixel circuits, wherein said pixel data update procedure is repeated (252), sequentially in time, for different subsets of said plurality of pixel circuits; and, thereafter, 50 55

simultaneously, for each pixel circuit of said plurality of pixel circuits, asserting (254) said latch line.

- 5 13. The method of claim 12, wherein each said subset corresponds to a row of pixels in said display.
14. A display controller (282) configured to carry out the method of any one of claims 12-13.
15. A non-transitory computer-readable storage medium having stored thereon instructions for implementing the method according to any one of claims 12-13, when executed on a device having processing capabilities.

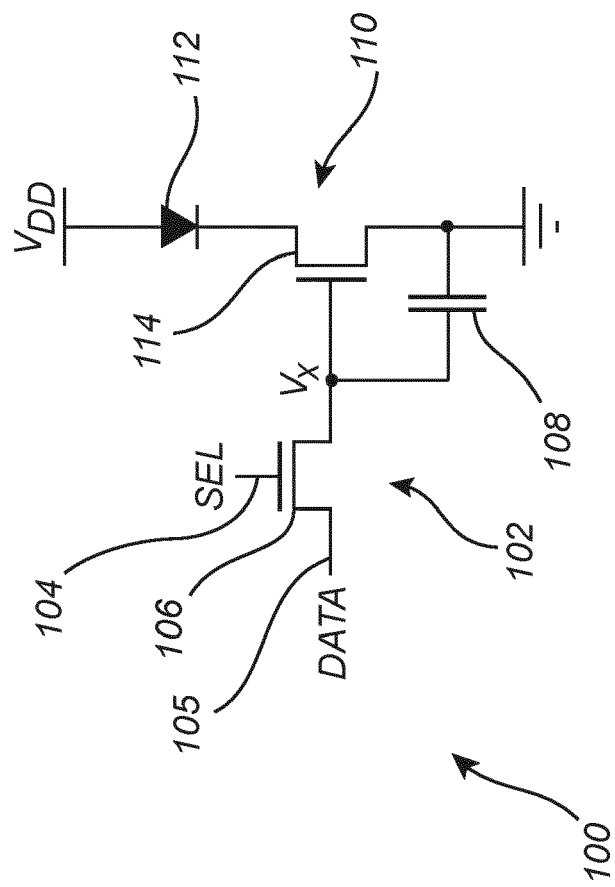


Fig. 1A

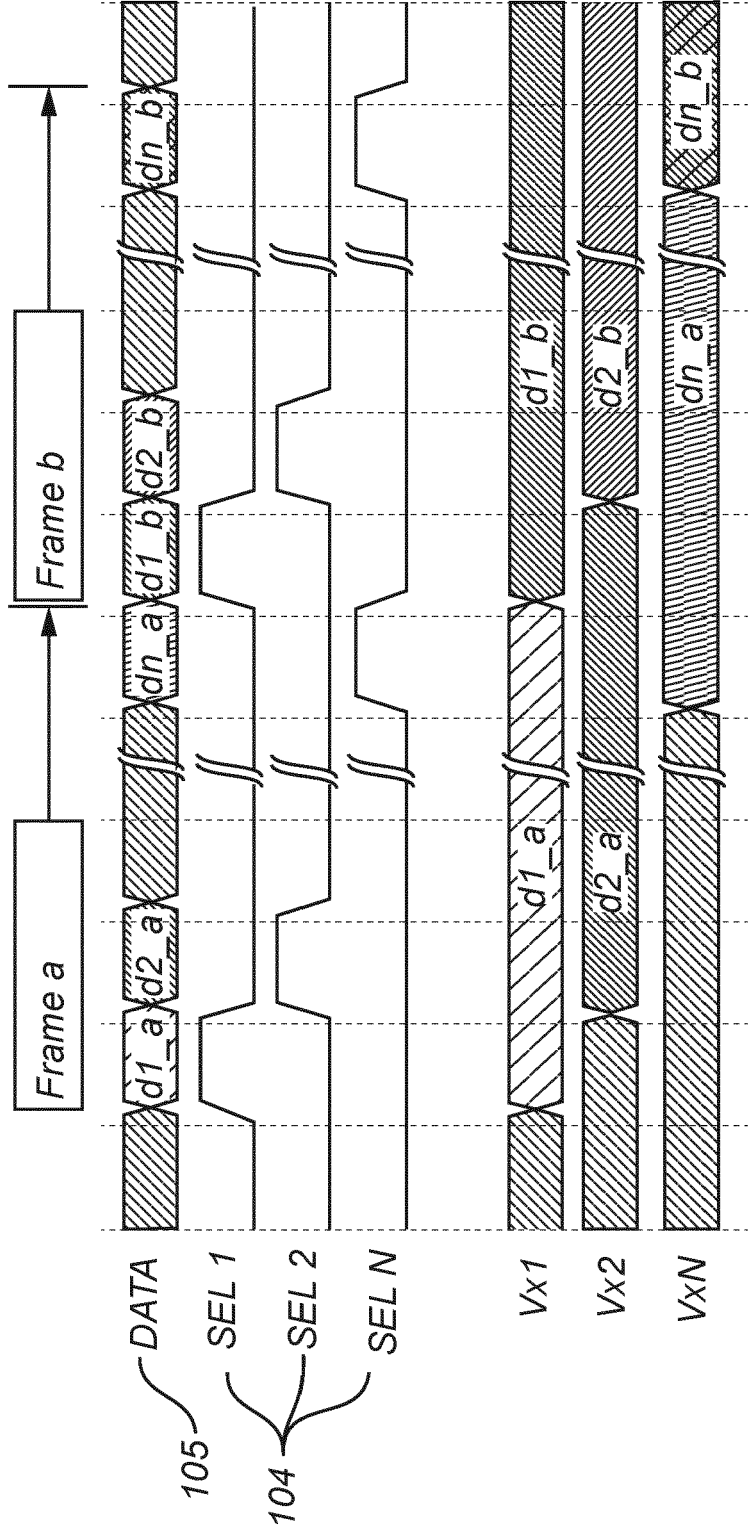


Fig. 1B

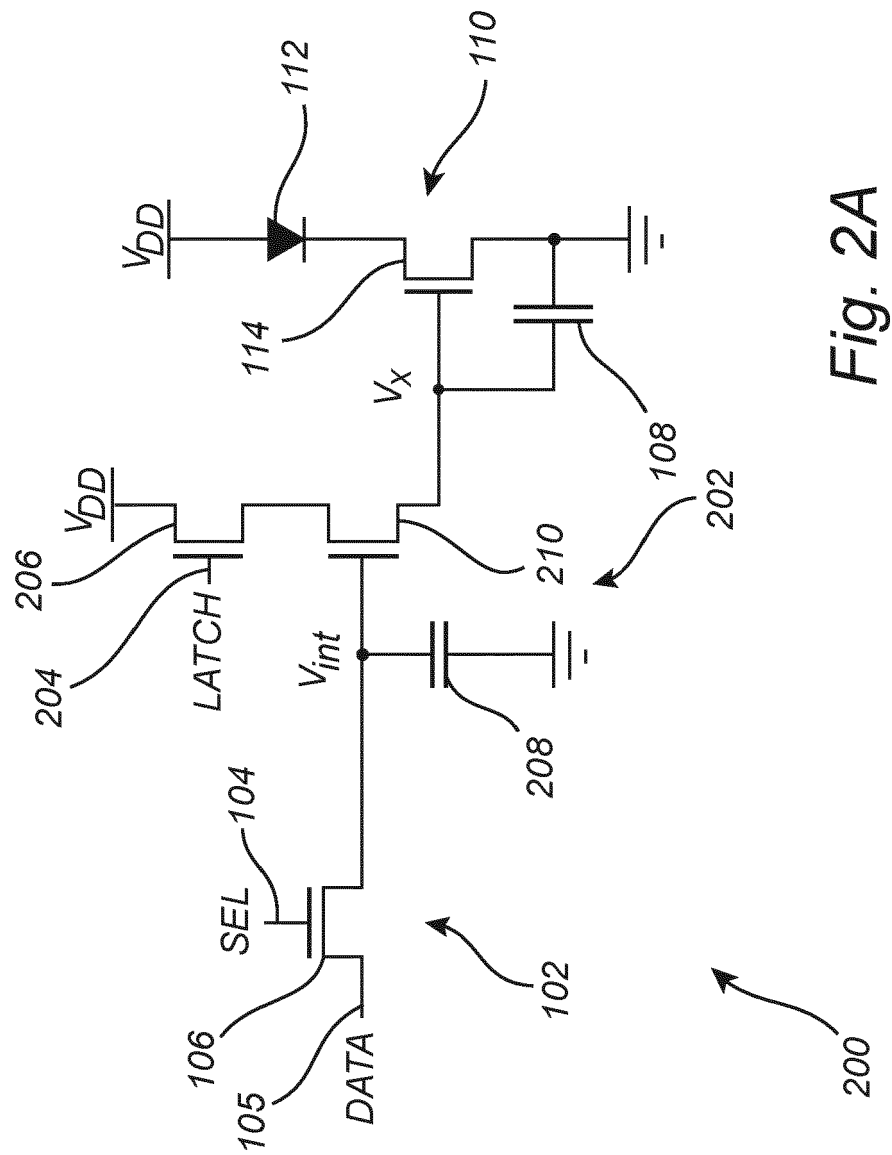


Fig. 2A

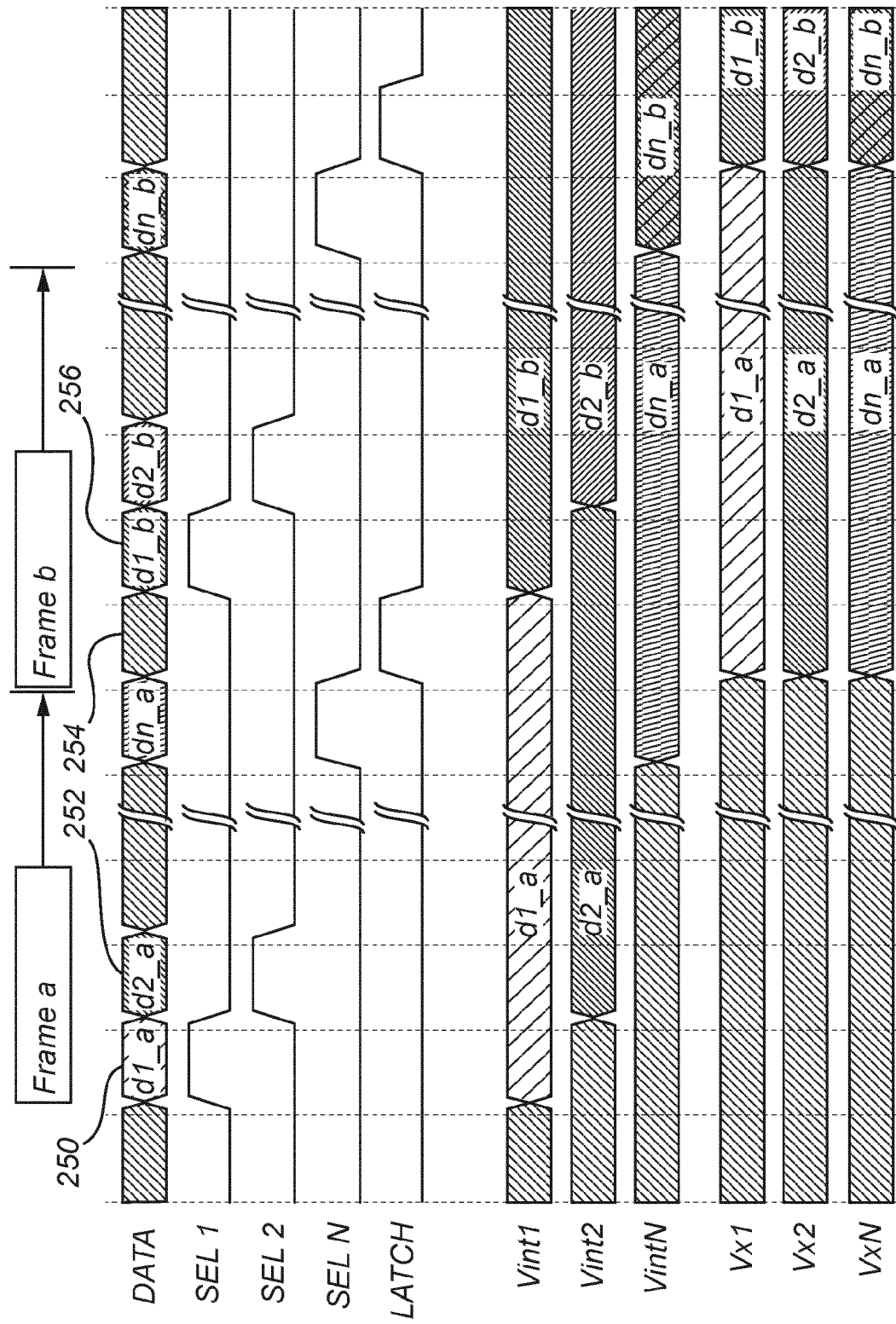


Fig. 2B

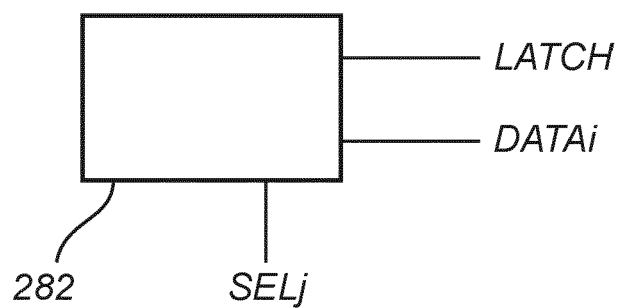
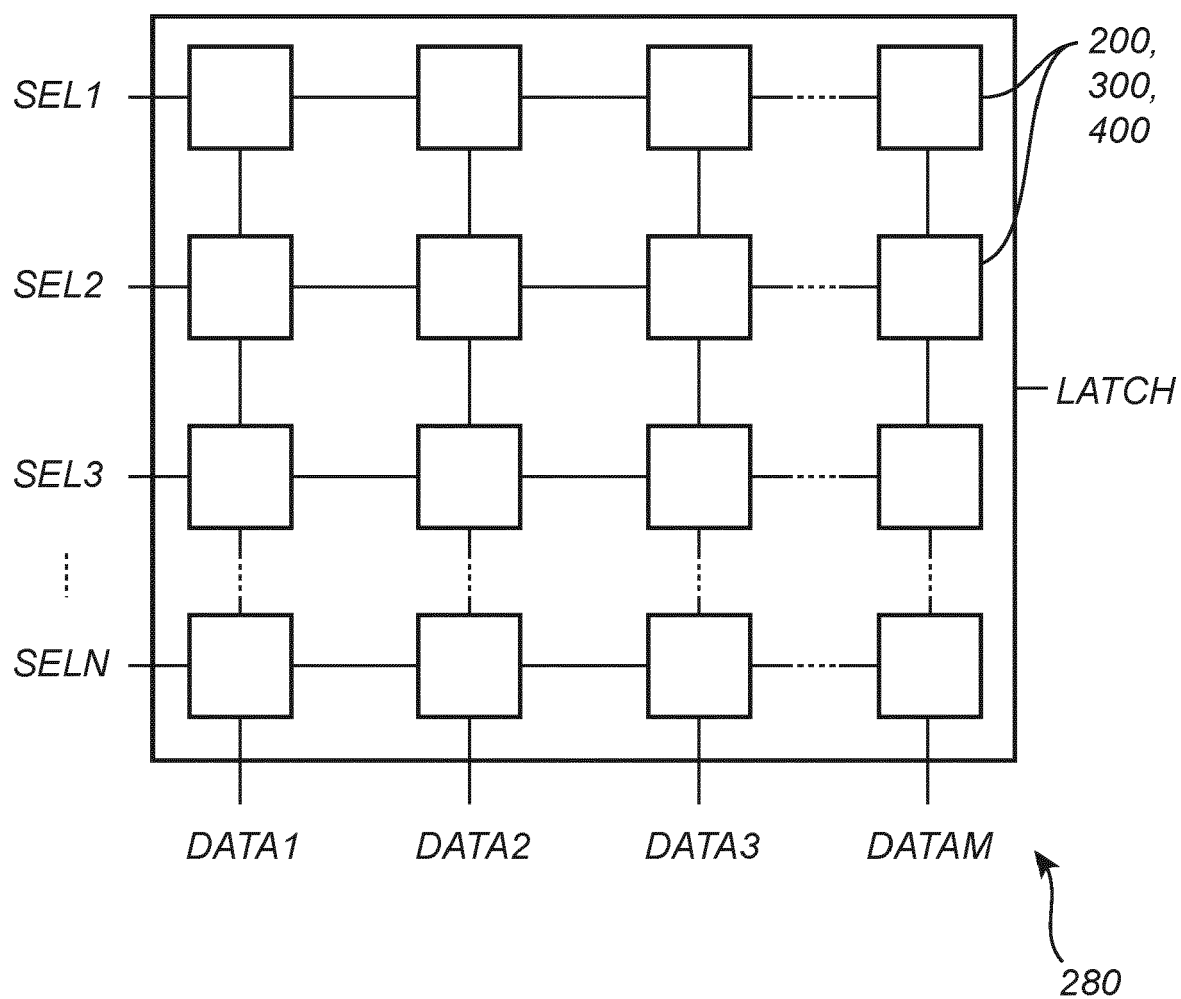


Fig. 2C

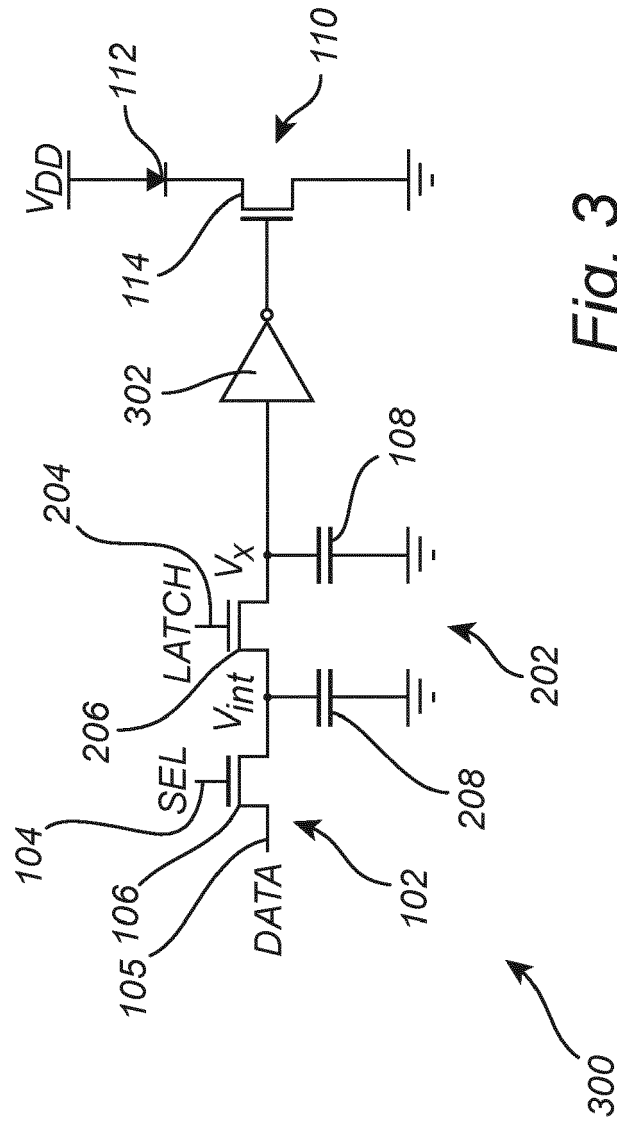


Fig. 3

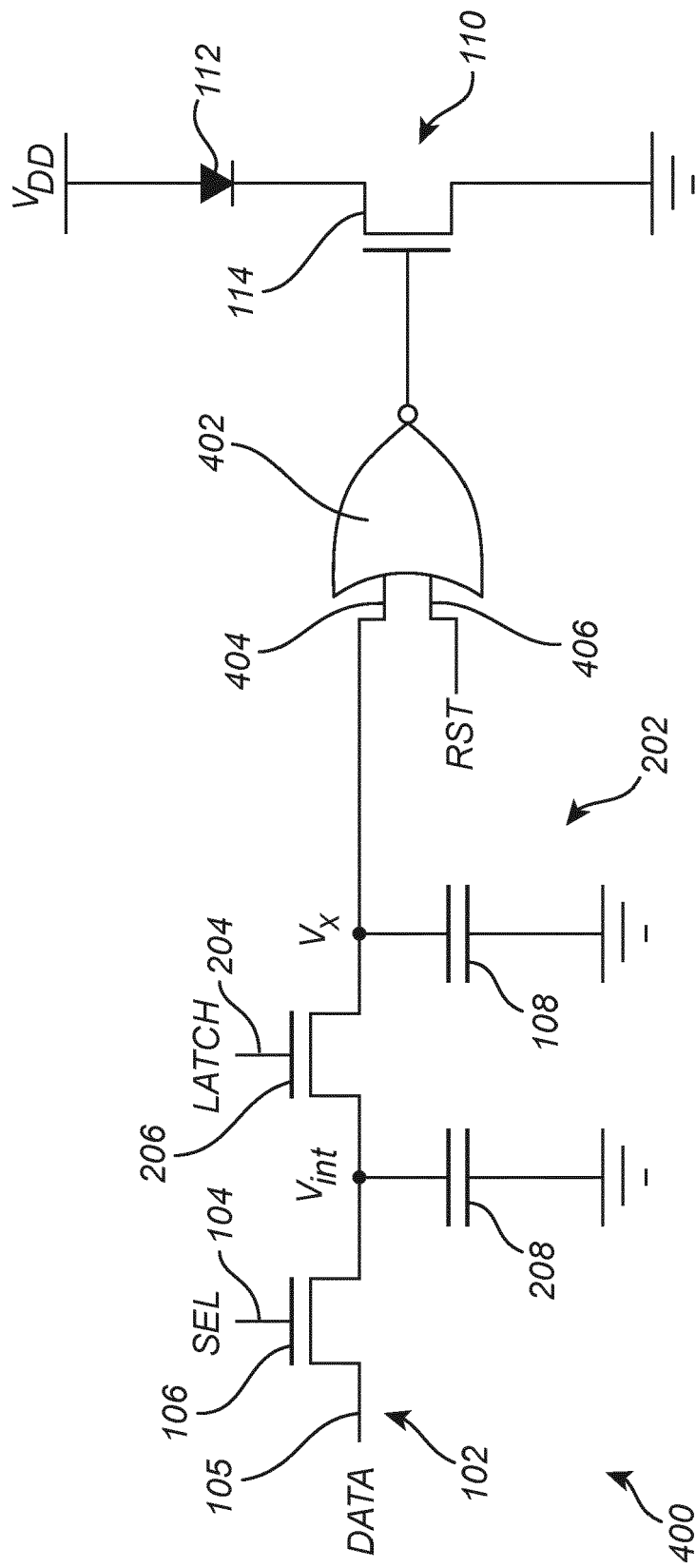


Fig. 4



EUROPEAN SEARCH REPORT

Application Number

EP 21 20 6318

DOCUMENTS CONSIDERED TO BE RELEVANT

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2018/144682 A1 (TAO YI [US] ET AL) 24 May 2018 (2018-05-24)	1, 2, 4, 8-15	INV. G09G3/3233
Y	* paragraph [0010] - paragraph [0038];	5-7	
A	figures 1-5 *	3	
Y	JP 2004 198683 A (SEMICONDUCTOR ENERGY LAB) 15 July 2004 (2004-07-15) * paragraph [0007] - paragraph [0052]; figures 1-11 *	5, 6	
Y	US 2004/196221 A1 (SHIH LI-WEI [TW]) 7 October 2004 (2004-10-07) * paragraph [0019] - paragraph [0023]; figure 2 *	5, 6	TECHNICAL FIELDS SEARCHED (IPC) G09G
Y	US 2020/020275 A1 (LI BO [US]) 16 January 2020 (2020-01-16) * paragraph [0018] - paragraph [0048]; figures 1a-2b *	5, 7	
The present search report has been drawn up for all claims			
Place of search Munich			
Date of completion of the search 14 June 2022			
Examiner Harke, Michael			
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone			
Y : particularly relevant if combined with another document of the same category			
A : technological background			
O : non-written disclosure			
P : intermediate document			
T : theory or principle underlying the invention			
E : earlier patent document, but published on, or after the filing date			
D : document cited in the application			
L : document cited for other reasons			
& : member of the same patent family, corresponding document			

EPO FORM 1503 03/82 (P04C01)



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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).



LACK OF UNITY OF INVENTION SHEET B

Application Number

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The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-4, 8-15

The first invention concerns a device as claimed in claim 1, i.e. a pixel circuit integrable as part of a display, said pixel circuit comprising: a selection block connected to a selection line and to a data line and configured to receive pixel data on said data line upon assertion of said selection line; a driver-side pixel data storage element; and a driver block connectable to a self-emitting pixel element for driving said self-emitting pixel element, wherein an instantaneous brightness of said self-emitting pixel element is controlled based on said driver-side pixel data storage element, said pixel circuit further comprising: an intermediate storage block comprising an intermediate pixel data storage element and connected to said selection block, to said driver-side pixel data storage element, and to a latch line, wherein said pixel circuit is configured so that the pixel data input on said data line is transferred to said intermediate pixel data storage element upon assertion of said selection line, and so that pixel data is transferred from said intermediate pixel data storage element to said driver-side pixel data storage element upon assertion of said latch line, wherein, as claimed in claim 3, said intermediate storage block further comprises a forwarding transistor, wherein said latch transistor is connected to a supply voltage and to said forwarding transistor and said forwarding transistor is controlled by said intermediate pixel data storage element and further is connected to said driver-side pixel data storage element.

2. claims: 5-7

The second invention concerns a device as claimed in claim 1 (see the first invention for further details), wherein, as claimed in claim 5, said driver-side pixel data storage element is connected to a logic gate, and said logic gate is connected to said driver block.

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 21 20 6318

5 This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-06-2022

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US 2018144682 A1	24-05-2018	CN 108091297 A	29-05-2018
		EP 3545514 A1	02-10-2019
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