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(71) Applicant: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95054 (US).

(72) Inventors: **BLACKWELL, James M.**; 2637 SW Patton Court, Portland, Oregon 97201 (US). **BRISTOL, Robert L.**; 9325 NW Skyline Boulevard, Portland, Oregon 97231 (US). **KRYSAK, Marie**; 536 NE Thompson Street, Apt A, Portland, Oregon 97212 (US). **EL-MANSY, Mohamed H.**; 8680 SW 190th Avenue, Aloha, Oregon 97007 (US). **LIN, Kevin L.**; 19953 SW Mohican Street, Beaverton, Oregon 97006 (US). **SCHENKER, Richard E.**; 15151 NW Casey

Drive, Portland, Oregon 97229 (US). **GSTREIN, Florian**; 2523 NE 10th Avenue, Portland, Oregon 97212 (US).

(74) Agent: **BRASK, Justin, K.** et al.; Schwabe, Williamson & Wyatt, 1211 SW 5th Ave., Suite 1900, Portland, OR 97204 (US).

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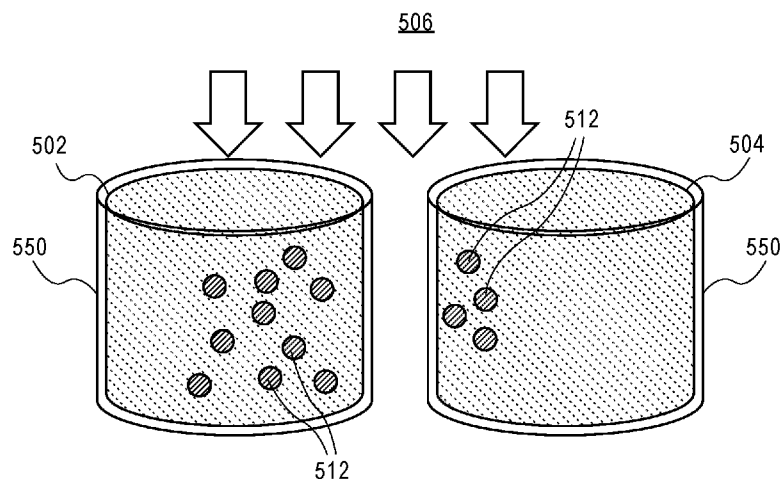


FIG. 5

(57) Abstract: Photoresists with electron-activated photosensitizers for confined patterning lithography, e.g., for fabricating back end of line (BEOL) interconnects, and the resulting structures, are described. In an example, an integrated circuit structure includes a first layer of an interconnect structure above a substrate, the first layer including a first grating of alternating metal lines and dielectric lines in a first direction. A second layer of the interconnect structure is above the first layer. The second layer includes a second grating of alternating metal lines and dielectric lines in a second direction, perpendicular to the first direction. A region of dielectric material is between the metal lines of the first grating and the metal lines of the second grating. The region of dielectric material includes a cross-linked photolizable material having a bottom and sidewall surfaces lined with a layer including electron-activated photosensitizers.

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PHOTORESIST WITH ELECTRON-ACTIVATED PHOTSENSITIZERS FOR CONFINED PATTERNING LITHOGRAPHY

TECHNICAL FIELD

5 Embodiments of the disclosure are in the field of semiconductor structures and processing and, in particular, photoresists with electron-activated photosensitizers for confined patterning lithography, e.g., for fabricating back end of line (BEOL) interconnects.

BACKGROUND

10 For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products
15 with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

 Integrated circuits commonly include electrically conductive microelectronic structures, which are known in the art as vias, to electrically connect metal lines or other interconnects above the vias to metal lines or other interconnects below the vias. Vias are typically formed by
20 a lithographic process. Representatively, a photoresist layer may be spin coated over a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to as a via opening.
25 Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

BRIEF DESCRIPTION OF THE DRAWINGS

 Figures 1A-1C illustrates cross-sectional views and corresponding plan views of various
30 operations in a method of patterning using photobuckets including a photoresist composition having electron-activated photosensitizers, in accordance with an embodiment of the present disclosure.

 Figures 2A-2C illustrates cross-sectional views and corresponding plan views of various operations in a method of patterning using photobuckets including a photoresist structure
35 including a grafted layer having electron-activated photosensitizers, in accordance with an

embodiment of the present disclosure.

Figure 3 illustrates a cross-sectional view of a conventional resist photobucket structure following photobucket development after a mis-aligned exposure.

Figure 4 illustrates a schematic view of an operation in a method of patterning using photobuckets, in accordance with an embodiment of the present disclosure.

Figure 5 illustrates a schematic view of an operation in another method of patterning using photobuckets, in accordance with another embodiment of the present disclosure.

Figure 6 illustrates a schematic view of an operation in another method of patterning using photobuckets, in accordance with another embodiment of the present disclosure.

Figures 7A-7H illustrate portions of integrated circuit layers representing various operations in a method of subtractive self-aligned via patterning using photobuckets including a photoresist having electron-activated photosensitizers, in accordance with an embodiment of the present disclosure, where:

Figure 7A illustrates a cross-sectional view of a starting structure following deposition, but prior to patterning, of a hardmask material layer formed on an interlayer dielectric (ILD) layer;

Figure 7B illustrates the structure of Figure 7A following first time patterning of the first hardmask layer and subsequent first photobucket fill;

Figure 7C illustrates the structure of Figure 7B following second time patterning of the first hardmask layer and subsequent second photobucket fill;

Figure 7D illustrates the structure of Figure 7C following planarization to isolate the first and second photobuckets from one another;

Figure 7E illustrates the structure of Figure 7D following exposure and development of select photobuckets to leave select via locations;

Figure 7F illustrates the structure of Figure 7E following etching to form via locations;

Figure 7G illustrates the structure of Figure 7F following preparation for metal fill; and

Figure 7H illustrates the structure of Figure 7G following metal fill.

Figures 8A-8I illustrate portions of integrated circuit layers representing various operations in a method of subtractive self-aligned via patterning using photobuckets including a photoresist having electron-activated photosensitizers, in accordance with another embodiment of the present disclosure, where:

Figure 8A illustrates a starting point structure for a subtractive via process following deep metal line fabrication;

Figure 8B illustrates the structure of Figure 8A following recessing of the metal lines;

Figure 8C illustrates the structure of Figure 8B following formation of an inter layer

dielectric (ILD) layer;

Figure 8D illustrates the structure of Figure 8C following deposition and patterning of a hardmask layer;

Figure 8E illustrates the structure of Figure 8D following trench formation defined using the pattern of the hardmask of Figure 8D;

Figure 8F illustrates the structure of Figure 8E following photobucket formation using a photoresist composition having electron-activated photosensitizers in all possible via locations;

Figure 8G illustrates the structure of Figure 8F following via location selection;

Figure 8H illustrates the structure of Figure 8G following conversion of the remaining photobuckets to permanent ILD material; and

Figure 8I illustrates the structure of Figure 8H following metal line and via formation.

Figure 9 illustrates a computing device in accordance with one implementation of an embodiment of the present disclosure.

Figure 10 is an interposer implementing one or more embodiments of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

In the past, the sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset components, graphics chips, etc.). One measure of the size of the vias is the critical dimension of the via opening. One measure of the spacing of the vias is the via pitch. Via pitch represents the center-to-center distance between the closest adjacent vias.

When patterning extremely small vias with extremely small pitches by such lithographic processes, several challenges present themselves, especially when the pitches are around 70 – 90 nanometers (nm) or less and/or when the critical dimensions of the via openings are around 35nm or less. One such challenge is that the overlay between the vias and the overlying interconnects, and the overlay between the vias and the underlying landing interconnects, generally need to be controlled to high tolerances on the order of a quarter of the via pitch. As via pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than lithographic equipment is able to keep up.

Another such challenge is that the critical dimensions of the via openings generally tend to scale faster than the resolution capabilities of the lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the via openings. However, the shrink amount tends to be limited by the minimum via pitch, as well as by the ability of the shrink process to be

sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) and/or critical dimension uniformity (CDU).

Yet another such challenge is that the LWR and/or CDU characteristics of photoresists generally need to improve as the critical dimensions of the via openings decrease in order to maintain the same overall fraction of the critical dimension budget. However, currently the LWR and/or CDU characteristics of most photoresists are not improving as rapidly as the critical dimensions of the via openings are decreasing.

A further such challenge is that the extremely small via pitches generally tend to be below the resolution capabilities of even extreme ultraviolet (EUV) lithographic scanners. As a result, commonly several different lithographic masks may be used, which tend to increase the costs. At some point, if pitches continue to decrease, it may not be possible, even with multiple masks, to print via openings for these extremely small pitches using EUV scanners.

Thus, improvements are needed in the area of back end metallization manufacturing technologies for fabricating metal vias.

Photoresists with electron-activated photosensitizers for confined patterning lithography, e.g., for fabricating back end of line (BEOL) interconnects are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

One or more embodiments described herein are directed to resists including electron-activated photosensitizers or photoresist structures including a photoresist proximate to a layer including electron-activated photosensitizers. Applications may be directed toward one or more

of confined lithography, deep ultra-violet (DUV), extreme ultra-violet (EUV) lithography, electron beam (e-beam) lithography, general lithography applications, solutions for overlay issues, and general photoresist technologies. In an embodiment, materials are described that are suitable for improving performance of so-called "PhotoBucket" based approaches. In such an approach, a resist material is confined to a pre-patterned hardmask. Select ones of the photobuckets are then removed using a high-resolution lithography tool, e.g., an EUV lithography tool. Specific embodiments may be implemented to improve uniformity of the resist material response across a given photobucket.

Some embodiments described herein relate to photobucket patterning and provide a method for incorporating sensitizers as part of a resist formulation used in the photobuckets. Other embodiments described herein relate to photobucket patterning and provide a method for incorporating sensitizers that are pre-grafted to a surface of a photobucket via electron/photon sensitive linkages. The grafting group may be released from the photobucket sidewalls and floors when exposed to light. Upon low temperature bake processing, the sensitizer may be diffused evenly throughout the photobucket. Subsequent exposure with UV light matched to the sensitizer may be performed for sensitizer activation and energy transfer to a photo-acid generator (PAG) within the photoresist. In one embodiment, the amount of PAG activated will be proportional to amount of photosensitizer released into film.

Approaches described herein may be implemented to lower an EUV (or e-beam) dose normally required for patterning by relying on a lower cost deep UV (DUV) operation to carry out part of a PAG activation operation. Although not so limited, photoresists having electron-activated photosensitizers can be in the form of (1) a photoresist composition having electron-activated photosensitizers (e.g., Figures 1A-1C and 4, described below), or (2) a photoresist structure including a grafted layer having electron-activated photosensitizers (e.g., Figures 2A-2C and 5), or (3) a photoresist structure including an over layer having electron-activated photosensitizers (e.g., Figure 6).

Embodiments described herein may be implemented to enable a "digital" photobucket response, in which an entire photobucket either clears out or does not. In specific embodiments, such a response is more tolerant to edge-placement errors, in which an aerial image does not perfectly align to the photobucket grid. Additionally, photobuckets formed and developed using approaches described herein may be implemented to enable lower dose requirements.

In a first example of one or more of the concepts involved herein, Figures 1A-1C illustrates cross-sectional views and corresponding plan views of various operations in a method of patterning using photobuckets including a photoresist composition having electron-activated photosensitizers, in accordance with an embodiment of the present disclosure.

Referring to Figure 1A, a pre-patterned hardmask 104 is disposed above a substrate 102. The pre-patterned hardmask 104 has openings filled with a photoresist composition 106 having electron-activated photosensitizers. The photoresist composition 106 is confined to the openings in the pre-patterned hardmask 104, e.g., to provide a grid of potential via locations.

5 Referring to Figure 1B, select ones of the photobuckets are subjected to an exposure 107 from a lithography tool. The photoresist composition 106 is exposed with a lithography tool, e.g., an EUV lithography tool or e-beam tool, to select which vias to open. In an embodiment, alignment between the lithography tool and the pre-patterned hardmask 104 grid is imperfect resulting in an asymmetry of exposure in the target bucket and/or partial exposure in the
10 neighboring bucket. As seen in the plan view, the exposure 107 is a displaced aerial image 108.

In an embodiment, the exposure 107 leads to release of the electron-activated photosensitizers. Some activation of photo-acid generator (PAG) to acid may also occur, but below an amount needed for polymer de-protection to occur. With electron-activated photosensitizers released, the released sensitizers can diffuse throughout the photobucket with a
15 low temperature bake, e.g., near glass transition temperature (T_g) of the polymer. In one embodiment, once diffused, a deep UV (DUV) exposure specific to the chromophore of the electron-activated photosensitizers is performed (e.g., 365nm exposure for anthracene-based sensitizer). The DUV exposure, such as a flood exposure, activates the sensitizer but does not activate the PAG directly. The sensitizer in turn activates PAG in proximity, creating acid. In
20 accordance with an embodiment of the present invention, the amount of acid is greater in the photobucket which receives the most EUV or e-beam exposure since a greater amount of sensitizer is within that photobucket. In one embodiment, a second bake operation, e.g., a deprotection bake, is performed following the DUV exposure.

Referring to Figure 1C, although the exposure of Figure 1B may have involved mis-
25 alignment and partial exposure of non-selected photobuckets, only the selected photobuckets are cleared to form openings 120, leaving unselected photobuckets as closed photobuckets 112. Accordingly, in an embodiment, the process ensures only select photobuckets are ultimately opened following exposure 107. As a result, the select locations which receive a greater exposure are ultimately cleared to provide open photobucket locations 120 following
30 development. The non-selected locations which receive no exposure, or only partial exposure but to a lesser extent in the case of mis-alignment, remain as closed photobucket locations 112 following development. It is to be appreciated that the pattern of the structure of Figure 1C can ultimately be used to pattern an underlying substrate of layer, examples of which are described below.

35 In a second example of one or more of the concepts involved herein, Figures 2A-2C

illustrates cross-sectional views and corresponding plan views of various operations in a method of patterning using photobuckets including a photoresist structure including a grafted layer having electron-activated photosensitizers, in accordance with an embodiment of the present disclosure.

5 Referring to Figure 2A, a pre-patterned hardmask 104 is disposed above a substrate 102. The pattern of the pre-patterned hardmask 104 defines a plurality of photo-buckets. In particular, the pre-patterned hardmask 104 has openings filled with a photoresist structure including a grafted layer 200 having an electron-activated photosensitizer. The grafted layer 200 is along a bottom and sidewalls of the photobuckets. A photolyzable composition 202 is formed within the
10 grafted layer 200. In one embodiment, the photolyzable composition 202 includes an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component.

Referring to Figure 2B, select ones of the photobuckets are subjected to an exposure 207 from a lithography tool. A select location (selected photobucket) of the photoresist structure 202/200 are exposed with a lithography tool, e.g., an EUV lithography tool or e-beam tool, to
15 select which vias to open. In an embodiment, alignment between the lithography tool and the pre-patterned hardmask 104 grid is imperfect resulting in an asymmetry of exposure in the target bucket and/or partial exposure in the neighboring bucket.

In an embodiment, the exposure 207 leads to release of the electron-activated photosensitizers 204 via decomposition of the grafting linkage of portions of the grafted layer
20 200. Some activation of photo-acid generator (PAG) to acid may also occur, but below an amount needed for polymer de-protection to occur. With electron-activated photosensitizers 204 released from the sidewall or bottom, the sensitizers can diffuse throughout the photobucket with a low temperature bake, e.g., near glass transition temperature (T_g) of the polymer. In one embodiment, once diffused, a deep UV (DUV) exposure specific to the chromophore of the
25 electron-activated photosensitizers is performed (e.g., 365nm exposure for anthracene-based sensitizer). The DUV exposure, such as a flood exposure, activates the sensitizer but does not activate the PAG directly. The sensitizer in turn activates PAG in proximity, creating acid. In accordance with an embodiment of the present invention, the amount of acid is greater in the photobucket which receives the most EUV or e-beam exposure since a greater amount of
30 sensitizer is within that photobucket. In one embodiment, a second bake operation, e.g., a deprotection bake, is performed following the DUV exposure.

Referring to Figure 2C, although the exposure of Figure 2B may have involved mis-alignment and partial exposure of non-selected photobuckets, only the selected photobucket 208 is cleared to form an opening, leaving unselected photobucket 210 as a closed photobuckets, with
35 patterned resist layer 206. In an embodiment, then, the process ensures only select photobuckets

are ultimately opened following exposure 207. As a result, the select locations which receive a greater exposure are ultimately cleared to provide open photobucket locations following development. The non-selected locations which receive no exposure, or only partial exposure but to a lesser extent in the case of mis-alignment, remain as closed photobucket locations

5 following development.

It is to be appreciated that the pattern of the structure of Figure 2C can ultimately be used to pattern an underlying substrate of layer, examples of which are described below. Such patterning may be performed by etching through any residual of the grafted layer 200 in the open photobucket locations. Alternatively, any residual of the grafted layer 200 in the open

10 photobucket locations is removed prior to using the structure of Figure 2C as a patterning mask.

To exemplify a scenario where a conventional photoresist is used, contrasting the scenarios described above for Figures 1A-1C and 2A-2C, Figure 3 illustrates a cross-sectional view of a conventional resist photobucket structure following photobucket development after a mis-aligned exposure. A photobucket region 304 is shown as only partially cleared 300 with some residual photoresist 302 remaining. In the case that the photobucket 304 is a selected photobucket, a misaligned exposure 307 only partially clears the photobucket, which may lead to subsequent poor quality fabrication of conductive structure in such locations. In the case that the photobucket 304 is a non-selected photobucket, some unwanted opening 300 occurs, potentially leading to subsequent formation of conductive structures in unwanted locations.

20 In an exemplary photobucket process including a single photoresist composition having electron-activated photosensitizers, Figure 4 illustrates a schematic view of an operation in a method of patterning using photobuckets, in accordance with an embodiment of the present disclosure.

Referring to Figure 4, first 402 and second 404 photobuckets each include a photolyzable composition including an acid-deprotectable photoresist material, a photo-acid-generating (PAG) component 410, and an electron-activated photosensitizer component 412. A misaligned EUV or e-beam exposure 406 is performed on a selected photobucket 402 and a non-selected photobucket 404, which heavily exposes the selected photobucket 402 and partially exposes the non-selected photobucket 404 but to a lesser extent. The photobuckets 402 and 404 are the subjected to a further exposure and development processing, examples of which are described in greater detail below. The selected photobucket 402 is cleared upon development to provide a cleared photobucket. The non-selected photobucket 404 is not cleared upon development and remains a blocked photobucket. In this way, even in the event of a mis-aligned exposure, a digital photobucket response (open or closed only, without partial open) is achieved.

35 It is to be appreciated that not all embodiments require a single photoresist composition.

In an exemplary photobucket process including a multi-component photoresist composition having electron-activated photosensitizers, Figure 5 illustrates a schematic view of an operation in another method of patterning using photobuckets, in accordance with another embodiment of the present disclosure. Referring to Figure 5, first 502 and second 504 photobuckets each include a grafted layer 550 having an electron-activated photosensitizer. The grafted layer 550 is along a bottom and sidewalls of the first 502 and second 504 photobuckets. A photolyzable composition is formed within the grafted layer 550. The photolyzable composition includes an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component. A misaligned EUV or e-beam exposure 506 is performed on a selected photobucket 502 and a non-selected photobucket 504, which heavily exposes the selected photobucket 502 and partially exposes the non-selected photobucket 504 but to a lesser extent, releasing differing amounts of the electron-activated photosensitizer 512 into from the grafted layer 550 into the photolyzable composition. The photobuckets 502 and 504 are the subjected to a further exposure and development processing, examples of which are described in greater detail below. The selected photobucket 502 is cleared upon development to provide a cleared photobucket. The non-selected photobucket 504 is not cleared upon development and remains a blocked photobucket. In this way, even in the event of a mis-aligned exposure, a digital photobucket response (open or closed only, without partial open) is achieved.

In another exemplary photobucket process including a multi-component photoresist composition having electron-activated photosensitizers, Figure 6 illustrates a schematic view of an operation in another method of patterning using photobuckets, in accordance with another embodiment of the present disclosure. Referring to Figure 6, first 602 and second 604 photobuckets each include an over layer 660 having an electron-activated photosensitizer. The over layer 660 is along top surfaces of the first 602 and second 604 photobuckets. A photolyzable composition is below the over layer 660. The photolyzable composition includes an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component. A misaligned EUV or e-beam exposure 606 is performed on a selected photobucket 602 and a non-selected photobucket 604, which heavily exposes the selected photobucket 602 and partially exposes the non-selected photobucket 604 but to a lesser extent, releasing differing amounts of the electron-activated photosensitizer 612 into from the over layer 660 into the photolyzable composition. The photobuckets 602 and 604 are the subjected to a further exposure and development processing, examples of which are described in greater detail below. The selected photobucket 602 is cleared upon development to provide a cleared photobucket. The non-selected photobucket 604 is not cleared upon development and remains a blocked photobucket. In this way, even in the event of a mis-aligned exposure, a digital photobucket response (open or

closed only, without partial open) is achieved.

Referring again to Figures 4, 5, and 6, in accordance with an embodiment of the present disclosure, a method of selecting a photobucket for semiconductor processing includes providing a structure having a first photobucket 402 (or 502 or 602) neighboring a second photobucket 404 (or 504 or 604). The structure is exposed to extreme ultraviolet (EUV) or e-beam radiation 406 (or 506 or 606), where the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket. Subsequent to exposing the structure to EUV or e-beam radiation, a bake of the first and second photobuckets is performed as is described in association with Figures 1A-1C and 2A-2C. Subsequent to performing the bake, the structure is exposed to deep ultraviolet (DUV) radiation, where the first photobucket may be exposed to the DUV radiation to approximately the same extent as the second photobucket. Subsequent to performing the DUV exposure, the structure is developed. The developing opens the first photobucket and leaves the second photobucket closed. In one embodiment, a second bake operation, e.g., a de-protection bake, is performed between the DUV exposure and development.

In an embodiment, exposing the structure to extreme ultraviolet (EUV) or e-beam radiation includes exposing the structure to energy having a wavelength approximately 13.5 nanometers. In another embodiment, exposing the structure to extreme ultraviolet (EUV) or e-beam radiation includes exposing the structure to energy in the range of 5-150 keV. In an embodiment, the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes. In an embodiment, exposing the structure to DUV radiation includes exposing the structure to energy having a wavelength approximately 365 nanometers and, in one embodiment, a flood exposure is implemented.

In any of the above described cases, in an embodiment, developing the structure includes, in the case of positive tone development, immersion or coating with standard aqueous TMAH developer (e.g., in a concentration range from 0.1M – 1M) or other aqueous or alcoholic developer based on tetraalkylammonium hydroxides for 30-120 seconds followed by rinse with DI water. In another embodiment, in the case of negative tone development, developing the structure includes immersion or coating with organic solvents such as cyclohexanone, 2-heptanone, propylene glycol methylethyl acetate or others followed by rinse with another organic solvent such as hexane, heptane, cyclohexane or the like.

Applications of the above described photoresist compositions, structures and approaches may be implemented for to create regular structures covering all possible via (or plug) locations, followed by selective patterning of only the desired features.

To provide further material details, in an embodiment, referring specifically to Figures

1A-1C and 4, photobuckets such as photobuckets 402 and 404 include a photolyzable composition. The photolyzable composition includes an acid-deprotectable photoresist material. The photolyzable composition also includes a photo-acid-generating (PAG) component 410 and an electron-activated photosensitizer component 412.

5 In another embodiment, referring specifically to Figures 2A-2C and 5, photobuckets such as photobuckets 502 and 504 include a grafted layer 550 along a bottom and sidewalls of the first 502 and second 504 photobuckets. The grafted layer 550 includes an electron-activated photosensitizer component. Photobuckets 502 and 504 also include a photolyzable composition formed within the grafted layer 550. The photolyzable composition includes an acid-
10 deprotectable photoresist material and a photo-acid-generating (PAG) component.

In another embodiment, referring specifically to Figure 6, photobuckets such as photobuckets 602 and 604 include an over layer 660 along a top surface of the first 602 and second 604 photobuckets. The over layer 660 includes an electron-activated photosensitizer component. Photobuckets 602 and 604 also include a photolyzable composition formed below
15 the over layer 660. The photolyzable composition includes an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component.

In an embodiment, as referred to herein, the acid-deprotectable photoresist material is an acid-deprotectable material selected from the group consisting of a polymer, a molecular glass, a carbosilane and a metal oxide. In an embodiment, the acid-deprotectable photoresist material
20 includes a material selected from the group consisting of a polyhydroxystyrene, a polymethacrylate, small molecular weight molecular glass versions of a polyhydroxystyrene or a polymethacrylate which contain ester functionality sensitive to acid-catalyzed deprotection to carboxylic acid, a carbosilane, and a metal oxide possessing functionality sensitive to acid catalyzed deprotection or cross-linking. In an embodiment, the acid-deprotectable photoresist
25 material is substantially absorbing at a wavelength of approximately 13.5 nanometers. In an embodiment, the acid-deprotectable photoresist material is substantially absorbing at an energy approximately in the range of 5-150 keV.

In an embodiment, as referred to herein, the PAG component includes a material selected from the group consisting of triethyl, trimethyl and other trialkylsulfonates, where the sulfonate
30 group is selected from the group consisting of trifluoromethylsulfonate, nonanfluorobutanesulfonate, and p-tolylsulfonate, or other examples containing $-\text{SO}_3$ sulfonate anion bound to organic group.

In an embodiment, as referred to herein, the electron-activated photosensitizer component is a PAG sensitizer. In one such embodiment, the PAG sensitizer includes an aromatic material
35 selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and

benzophenone. In an embodiment, the electron-activated photosensitizer component is absorbing at a wavelength of approximately 365nm. In an embodiment, where the electron-activated photosensitizer component is included in a grafted layer (such as grafted layer 550 of Figure 5) or an over layer (such as over layer 660), the electron-activated photosensitizer component is

5 attached to a surface by photo- or electron activated groups such as sulfoniums or phosphoniums.

In an embodiment, in order to maximize an amount of sensitizer released relative to a PAG activated by EUV light or e-beam, the sensitizer is attached to a thin, highly absorbing layer such as a metal oxide layer. The sensitizer can also be designed to seek out PAG during a diffusion bake operation through hydrogen bonding or other type of interaction/reaction. In one

10 embodiment, such an approach provides higher efficiency in a DUV exposure operation minimizing dose needed and lowering the amount of PAG activated along sidewalls where PAG is not proximal.

In an embodiment, the sensitizer can be introduced as a protected sensitizer which only becomes activated by EUV or electron impact. For example, in one embodiment, an anthracene

15 dimer is converted to an anthracene creating a very specific chromophore. Embodiments include use of the sensitizer in bulk or at a surface where (1) EUV or e-beam exposure activates the sensitizer, (2) a first bake diffuses sensitizer throughout the photobucket, (3) UV exposure causes release of photoacid, and (4) a second bake causes acid to deprotect the polymer (solubility switch).

In an exemplary embodiment, approaches described above build on approaches using so-called “photobuckets,” in which every possible feature, e.g. via, is pre-patterned into a substrate. Then, a photoresist is filled into patterned features and the lithography operation is merely used to choose select vias for via opening formation. In a particular embodiment described below, a lithography operation is used to define a relatively large hole above a plurality of photobuckets

20 that include a photoresist having electron-activated photosensitizers, as described above. The electron-activated photosensitizer photobucket approach allows for larger critical dimensions (CD)s and/or errors in overlay while retaining the ability to choose the via of interest.

To provide further context, current fabrication techniques for vias involves a “blind” process in which a via opening is patterned in a stack far above an ILD trench. The via opening

30 pattern is then etched deep down into the trench. Overlay errors accumulate and can cause various problems, e.g., shorts to neighboring metal lines. In an example, patterning and aligning of features at less than approximately 50 nanometer pitch requires many reticles and critical alignment strategies that are otherwise extremely expensive for a semiconductor manufacturing process. In an embodiment, by contrast, approaches described herein enable fabrication of self-

35 aligned plugs and/or vias, greatly simplifying the web of overlay errors, and leaving only one

critical overlay step ($Mx+1$ grating). In an embodiment, then, offset due to conventional lithograph/dual damascene patterning that must otherwise be tolerated, is not a factor for the resulting structures described herein.

In general, one or more embodiments are directed to an approach that employs a subtractive technique to ultimately form conductive vias and, possibly, non-conductive spaces or interruptions between metals (referred to as “plugs”). Vias, by definition, are used to land on a previous layer metal pattern. In this vein, embodiments described herein enable a more robust interconnect fabrication scheme since alignment by lithography equipment is no longer relied on. Such an interconnect fabrication scheme can be used to save numerous alignment/exposures, can be used to improve electrical contact (e.g., by reducing via resistance), and can be used to reduce total process operations and processing time otherwise required for patterning such features using conventional approaches.

More specifically, one or more embodiment described herein involves the use of a subtractive method to pre-form every via or via opening using the trenches already etched. An additional operation is then used to select which of the vias and plugs to retain. Such operations can be illustrated using “photobuckets,” although the selection process may also be performed using a more conventional resist expose and ILD backfill approach.

In one aspect, a self-aligned via opening approach is used. As an example, Figures 7A-7H illustrate portions of integrated circuit layers representing various operations in a method of subtractive self-aligned via patterning using photobuckets including a photoresist having electron-activated photosensitizers, in accordance with an embodiment of the present disclosure. In each illustration at each described operation, cross-sectional views are shown.

Figure 7A illustrates a cross-sectional view of a starting structure 700 following deposition, but prior to patterning, of a first hardmask material layer 704 formed on an interlayer dielectric (ILD) layer 702 formed on a substrate 701, in accordance with an embodiment of the present disclosure. Referring to Figure 7A, a patterned mask 706 has spacers 708 formed along sidewalls thereof, on or above the first hardmask material layer 704.

Figure 7B illustrates the structure of Figure 7A following first time patterning of the first hardmask layer and subsequent first photobucket fill, in accordance with an embodiment of the present disclosure. Referring to Figure 7B, the patterned mask 706 and corresponding spacers 708 are used together as a mask during an etch to form trenches 710 through the first hardmask material layer 704 and partially into the ILD layer 702. The trenches 710 are then filled with first photobuckets 712 which include a photoresist having electron-activated photosensitizers. In one embodiment, the first photobuckets 712 include a photoresist composition having electron-activated photosensitizers. In another embodiment, the first photobuckets 712 include a

photoresist structure having a grafted layer having electron-activated photosensitizers.

Figure 7C illustrates the structure of Figure 7B following second time patterning of the first hardmask layer and subsequent second photobucket fill, in accordance with an embodiment of the present disclosure. Referring to Figure 7C, the patterned mask 706 is removed and a second plurality of trenches 714 is etched through the first hardmask material layer 704 and partially into the ILD layer 702, between spacers 708. Subsequently, the trenches 714 are filled with second photobuckets 718 which include a photoresist having electron-activated photosensitizers. In one embodiment, the second photobuckets 718 include a photoresist composition having electron-activated photosensitizers. In another embodiment, the second photobuckets 718 include a photoresist structure having a grafted layer having electron-activated photosensitizers. In a specific embodiment, the second photobuckets 718 and the first photobuckets 712 are filled with a same photoresist having electron-activated photosensitizers.

Referring again to Figure 7C, the negative pattern of the spacers 708 is thus transferred, e.g., by two etch processes forming trenches 710 and 714, to the first hardmask material layer 704. In one such embodiment, the spacers 708 and, hence, the trenches 710 and 714 are formed with a grating pattern, as is depicted in Figure 7C. In an embodiment, the grating pattern is a tight pitch grating pattern. In a specific such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a pattern based on conventional lithography may first be limited to mask 706, but the pitch may be halved by the use of negative spacer mask patterning, as is depicted in Figures 7A-7C. Even further, although not shown, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, in one embodiment, the grating-like pattern of the photobuckets 712 and 718, collectively, is spaced at a constant pitch and has a constant width.

Figure 7D illustrates the structure of Figure 7C following planarization to isolate the first and second photobuckets from one another, in accordance with an embodiment of the present disclosure. Referring to Figure 7D, the second photobuckets 718 and the top portions of the spacers 708 are planarized, e.g., by chemical mechanical polishing (CMP), until the top surfaces of the first photobuckets 712 are exposed, forming discrete second photobuckets 718. In one embodiment, the combination of first photobuckets 712 and second photobuckets 718 represent all possible via locations in a subsequently formed metallization structure. One of the first photobuckets 712 is labeled as 712A to indicate that it is selected from removal for ultimate via fabrication.

Figure 7E illustrates the structure of Figure 7D following exposure and development of two photobuckets to leave selected via locations, in accordance with an embodiment of the present disclosure. Referring to Figure 7E, a second hardmask 720 is formed and patterned on

the structure of Figure 7D. The patterned second hardmask 720 reveals two of the first photobuckets 712. The selected photobuckets are exposed to light irradiation, such as an extreme UV (EUV) or e-beam exposure 721. It is to be appreciated that description herein concerning forming and patterning a hardmask layer involves, in an embodiment, mask

5 formation above a blanket hardmask layer. The mask formation may involve use of one or more layers suitable for lithographic processing. Upon patterning the one or more lithographic layers, the pattern is transferred to the hardmask layer by an etch process to provide a patterned hardmask layer.

In accordance with one embodiment, referring again to Figure 7E, neighboring one of the
10 second photobuckets 718 are partially exposed, e.g., due to mis-alignment in the patterning of second hardmask 720. In particular, two of the second photobuckets 718 are inadvertently exposed at regions 750, even though they have not been selected as locations for via fabrication. Thus, the selected ones of the first photobuckets 712 are exposed to the EUV or e-beam radiation to a greater extent than the neighboring partially exposed ones of the second photobuckets 718.

15 Subsequent to exposing the structure to EUV or e-beam radiation 721, a bake of the photobuckets is performed. Subsequent to performing the bake, the structure is exposed to deep ultraviolet (DUV) radiation.

In one embodiment, the mask 720 remains during the DUV radiation exposure and is then subsequently removed. However, in another embodiment, the mask 720 is first removed and the
20 photobuckets are then all exposed to the DUV radiation (flood exposure) to approximately the same extent. In either case, subsequent to exposing the structure to DUV radiation, a second bake of the photobuckets may be performed.

Referring again to Figure 7E, the photobuckets are subjected to a develop process. During the develop process, the select one of the first photobuckets 712 targeted for via
25 fabrication are emptied in that the photoresist is removable. However, locations not selected for via fabrication, including the ones of the second photobuckets 718 that were partially exposed at regions 750, are not opened during the develop process, in that the resist material is not removable in the develop process. In an embodiment, as described above, since the ones of the second photobuckets 718 that were partially exposed at regions 750 are only partially exposed
30 and are not select via locations, the electron-activated photosensitizer photobucket approach enables retention of all portions of the second photobuckets 718 that were partially exposed at regions 750. The developing provides selected via openings 713A.

Figure 7F illustrates the structure of Figure 7E following etching to form via locations, in accordance with an embodiment of the present disclosure. Referring to Figure 7F, the pattern of
35 the via openings 713A are subjected to a selective etch process, such as a selective plasma etch

process, to extend the via openings deeper into the underlying ILD layer 702, forming via patterned ILD layer 702' with via locations 724. The etching is selective to remaining photobuckets 712 and 718 and to the spacers 708.

Figure 7G illustrates the structure of Figure 7F in preparation for metal fill, in accordance with an embodiment of the present disclosure. Referring to Figure 7G, all remaining first and second photobuckets 712 and 718 are removed. The remaining first and second photobuckets 712 and 718 may be removed directly, or may first be exposed and developed to enable removal. The removal of the remaining first and second photobuckets 712 and 718 provides metal line trenches 726, some of which are coupled to via locations 724 in patterned ILD layer 702'.

Referring to Figure 7H, subsequent processing can include removal of spacers 708 and hardmask layer 704, and metal fill of metal line trenches 726 and via locations 724 to form conductive metal lines 740 and conductive vias 742, respectively. In one such embodiment, metallization is formed by a metal fill and polish back process. The structure of Figure 7H may subsequently be used as a foundation for forming subsequent metal line/via and ILD layers.

Alternatively, the structure of Figure 7H may represent the final metal interconnect layer in an integrated circuit. It is to be appreciated that the above process operations may be practiced in alternative sequences, not every operation need be performed and/or additional process operations may be performed. Referring again to Figure 7H, self-aligned fabrication by the subtractive approach may be complete at this stage. A next layer fabricated in a like manner likely requires initiation of the entire process once again. Alternatively, other approaches may be used at this stage to provide additional interconnect layers, such as conventional dual or single damascene approaches.

Additionally, it is to be appreciated that the approaches described in association with Figures 7A-7H are not necessarily performed as forming vias aligned to an underlying metallization layer. As such, in some contexts, these process schemes could be viewed as involving blind shooting in the top down direction with respect to any underlying metallization layers. In a second aspect, a subtractive approach provides alignment with an underlying metallization layer. As an example, Figures 8A-8I illustrate portions of integrated circuit layers representing various operations in a method of subtractive self-aligned via patterning using photobuckets including a photoresist having electron-activated photosensitizers, in accordance with another embodiment of the present disclosure. In each illustration at each described operation, an angled three-dimensional cross-section view is provided.

Figure 8A illustrates a starting point structure 800 for a subtractive via process following deep metal line fabrication, in accordance with an embodiment of the present disclosure.

Referring to Figure 8A, structure 800 includes metal lines 802 with intervening interlayer

dielectric (ILD) lines 804. It is to be appreciated that some of the lines 802 may be associated with underlying vias for coupling to a previous interconnect layer. In an embodiment, the metal lines 802 are formed by patterning trenches into an ILD material (e.g., the ILD material of lines 804). The trenches are then filled by metal and, if needed, planarized to the top of the ILD lines 804. In an embodiment, the metal trench and fill process involves high aspect ratio features. For example, in one embodiment, the aspect ratio of metal line height (h) to metal line width (w) is approximately in the range of 5-10.

Figure 8B illustrates the structure of Figure 8A following recessing of the metal lines, in accordance with an embodiment of the present disclosure. Referring to Figure 8B, the metal lines 802 are recessed selectively to provide first level metal lines 806. The recessing is performed selectively to the ILD lines 804. The recessing may be performed by etching through dry etch, wet etch, or a combination thereof. The extent of recessing may be determined by the targeted thickness of the first level metal lines 806 for use as suitable conductive interconnect lines within a back end of line (BEOL) interconnect structure.

Figure 8C illustrates the structure of Figure 8B following formation of an inter layer dielectric (ILD) layer, in accordance with an embodiment of the present disclosure. Referring to Figure 8C, an ILD material layer 808 is deposited and, if necessary, planarized, to a level above the recessed metal lines 806 and the ILD lines 804.

Figure 8D illustrates the structure of Figure 8C following deposition and patterning of a hardmask layer, in accordance with an embodiment of the present disclosure. Referring to Figure 8D a hardmask layer 810 is formed on the ILD layer 808. In one such embodiment, the hardmask layer 810 is formed with a grating pattern orthogonal to the grating pattern of the first level metal lines 806/ILD lines 804, as is depicted in Figure 8D. In an embodiment, the grating structure formed by the hardmask layer 810 is a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a pattern based on conventional lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like pattern of the second hardmask layer 810 of Figure 8D may have hardmask lines spaced at a constant pitch and having a constant width.

Figure 8E illustrates the structure of Figure 8D following trench formation defined using the pattern of the hardmask of Figure 8D, in accordance with an embodiment of the present disclosure. Referring to Figure 8E, the exposed regions (i.e., unprotected by 810) of the ILD layer 808 are etched to form trenches 812 and patterned ILD layer 814. The etch stops on, and thus exposes, the top surfaces of the first level metal lines 806 and the ILD lines 804.

Figure 8F illustrates the structure of Figure 8E following photobucket formation in all possible via locations, in accordance with an embodiment of the present disclosure. Referring to Figure 8F, photobuckets 516 are formed in all possible via locations above exposed portions of the recessed metal lines 806. In one embodiment, the photobuckets 816 are formed essentially
5 co-planar with the top surfaces of the ILD lines 804, as depicted in Figure 8F. Additionally, referring again to Figure 8F, the hardmask layer 810 may be removed from the patterned ILD layer 814.

Referring again to Figure 8F, in an embodiment, the photobuckets 816 include a photoresist having electron-activated photosensitizers. In one embodiment, the photobuckets 816
10 include a photoresist composition having electron-activated photosensitizers. In another embodiment, the photobuckets 816 include a photoresist structure having a grafted layer 817 having electron-activated photosensitizers, as is depicted in Figure 8F. Three different possible via locations 816A, 816B and 816C can be seen in the view provided in Figure 8F.

Figure 8G illustrates the structure of Figure 8F following via location selection, in
15 accordance with an embodiment of the present disclosure. Referring to Figure 8G, the photobuckets 816 from Figure 8F in select via locations 818 are removed (i.e., photobuckets 816A and 816C are removed). In locations where vias are not selected to be formed, the photobuckets 816 are retained (i.e., photobucket 816B remains after the development process). In one embodiment, photobucket 816B is partially exposed during exposure of photobuckets
20 816A and 816C. However, as described above, since the photobucket 816B is only partially exposed and is not a select via location, the electron-activated photosensitizer photobucket approach enables retention of all of photobucket 816B.

Figure 8H illustrates the structure of Figure 8G following conversion of the remaining photobuckets to permanent ILD material, in accordance with an embodiment of the present
25 disclosure. Referring to Figure 8H, the material of the photobuckets 816 is modified, e.g., by cross-linking upon a baking operation, in the locations to form a final ILD material 820. In one such embodiment, the cross-linking provides for a solubility switch upon the baking. The final, cross-linked material has inter-dielectric properties and, thus, can be retained in a final metallization structure. In a specific embodiment, where the photoresist having electron-
30 activated photosensitizers is a photoresist structure having grafted layer 817 with electron-activated photosensitizers, the grafted layer 817 is also retained in the final structure as a layer that lines bottom and sidewall surfaces of the final ILD material 820, as is depicted in Figure 8H.

Although not depicted, in other embodiments, the photobucket material of photobucket 816B is not converted to an ILD material and is instead ultimately removed and replaced with a
35 permanent ILD material.

Referring again to Figure 8H, in an embodiment, the resulting structure includes up to three different dielectric material regions (ILD lines 804 + ILD lines 814 + cross-linked photobucket 820 (or 820/817), in one embodiment) in a single plane 850 of the metallization structure. In one such embodiment, two or all of ILD lines 804, ILD lines 814, and cross-linked photobucket 820 (or 820/817) are composed of a same material. In another such embodiment, ILD lines 804, ILD lines 814, and cross-linked photobucket 820 (or 820/817) are all composed of different ILD materials. In either case, in a specific embodiment, a distinction such as a vertical seam between the materials of ILD lines 804 and ILD lines 814 (e.g., seam 897) and/or between ILD lines 804 and cross-linked photobucket 820 (or 820/817) (e.g., seam 898) and/or between ILD lines 814 and cross-linked photobucket 820 (or 820/817) (e.g., seam 899) may be observed in the final structure.

Figure 8I illustrates the structure of Figure 8H following metal line and via formation, in accordance with an embodiment of the present disclosure. Referring to Figure 8I, metal lines 822 and vias 824 are formed upon metal fill of the openings of Figure 8H. The metal lines 822 are coupled to the underlying metal lines 806 by the vias 824. In an embodiment, the openings are filled in a damascene approach or a bottom-up fill approach to provide the structure shown in Figure 8I. Thus, the metal (e.g., copper and associated barrier and seed layers) deposition to form metal lines and vias in the above approach may be that typically used for standard back end of line (BEOL) processing. In an embodiment, in subsequent fabrication operations, the ILD lines 814 may be removed to provide air gaps between the resulting metal lines 824.

The structure of Figure 8I may subsequently be used as a foundation for forming subsequent metal line/via and ILD layers. Alternatively, the structure of Figure 8I may represent the final metal interconnect layer in an integrated circuit. It is to be understood that the above process operations may be practiced in alternative sequences, not every operation need be performed and/or additional process operations may be performed. In any case, the resulting structures enable fabrication of vias that are directly centered on underlying metal lines. That is, the vias may be wider than, narrower than, or the same thickness as the underlying metal lines, e.g., due to non-perfect selective etch processing. Nonetheless, in an embodiment, the centers of the vias are directly aligned (match up) with the centers of the metal lines. Furthermore, the ILD used to select which plugs and vias will likely be very different from the primary ILD and will be perfectly self-aligned in both directions. As such, in an embodiment, offset due to conventional lithograph/dual damascene patterning that must otherwise be tolerated, is not a factor for the resulting structures described herein. Referring again to Figure 5I, then, self-aligned fabrication by the subtractive approach may be complete at this stage. A next layer fabricated in a like manner likely requires initiation of the entire process once again. Alternatively, other approaches

may be used at this stage to provide additional interconnect layers, such as conventional dual or single damascene approaches.

Overall, in accordance with one or more embodiments of the present disclosure, approaches described herein involve use of photobucket interlayer dielectric (ILD) to select
5 locations for plugs and vias. The details above regarding Figures 7A-7H and 8A-8I focus primarily on photobuckets having electron-activated photosensitizers as used for via patterning. However, it is to be appreciated that photobuckets having electron-activated photosensitizers may also be used for plug patterning.

In an embodiment, the term “grating structure” for metal lines, ILD lines or hardmask
10 lines is used to refer to a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through conventional lithography. For example, a pattern based on conventional lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning, as is known in the art. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like patterns described above
15 may have metal lines, ILD lines or hardmask lines spaced at a constant pitch and having a constant width. The pattern may be fabricated by a pitch halving or pitch quartering approach.

In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide
20 (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, interconnect
25 material (e.g., metal lines and/or vias) is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The
30 interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

In an embodiment, as is also used throughout the present description, plug and/or cap and/or hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, these materials are sacrificial, while interlayer dielectric
35 materials are preserved at least somewhat in a final structure. In some embodiments, a plug

and/or cap and/or hardmask material includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a plug and/or cap and/or hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other plug and/or cap and/or hardmask material layers known in the arts may be used depending upon the particular implementation. The plug and/or cap and/or hardmask material layers maybe formed by CVD, PVD, or by other deposition methods.

It is to be appreciated that the layers and materials described above are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structures depicted above may be fabricated on underlying lower level back end of line (BEOL) interconnect layers.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figure 9 illustrates a computing device 900 in accordance with one implementation of the disclosure. The computing device 900 houses a board 902. The board 902 may include a number of components, including but not limited to a processor 904 and at least one communication chip 906. The processor 904 is physically and electrically coupled to the board

902. In some implementations the at least one communication chip 906 is also physically and electrically coupled to the board 902. In further implementations, the communication chip 906 is part of the processor 904.

Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to the board 902. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 906 enables wireless communications for the transfer of data to and from the computing device 900. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 906 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 904 of the computing device 900 includes an integrated circuit die packaged within the processor 904. In some implementations of the disclosure, the integrated circuit die of the processor includes one or more structures, such as conductive vias fabricated using a photoresist having electron-activated photosensitizers, built in accordance with implementations of embodiments of the disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 606 also includes an integrated circuit die packaged within the

communication chip 606. In accordance with another implementation of the disclosure, the integrated circuit die of the communication chip includes one or more structures, such as conductive vias fabricated using a photoresist having electron-activated photosensitizers, in accordance with embodiments of the disclosure.

5 In further implementations, another component housed within the computing device 900 may contain an integrated circuit die that includes one or more structures, such as conductive vias fabricated using a photoresist having electron-activated photosensitizers, in accordance with embodiments of the disclosure.

10 In various implementations, the computing device 900 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

15 Figure 10 illustrates an interposer 1000 that includes one or more embodiments of the disclosure. The interposer 1000 is an intervening substrate used to bridge a first substrate 1002 to a second substrate 1004. The first substrate 1002 may be, for instance, an integrated circuit die. The second substrate 1004 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1000 is to
20 spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1000 may couple an integrated circuit die to a ball grid array (BGA) 1006 that can subsequently be coupled to the second substrate 1004. In some embodiments, the first and second substrates 1002/1004 are attached to opposing sides of the interposer 1000. In other
25 embodiments, the first and second substrates 1002/1004 are attached to the same side of the interposer 1000. And in further embodiments, three or more substrates are interconnected by way of the interposer 1000.

30 The interposer 1000 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

35 The interposer may include metal interconnects 1008 and vias 1010, including but not limited to through-silicon vias (TSVs) 1012. The interposer 1000 may further include embedded devices 1014, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers,

sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1000. In accordance with
5 fabrication of interposer 1000 or in one or more of the components of the interposer 1000.

Thus, embodiments of the present disclosure include photoresists with electron-activated photosensitizers for confined patterning lithography, e.g., for fabricating back end of line (BEOL) interconnects.

Example embodiment 1: An integrated circuit structure includes a first layer of an
10 interconnect structure above a substrate, the first layer including a first grating of alternating metal lines and dielectric lines in a first direction. The dielectric lines have an uppermost surface higher than an uppermost surface of the metal lines. A second layer of the interconnect structure is above the first layer. The second layer includes a second grating of alternating metal lines and dielectric lines in a second direction, perpendicular to the first direction. The dielectric lines
15 have a lowermost surface lower than a lowermost surface of the metal lines of the second grating. The dielectric lines of the second grating overlap and contact the dielectric lines of the first grating. A region of dielectric material is between the metal lines of the first grating and the metal lines of the second grating, and in a same plane as upper portions of the dielectric lines of the first grating and lower portions of the dielectric lines of the second grating. The region of
20 dielectric material includes a cross-linked photolyzable material having a bottom and sidewall surfaces lined with a layer including electron-activated photosensitizers.

Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein the layer including electron-activated photosensitizers includes a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

25 Example embodiment 3: The integrated circuit structure of example embodiment 1 or 2, wherein the layer including electron-activated photosensitizers further includes a sulfonium group or a phosphonium group.

Example embodiment 4: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the layer including electron-activated photosensitizers is absorbing at a wavelength of
30 approximately 365nm.

Example embodiment 5: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the cross-linked photolyzable material is a photo-acid generator (PAG)-based cross-linked photolyzable material.

Example embodiment 6: The integrated circuit structure of example embodiment 1, 2, 3,
35 4, 5 or 6, further including a conductive via between and coupling a metal line of the first grating

to a metal line of the second grating, the conductive via in the same plane as the region of dielectric material.

Example embodiment 7: The integrated circuit structure of example embodiment 6, wherein the conductive via has a center directly aligned with a center of the metal line of the first grating and with a center of the metal line of the second grating.

Example embodiment 8: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5, 6 or 7, wherein the dielectric lines of the first grating include a first dielectric material, and the dielectric lines of the second grating include a second, different dielectric material, and wherein the first and second dielectric materials are different than the cross-linked photolyzable material.

Example embodiment 9: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5, 6 or 7, wherein the dielectric lines of the first grating and the dielectric lines of the second grating include a same dielectric material different than the cross-linked photolyzable material.

Example embodiment 10: A method of selecting a photobucket for semiconductor processing includes providing a structure having a first photobucket neighboring a second photobucket, wherein the first and second photobuckets each include a photolyzable composition including an acid-deprotectable photoresist material, a photo-acid-generating (PAG) component, and an electron-activated photosensitizer component. The method also includes exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket. The method also includes, subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the first and second photobuckets. The method also includes, subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV) radiation, wherein the first photobucket is exposed to the DUV radiation to approximately the same extent as the second photobucket. The method also includes, subsequent to exposing the structure to DUV radiation, developing the structure, wherein the developing opens the first photobucket and leaves the second photobucket closed.

Example embodiment 11: The method of example embodiment 10, wherein the electron-activated photosensitizer component is a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

Example embodiment 12: The method of example embodiment 10 or 11, wherein exposing the structure to extreme ultraviolet (EUV) or e-beam radiation includes exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

Example embodiment 13: The method of example embodiment 10, 11 or 12, wherein

exposing the structure to DUV radiation includes exposing the structure to energy having a wavelength approximately 365 nanometers.

Example embodiment 14: The method of example embodiment 10, 11, 12 or 13, wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes.

Example embodiment 15: A method of selecting a photobucket for semiconductor processing includes providing a structure having a first photobucket neighboring a second photobucket, wherein the first and second photobuckets each include a grafted electron-activated photosensitizer component along a bottom and sidewalls of the first and second photobuckets, and a photolyzable composition formed within the grafted electron-activated photosensitizer component, the photolyzable composition including an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component. The method also includes exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket. The method also includes, subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the first and second photobuckets. The method also includes, subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV) radiation, wherein the first photobucket is exposed to the DUV radiation to approximately the same extent as the second photobucket. The method also includes, subsequent to exposing the structure to DUV radiation, developing the structure, wherein the developing opens the first photobucket and leaves the second photobucket closed.

Example embodiment 16: The method of example embodiment 15, wherein the electron-activated photosensitizer component includes a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

Example embodiment 17: The method of example embodiment 15 or 16, wherein the grafted electron-activated photosensitizer component further includes a sulfonium group or a phosphonium group.

Example embodiment 18: The method of example embodiment 15, 16 or 17, wherein exposing the structure to extreme ultraviolet (EUV) or e-beam radiation includes exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

Example embodiment 19: The method of example embodiment 15, 16, 17 or 18, wherein exposing the structure to DUV radiation includes exposing the structure to energy having a wavelength approximately 365 nanometers.

Example embodiment 20: The method of example embodiment 15, 16, 17, 18, 19 or 20,

wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes.

Example embodiment 21: A method of selecting a photobucket for semiconductor processing includes providing a structure having a first photobucket neighboring a second photobucket, wherein the first and second photobuckets each include an over layer including an electron-activated photosensitizer component, and a photolyzable composition formed below the over layer, the photolyzable composition comprising an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component. The method also includes exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket. The method also includes, subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the first and second photobuckets. The method also includes, subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV) radiation, wherein the first photobucket is exposed to the DUV radiation to approximately the same extent as the second photobucket. The method also includes, subsequent to exposing the structure to DUV radiation, developing the structure, wherein the developing opens the first photobucket and leaves the second photobucket closed.

Example embodiment 22: The method of example embodiment 21, wherein the over layer includes a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

Example embodiment 23: The method of example embodiment 21 or 22, wherein the over layer further includes a sulfonium group or a phosphonium group.

Example embodiment 24: The method of example embodiment 21, 22 or 23, wherein exposing the structure to extreme ultraviolet (EUV) or e-beam radiation includes exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

Example embodiment 25: The method of example embodiment 21, 22, 23 or 24, wherein exposing the structure to DUV radiation includes exposing the structure to energy having a wavelength approximately 365 nanometers, and wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:

5 a first layer of an interconnect structure above a substrate, the first layer comprising a first grating of alternating metal lines and dielectric lines in a first direction, wherein the dielectric lines have an uppermost surface higher than an uppermost surface of the metal lines; and

10 a second layer of the interconnect structure above the first layer, the second layer comprising a second grating of alternating metal lines and dielectric lines in a second direction, perpendicular to the first direction, wherein the dielectric lines have a lowermost surface lower than a lowermost surface of the metal lines of the second grating, and wherein the dielectric lines of the second grating overlap and contact the dielectric lines of the first grating; and

15 a region of dielectric material between the metal lines of the first grating and the metal lines of the second grating, and in a same plane as upper portions of the dielectric lines of the first grating and lower portions of the dielectric lines of the second grating, the region of dielectric material comprising a cross-linked photolyzable material having a bottom and sidewall surfaces lined with a layer comprising electron-activated photosensitizers.

20 2. The integrated circuit structure of claim 1, wherein the layer comprising electron-activated photosensitizers includes a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

25 3. The integrated circuit structure of claim 2, wherein the layer comprising electron-activated photosensitizers further comprises a sulfonium group or a phosphonium group.

4. The integrated circuit structure of claim 1, wherein the layer comprising electron-activated photosensitizers is absorbing at a wavelength of approximately 365nm.

30 5. The integrated circuit structure of claim 1, wherein the cross-linked photolyzable material is a photo-acid generator (PAG)-based cross-linked photolyzable material.

6. The integrated circuit structure of claim 1, further comprising:

35 a conductive via between and coupling a metal line of the first grating to a metal line of the second grating, the conductive via in the same plane as the region of dielectric material.

7. The integrated circuit structure of claim 6, wherein the conductive via has a center directly aligned with a center of the metal line of the first grating and with a center of the metal line of the second grating.

5

8. The integrated circuit structure of claim 1, wherein the dielectric lines of the first grating comprise a first dielectric material, and the dielectric lines of the second grating comprise a second, different dielectric material, and wherein the first and second dielectric materials are different than the cross-linked photolyzable material.

10

9. The integrated circuit structure of claim 1, wherein the dielectric lines of the first grating and the dielectric lines of the second grating comprise a same dielectric material different than the cross-linked photolyzable material.

15

10. A method of selecting a photobucket for semiconductor processing, the method comprising: providing a structure having a first photobucket neighboring a second photobucket, wherein the first and second photobuckets each comprise a photolyzable composition comprising an acid-deprotectable photoresist material, a photo-acid-generating (PAG) component, and an electron-activated photosensitizer component;

20

exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket;

subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the first and second photobuckets;

25

subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV) radiation, wherein the first photobucket is exposed to the DUV radiation to approximately the same extent as the second photobucket; and

subsequent to exposing the structure to DUV radiation, developing the structure, wherein the developing opens the first photobucket and leaves the second photobucket closed.

30

11. The method of claim 10, wherein the electron-activated photosensitizer component is a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

35

12. The method of claim 10, wherein exposing the structure to extreme ultraviolet (EUV) or e-

beam radiation comprises exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

13. The method of claim 10, wherein exposing the structure to DUV radiation comprises exposing the structure to energy having a wavelength approximately 365 nanometers.

14. The method of claim 10, wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes.

15. A method of selecting a photobucket for semiconductor processing, the method comprising: providing a structure having a first photobucket neighboring a second photobucket, wherein the first and second photobuckets each comprise a grafted electron-activated photosensitizer component along a bottom and sidewalls of the first and second photobuckets and a photolyzable composition formed within the grafted electron-activated photosensitizer component, the photolyzable composition comprising an acid-deprotectable photoresist material and a photo-acid-generating (PAG) component; exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first photobucket is exposed to the EUV or e-beam radiation to a greater extent than the second photobucket; subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the first and second photobuckets; subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV) radiation, wherein the first photobucket is exposed to the DUV radiation to approximately the same extent as the second photobucket; and subsequent to exposing the structure to DUV radiation, developing the structure, wherein the developing opens the first photobucket and leaves the second photobucket closed.

16. The method of claim 15, wherein the grafted electron-activated photosensitizer component comprises a material selected from the group consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

17. The method of claim 16, wherein the grafted electron-activated photosensitizer component further comprises a sulfonium group or a phosphonium group.

18. The method of claim 15, wherein exposing the structure to extreme ultraviolet (EUV) or e-beam radiation comprises exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

5 19. The method of claim 15, wherein exposing the structure to DUV radiation comprises exposing the structure to energy having a wavelength approximately 365 nanometers.

20. The method of claim 15, wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5
10 minutes.

21. A method of selecting a photobucket for semiconductor processing, the method comprising:
providing a structure having a first photobucket neighboring a second photobucket, wherein
the first and second photobuckets each comprise an over layer comprising an electron-
15 activated photosensitizer component, and a photolyzable composition formed below the
over layer, the photolyzable composition comprising an acid-deprotectable photoresist
material and a photo-acid-generating (PAG) component;

exposing the structure to extreme ultraviolet (EUV) or e-beam radiation, wherein the first
photobucket is exposed to the EUV or e-beam radiation to a greater extent than the
20 second photobucket;

subsequent to exposing the structure to EUV or e-beam radiation, performing a bake of the
first and second photobuckets;

subsequent to performing the bake, exposing the structure to deep ultraviolet (DUV)
radiation, wherein the first photobucket is exposed to the DUV radiation to approximately
25 the same extent as the second photobucket; and

subsequent to exposing the structure to DUV radiation, developing the structure, wherein the
developing opens the first photobucket and leaves the second photobucket closed.

22. The method of claim 21, wherein the over layer comprises a material selected from the group
30 consisting of anthracene, coumarin, biphenyl, naphthalene, and benzophenone.

23. The method of claim 22, wherein the over layer further comprises a sulfonium group or a
phosponium group.

35 24. The method of claim 21, wherein exposing the structure to extreme ultraviolet (EUV) or e-

beam radiation comprises exposing the structure to energy having a wavelength approximately 13.5 nanometers or to energy in the range of 5-150 keV.

25. The method of claim 21, wherein exposing the structure to DUV radiation comprises
- 5 exposing the structure to energy having a wavelength approximately 365 nanometers, and wherein the bake is performed at a temperature approximately in the range of 50-120 degrees Celsius for a duration of approximately in the range of 0.5-5 minutes.

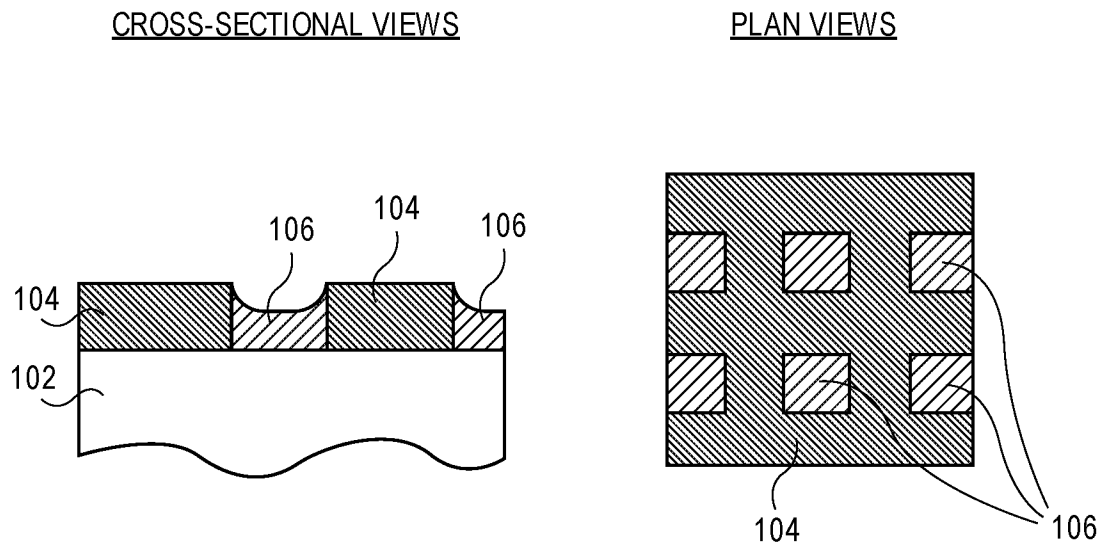


FIG. 1A

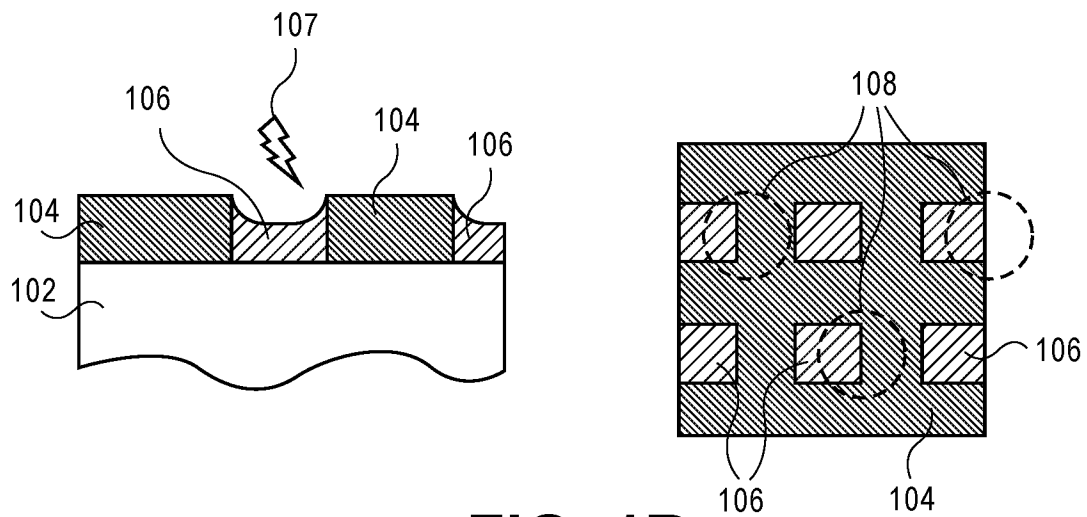


FIG. 1B

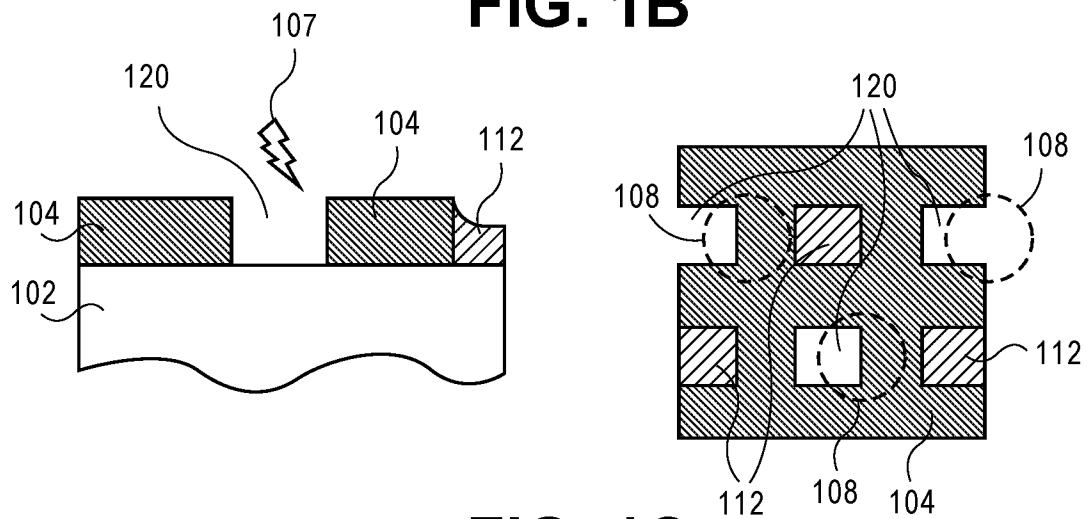


FIG. 1C

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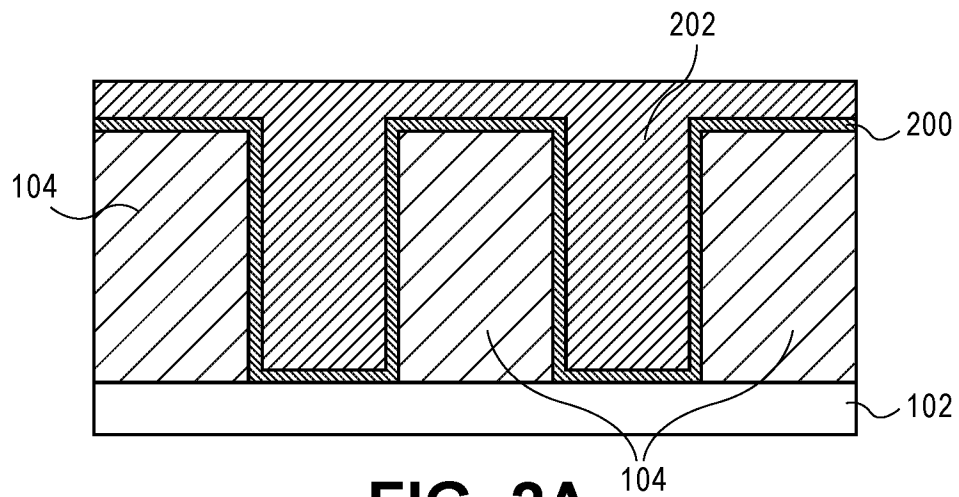


FIG. 2A

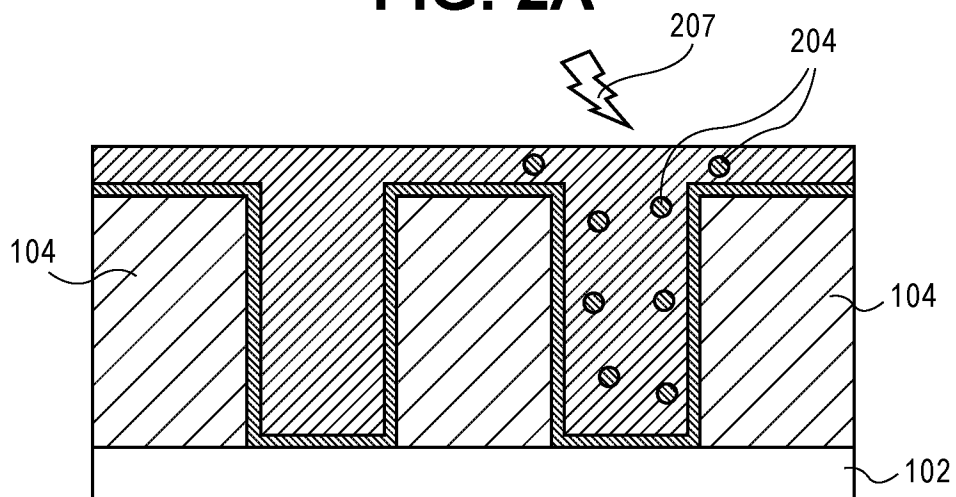


FIG. 2B

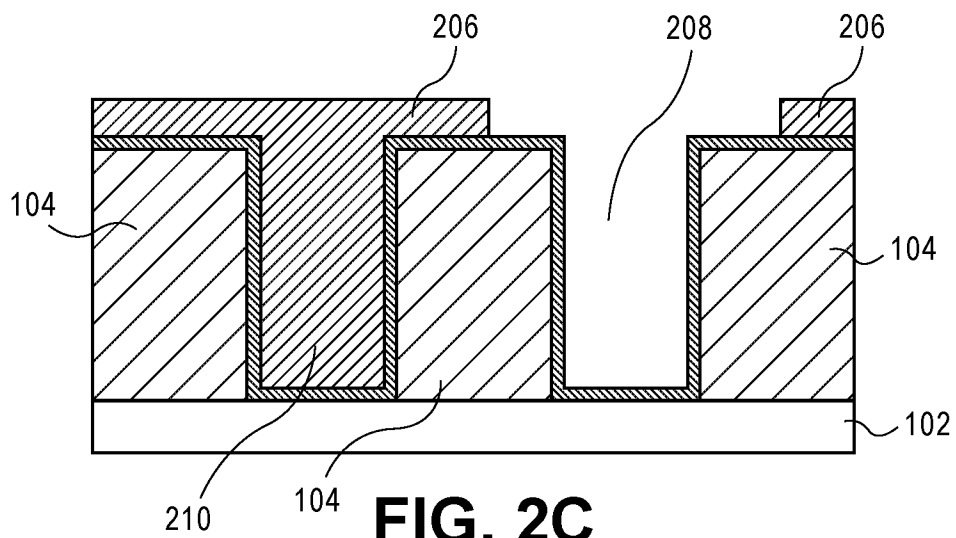
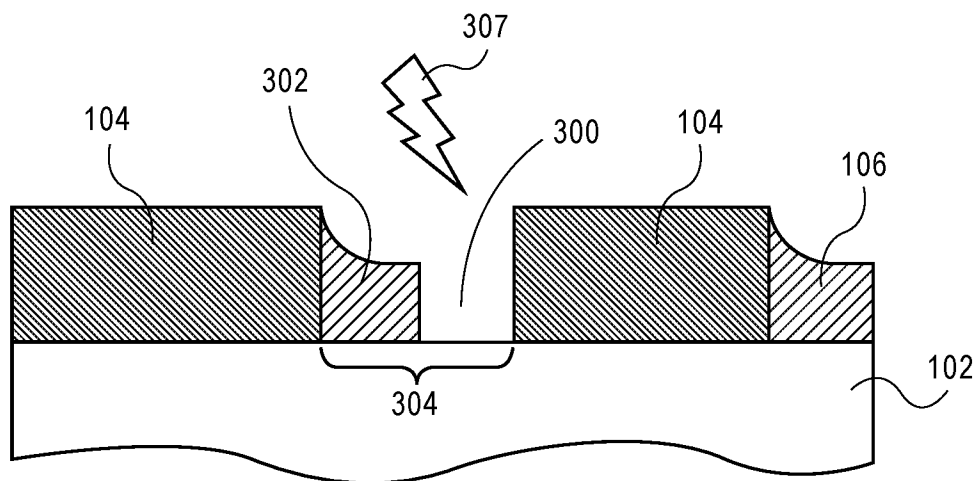
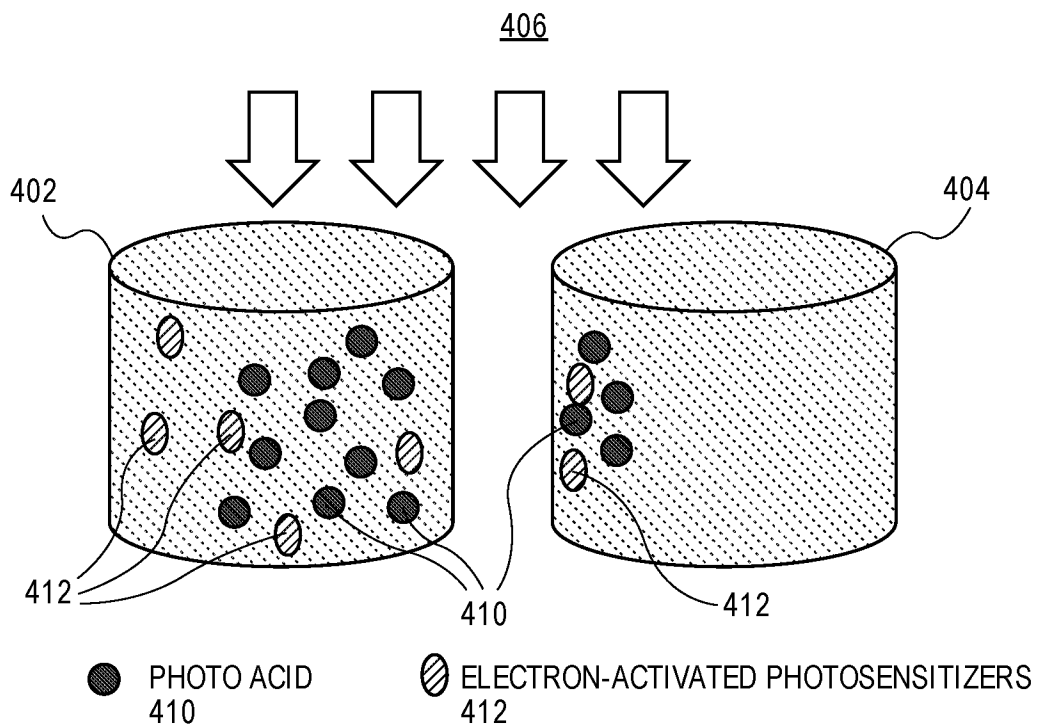
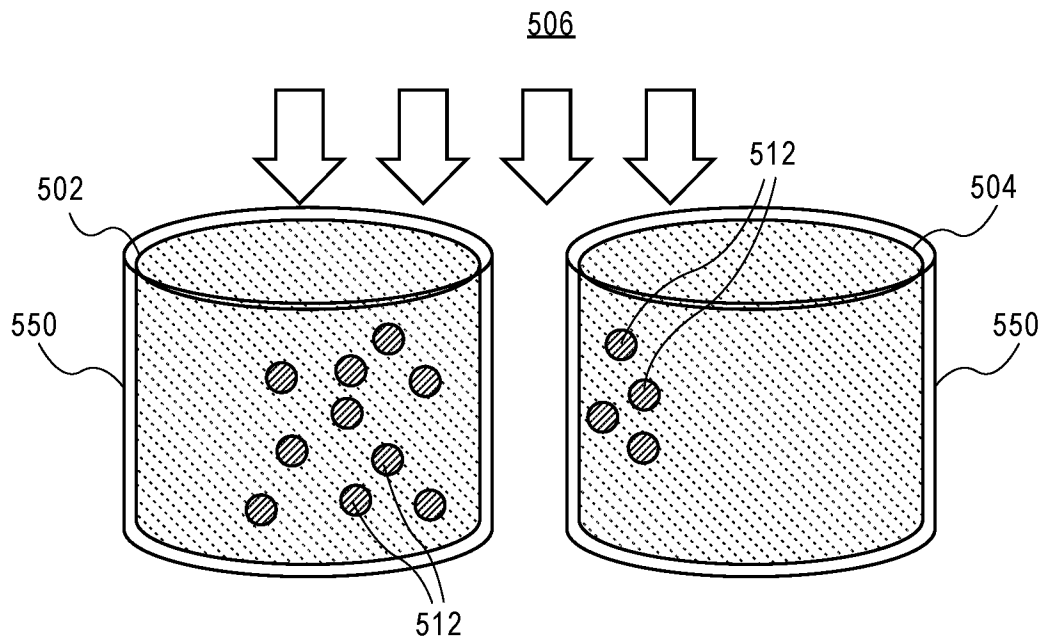
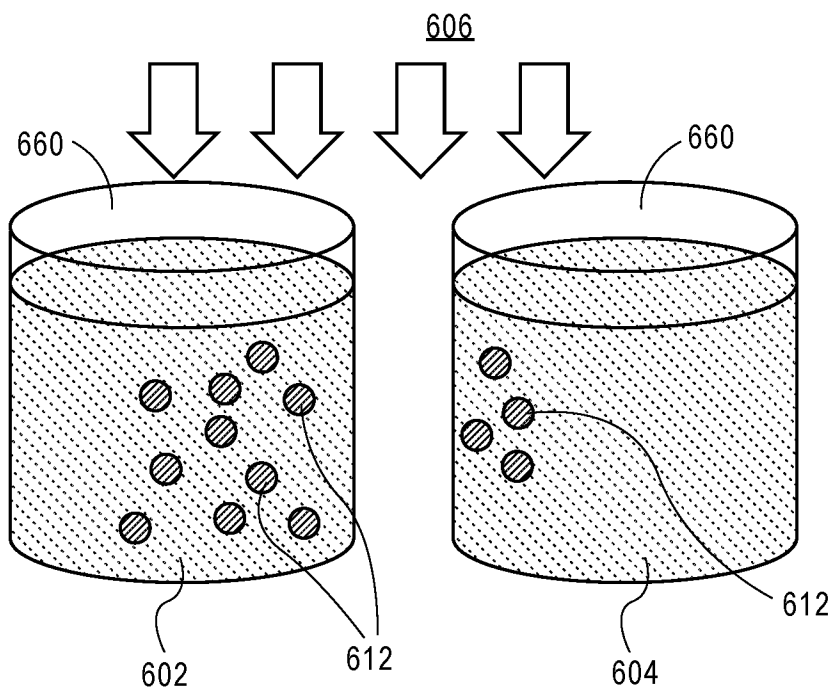


FIG. 2C

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**FIG. 3****FIG. 4**

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**FIG. 5****FIG. 6**

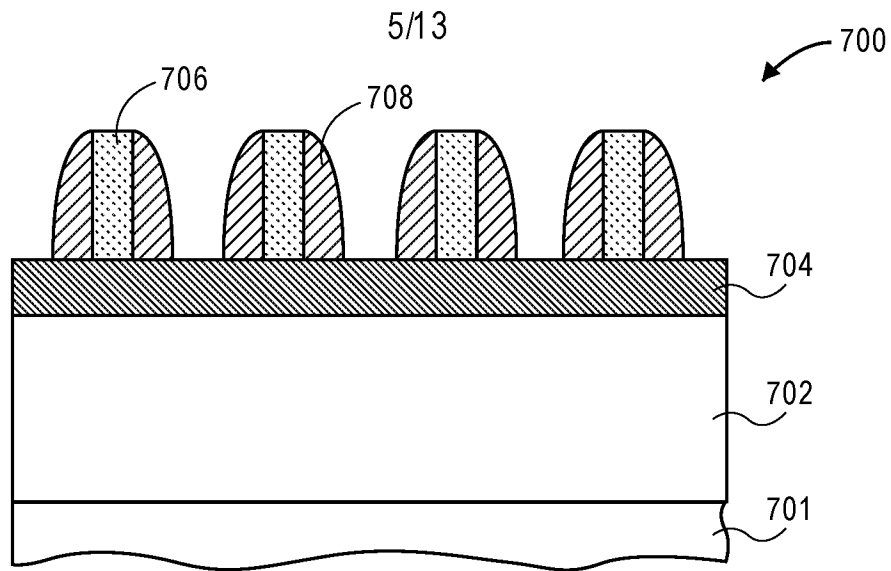


FIG. 7A

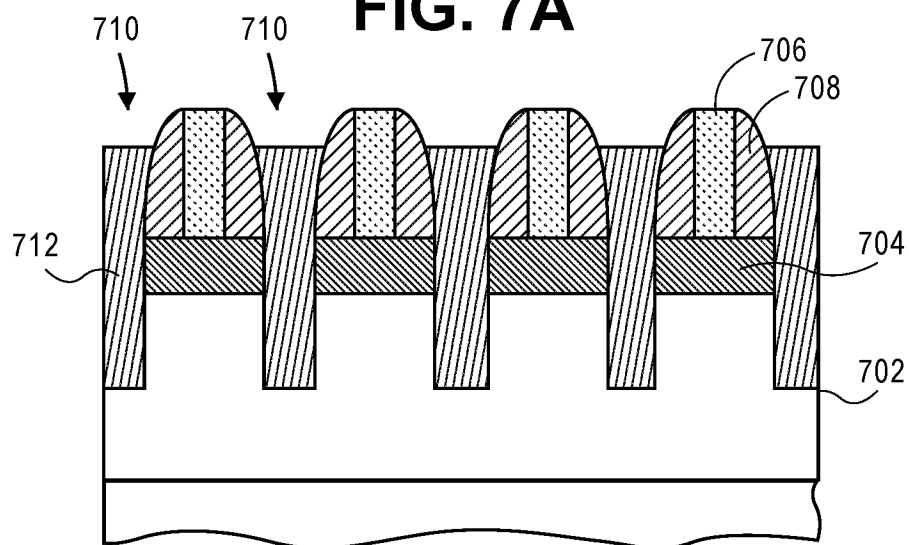


FIG. 7B

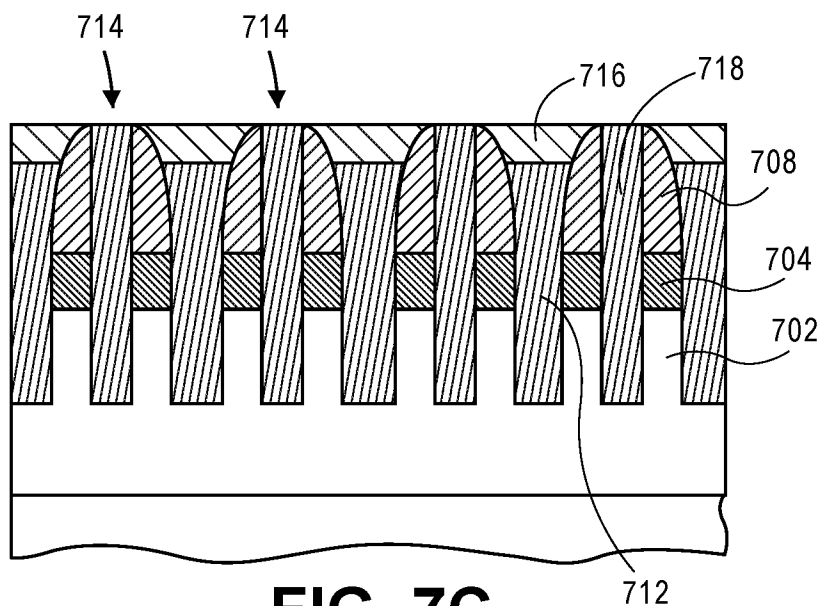


FIG. 7C

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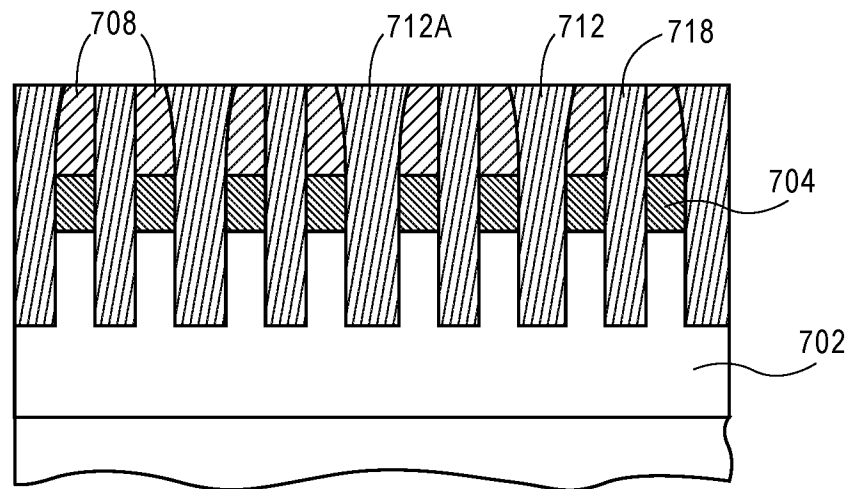


FIG. 7D

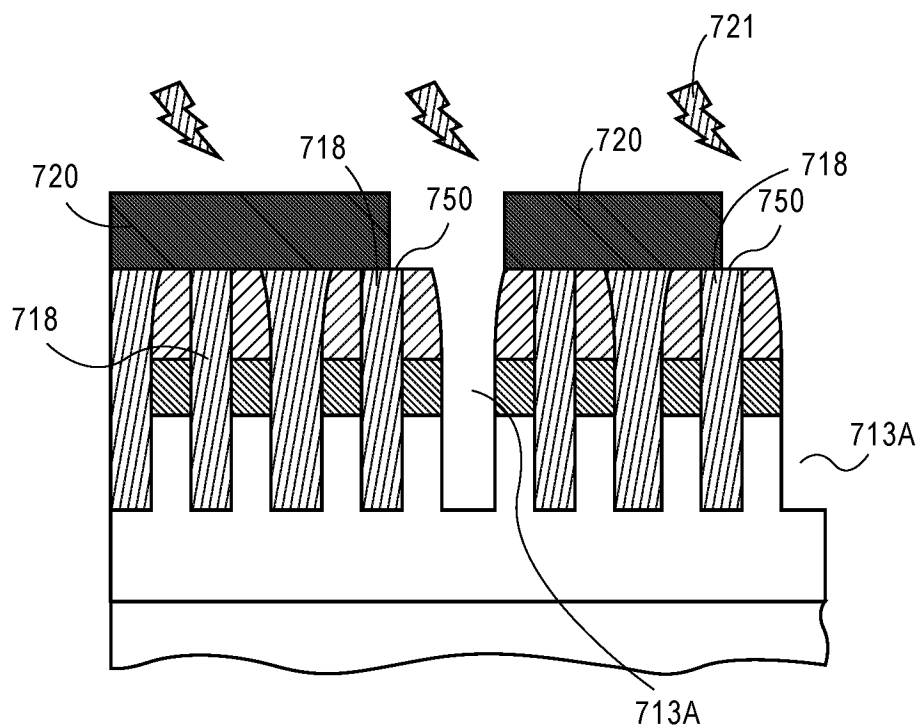


FIG. 7E

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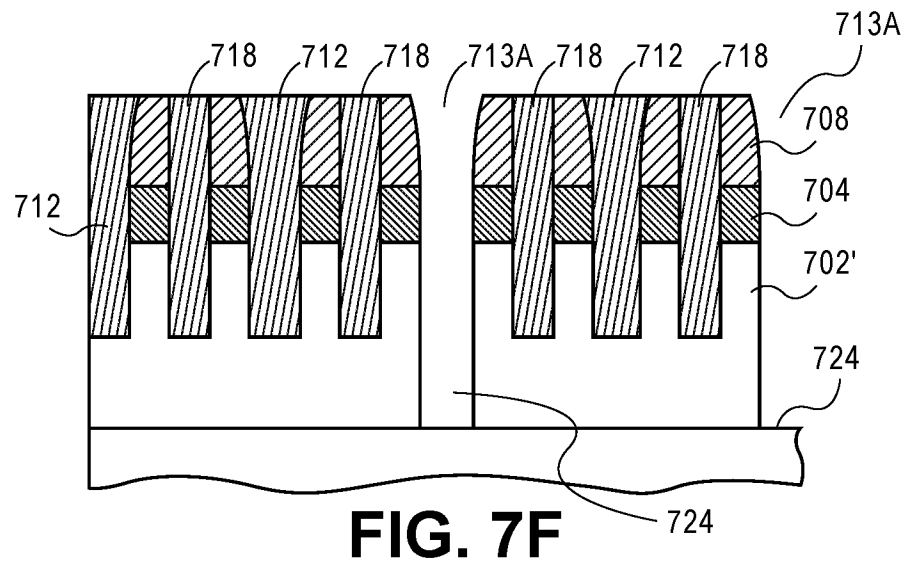


FIG. 7F

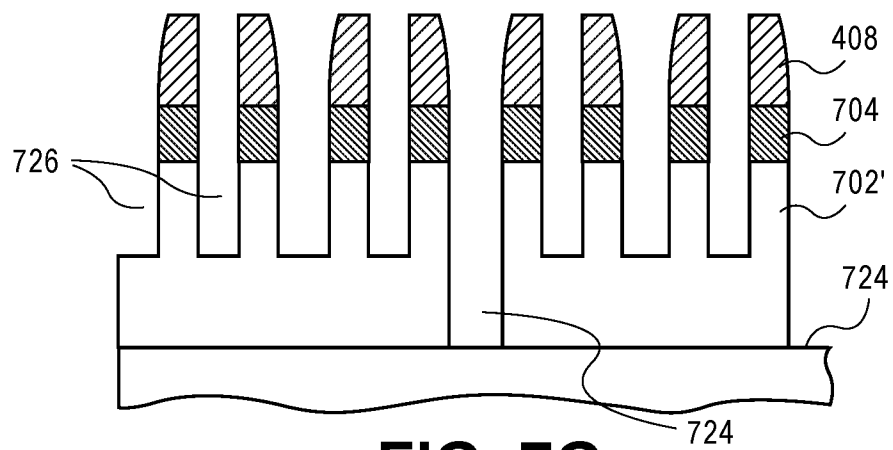


FIG. 7G

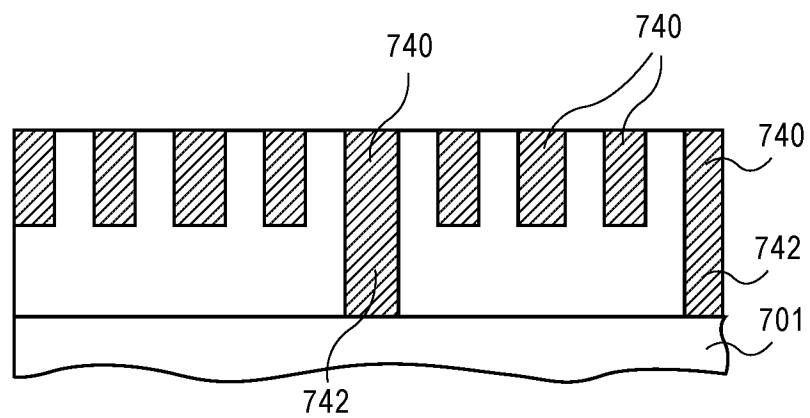


FIG. 7H

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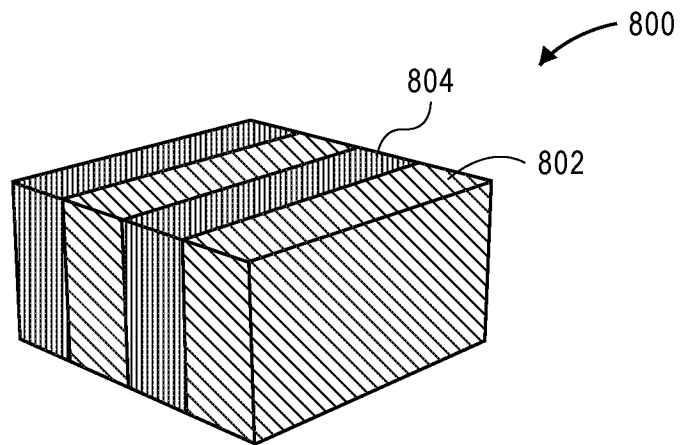


FIG. 8A

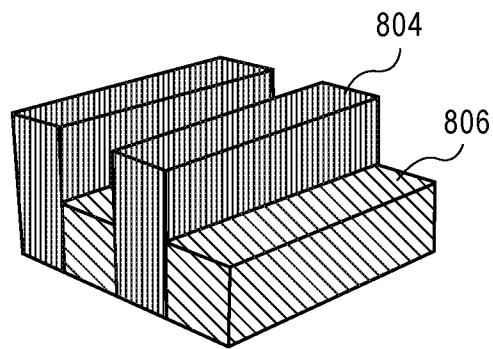


FIG. 8B

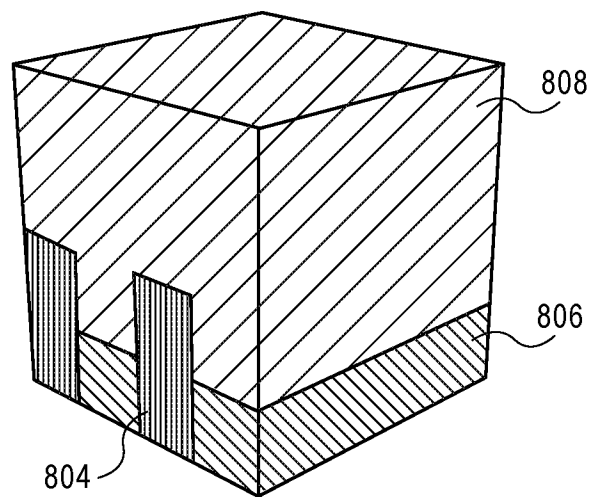


FIG. 8C

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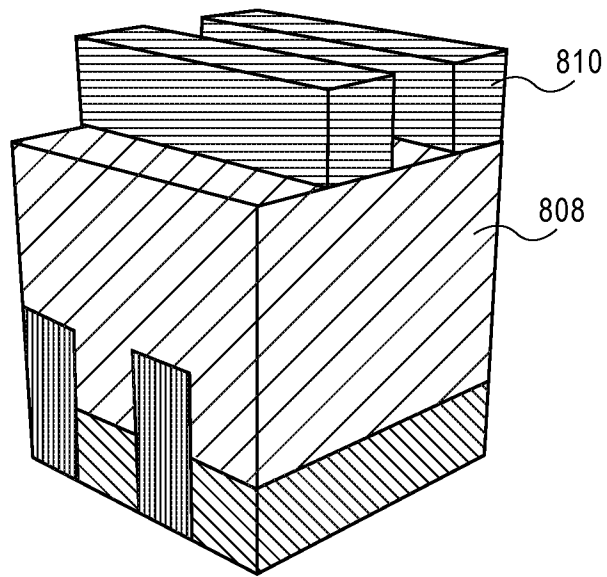


FIG. 8D

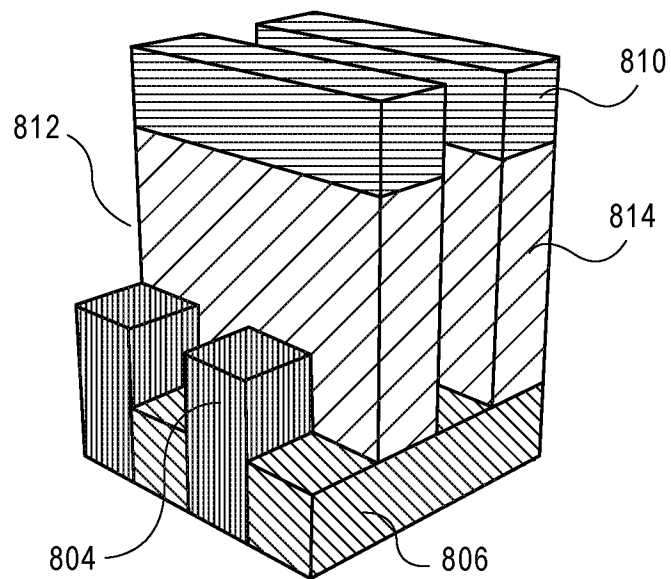


FIG. 8E

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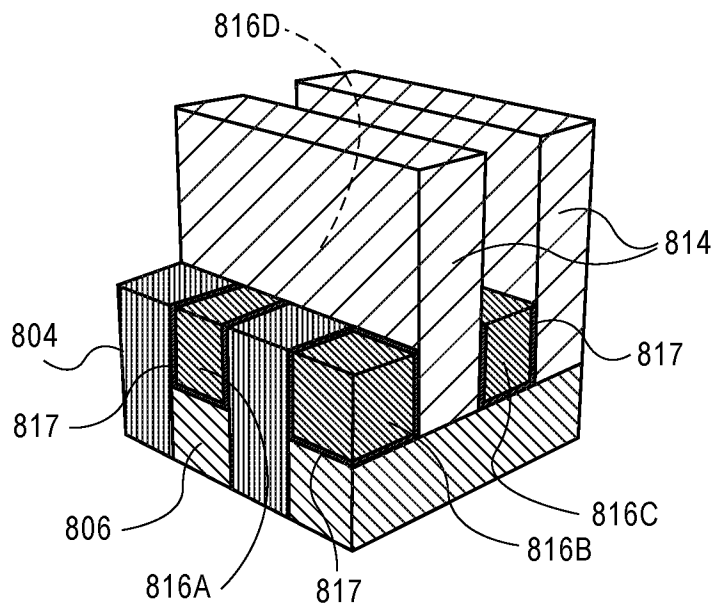


FIG. 8F

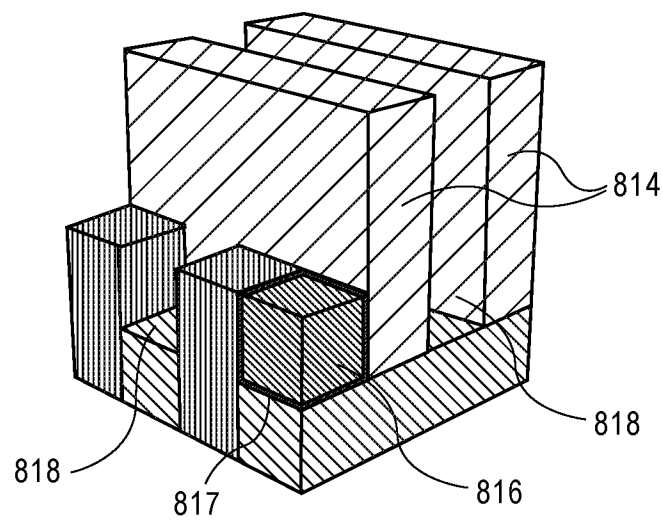


FIG. 8G

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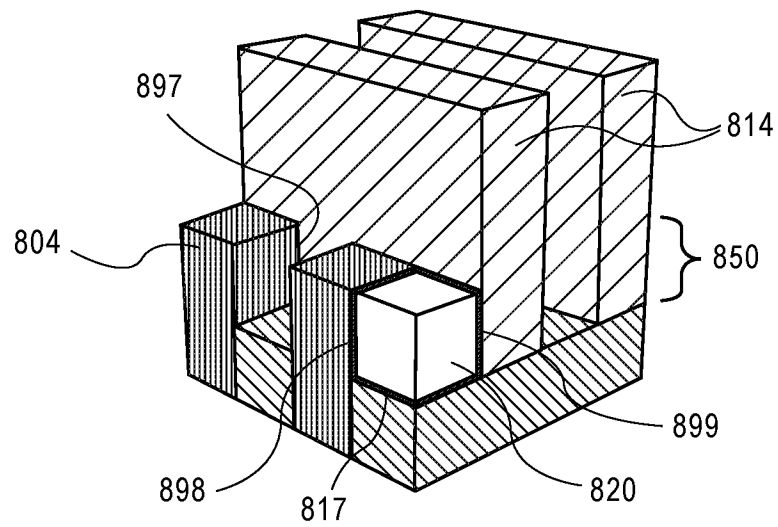


FIG. 8H

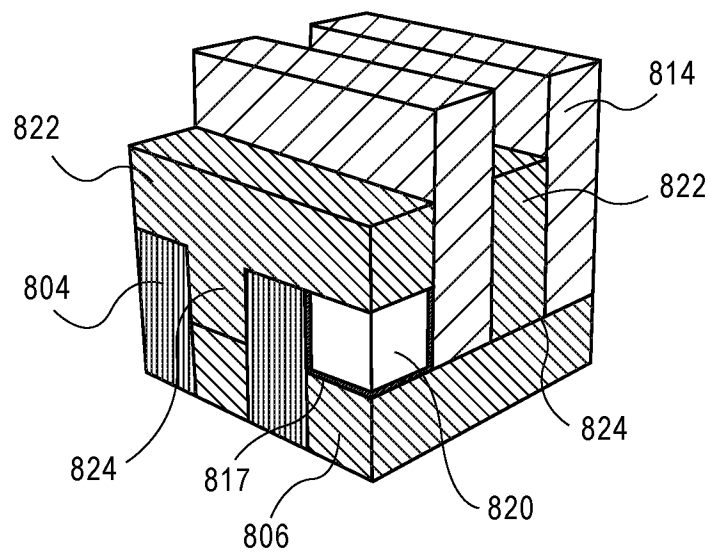


FIG. 8I

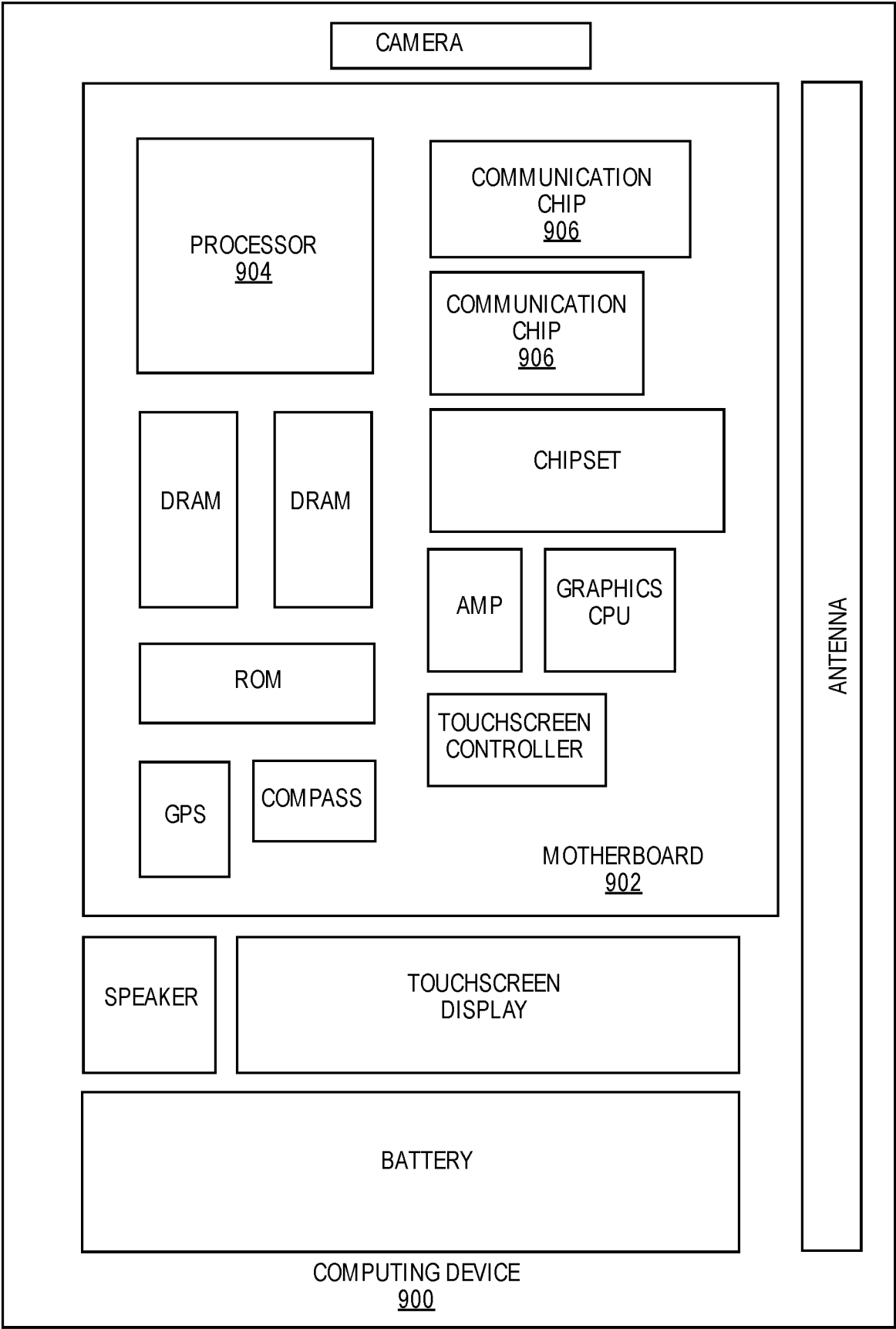


FIG. 9

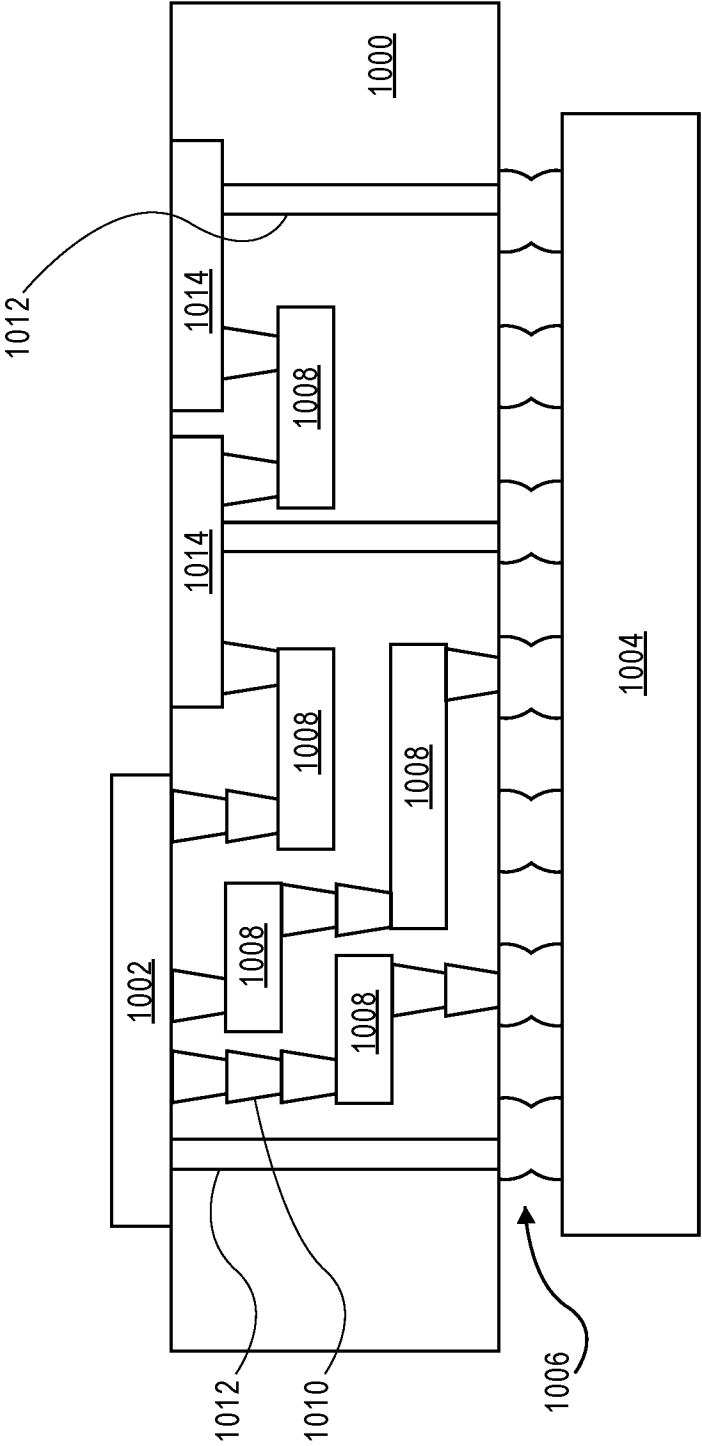


FIG. 10

A. CLASSIFICATION OF SUBJECT MATTER**H01L 21/027(2006.01)i, G03F 7/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/027; H01L 21/768; H01L 21/311; H01L 21/469; H01L 21/033; G03C 5/00; H01B 13/00; G03F 7/20

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: integrated circuit structure, interconnect structure, dielectric, metal, grating, photosensitizer, photobucket, extreme ultraviolet, e-beam radiation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 9406512 B2 (ROBERT L. BRISTOL et al.) 02 August 2016 See column 4, line 49 - column 13, line 15 and figures 1A-3I.	1-25
A	US 9553018 B2 (INTEL CORPORATION) 24 January 2017 See column 4, line 57 - column 13, line 23 and figures 1A-3I.	1-25
A	US 6245488 B1 (TOSHIHARU FURUKAWA et al.) 12 June 2001 See column 4, line 49 - column 6, line 26 and figures 1-7.	1-25
A	US 7468330 B2 (ROBERT DAVID ALLEN et al.) 23 December 2008 See column 3, line 1 - column 4, line 32 and figures 1A-1F.	1-25
A	US 8728332 B2 (CHUNG-YI LIN et al.) 20 May 2014 See column 2, line 15 - column 7, line 18 and figures 1-10.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

17 November 2017 (17.11.2017)

Date of mailing of the international search report

17 November 2017 (17.11.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/022661

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