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## Description

This invention relates to gas discharge panels and, more particularly to gas discharge panels which make use of plasma coupling for write and erase cycles.

Plasma display panels, or gas discharge panels, are well known in the art and, in general, comprise a structure including a pair of substrates respectively supporting thereon column and row electrodes each coated with a dielectric layer such as a glass material and disposed in parallel spaced relation to define a gap therebetween in which an ionizable gas is sealed. Moreover, the substrates are arranged such that the electrodes are disposed in orthogonal relation to one another thereby defining points of intersection which in turn define discharge cells at which selective discharges may be established to provide a desired storage or display function. It is also known to operate such panels with AC voltages and particularly to provide a write voltage which exceeds the firing voltage at a given discharge point, as defined by a selected column and row electrode, thereby to produce a discharge at a selected cell. The discharge at the selected cell can be continuously "sustained" by applying an alternating sustain voltage (which, by itself is insufficient to initiate a discharge). This technique relies upon the wall charges which are generated on the dielectric layers of the substrates which, in conjunction with the sustain voltage, operate to maintain discharges.

Details of the structure and operation of such gas discharge panels or plasma displays are set forth in U.S. Pat. US-A-3,559,190 issued Jan. 26, 1971 to Donald L. Bitzer, et al.

In the past two decades, AC plasma displays have found widespread use due to their excellent optical qualities and flat panel characteristics. These qualities have made plasma displays a leader in the flat-panel display market. However, plasma panels have gained only a small portion of their potential market because of competition from lower cost CRT products.

The expense of the display electronics, not the display itself, is the most significant cost factor in plasma displays. Because of the matrix addressing schemes used, a separate voltage driver is required for each display electrode. Therefore, a typical 512X512 pixel display requires a total of 1024 electronic drivers and connections which add considerable bulk and cost to the final product. To combat this problem, many techniques have been suggested to reduce the number of electrodes that need separate circuit drivers. The most popular methods have resulted in shift and logic panels. However, the use of these products have been limited by inherently slow panel update rates and

by the expensive manufacturing processes required to fabricate the complex panels.

In a shift panel, all of the display information is typically entered along the vertical edge of the panel and then shifted across it. This method requires the same number of drivers along the vertical edge but only a small number along the horizontal edge (usually less than ten). Thus almost a two to one reduction in circuit requirements can be achieved.

The state of a particular cell within a shift panel, whether on or off, is shifted to the next adjacent cell by using either priming coupling or wall-charge coupling. The first method, priming coupling, uses priming particles produced by a nearby on cell to reduce the firing voltage at the next cell location in the shift sequence. A voltage is applied to the next cell in the sequence so that it will turn on only if it receives sufficient priming from its neighboring cell. Thus information is shifted from cell to cell across the entire display.

The priming technique relies on the presence of priming particles generated at an addressed cell location to effect one of its surrounding display pixels in such a way that allows it to be written or erased. Therefore, to use the priming technique in other than a shift mode, the proximity of the selected pixel to the selected address cell must be the controlling effect that allows it to be selected from the thousands of other display pixels receiving the same voltage signals.

The priming particles produced from a discharge are somewhat locally constrained. Put simply, electrons, ions, metastables, and photons produced in a gas-discharge can serve as agents in priming other nearby cells. The electrons, ions, and metastables are confined to affect only nearby cells because of their interactions with the electric fields and reactions with other gas-discharge phenomena. The photons, however, are unhindered by any of the events in the gas volume and can effectively prime cells at some distance. Thus, the main drawback of priming is that other cells at a distance are caused to be "primed" in addition to the selected cells, resulting in spurious discharges - an undesirable result.

Wall-charge coupling, as its name implies, uses the actual transfer of charge from one cell to the next to accomplish the shifting. In this scheme, a cell will only fire if it receives a transfer of electrons produced when proper voltages are applied to a neighboring cell, one of whose electrodes is common to both cells. In such case, the common electrode acquires a wall charge which influences the discharge state of the next cell in line. Such types of devices are described by W. E. Coleman et al, in "Device Characteristics of the Plasma Charge Transfer Shift Display," IEEE

Transactions on Electron Devices, Vol. ED-28, pp. 673-679, June, 1981.

A somewhat different type of shift panel is described in U.S. Patents, US-A-4,430,601 and US-A-4,328,489 to Peter D. T. Ngo. The shift panels disclosed therein include both display columns and "transfer" columns. When a transfer of data is desired, an excitation pulse is applied to the display column and a priming pulse to the transfer column. The plasma discharge created by the excitation pulse is said to be transported to the transfer column by the action of the priming pulse causing it to switch to the ON state. Careful analysis of the Ngo structure shows, however, that the plasma discharge is actually forced to migrate to an area whose residual wall voltages are invariably more negative than the wall voltage at the display site where the plasma originated. In essence the plasma is forced to travel "uphill" and the resulting panel operation has been shown to have poor operational margins.

Shift panels suffer from a number of other disadvantages such as slow panel update rates; no random access ability; and poor yields due to the fact that one defective pixel will cause the loss of an entire line.

Another approach to reducing circuit requirements involves the use of gas-discharge logic. One such scheme is described in Schermerhorn U.S. Patent 3,925,703 and by Schermerhorn and Miller in "Discharge Logic Drive Schemes", IEEE Transactions in Electron Devices, Vol. ED-22, No. 9, pp. 669-673, Sept., 1975. In that arrangement, a display pixel is defined by the intersection of two pairs of orthogonal electrodes. The electrodes are grouped in such a way as to give each pixel four distinct inputs. A particular pixel may be erased only when all four of its inputs are selected. This gas-discharge action is functionally equivalent to a four input AND gate and employs a plasma coupling or spreading technique.

Schermerhorn's logic technique results in a rather dramatic reduction in line driver requirements. In a typical 512X512 panel, 48 lines per axis or a total of 96 lines are required. This represents an order of magnitude in savings over the normal 1024 required drivers. However, the savings in circuit costs are offset by the increase in panel manufacturing cost. Crossovers increase in number and area with increasing panel size and add expensive fabrication cost to the panel. Furthermore, the sustain signal is applied to all drive lines resulting in the sustain driver being a very high current device with a corresponding requirement that it exhibit a low impedance, a particularly difficult and expensive set of criteria to meet.

One method to reduce the electronics cost has been the development of plasma AND gates as

described in U.S. patent US-A-4,574,280 issued 4 March, 1986 to Larry F. Weber. Such AND gates can be integrated into the display panel itself, increasing its cost only slightly, while reducing electronics requirements by more than an order of magnitude. These devices have the capability of driving the capacitive load of an address electrode in a standard AC plasma panel; however, it has been found that the 20mA sustain discharge current that is required when all the pixels along an electrode are discharging causes an undesirable voltage droop which is likely to reduce the panel operating margin excessively.

Attempts have been made to separate the sustain operation from the address circuitry. In this regard Andoh, et al. U.S. Patent US-A-4,044,349 employs 4 discharge site pixel locations and applies enhanced X and Y sustain-type pulses to one discharge site and a standard sustain signal to another site. When the addressed site discharges, particles from the discharge affect the other three discharge sites and reduce their firing levels. As a result the subsequent application of a sustain signal to the pixel site turns on the pixel site as well as the other sites. Andoh's write technique, which employs sustain-type signals, is very slow, and the use of the priming particles to influence adjacent discharge sites leads to poor operational voltage margins for the panel.

This invention is generally concerned with a plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining address locations at which plasma discharges are selectively effected by selective energisation of the address conductors.

Plasma display panels of the kind set forth in the preceding paragraph are disclosed in specifications U.S.-A-3,886,404 (Kurahashi et al) and GB-A-2 129 595 (Western Electric).

Copending European patent application 87113568.9, published under the number EP-A-0 261 584 on the 30th March, 1988, discloses a plasma display panel of the kind set forth in which each address conductor of each set has a sustain conductor on each side thereof offset from the address conductor and parallel thereto, such that adjacent to each address location there are four sustain conductor intersections defining pixel dis-

charge positions to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors;

said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of each of the address conductors intersecting at a selected address location at which a plasma discharge has been effected for selecting one of the four pixel discharge positions associated with that address location for a sustained pixel display discharge at the selected one pixel position.

The characteristics of the plasma display panel given above are not found in the prior art referred to previously.

Certain aspects of the invention relate to a plasma display panel of the kind set forth and having the characteristics defined above. Such a plasma display panel will be referred to as a plasma display panel having the characteristics stated.

According to a first aspect of the invention in a plasma display panel having the characteristics stated, said first energising means includes a gas discharge shift register for controlling the selection of the address conductors of one set.

According to a second aspect of the invention in a plasma display panel having the characteristics stated, the address conductors and sustain conductors of both sets are supported at a single one of said dielectric walls.

According to a third aspect of the invention in a plasma display means having the characteristics stated, the address conductors of one set are arranged to have the address conductors connected in groups such that an address operation simultaneously selects a plurality of address locations in a group, and in which said second means includes a plurality of sustain sources for the sustain conductors associated with the address conductors of said one set, the sustain sources being so arranged that the two sustain conductors located on each side of each address conductor of said one set are connected to different sustain sources to differentially energise the two sustain conductors, and the sustain conductors associated with the address conductors of a group are connected to different sustain sources to enable pixel discharge position selection with respect to the simultaneously addressed address locations.

In a further aspect of the invention there is provided a plasma display panel of the kind set forth, characterized in that:

each address conductor of one set has a sustain conductor on each side thereof, offset from the

address conductor and parallel thereto, such that adjacent to each address location along the address conductor there are two conductor intersections defining pixel discharge points which are on opposite sides of the address conductor, between which a pixel display position is defined and to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors; and

said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of an address conductor of said one set at a selected address location along which a plasma discharge has been effected so as to establish a sustained pixel display discharge between the two pixel discharge points associated with that address location.

In a still further aspect of the invention there is provided a plasma display panel of the kind set forth, characterized in that:

each address conductor of one set has two sustain conductors on each side thereof, offset from the address conductor and parallel thereto, such that adjacent to each address location there are four conductor intersections defining two pairs of pixel discharge points which are on opposite sides of the address conductor and between each pair of which points a pixel display position is defined, and to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors;

said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors comprising first and second sustain sources to which alternate ones of said sustain conductors are connected and which differentially energise the sustain conductors on opposite sides of an address conductor along which an address location discharge has been effected by said first means in order to select one of the two pixel discharge position associated with that address location for a sustained pixel display discharge.

In general the various forms of gas discharge panel embodying the present invention employ the phenomenon of plasma spreading. In such a panel, plasma spreading or "coupling" is employed to couple the plasma at an addressed location or cell to one of a plurality of pixels to be illuminated. The pixels are defined by pixel positions or cells comprising one or more pixel discharge points. The spreading is controlled by assuring that the wall

voltages are properly related so that the plasma electrons migrate to a region where the voltages are approximately equal to or more positive than the wall voltages where the plasma originated and deposit residual wall charges. Paired sustain electrodes are subsequently selectively energized, which, in combination with the residual wall charges cause the desired discharge site to be turned on or off.

The invention and its practice will be further described with reference to the accompanying drawings, in which:

Fig. 1 is a cross-section of several pixel locations in a gas discharge panel and is used to enable a better understanding of the function of plasma coupling.

Fig. 2 is a plan view of an electrode layout in a plasma discharge panel having a construction incorporating the characteristics stated above.

Fig. 3 is an expanded view of a portion of the electrode arrangement in Fig. 2.

Fig. 4 are wave form diagrams useful in understanding the operation of Fig. 2.

Fig. 5 shows the charge state at a group of pixel sites at various times during the operation of the invention.

Fig. 6 is an expanded view of a pixel site during the erase operation.

Fig. 7 are waveform diagrams useful in understanding the erase operation and the operation of the panel in a video mode.

Fig. 8 is a plan view of an electrode layout of a hybrid version plasma discharge panel constructed in accordance with invention.

Fig. 9 is a plan view of another electrode layout of a hybrid version plasma discharge panel constructed in accordance with the invention.

Fig. 10 is a sectional view of a pixel location of the electrode layout of Fig. 8.

Fig. 11 are waveform diagrams useful in understanding the operation of Fig. 8.

Fig. 12 is a cross-section of several pixel locations of the electrode layout shown in Fig. 9.

Fig. 13 are waveform diagrams useful in understanding the operation of Fig. 9.

A description of the physics of operation of a plasma discharge device will enable a more complete understanding of the preferred embodiments of the invention. A plasma discharge is, in essence, a region with a high density of positive and negative charges of nearly equal proportions. In a gas-discharge panel, ions and electrons make up the charges within the plasma. After the discharge, the charged particles move to offset the electric field induced by the applied voltage. The plasma acts like a metal conductor by carrying charges in the presence of a field until the field is sufficiently offset to stop the breakdown of the gas. In other

words, positive and negative charges are transferred to opposite dielectric walls by the plasma to oppose the field created by the applied voltage. The polarity of the applied voltage during the sustain sequence is usually reversed after a period of time. When this happens, a high electric field will again exist across the gas which is additive to the field created by the positive and negative charges existing on the walls from the previous discharge. In the presence of these additive electric fields, a discharge will occur causing a plasma to again develop and thus create a current path between the anode and cathode. Wall charges are again conducted to opposite ends of the gas cavity and reduce the voltage seen by the gas. While the plasma is active, it will transfer negative charges from the cathode to the anode and positive charges from the anode to the cathode. This action creates a "pulsing" light discharge, which if repeated at a high enough frequency, provides a constant pixel illumination with no perceivable flicker.

A phenomenon known as plasma spreading has been observed in the past in plasma discharge panels. Some designers have sought ways to avoid such spreading due to the "bloom" which it causes at pixel sites and the resultant degradation of the display's quality. Others (i.e. Schermerhorn in U.S. Patent US-A-3,925,703) have used it to assure that all gas cells in a multi-cell pixel are illuminated upon the application the sustain signal. Only recently has quantitative data been taken which supports the existence of plasma spreading along both the anode and cathode. The speed of plasma spread along the cathode has been measured to average about 460 meters per second, whereas along the anode it spreads at 6250 meters per second, an order of magnitude greater than the cathode plasma speed. It is believed that the difference in the plasma speed is due to the difference in the mobilities of the electrons and heavy ions. Since the highly mobile electrons are acting along the anode, the speed of the plasma in this area would be higher than in the area of the cathode where the slow ions control the discharge rate.

Referring now to Fig. 1, a cross section of a series of pixel sites are shown. Conductors 10, 12 and 14 are supported on glass plate 16 and are provided with a dielectric overcoat 18. Dielectric 18 is preferably glass with a magnesium oxide overcoat. Orthogonally oriented conductor 20 is supported by glass plate 22 and also is coated with glass/MgO dielectric 24. When appropriate voltages are applied across conductors 12 and 20, a plasma discharge 26 will occur and wall charges immediately begin to build up in opposition to the applied voltage. Additionally, plasma discharge 26 will preferentially spread along the portion of dielectric layer 24 which immediately overlays conductor 20

(anode) and will deposit negative charges onto the dielectric surface. If prior to discharge, preexisting wall voltages on dielectric layer 24 at pixel sites corresponding to the intersections of conductors 10 and 20, and 14 and 20 are substantially equal to or more positive than the initial wall voltage on dielectric layer 24 at the site of discharge, the plasma so created will spread nonpreferentially in both directions on dielectric layer 24 over conductor 20. On the other hand, if the wall voltage on dielectric layer 24 at an adjacent pixel site is negative with respect to the wall voltage on dielectric layer 24 at the originating discharge site, the direction of plasma electron travel is preferentially away from that adjacent pixel site. (Of course, the ions in the plasma will be attracted to the adjacent pixel site, but at a rate at least ten times slower than the electron movement). By the time the ions arrive at the adjacent pixel site, most of the discharge activity will have terminated and little wall charge effect is seen. It is the electrons movement phenomenon which is utilized throughout this invention to control pixel operations.

The aforementioned spreading of the plasma can be used to "write" pixels. If it is assumed that dielectric layer 24 at all discharge sites in Fig. 1 have zero initial wall charges, the plasma discharge spreads along conductor 20 (anode) and deposits electrons on dielectric layer 24 at all three sites. A smaller population of ions is deposited on the portions of dielectric 18 which cover conductors 10, and 14. These deposited charges leave residual wall voltages at the two outside discharge sites. If the residual wall voltages are sufficiently large, the cells will be caused to discharge upon the application of subsequently applied sustain voltage transitions. The residual wall voltage levels at the outer pixel sites have been found to be dependent substantially on the strength of the discharge at the central cell.

Referring now to Fig. 2, a plan view of a plasma panel constructed in accordance with the invention is shown. All horizontal electrodes in Fig. 2 (along with their associated electronics) reside on one substrate of the panel and are referred to as Y electrodes. All of the vertical electrodes (and their associated electronics) reside on the opposite substrate and are termed the X electrodes. In this arrangement, electrodes used for addressing are separated from those used to perform the sustaining operation. In Fig. 2 there are 8X8 or 64 display pixels indicated by black dots 31. Each of X address electrodes 30, 32, 34, and 36 are connected to a suitable circuit driver 38, 40, 42 and 46, respectively. Likewise, each of Y address electrodes 48, 50, 52 and 54 are connected to circuit driver 56, 58, 60 and 62, respectively. The intersections of each X and Y address electrode forms

what will be referred to as an "address" cell. This address cell is used only during addressing operation and is not used as a normal display pixel. Each of the  $4 \times 4 = 16$  address cells are identified by a small  $\times$  33 in Fig. 2.

The X sustain signals are provided by two sustain generators 70 and 72, whereas the Y sustain signals are applied from sustain generators 74 and 76. Each successive pair of sustain electrodes (eg. 78 and 80) are shorted together by shorting bars 82 and 84 at either end thereof, thus forming what shall be referred to hereinafter as a sustain electrode pair. Alternating sustain electrode pairs on a given substrate are bussed together by a sustain bus resulting in two sustain busses on each substrate. On the X substrate, busses 71 and 73 are respectively connected to sustain generators 70 and 72 and on the Y substrate, buses 75 and 77 are connected to sustain generators 74 and 76. It should be noted that this arrangement results in only two connections along the X sustain edge of the panel and two connections along the Y sustain edge. With this sustain arrangement, four circuits are needed to completely sustain the panel. This remains true regardless of whether the panel is 8X8 or 512X512 pixels in size.

Also shown in Fig. 2 are edge field electrodes 90, 92, 94 and 96. These are sustain electrodes which reside along the four edges of the addressable area of the panel. The pixels at these locations are not addressable. These extra sustain electrodes are required in order that the outer-most addressable pixels see a similar field as the other pixels in the panel. Also, these extra sustain electrodes complete the loop of the sustain electrode pairs along the border of the display.

The area encircled by the dashed line and denoted as 100 in Fig. 2 is shown in detail in Fig. 3. Note, that as in Fig. 2, all X-level electrodes are supported by one substrate, and all Y electrodes are supported by the other substrate with an ionizable gas disposed therebetween.

Address cell A resides at the center of the Fig. 3. The four nearest neighboring display pixels to address cell A are labeled as P1, P2, P3, and P4. Four additional discharge locations act as "coupling" cells with the two vertical coupling cells being labeled C1 and C4, and the horizontal coupling cells denoted as C2 and C3. Note that each of the four display pixels, P1-P4, are controlled by a different combination of X and Y sustainer conductors. Pixel P1 is defined by the intersection of the XS<sub>a</sub>/YS<sub>a</sub> sustain electrodes, whereas pixel P2 is defined by the intersection of the XS<sub>b</sub>/YS<sub>a</sub> electrodes, etc.

Because of the bussing structure of the sustain electrodes, the voltage applied to pixel P1 is also applied to one quarter of all of the display pixels on

the panel. The same is true for pixels P2-P4. Thus, a single display pixel cannot be individually selected for write and erase operations by using sustain electrodes to control the pixels as is the case in the standard matrix addressable plasma panels. For that reason, the X and Y address electrodes must be used to access them. In summary therefore, each address cell is surrounded by eight discharge sites wherein four (P1-P4) are used as actual pixel display sites, and four (C1-C4) are used to accomplish the selective control of the display pixel sites.

Prior to discussing the operation of an exemplary address site, the overall addressing technique for the display panel will be briefly discussed. A video addressing technique was employed since it is the most common interface found in current display products. Video data is entered along the column electrodes for one horizontal row at a time. The top row of the panel is addressed first. After a row is completely addressed, a horizontal sync signal signifies that the next row in the panel is to be addressed. This row by row scanning continues until the bottom row in the panel is addressed at which time a vertical sync signal indicates the start of a new frame and the scanning sequence begins again at the top row of the panel. In applying this addressing technique to the panel shown in Fig. 2, initially all display pixels in the two rows on either side of a Y address electrode are written. Those display pixels in the same two rows that need to be in the off state are subsequently erased. The video scanning sequence then continues by writing the next two rows of display pixels, etc. This method requires two distinct types of cycles. The first being a "Write Two Rows" cycle, where the two rows of display pixels that run parallel to a selected Y address electrode are turned on; and the second being a selective erase cycle where the display pixels specified as off in the video bit stream are erased. Each of the specific cycles described above will be discussed herein below separately.

Referring now to the wave forms shown in Fig. 4 in conjunction with Fig. 5, the "Write Two Rows" cycle will be described. In Fig. 4, the applied voltages to each of the sustain and address lines are indicated; the net applied voltages experienced by each of pixels P1-P4, coupling cells C1-C4 and the address cell A; and their respective wall voltages (drawn dashed and inverted-as is conventional). The diagrams in Fig. 5 show the respective cell states after the discharge caused by the applied voltage transitions at the various times t<sub>1</sub>-t<sub>10</sub>. The plus signs represent positive charges and minus signs negative charges. The charges have been placed on either the top or the bottom electrodes to reflect on which side of the cell they

reside after the discharge activity has been completed at the given time. If four diagonal lines surround the cell, it indicates that the cell discharges at the time indicated.

During the "Write Two Rows" cycle, all four sustain generators XSa, XSB, YSa, and YSB and all of the X address electrodes function as they would in a normal sustain cycle. A large negative pulse is placed on Y address electrode 52 at time T2 while positive sustain pulses are present on sustain lines YSA and YSB. The negative pulse causes a large discharge to occur in address cell "A" and horizontal coupling cells C2 and C3. While the address voltage is shown at -150 volts, that is merely for explanatory purposes and can be varied in accordance with the design features of the particular panel. The other voltage levels indicated in Fig. 4 are also exemplary and for descriptive purposes only.

As aforesaid, the application of the negative going pulse at T2 on Y address electrode 52 causes discharges to occur in both the A address cell as well as coupling cells C2 and C3. Note that during the application of the address pulse on Y address electrode 52, both XSa and XSB electrodes are approximately 150 volts more positive for the period between T<sub>2</sub> and T<sub>3</sub>. As a result, the electrons from the plasmas which are created by the discharges at coupling cells C2 and C3 and address cell A travel along the vertical electrodes into the pixel sites P1-P4 on either side of the discharging cells (See Fig. 5 at time T2).

At time T3, both XSa and XSB sustain electrodes have positive pulses applied thereto and, in conjunction with the prestored wall charges, pixels P1, - P4 are caused to discharge and to emit a light pulse. (It should be remembered that only a pulse of light is given off at each wall voltage excursion).

Upon the next negative going excursion of sustain electrodes XSa and XSB, pixels P1 - P4 do not discharge since there is insufficient voltage drop across the cells. Subsequently, the positive going excursion on the YSA and YSB sustain lines cause pixels P1 - P4 to discharge. At time T4, the negative going excursion of the sustain lines resets the wall charges in the horizontal coupling cells C2 and C3 to their original state.

In sum, during the Write Two Rows cycle, horizontal coupling cells C2 and C3 initiate discharges which affect display pixels P1 - P4. The associated X dimension sustain electrodes act as anodes during the C<sub>2</sub>, C<sub>3</sub> discharges thereby allowing the plasma generated by the discharging coupling cells to reach into the display pixels and to deposit electrons beneath the sustain electrodes. The deposited electrons reduce the wall voltages from near 0 to some negative value which, upon

future sustain cycles, cause display pixels P1 - P4 to discharge.

While Fig. 4 shows one set of write two rows waveforms, other cases of write two rows have been found to work properly. Those cases consist of two possible polarities of the  $Y_A$  pulse (both positive and negative) in combination with the two possible polarities of the X and Y sustain pulses. All four cases work with excellent voltage margins even though each uses a different physical addressing mechanism.

Once both rows of pixels have been written, one or more sustain cycles generally will follow to stabilize the charge states within the panel. Then, an erase cycle is commenced which erases selected pixels to provide the desired information content for each display line. The selective erase of a pixel is a two step process and may be understood by referring to Fig. 6. In the first step, cell A is addressed by simultaneous application of positive and negative pulses to the X and Y address lines respectively. This causes a plasma to be created at address cell A which spreads along the X address line electrode (anode). The plasma reaches into vertical coupling cells C1 and C4, causing electrons to be deposited on their dielectric walls beneath the X address line electrode. In the second step of the erase cycle, vertical coupling cell C1 is discharged and the plasma so generated spreads along the YSa electrode reaching into display pixels P1 and P2. The voltages applied to the XSa and YSa sustain electrodes at this time are so phased that pixel P1 is erased and P2 left unaffected.

The detailed operation of the erase cycle will now be described with reference to both Fig. 4 and Fig. 5. In the first step of the erase sequence, address cell A must be used to influence the vertical coupling cells C1 and C4. For the purpose of example, consider erasing pixel P1 (upper left-hand pixel). As shown in Fig. 4, between times T6 and T7, the sustain voltages applied to XSa and XSb cause each of pixels P1 - P4 to discharge in the normal sustain mode (they having already been written into the "on" state during a previous Write Two Rows cycle). At time T7, a positive going pulse is induced on X address electrode 34 and a negative going select pulse is induced on Y address electrode 52. This results in a sizable discharge occurring at address cell A. In addition, since the X address electrode 34 acts as an anode during the discharge of address cell A, the plasma spreads along beneath it into the C1 and C4 coupling cells. As a result, a negative charge is deposited therein from the plasma. This can be seen in Fig. 4 on the wall voltage diagrams for both coupling cells C1 and C4 at T7.

The second step of the erase sequence starts at time T8. At such time, the C1 coupling cell whose X address electrode dielectric was negatively charged in the first step of the erase operation is used to erase pixel P1. At time T8, the voltages on both sustain lines XSa and YSa rise to approximately 100 volts. Due to the previously stored wall charges at C1 which are additive to the applied potential on sustain line YSa, cell C1 is caused to discharge. (Note that C1 would not discharge at this time if its wall voltage had not been raised at time T7). Also the raised voltage on the YSa electrode causes it to act as an anode during C1's discharge and allows the plasma created thereby to be coupled into the P1 pixel site. The electrons thus deposited by the spreading plasma during time T8 neutralize the previously stored charges at P1 thereby causing P1 to be erased. This is indicated in Fig. 4 by the slanted portion of the wall charge voltage on the P1 line after time T8.

During this erase cycle, it is vital that the other display pixels not be affected. While P1 is being erased, the plasma generated at coupling cell C1 will reach both into P1 and P2. Recall that P2 was turned on during the Write Two Rows cycle. When, however, the raised voltage is applied to the YSa electrode at time T8, that potential, added to the prestored wall charge causes P2 to discharge. This is a normal sustain discharge which keeps pixel P2 in the on state and prevents the C1 discharge from affecting it. It should be noted that if P2 was in the off state, the wall voltage potential under the YSa electrode at pixel P1 would be much higher than the YSa wall voltage at P2. Thus the plasma created by the discharge of C1 would reach out and discharge pixel P1 first, exhausting itself before it could transfer negative charge to pixel P2. Thus, P2 would remain off.

To insure that pixels P3 and P4 are not affected, coupling cell C4 must not discharge at time T8. This is assured by controlling sustain electrode YSb differently from sustain electrode YSa. Note that there is no positive going transition at time T8 on YSb thereby preventing any discharge at coupling cell C4. On the other hand, when the x and y address line voltages fall, there is a substantial voltage change impressed across address cell A which creates a discharge. In this instance, as contrasted to prior instances, it is the ions which migrate (slowly) towards cell C4 and act to neutralize the prestored wall charges therein. This sets up C4 for a subsequent address cycle.

At time T9, the voltage on sustain line XSa falls to 0. One hundred volt levels are present on sustain lines YSa and YSb. As a result, a sustain discharge occurs in pixels P3 and P4 (remembering that they were previously in the on

state). These transitions occur due to the combined voltage transitions on sustain lines XS<sub>a</sub> and YS<sub>b</sub>. At time T10, coupling cell C1 is discharged by the application of the negative going potential on sustain electrode YS<sub>a</sub>. That negative going potential when added to the wall charges stored therein effects the discharge of cell C1 thereby resetting it for the next address cycle.

To employ the plasma coupling technique in a video addressing mode, it is preferred to break up the erase cycle into four distinct subcycles (See Fig. 7). The first erase subcycle is used to erase pixels on the top row that are controlled by the XS<sub>a</sub> sustain electrode. The second erase subcycle is used to erase any of the display pixels along the top row controlled by the XS<sub>b</sub> sustain electrode. The third and fourth erase subcycles are used to erase the display pixels on the the XS<sub>a</sub> and XS<sub>b</sub> sustain electrodes along the bottom row. Referring now to Fig. 7, the waveforms required for the subcycle erase operation are shown. The dashed line on the X<sub>a</sub> address line shows the voltage as applied to the X address electrode if the pixel corresponding to the particular erase cycle is to be erased. The dashed line on the Y<sub>a</sub> address line shows the voltage applied to the single Y address electrode that runs between the two horizontal rows of pixel electrodes being addressed. The solid line along the Y<sub>a</sub> address indicates that all other Y<sub>a</sub> electrodes are not perturbed.

In the erase P1 subcycle, the XS<sub>a</sub> and YS<sub>a</sub> address lines are both at a high level just after the fall of the X<sub>a</sub> erase pulse. This erases any pixel that is at the XS<sub>a</sub>/YS<sub>a</sub> intersection providing a discharge first occurred at its address cell. In the erase P2 subcycle, XS<sub>b</sub> and YS<sub>a</sub> sustain lines are both at a high level. Any "on" pixel residing at the intersection of the XS<sub>b</sub>/YS<sub>a</sub> sustain electrodes will be erased providing that its address cell was selected at the beginning of the erase cycle. Succeeding cycles work in a similar fashion. Note that the YS<sub>a</sub> address line is selected in the first two cycles when the pixels on the top electrodes are being erased, while the YS<sub>b</sub> electrode is selected during the last two cycles when the bottom row of pixels are being erased. It will also be noted that each of the erase cycles is actually composed of an erase and a sustain. A single sustain discharge is needed after the erase cycle to complete the subcycle.

The advantages of the above-described address and sustain technique are numerous. Most notable is the two-to-one reduction in the address electrodes. Thus, only half the number of circuit drivers are required to address a panel based on the plasma coupling concept. In addition, since the sustain and address circuits have been separated, the load seen by the address circuit is substantially

lessened because the sustain load is relegated to those sustain drivers. Because of this separation of function, high impedance address drivers become usable. (essentially are cheaper than low impedance circuits.) Furthermore, the gas discharge gate structures shown in US-A-4,574,280 (which are inherently, high impedance) may be constructed directly on the plasma panel structure further reducing the requirement for off-panel driver circuitry.

A further advantage of the above-described design is the reduction in the number of potentially defective panels during manufacturing. It can be demonstrated that the electrode yield is increased by a factor of two over the standard electrode design. This is due to the fact that panel yield is most often hurt by electrode breaks. The key factor that contributes to the increased yield are the sustainer electrode design and the decreased number of address electrodes. In essence, each sustain electrode is doubled so that a break on one does not necessarily disconnect pixels below the break from the drive circuitry. The pixels below the break are still connected to the line drivers via the shorting bar that connects to the neighboring sustain electrode. This alternate conduction path allows all pixels on the broken electrodes to remain fully operational.

A further feature of this development is that there are less sustain bus crossovers than in previous designs. In addition, the peak currents required from the sustain drivers are lessened due to their duplication.

A plasma panel constructed in accordance with the above teaching has been successfully operated. Its specifications are as follows:

Dielectric Glass thickness: 25 um  
 Dielectric Glass Dielectric Constant: 15  
 MgO Overcoat Thickness: 150 nm  
 Gas Gap Distance Between Substrates: 100um  
 Gas Mixture: 400 torr ( $5.3 \times 10^4$  Nm<sup>-2</sup>) Ne + 0.1% Ar  
 Electrode Width: 75um  
 Center to Center Spacing of Pixels: 400 um  
 Center to Center Spacing of Address and Sustain Electrodes: 200um

#### Waveform Timing

Sustain Pulse Width: 6 us or longer  
 Y<sub>a</sub> Write Pulse Width: 10 us or longer  
 Erase Pulse Width: 5 us or longer

#### Waveform Voltage Amplitudes

Sustain Voltage: 89 to 98 volts  
 Y<sub>a</sub> Write Pulse: -140 to -260 Volts  
 X<sub>a</sub> and Y<sub>a</sub> Erase Pulses: 80 to 140 Volts

The number of connections to the panel can

be further reduced by employing a gas discharge serial-to-parallel shift register to load the gas discharge X and Y address gates. Such gas discharge shift registers are compatible with the technology of the herein-described plasma coupling structures. Such a serial shift register operates in principle similarly to that shown in the Coleman, et al. article cited hereinabove. The parallel output from the shift register would be applied directly to the X and Y address gates.

When gas discharge AND gates are connected to the address electrodes of the circuit of Fig. 2 to reduce the number of address drivers, the input electrodes of these AND gates are normally connected in a multiplexing arrangement that allows for a reduced number of drivers. For instance, to drive 256 address electrodes, 256 AND gates would be used and the AND gate inputs would be bussed in two groups of 16, ( $16 \times 16 = 256$ ) so that only  $16 + 16 = 32$  drivers are required, (see Fig. 1 of US-A-4,574 280). This number can be reduced even further by using a gas discharge shift register to drive the inputs of the AND gates. This approach is especially attractive for driving the Y axis AND gates for a display operating in video mode. Such operation requires that only one Y address electrode (horizontal) be selected at any one time. The gas discharge shift register for the Y axis needs to shift only one bit along the Y axis to select the single AND gate that addresses the single Y address electrode. Since suitable gas discharge shift registers can be designed with as few as 4 electrode inputs, such a technique offers a considerable advantage over other techniques such as the one discussed above requiring 32 drivers. In video mode, only these 4 inputs would need be driven for a display of any number of Y address electrodes. Such a gas discharge shift register could also be used for the X axis address drivers, however, the data input to this X shift register would be more complicated, reflecting the video input to the display.

There are a number of ways that a gas discharge shift register could be designed to drive the AND gates. Such shift register devices have been developed for display purposes and are reviewed in the paper by Coleman, et al. referred to above. The output of the shift register can be in the form of a voltage on an electrode that is connected to the input electrode of the gas discharge AND gate. Alternatively, the output of the shift register can be a plasma in the shift register that couples to the gas discharge AND gate to deposit wall charges that will cause the AND gate to discharge.

The gas discharge AND gates can also act as storage registers to hold binary information by means of the wall charges in the AND gate. If these wall charges are present and the appropriate

5 pulses are applied to the electrodes of the AND gate, then the gate will generate an output pulse that can be used to drive a plasma panel address electrode. The gas discharge shift register having video or other data can be used to transfer data to the storage register in the AND gate and then the AND gate can be pulsed at a later time as required by the addressing requirements of the plasma display. These independent AND gate load and pulse output times facilitate the rapid distribution of data to the AND gates at a time when the plasma panel does not require address pulses. This yields a considerable time savings that allows faster display scanning and data transfer rates.

10 The invention disclosed here has been discussed in terms of the conventional two substrate display shown in Fig. 1. It is equally applicable to a single substrate display wherein both sets of orthogonal electrodes are placed on the same substrate. Such a plasma display is constructed by first depositing a set of parallel electrodes on the substrate glass. For purposes of illustration these will be designated the X electrodes. A dielectric layer is then deposited over the substrate which covers the X electrodes. Next a set of parallel Y electrodes is deposited on the dielectric layer and are positioned to be orthogonal to the parallel X electrodes. Next a dielectric layer is deposited over the Y electrodes. A suitable gas is then placed in contact with this dielectric layer so that a gas discharge can be ignited by means of the fringing fields that extend into the gas from the X and Y electrodes. The properties of this single substrate plasma display are discussed in a paper entitled "A Planar Single Substrate AC Plasma Display" written by G. W. Dick and M. R. Biazzo, which appears in IEEE Transactions on Electron Devices, Vol. ED-23, pp. 429-437, April, 1976.

15 An alternate form of selective erase may be employed in comparison to that shown in Fig. 6. Recall that the selective erase technique is a two step process whereby the pixel  $P_1$  is addressed by means of discharges in, coupling cell  $C_1$  and address cell A. It is also possible to address pixel  $P_1$  through coupling cell  $C_2$ . In this case during step 1 the  $Y_A$  electrode would be made the anode so that the plasma would spread along the horizontal direction to horizontal coupling cells  $C_2$  and  $C_3$ . Then in step 2, one of the horizontal coupling cells  $C_2$  or  $C_3$  would be discharged to address one of the pixels.

20 25 30 35 40 45 50 55 The waveforms to accomplish this are virtually the same as shown in Fig. 4 with the exception that all of the applied X and Y waveforms are exchanged. Also appropriate modifications are made in the sequencing of the sustain pulses during the four erase periods shown in Fig. 7 so that the erase sequence of  $P_1$ ,  $P_2$ ,  $P_3$ , and  $P_4$  is preserved. It is

desirable to preserve this erase sequence so to accommodate the video input data stream. This sequence has an advantage that the discharge sequence of the coupling cells is staggered. For example, when erasing through the horizontal coupling cells, the coupling cell firing sequence for the four erase cycles would be C<sub>2</sub>, C<sub>3</sub>, C<sub>2</sub>, C<sub>3</sub>. The technique shown in Fig. 7 that uses the vertical coupling cells, has the firing sequence C<sub>1</sub>, C<sub>1</sub>, C<sub>4</sub>, C<sub>4</sub>. By staggering the sequence of the horizontal coupling cells, successive discharges of a cell during the erase cycle are avoided and the coupling cell's wall voltage is allowed to come to an equilibrium value that will set up the coupling cell for the proper discharge amplitude.

A further reduction in the number of address circuit drivers can be achieved with an electrode connection technique that uses more sustain generators. For instance, the technique shown in Fig. 2 shows that 8 rows can be addressed with 4 address drivers 56, 58, 60 and 62 by utilizing two Y sustain drivers 74 and 76. It is possible to use these 4 address drivers to address 16 rows if the number of Y sustain drivers is increased to 4. The modifications to the circuit of Fig. 2 would involve the replication of the illustrated sustain lines for Y addresses 8 to 15 and the connection of two additional Y sustain drivers in much the same manner as Y sustain drivers 74 and 76 are connected to their respective sustain pairs. Each of the address driver lines would be similarly positioned between sustain line pairs. Address driver 56 would be connected, in addition to electrode 48, to the electrode between Y address sustain lines 8 and 9; address driver 58 to the electrode between sustain lines 10 and 11; etc.

The pixel that is to be addressed would be determined by which of the four sustain generators is selected during the address period. For example, to address the row electrode with Y address = 9, address driver 56 is pulsed in conjunction with proper phasing of the sustain driver connected to the proper sustain electrode pair. The other rows associated with address driver 56 (Y address rows 0, 1 and 8) would not be influenced because their respective sustainers would be phased differently. This technique could further be extended for additional reduction in the number of address drivers by the addition of more sustain generators.

This alternative technique connects two address electrodes together along the right hand edge of the panel. By also connecting each connected address electrode pair along the left hand edge of the panel, additional redundancy could be achieved to protect against electrode breakage. Since each address electrode is connected, at both ends, a single break in one address electrode of the address electrode pair will not cause any ad-

dress failures because of the alternate conduction path. This technique would allow for very significant increase in panel yield beyond that already achieved by pairing the sustain electrodes. Of course, the cost of this modification is seen in a number of added cross-overs.

The above example discusses address driver reduction for the Y axis. Of course, similar techniques are applicable to the X axis.

The examples presented have assumed that the plasma display will be addressed in the video mode which is commonly used for computer and television displays. It is also desirable for displays to be addressed in the random access mode of operation. In such a mode the display receives an address which can be used to turn a selected pixel or pixels either on or off. The techniques presented here could readily be applied to a display operating in random access mode.

Referring now to Figs. 8 and 10, a hybrid design for an AC plasma display panel is shown which employs concepts used in both single and double substrate panel structures. In this structure, all X dimension electrodes are on the upper substrate and all Y dimension electrodes are on the lower substrate. The sustain generators are applied only to the Y axis of the display (lower substrate). The X electrodes are used only for addressing and no sustain signals are applied thereto. One advantage of this type of structure is that only the XA electrode is present on the upper glass substrate of the panel and allows a greater amount of light to be emitted than other panel constructions. One disadvantage of this design is that the plasma discharge tends to spread along the length of the Y electrodes and to make the display useful, physical barriers 104, 106, and 108 are emplaced between each row of pixel locations. These barriers can take the form of solid ribs placed in the glass gap between the substrates.

In Fig. 10, the cross-sectional view of a single pixel region of the hybrid display of Fig. 8 is shown. In this case, the actual display pixel discharge occurs between the Y<sub>Sa</sub>, Y<sub>Sb</sub> electrodes. Coupling cells C<sub>1</sub>, C<sub>2</sub>, C<sub>3</sub>, and C<sub>4</sub> exist as shown. The address cell A is shown between the X<sub>Aa</sub> and Y<sub>Aa</sub> electrodes.

The waveforms for the operation of the display of Figs. 8 and 10 in a video mode are shown in Fig. 11. Initially, there occurs a "WRITE ROW" cycle that selects a single row of the display and sets all of the pixels in that row to the ON state. Subsequently, a two-step selective erase cycle occurs to set the appropriate pixels in that row to correspond to the data.

Referring now to Fig. 11, in combination with Fig. 10, time T<sub>1</sub> is the beginning of the write row cycle where the Y<sub>Sa</sub> pulse is raised high. This is a

normal sustain transition that causes all ON pixels in the display to discharge. At T2, a large negative pulse is applied to the selected YAa electrode. All other YA electrodes in the display remain at the initial +100 volt level. This negative pulse causes coupling cell C<sub>2</sub> to discharge because of the large voltage appearing between YSa and YAa. This discharge causes wall voltage changes on the dielectrics that cover YSa and YAa with YSa acquiring a negative wall voltage and YAa, a positive wall voltage. Because the YSa electrode is in common with pixel P, the negative wall voltage on YSa reaches a level that corresponds to the ON state for pixel P. Thus, the discharge of coupling cell C<sub>2</sub> causes the writing of pixel P. Note there is a wall voltage transition associated with the YAa pulse at T2 for all of the cells that are associated with the same electrodes that are in common with coupling cell C<sub>2</sub>.

At T3, the large negative pulse on the selected YAa electrode is returned to its initial +100 volt level and simultaneously the YSb electrode is raised to 100 volts. These transitions do not cause any discharge activity because none of the cells have sufficient voltage across them.

At time T4, the YSa electrode is returned to 0 volts. This is a normal sustain transition that causes all the ON pixels in the panel to discharge. Since the row of pixels that are addressed during this write cycle have a wall charge on them deposited during the YAa pulse at time T2, those pixels discharge just as if they are in the ON state and continue to discharge on sustain transitions until an erase pulse occurs. The sustain transition at T4 also causes the wall voltage at coupling cell C<sub>2</sub> to return to near its initial state which occurred before the T2 address cycle.

Once the selected row of pixels is turned on and has stabilized, the selective erase waveforms are applied. Time T5 marks the beginning of the selective erase cycle with a rise of YSa and the fall of YSb. This is a normal sustain transition that causes all P pixels in the display to discharge. The sustain discharge leaves a positive wall charge on the dielectric covering the YSb electrode which will be employed during subsequent phases of the erase cycle. Note that this sustain discharge causes small wall voltage transitions in the coupling cells because they have common electrodes with the discharging pixel. The address cell does not show significant wall voltage change at this time because the XAa and YAa electrodes do not change, and also the wall voltage in the address cell has already come to equilibrium.

Step 1 of the erase cycle starts at time T6 with a negative going pulse applied to the selected YA electrode. If the pixel is to be erased, then a positive 100 volt pulse is applied to the XA elec-

trode that intersects the selected pixel. If the pixel is to remain in the ON state, then no XA pulse is applied. Time T6 shows the waveforms applied when the selected pixel is to be erased. The XAa and YAa pulses add across the A address cell to discharge it. In this case, the XAa electrode is the anode, and its potential is nearly equal for the locations corresponding to the C<sub>1</sub>, A and C<sub>4</sub> coupling cells. This means that plasma coupling occurs and the plasma spreads from address cell in both directions towards coupling cells C<sub>1</sub> and C<sub>4</sub> thereby causing negative charges to be deposited on the XAa dielectric in the regions of the C<sub>1</sub> and C<sub>4</sub> coupling cells.

The second step of the erase cycle commences at time T7. The XAa and YAa pulses are returned to their initial levels of 0 volts and +100 volts respectively. Also the YSb pulse rises to the +100 volt level which, in combination with the negative charge deposited on the XAa electrode due to plasma coupling at T6 and the previously deposited positive wall charge on the dielectric covering the YSb electrode, causes a discharge in coupling cell C<sub>4</sub>. This discharge causes electrons (a negative wall voltage) to be deposited on the YSb dielectric since it is the anode for this discharge. These electrons cancel the positive charge that was on the YSb dielectric - due to the sustain discharge at T5. Canceling this charge on YSb results in altering the wall voltage of pixel P so that it goes to the OFF state. The waveforms transitions at T7 also cause a discharge at address cell A. In this discharge, the wall voltage of the address cell is returned to its initial level before the application of the pulse at T6.

At T8, a normal sustain transition due to the fall of the YSa pulse occurs. All of the ON pixels in the panel discharge; however, the pixel which was just erased shows no discharge activity. At T9, a normal sustain discharge again occurs for all of the ON pixels in the panel. Time T9 represents the start of a new cycle which could be either a write row cycle, a selective erase cycle, or a normal sustain cycle.

The display panel shown in Figs. 8 and 10 has a number of advantages. It enables the employment of high impedance address drivers; exhibits low sustain capacitance characteristics and, due to the use of paired sustain conductors, has a potentially higher panel yield. Its major negative is that it does not allow for any reduction in the number of address drivers.

Referring now to Fig. 9 in conjunction with Figs. 12 and 13, a further embodiment of this invention will be described. As in Fig. 8, all Y dimension electrodes reside on one substrate whereas the X drive electrodes reside on the other substrate. As in Fig. 8, barriers 110, 112, and 114

are provided to prevent the spread of plasma discharges. Each of the discharge pixels is noted by a dashed circle. Referring to Fig. 12, a cross-section of the display panel shown in Fig. 9, indicates the position of various coupling cells C<sub>1</sub> - C<sub>6</sub> and pixel discharge sites P1 and P2. In addition, address cell A exists between drive electrodes YAa and XAa. Address cell A in this instance controls two display pixels P1 and P2. The choice of which pixel is to be addressed is determined by the phase of the sustain voltages applied to electrodes YSa and YSb. This allows the number of Y address drivers to be reduced by a factor of 2 over the design shown in Fig. 8. In this circuit, however, the advantage gained by virtue of the provision of coupled sustain electrodes is not present.

In Fig. 13, the waveforms are illustrated which drive the circuit of Figs. 9 and 12. These waveforms illustrate three cycles used to drive the display in a video mode. The cycles consist of a "Write Two Rows" cycle that turns on all of the pixels in two selected rows. The following two erase cycles are employed to erase pixels in each of these two rows depending on the video data.

The write two rows cycle begins with a rise on the YSa electrode which causes a normal sustain discharge in all of the pixels in the panel that are in the ON state. At T2, a large positive pulse is placed on a single selected YA electrode and all other YA electrodes remain at 0 level. In this instance, the positive pulse is placed on the YAa electrode and causes a large discharge in address cell A and in coupling cells C<sub>3</sub> and C<sub>4</sub>. The discharge in coupling cells C<sub>3</sub> and C<sub>4</sub> cause the deposition of positive charge on the dielectric layers which cover electrodes YSb and YSa that are on either side of the YAa electrode. Since both of these electrodes are associated with pixels P1 and P2, this positive charge alters the wall voltage of these pixels. This may be seen in Fig. 13 just after T2 as a rise in the wall voltage of P1 and a fall in the wall voltage of P2. These wall voltages appear to go in different directions for the same influx of positive charge because this charge goes on YSb for P1 and YSa for P2 (oppositely poled). Thus, the discharge which occurs at T2 acts as a write for both P1 and P2.

At time T3, the YAa potential falls and YSb rises to +100 volts. This results in a discharge in all ON pixels in the panel except those in the row associated with P2. The P2 pixels that are ON do not discharge because the positive charge deposited on the P2 YSa electrode previously cancels out the affects of the positive transition of YSb at T3. This serves to set the wall voltages of pixels P1 and P2 to the same state.

At time T4, the YSa electrodes rise to +100 volts and the YSb electrodes fall to 0. This is a

normal sustain discharge that results in all ON pixels in the panel discharging (eg. P1 and P2 discharge). Time T4 marks the end of the write cycle and the beginning of the erase cycle. Intervening sustain cycles may be placed between these two cycles in order for freshly written pixels to come to an equilibrium.

At T5, the YSa potential falls and the YSb electrodes rise causing a normal sustain transition. This places a positive charge on the dielectric covering the YSa electrodes if the associated pixel is in the ON state. The positive charge on the YSa electrode of P2 will be used in the erase discharge at time T6. At T6, a +100 volt level is applied to the selected row address electrode (in this case YAa) and the YSb level falls to 0. If the P2 pixel associated with the selected XAa and YAa electrodes is to be erased, then the intersecting XAa electrode goes to 0. Alternatively, if the pixel is to remain ON, then the XAa electrode remains at +100 volts. The pulses on the XAa and YAa electrode cause a large discharge in the address cell A. Because of the positive charge on the dielectric covering, the YSa electrode associated with pixel P2, the potential of this dielectric is nearly equal to the potential of the dielectric covering the YAa electrode.

The address cell A discharge at T6 creates a plasma which couples along coupling cell C<sub>4</sub> from the YA electrode to the YSa electrode of P2. Note that in this instance, the coupling occurs between different electrodes, as contrasted to the previously described structures wherein the coupling occurred along a single electrode. This coupling deposits negative charge on the dielectric covering the YSa electrode associated with P2 and this negative charge cancels the positive charge placed there by the sustain discharge at time T5. This cancellation is an erasure of P2. P1 is not influenced by this discharge because the potential of the dielectric covering the YSb electrode associated with P1 is quite negative relative to the potential covering the YA electrode. This negative potential repels the electrons and prevents plasma coupling from influencing P1 at time T6.

At T7, (end of the erase P2 cycle and the beginning of the erase P1 cycle) the XAa and YAa address pulses are removed and the YSa potential is raised. This results in a normal sustain discharge in all pixels in the panel that are in the ON state. The discharge activity at time T8 corresponds in a similar fashion to that at T6 with the exception that during the T8 pulses, the P1 pixel is erased. In a similar fashion as for P2, pixel P1 is erased by the action of the selected address cell, discharging and causing plasma coupling along the C<sub>3</sub> coupling cell which deposits negative charge on the YSb electrode associated with pixel P1. This negative

charge erases P1.

At time T9, the XAa and YAa address pulses are returned to their initial levels and YSb rises. This results in a normal sustain discharge in all pixels in the panel that are in the ON state. It also causes the wall voltages of the address cell to return to their initial value. There is no discharge activity in the erased pixels P1 and P2. Time T10 marks the end of the erase cycle and the beginning of the next cycle.

## Claims

1. A plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining address locations at which plasma discharges are selectively effected by selective energisation of the address conductors, characterized in that:

each address conductor of each set has a sustain conductor on each side thereof offset from the address conductor and parallel thereto, such that adjacent to each address location there are four sustain conductor intersections defining pixel discharge positions to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors;

said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of each of the address conductors intersecting at a selected address location at which a plasma discharge has been effected for selecting one of the four pixel discharge positions associated with that address location for a sustained pixel display discharge at the selected one pixel position, and

said first energising means includes a gas discharge shift register for controlling the selection of the address conductors of one set.

2. A plasma display panel as claimed in Claim 1 in which the column address conductors and their associated sustain conductors are supported at one of said dielectric walls and the row address conductors and their associated sustain conductors are supported at the other of said dielectric walls.

3. A plasma display panel as claimed in Claim 1 in which the address conductors and sustain conductors are all supported at a single one of said dielectric walls.

4. A plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining address locations at which plasma discharges are selectively effected by selective energisation of the address conductors, characterized in that:

each address conductor of each set has a sustain conductor on each side thereof offset from the address conductor and parallel thereto, such that adjacent to each address location there are four sustain conductor intersections defining pixel discharge positions to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors;

said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of each of the address conductors intersecting at a selected address location at which a plasma discharge has been effected for selecting one of the four pixel discharge positions associated with that address location for a sustained pixel display discharge at the selected one pixel position, and

the address conductors and sustain conductors of both sets are supported at a single one of said dielectric walls.

5. A plasma display panel as claimed in any one of Claims 1 to 4, in which said first and second means are controllably operable in response to video information to be displayed to differentially energise the address and sustain conductors associated with an address location at which a discharge has been effected whereby the four pixel positions are selectively activatable for sustained pixel display discharge thereat.
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6. A plasma display panel as claimed in any one of Claims 1 to 5, in which the two sustain conductors disposed between, and associated with respective ones of, each pair of next adjacent column address conductors are connected together as a column sustain pair, and in which said second means comprises two column sustain sources a first of which is connected to energise alternate column sustain pairs and a second of which is connected to the remaining column sustain pairs.
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7. A plasma display panel as claimed in Claim 6, in which the sustain conductors of each column sustain pair are connected together at both ends.
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8. A plasma display panel as claimed in any one of Claims 1 to 7, in which the two sustain conductors disposed between, and associated with a respective one of, each pair of next adjacent row address conductors, are connected together as a row sustain pair, and in which said second means comprises two row sustain sources a first of which is connected to energise alternate row sustain pairs and a second of which is connected to energise the remaining row sustain pairs.
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9. A plasma display panel as claimed in Claim 8, in which the sustain conductors of each row sustain pair are connected together at both ends.
- 30
10. A plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining
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- address locations at which plasma discharges are selectively effected by selective energisation of the address conductors, characterized in that:
- each address conductor of each set has a sustain conductor on each side thereof offset from the address conductor and parallel thereto, such that adjacent to each address location there are four sustain conductor intersections defining pixel discharge positions to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors;
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- said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of each of the address conductors intersecting at a selected address location at which a plasma discharge has been effected for selecting one of the four pixel discharge positions associated with that address location for a sustained pixel display discharge at the selected one pixel position; and
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- in which the address conductors of one set are arranged to have the address conductors connected in groups such that an address operation simultaneously selects a plurality of address locations in a group, and in which said second means includes a plurality of sustain sources for the sustain conductors associated with the address conductors of said one set, the sustain sources being so arranged that the two sustain conductors located on each side of each address conductor of said one set are connected to different sustain sources to differentially energise the two sustain conductors, and the sustain conductors associated with the address conductors of a group are connected to different sustain sources to enable pixel discharge position selection with respect to the simultaneously addressed address locations.
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11. A plasma display panel as claimed in Claim 10 in which the address conductors and sustain conductors of both sets are supported at a single one of said dielectric walls.
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12. A plasma display panel as claimed in Claim 10 or 11, in which the two sustain conductors disposed between, and associated with respective ones of, each pair of next adjacent column address conductors are connected together as a column sustain pair.
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13. A plasma display panel as claimed in Claim 12 in which the column sustain conductors of each pair are connected together at both ends.
14. A plasma display panel as claimed in any one of Claims 10 to 13, in which the two sustain conductors disposed between, and associated with respective ones of, each pair of next adjacent row address conductors are connected together as a row sustain pair. 5
15. A plasma display panel as claimed in Claim 13 in which the row sustain conductors of each pair are connected together at both ends. 10
16. A plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining address locations at which plasma discharges are selectively effected by selective energisation of the address conductors, characterized in that: 15
- each address conductor of one set has a sustain conductor on each side thereof, offset from the address conductor and parallel thereto, such that adjacent to each address location along the address conductor there are two conductor intersections defining pixel discharge points which are on opposite sides of the address conductor, between which a pixel display position is defined and to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors; and 20
- said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors, said second means being arranged to differentially energise the sustain conductors on opposite sides of an address conductor of said one set at a selected address location along which a plasma discharge has been effected so as to establish a sustained pixel display discharge between the two pixel discharge points associated with that address location. 25
17. A plasma display panel as claimed in Claim 16, in which the two sustain conductors disposed between, and associated with respective ones of, each pair of next adjacent address conductors of said one set are connected together as a sustain pair, and in which said second means comprises two sustain sources a first of which is connected to energise alternate sustain pairs and a second of which is connected to the remaining sustain pairs. 30
18. A plasma display panel as claimed in Claim 17, in which the sustain conductors of each sustain pair are connected together at both ends. 35
19. A plasma display panel of the kind comprising a space bounded by opposed dielectric walls and containing an ionizable gas, address and sustain conductors separated from the gas by dielectric material and disposed in an array to define an array of pixel discharge positions at which plasma discharges are selectively effected in response to the selective energisation of the address and sustain conductors, and means to selectively energise the address and sustain conductors, wherein the address conductors are in a matrix array comprising a set of column and a set of row conductors defining address locations at which plasma discharges are selectively effected by selective energisation of the address conductors, characterized in that: 40
- each address conductor of one set has two sustain conductors on each side thereof, offset from the address conductor and parallel thereto, such that adjacent to each address location there are four conductor intersections defining two pairs of pixel discharge points which are on opposite sides of the address conductor and between each pair of which points a pixel display position is defined, and to which wall charges are transferable from the plasma generated at the associated address location by selective energisation of the address and sustain conductors; 45
- said means to energise the address and sustain conductors comprises: first means for energising the address conductors, and second means for energising the sustain conductors comprising first and second sustain sources to which alternate ones of said sustain conductors are connected and which differentially energise the sustain conductors on opposite sides of an address conductor along which an address location discharge has been effected by said first means in order to select one of the two pixel discharge positions asso- 50
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ciated with that address location for a sustained pixel display discharge.

- 20.** A plasma display panel as claimed in any one of Claims 16 to 19 in which means are provided between the address conductors of the other set to prevent the spread of plasma from plasma discharge points associated with one address location in the direction of the address conductors of said one set.

## **Patentansprüche**

1. Plasmaanzeigetafel der Art, die einen Raum umfasst, der von gegenüberliegenden dielektrischen Wänden begrenzt wird und ein ionisierbares Gas enthält, Adressier- und Erhaltungsleiter, die von dem Gas durch dielektrisches Material getrennt sind, und in einem Feld angeordnet sind, um ein Feld von Bildelemententladungsstellungen zu definieren, bei denen Plasmaentladungen selektiv in Reaktion auf die selektive Erregung der Adressier- und Erhaltungsleiter bewirkt wird, und ein Mittel, um die Adressier- und Erhaltungsleiter selektiv zu erregen, worin die Adressierleiter in einem Matrixfeld liegen, das einen Satz von Spalten- und einen Satz von Zeilenleitern umfasst, die Adressierstellen definieren, an denen Plasmaentladungen selektiv durch selektive Erregung der Adressierleiter bewirkt werden, dadurch gekennzeichnet, dass:  
jeder Adressierleiter von jedem Satz einen Erhaltungsleiter auf jeder Seite hat, der von dem Adressierleiter versetzt und parallel dazu angeordnet ist, so dass neben jeder Adressierstelle vier Erhaltungsleiterschnittpunkte liegen, die Bildelemententladungsstellungen definieren, auf welche Wandladungen von dem Plasma übertragen werden können, das an der zugeordneten Adressierstelle durch selektive Erregung der Adressier- und Erhaltungsleiter erzeugt wird;  
wobei das Mittel zum Erregen der Adressier- und Erhaltungsleiter folgendes umfasst: ein erstes Mittel zum Erregen der Adressierleiter, und ein zweites Mittel zum Erregen der Erhaltungsleiter, wobei das zweite Mittel angeordnet ist, um die Erhaltungsleiter differentiell auf gegenüberliegenden Seiten jeder der Adressierleiter zu erregen, die sich bei einer selektiven Adressierstelle schneiden, an der eine Plasmaentladung bewirkt worden ist, um eine der vier Bildelemententladungsstellungen auszuwählen, die der Adressierstelle zugeordnet sind, für eine erhaltende Bildelementanzeigeentladung an der einen ausgewählten Bildelementstellung, und

wobei das erste Erregungsmittel ein Gasentladungsverschiebungsregister einschliesst, um die Auswahl der Adressierleiter eines Satzes zu kontrollieren.

2. Plasmaanzeigetafel nach Anspruch 1, in der die Spaltenadressierleiter und ihre zugeordneten Erhaltungsleiter von einer der dielektrischen Wände unterstützt werden, und die Zeilenadressierleiter und ihre zugeordneten Erhaltungsleiter von der anderen der dielektrischen Wände unterstützt werden.

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3. Plasmaanzeigetafel nach Anspruch 1, in der die Adressierleiter und die Erhaltungsleiter alle von einer einzelnen der dielektrischen Wände unterstützt sind.

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4. Plasmaanzeigetafel der Art, die einen Raum umfasst, der von gegenüberliegenden dielektrischen Wänden begrenzt wird und ein ionisierbares Gas enthält, Adressier- und Erhaltungsleiter, die von dem Gas durch dielektrisches Material getrennt sind, und in einem Feld angeordnet sind, um ein Feld von Bildelemententladungsstellungen zu definieren, bei denen Plasmaentladungen selektiv in Reaktion auf die selektive Erregung der Adressier- und Erhaltungsleiter bewirkt wird, und ein Mittel, um die Adressier- und Erhaltungsleiter selektiv zu erregen, worin die Adressierleiter in einem Matrixfeld liegen, das einen Satz von Spalten- und einen Satz von Zeilenleitern umfasst, die Adressierstellen definieren, an denen Plasmaentladungen selektiv durch selektive Erregung der Adressierleiter bewirkt werden, dadurch gekennzeichnet, dass:

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jeder Adressierleiter von jedem Satz einen Erhaltungsleiter auf jeder Seite hat, der von dem Adressierleiter versetzt und parallel dazu angeordnet ist, so dass neben jeder Adressierstelle vier Erhaltungsleiterschnittpunkte liegen, die Bildelemententladungspunkte definieren, auf welche Wandladungen von dem Plasma übertragen werden können, das an der zugeordneten Adressierstelle durch selektive Erregung der Adressier- und Erhaltungsleiter erzeugt wird;

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wobei das Mittel zum Erregen der Adressier- und Erhaltungsleiter folgendes umfasst: ein erstes Mittel zum Erregen der Adressierleiter, und ein zweites Mittel zum Erregen der Erhaltungsleiter, wobei das zweite Mittel angeordnet ist, um die Erhaltungsleiter differentiell auf gegenüberliegenden Seiten jeder der Adressierleiter zu erregen, die sich bei einer selektiven Adressierstelle schneiden, an der eine Plasmaentladung bewirkt worden ist, um eine der vier

- Bildelemententladungsstellungen auszuwählen, die der Adressierstelle zugeordnet sind, für eine erhaltende Bildelementanzeigeentladung an der einen ausgewählten Bildelementstellung, und  
 5 die Adressierleiter und Erhaltungsleiter von beiden Sätzen von einer einzelnen der dielektrischen Wände unterstützt werden.
5. Plasmaanzeigetafel nach einem der Ansprüche 1 bis 4, in der die ersten und zweiten Mittel kontrollierbar in Reaktion auf Videoinformation betrieben werden können, die angezeigt werden soll, um die Adressier- und Erhaltungsleiter, die einer Adressierstelle zugeordnet sind, differentiell zu erregen, an der eine Entladung bewirkt wurde, wobei die vier Bildelementstellungen selektiv für erhaltende Bildelementanzeigeentladung dort aktiviert werden können.  
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6. Plasmaanzeigetafel nach einem der Ansprüche 1 bis 5, in der die beiden Erhaltungsleiter, die zwischen jedem Paar von nächsten benachbarten Spaltenadressierleitern angeordnet sind, und entsprechenden davon zugeordnet sind, als ein Spaltenerhaltungspaar aneinander angeschlossen sind, und in der das zweite Mittel zwei spaltenerhaltungsquellen umfasst, von denen die erste angeschlossen ist, um abwechselnde Spaltenerhaltungspaare zu erregen, und die zweite angeschlossen ist, um die verbleibenden Spaltenerhaltungspaare zu erregen.  
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7. Plasmaanzeigetafel nach Anspruch 6, in der die Erhaltungsleiter von jedem Spaltenerhaltungspaar an beiden Enden miteinander verbunden sind.  
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8. Plasmaanzeigetafel nach einem der Ansprüche 1 bis 7, in der die beiden Erhaltungsleiter, die zwischen jedem Paar von nächsten benachbarten Zeilenadressierleitern angeordnet sind, und entsprechenden davon zugeordnet sind, als ein Zeilenerhaltungspaar aneinander angeschlossen sind, und in der das zweite Mittel zwei Zeilenerhaltungsquellen umfasst, von denen die erste angeschlossen ist, um abwechselnde Zeilenerhaltungspaare zu erregen, und die zweite angeschlossen ist, um die verbleibenden Zeilenerhaltungspaare zu erregen.  
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9. Plasmaanzeigetafel nach Anspruch 8, in der die Erhaltungsleiter von jedem Zeilenerhaltungspaar an beiden Enden miteinander verbunden sind.  
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10. Plasmaanzeigetafel der Art, die einen Raum umfasst, der von gegenüberliegenden dielektri-  
 schen Wänden begrenzt wird und ein ionisierbares Gas enthält, Adressier- und Erhaltungsleiter, die von dem Gas durch dielektrisches Material getrennt sind, und in einem Feld angeordnet sind, um ein Feld von Bildelemententladungsstellungen zu definieren, bei denen Plasmaentladungen selektiv in Reaktion auf die selektive Erregung der Adressier- und Erhaltungsleiter bewirkt wird, und ein Mittel, um die Adressier- und Erhaltungsleiter selektiv zu erregen, worin die Adressierleiter in einem Matrixfeld liegen, das einen Satz von Spalten- und einen Satz von Zeilenleitern umfasst, die Adressierstellen definieren, an denen Plasmaentladungen selektiv durch selektive Erregung der Adressierleiter bewirkt werden, dadurch gekennzeichnet, dass: jeder Adressierleiter von einem Satz einen Erhaltungsleiter auf jeder Seite hat, der von dem Adressierleiter versetzt und parallel dazu angeordnet ist, so dass neben jeder Adressierstelle vier Erhaltungsleiterschnittpunkte liegen, die Bildelemententladungsstellungen definieren, auf welche Wandladungen von dem Plasma übertragen werden können, das an der zugehörigen Adressierstelle durch selektive Erregung der Adressier- und Erhaltungsleiter erzeugt wird;  
 35 wobei das Mittel zum Erregen der Adressier- und Erhaltungsleiter folgendes umfasst: ein erstes Mittel zum Erregen der Adressierleiter, und ein zweites Mittel zum Erregen der Erhaltungsleiter, wobei das zweite Mittel angeordnet ist, die Erhaltungsleiter differentiell auf gegenüberliegenden Seiten jeder der Adressierleiter zu erregen, die sich bei einer selektiven Adressierstelle schneiden, an der eine Plasmaentladung bewirkt worden ist, um eine der vier Bildelemententladungsstellungen auszuwählen, die der Adressierstelle zugeordnet sind, für eine erhaltende Bildelementanzeigeentladung an der einen ausgewählten Bildelementstellung; und  
 40 in der die Adressierleiter eines Satzes angeordnet sind, die Adressierleiter in Gruppen angeschlossen zu haben, so dass ein Adressierbetrieb gleichzeitig eine Vielzahl von Adressierstellen in einer Gruppe auswählt, und in der das zweite Mittel eine Vielzahl von Erhaltungsquellen für die Erhaltungsleiter enthält, die den Adressierleitern des einen Satzes zugeordnet sind, wobei die Erhaltungsquellen so angeordnet sind, dass die beiden Erhaltungsleiter, die auf jeder Seite von jedem Adressierleiter von dem einen Satz angeordnet sind, an verschiedene Erhaltungsquellen angeschlossen sind, um die beiden Erhaltungsleiter differentiell zu erregen, und die den Adressierleitern einer Gruppe zugeordneten Erhaltungsleiter an  
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- verschiedene Erhaltungsquellen angeschlossen werden, um Bildelemententladungsstellungs- auswahl bezüglich der gleichzeitig adressierten Adressierstellen zu befähigen.
11. Plasmaanzeigetafel nach Anspruch 10, in der die Adressierleiter und die Erhaltungsleiter von beiden Sätzen von einer einzelnen der dielektrischen Wände unterstützt werden.
12. Plasmaanzeigetafel nach Anspruch 10 oder 11, in der die beiden Erhaltungsleiter, die zwischen jedem Paar von nächsten benachbarten Spaltenadressierleitern miteinander als ein Spaltenerhaltungspaar verbunden sind.
13. Plasmaanzeigetafel nach Anspruch 12, in der die Spaltenerhaltungsleiter von jedem Paar an beiden Enden miteinander verbunden sind.
14. Plasmaanzeigetafel nach einem der Ansprüche 10 bis 13, in der die beiden Erhaltungsleiter, die zwischen jedem Paar von nächsten benachbarten Zeilenadressierleitern angeordnet sind, und entsprechenden davon zugeordnet sind, miteinander als ein Zeilenerhaltungspaar verbunden sind.
15. Plasmaanzeigetafel nach Anspruch 13, in der die Zeilenerhaltungsleiter von jedem Paar an beiden Enden miteinander verbunden sind.
16. Plasmaanzeigetafel der Art, die einen Raum umfasst, der von gegenüberliegenden dielektrischen Wänden begrenzt wird und ein ionisierbares Gas enthält, Adressier- und Erhaltungsleiter, die von dem Gas durch dielektrisches Material getrennt sind, und in einem Feld angeordnet sind, um ein Feld von Bildelemententladungsstellungen zu definieren, bei denen Plasmaentladungen selektiv in Reaktion auf die selektive Erregung der Adressier- und Erhaltungsleiter bewirkt wird, und ein Mittel, um die Adressier- und Erhaltungsleiter selektiv zu erregen, worin die Adressierleiter in einem Matrixfeld liegen, das einen Satz von Spalten- und einen Satz von Zeilenleitern umfasst, die Adressierstellen definieren, an denen Plasmaentladungen selektiv durch selektive Erregung der Adressierleiter bewirkt werden, dadurch gekennzeichnet, dass:  
jeder Adressierleiter von jedem Satz einen Erhaltungsleiter auf jeder Seite hat, der von dem Adressierleiter versetzt und parallel dazu angeordnet ist, so dass neben jeder Adressierstelle entlang der Adressierleiter zwei Leiterschnittpunkte liegen, die Bildelemententladungspunkte definieren, die auf gegenüberliegenden Sei-
- ten des Adressierleiters liegen, zwischen denen eine Bildelementanzeigestellung definiert ist, und auf die Wandladungen von dem Plasma übertragen werden können, das an der zugeordneten Adressierstelle durch selektive Erregung der Adressier- und Erhaltungsleiter erzeugt wird; und wobei das Mittel zum Erregen der Adressier- und Erhaltungsleiter folgendes umfasst: ein erstes Mittel zum Erregen der Adressierleiter, und ein zweites Mittel zum Erregen der Erhaltungsleiter, wobei das zweite Mittel angeordnet ist, die Erhaltungsleiter differentiell auf gegenüberliegenden Seiten eines Adressierleiters von einem Satz von einer ausgewählten Adressierstelle zu erregen, entlang welcher eine Plasmaentladung bewirkt worden ist, um eine erhaltende Bildelementanzeigeentladung zwischen den beiden Bildelemententladungspunkten, die der Adressierstelle zugeordnet sind, festzusetzen.
17. Plasmaanzeigetafel nach Anspruch 16, in der die beiden Erhaltungsleiter, die zwischen jedem Paar von nächsten benachbarten Adressierleitern angeordnet sind, und entsprechenden davon zugeordnet sind, wobei jedes Paar von nächsten benachbarten Adressierleitern des einen Satzes als ein Erhaltungspaar aneinander angeschlossen sind, und in der das zweite Mittel zwei Erhaltungsquellen umfasst, von denen die erste angeschlossen ist, um abwechselnde Erhaltungspaare zu erregen, und die zweite angeschlossen ist, um die verbleibenden Erhaltungspaare zu erregen.
18. Plasmaanzeigetafel nach Anspruch 17, in der die Erhaltungsleiter von jedem Erhaltungspaar an beiden Enden miteinander verbunden sind.
19. Plasmaanzeigetafel der Art, die einen Raum umfasst, der von gegenüberliegenden dielektrischen Wänden begrenzt wird und ein ionisierbares Gas enthält, Adressier- und Erhaltungsleiter, die von dem Gas durch dielektrisches Material getrennt sind, und in einem Feld angeordnet sind, um ein Feld von Bildelemententladungsstellungen zu definieren, bei denen Plasmaentladungen selektiv in Reaktion auf die selektive Erregung der Adressier- und Erhaltungsleiter bewirkt wird, und ein Mittel, um die Adressier- und Erhaltungsleiter selektiv zu erregen, worin die Adressierleiter in einem Matrixfeld liegen, das einen Satz von Spalten- und einen Satz von Zeilenleitern umfasst, die Adressierstellen definieren, an denen Plasmaentladungen selektiv durch selektive Erregung der Adressierleiter bewirkt werden, dadurch

gekennzeichnet, dass:

jeder Adressierleiter eines Satzes zwei Erhaltungsleiter auf jeder Seite hat, die von dem Adressierleiter versetzt und parallel dazu angeordnet sind, so dass neben jeder Adressierstelle vier Leiterschnittpunkte liegen, die zwei Paar Bildelemententladungspunkte definieren, die auf gegenüberliegenden Seiten der Adressierleiter liegen, und zwischen jedem Paar der Punkte eine Bildelementanzeigestellung definiert ist, und auf welche Wandladungen von dem Plasma übertragen werden können, das an der zugehörigen Adressierstelle durch selektive Erregung der Adressier- und Erhaltungsleiter erzeugt wird;

wobei das Mittel zum Erregen der Adressier- und Erhaltungsleiter folgendes umfasst: ein erstes Mittel zum Erregen der Adressierleiter, und ein zweites Mittel zum Erregen der Erhaltungsleiter, das erste und zweite Erhaltungsquellen umfasst, an die abwechselnde Erhaltungsleiter angeschlossen sind, und die die Erhaltungsleiter differentiell auf gegenüberliegenden Seiten eines Adressierleiters erregen, entlang welcher eine Adressierstellenentladung mit Hilfe des ersten Mittels bewirkt worden ist, um eine der beiden Bildelemententladungsstellungen auszuwählen, die der Adressierstelle für eine erhaltende Bildelementanzeigeentladung zugeordnet ist.

20. Plasmaanzeigetafel nach einem der Ansprüche 16 bis 19, in der ein Mittel zwischen den Adressierleitern des anderen Satzes vorgesehen ist, um zu verhindern, das sich Plasma von Plasmaentladungspunkten verbreitet, die einer Adressierstelle in der Richtung der Adressierleiter des einen Satzes zugeordnet sind.

## Revendications

1. Un panneau d'affichage à plasma du modèle comprenant un espace limité par des parois diélectriques opposées et contenant un gaz ionisable, des conducteurs d'adresses et des conducteurs permanents séparés du gaz par un matériau diélectrique et disposés en réseau pour définir une matrice de positions de décharge de pixel auxquelles sont sélectivement envoyées des décharges de plasma en réponse à l'excitation sélective des conducteurs d'adresses permanents, et le moyen d'exciter sélectivement les conducteurs permanents d'adresses, dans lequel les conducteurs d'adresses sont disposés en un réseau matriciel constitué d'un ensemble de conducteurs en colonnes et d'un ensemble de

conducteurs en rangées définissant des emplacements d'adresses auxquels les décharges de plasma sont sélectivement envoyées par une excitation sélective des conducteurs d'adresses, caractérisé en ce que:

chaque conducteur d'adresses de chaque ensemble est entouré de chaque côté, tout en étant séparé, par un conducteur permanent qui lui est parallèle, de telle manière qu'à proximité de chaque emplacement d'adresse il y ait quatre intersections de conducteurs permanents, définissant les positions de décharge de pixel, auxquelles les charges de paroi sont transférables à partir du plasma généré à l'emplacement d'adresse associé par excitation sélective des conducteurs d'adresses et permanents;

ledit moyen d'excitation des conducteurs permanents et d'adresses comprend : un premier moyen pour exciter les conducteurs d'adresses, un second moyen pour exciter les conducteurs permanents, ledit second moyen étant organisé pour exciter de manière différentielle les conducteurs permanents situés de chaque côté de chacun des conducteurs d'adresses qui se croisent à un emplacement d'adresse choisi auquel une décharge de plasma est envoyée pour sélectionner l'une des quatre positions de décharge de pixel associée à cet emplacement d'adresse pour y maintenir la décharge d'affichage d'un pixel; et

ledit premier moyen d'excitation comprenant aussi un registre à décalage de décharge de gaz pour contrôler le choix des conducteurs d'adresses d'un des ensembles.

2. Un panneau d'affichage à plasma selon la revendication 1 dans lequel les conducteurs d'adresses en colonnes et leurs conducteurs permanents associés sont portés par l'une des parois diélectriques et les conducteurs d'adresses en rangées et leurs conducteurs permanents associés sont portés par l'autre paroi diélectrique.
3. Un panneau d'affichage à plasma selon la revendication 1 dans lequel les conducteurs d'adresses et les conducteurs permanents sont tous portés par une seule des parois diélectriques.
4. Un panneau d'affichage à plasma du modèle comprenant un espace limité par des parois diélectriques opposées et contenant un gaz ionisable, des conducteurs d'adresses et des conducteurs permanents séparés du gaz par un matériau diélectrique et disposés en réseau pour définir une matrice de positions

de décharge de pixel auxquelles sont sélectivement envoyées des décharges de plasma en réponse à une excitation sélective des conducteurs d'adresses permanents, et un moyen pour exciter sélectivement ces conducteurs permanents, dans lequel les conducteurs d'adresses sont disposés en un réseau matriciel constitué d'un ensemble de conducteurs en colonnes et d'un ensemble de conducteurs en rangées définissant des emplacements d'adresses auxquels les décharges de plasma sont sélectivement envoyées par une excitation sélective des conducteurs d'adresses, caractérisé en ce que:

chaque conducteur d'adresses de chaque ensemble est entouré de chaque côté, tout en en étant séparé, par un conducteur permanent qui lui est parallèle, de telle manière qu'à proximité de chaque emplacement d'adresse il y ait quatre intersections de conducteurs permanents, définissant les positions de décharge de pixel, auxquelles les charges de paroi sont transférables à partir du plasma généré à l'emplacement d'adresse associé par excitation sélective des conducteurs d'adresses permanents;

ledit moyen d'excitation des conducteurs permanents et d'adresses comprend : un premier moyen pour exciter les conducteurs d'adresses, un second moyen pour exciter les conducteurs permanents, ledit second moyen étant organisé pour exciter de manière différentielle les conducteurs permanents situés de chaque côté de chacun des conducteurs d'adresses qui se croisent à un emplacement d'adresse choisi auquel une décharge de plasma est envoyée pour sélectionner l'une des quatre positions de décharge de pixel associée à cet emplacement d'adresse pour y maintenir une décharge d'affichage d'un pixel; et

les conducteurs d'adresses et les conducteurs permanents des deux ensembles sont portés par une seule des parois diélectriques.

5. Un panneau d'affichage à plasma selon l'une quelconque des revendications 1 à 4, dans lequel le premier et second moyens sont mis en oeuvre de manière contrôlée, en réponse à l'information vidéo qui doit être affichée, pour exciter de manière différentielle les conducteurs d'adresses permanents associés à un emplacement d'adresse auquel une décharge a été envoyée, et par laquelle les quatre positions de pixel sont sélectivement activables pour envoyer à ce moment là une décharge d'affichage de pixel.

6. Un panneau d'affichage à plasma selon l'une quelconque des revendications 1 à 5, dans lequel les deux conducteurs permanents disposés entre et associés avec ceux respectifs de chaque paire la plus proche de conducteurs d'adresses en colonne, sont connectés ensemble comme paire permanente en colonne, et dans lequel le second moyen comprend deux sources permanentes en colonne dont une première est connectée pour exciter les paires permanentes en colonne alternées et dont une deuxième est connectée aux paires permanentes en colonne restantes.
- 15 7. Un panneau d'affichage à plasma selon la revendication 6, dans lequel les conducteurs permanents de chaque paire en colonne sont connectés ensemble aux deux extrémités.
- 20 8. Un panneau d'affichage à plasma selon l'une quelconque des revendications 1 à 7, dans lequel les deux conducteurs permanents disposés entre chaque paire, et associés respectivement avec la paire la plus proche de conducteurs d'adresses en rangée, sont connectés ensemble comme paire permanente en rangée, et dans lequel les seconds moyens comprennent deux sources permanentes en rangée dont une première est connectée pour exciter les paires permanentes alternées en rangée et dont une deuxième est connectée pour exciter les paires permanentes en rangée restantes.
- 25 30 35 9. Un panneau d'affichage à plasma selon la revendication 8, dans lequel les conducteurs permanents de chaque paire en rangée sont connectés ensemble aux deux extrémités.
- 40 45 50 55 10. Un panneau d'affichage à plasma du modèle comprenant un espace limité par des parois diélectriques opposées et contenant un gaz ionisable, des conducteurs d'adresses et des conducteurs permanents séparés du gaz par un matériau diélectrique et disposés en réseau pour définir une matrice de positions de décharge de pixel auxquelles sont sélectivement envoyées des décharges de plasma en réponse à une excitation des conducteurs d'adresses permanents, et un moyen pour exciter sélectivement les conducteurs d'adresses permanents, dans lequel les conducteurs d'adresses sont disposés en un réseau matriciel constitué d'un ensemble de conducteurs en colonnes et d'un ensemble de conducteurs en rangées définissant des emplacements d'adresses auxquels les décharges de plasma sont sélectivement réalisées par

une excitation sélective des conducteurs d'adresses, caractérisé en ce que:

chaque conducteur d'adresses de chaque ensemble est entouré de chaque côté, tout en étant séparé, par un conducteur permanent qui lui est parallèle, de telle manière qu'à proximité de chaque emplacement d'adresse il y ait quatre intersections de conducteurs permanents, définissant les positions de décharge de pixel, auxquelles les charges de paroi sont transférables à partir du plasma généré à l'emplacement d'adresse associé par excitation sélective des conducteurs d'adresses permanents;

ledit moyen d'excitation des conducteurs permanents et d'adresses comprend : un premier moyen pour exciter les conducteurs d'adresses, un second moyen pour exciter les conducteurs permanents, ledit second moyen étant organisé pour exciter de manière différentielle les conducteurs permanents situés de chaque côté de chacun des conducteurs d'adresses qui se croisent à un emplacement d'adresse choisi auquel une décharge de plasma est effectuée pour sélectionner l'une des quatre positions de décharge de pixel associée à cet emplacement d'adresse pour y maintenir une décharge d'affichage d'un pixel; et

dans lequel les conducteurs d'adresses d'un ensemble sont disposés de manière à ce que les conducteurs d'adresses soient connectés en groupes de telle sorte qu'une opération d'adresses sélectionne une pluralité d'emplacements d'adresses dans un groupe, et dans lequel le second moyen comprend une pluralité de sources permanentes pour les conducteurs permanents associés aux conducteurs d'adresses dudit ensemble, les sources permanentes étant disposées de telle manière que les deux conducteurs permanents situés de chaque côté de chaque conducteur d'adresses dudit ensemble soient connectés à différentes sources permanentes pour exciter différemment les deux conducteurs permanents, et que les conducteurs permanents associés aux conducteurs d'adresses d'un groupe soient connectés à différentes sources permanentes pour permettre la sélection de la position de décharge du pixel par rapport à l'adresses simultané des emplacements d'adresses.

**11.** Un panneau d'affichage à plasma selon la revendication 10, dans lequel les conducteurs d'adresses et les conducteurs permanents des deux ensembles sont portés par une seule des parois diélectriques.

**12.** Un panneau d'affichage à plasma selon les revendications 10 ou 11, dans lequel les deux conducteurs permanents disposés entre chaque paire, et associés respectivement avec la paire la plus proche, de conducteurs d'adresses en colonne, sont connectés ensemble comme paire permanente en colonne.

**13.** Un panneau d'affichage à plasma selon la revendication 12, dans lequel les conducteurs permanents en colonne de chaque paire sont connectés ensemble aux deux extrémités.

**14.** Un panneau d'affichage à plasma selon les revendications 10 à 13, dans lequel les deux conducteurs permanents disposés entre chaque paire, et associés respectivement avec la paire la plus proche, de conducteurs d'adresses en rangée, sont connectés ensemble comme paire permanente en rangée.

**15.** Un panneau d'affichage à plasma selon la revendication 13, dans lequel les conducteurs permanents en rangée de chaque paire sont connectés ensemble aux deux extrémités.

**16.** Un panneau d'affichage à plasma du modèle comprenant un espace limité par des parois diélectriques opposées et contenant un gaz ionisable, des conducteurs d'adresses et des conducteurs permanents séparés du gaz par un matériau diélectrique et disposés en réseau pour définir une matrice de positions de décharge de pixel auxquelles sont sélectivement envoyées des décharges de plasma en réponse à une excitation des conducteurs d'adresses permanents, et des moyens pour exciter sélectivement les conducteurs d'adresses permanents, dans lequel les conducteurs d'adresses sont disposés en un réseau matriciel constitué d'un ensemble de conducteurs en colonnes et d'un ensemble de conducteurs en rangées définissant des emplacements d'adresses auxquels les décharges de plasma sont sélectivement réalisées par une excitation sélective des conducteurs d'adresses, caractérisé en ce que:

chaque conducteur d'adresses d'un ensemble est entouré de chaque côté, tout en étant séparé, par un conducteur permanent qui lui est parallèle, de telle manière qu'à proximité de chaque emplacement d'adresse, le long du conducteur d'adresses, il y ait deux intersections de conducteurs, définissant les points de décharge de pixel, qui sont situés de manière opposée de chaque côté du conducteur d'adresses, entre lesquels est définie une position d'affichage de pixel et auxquels les



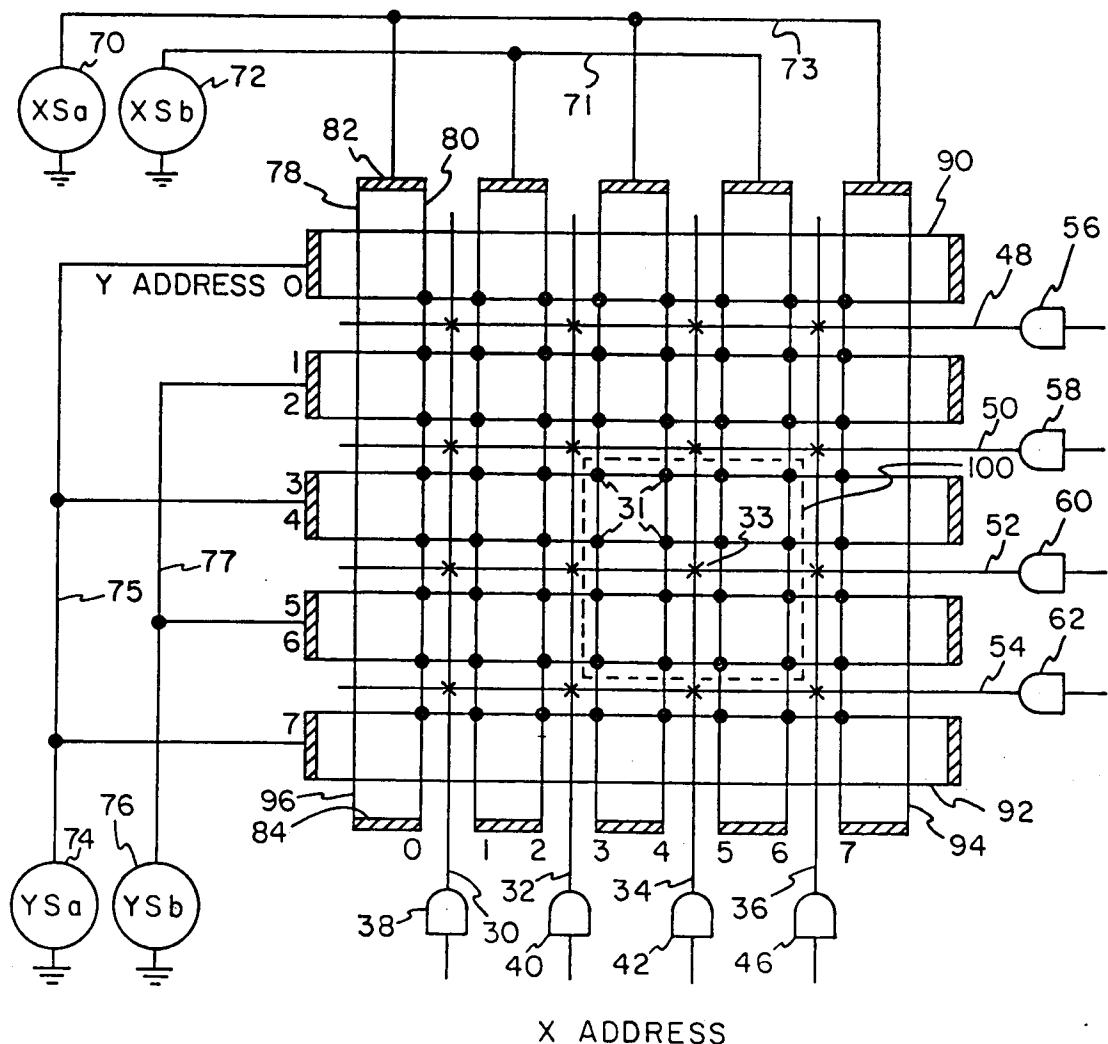
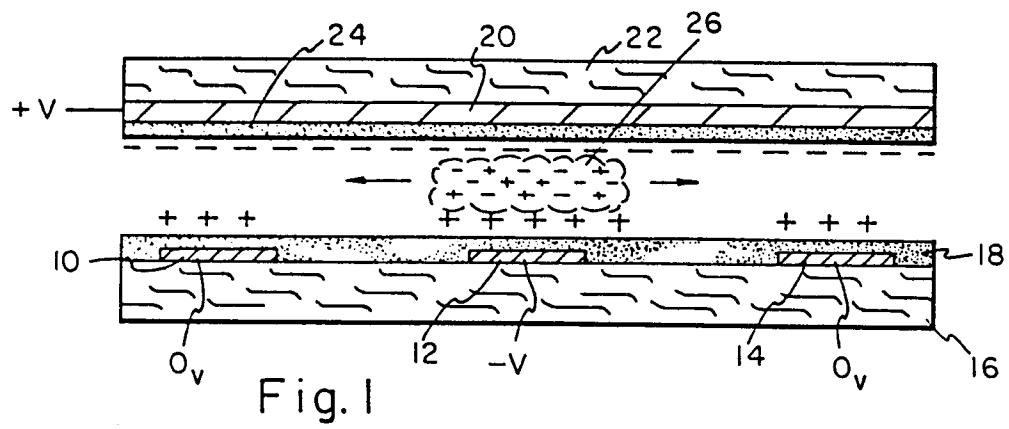


Fig. 2

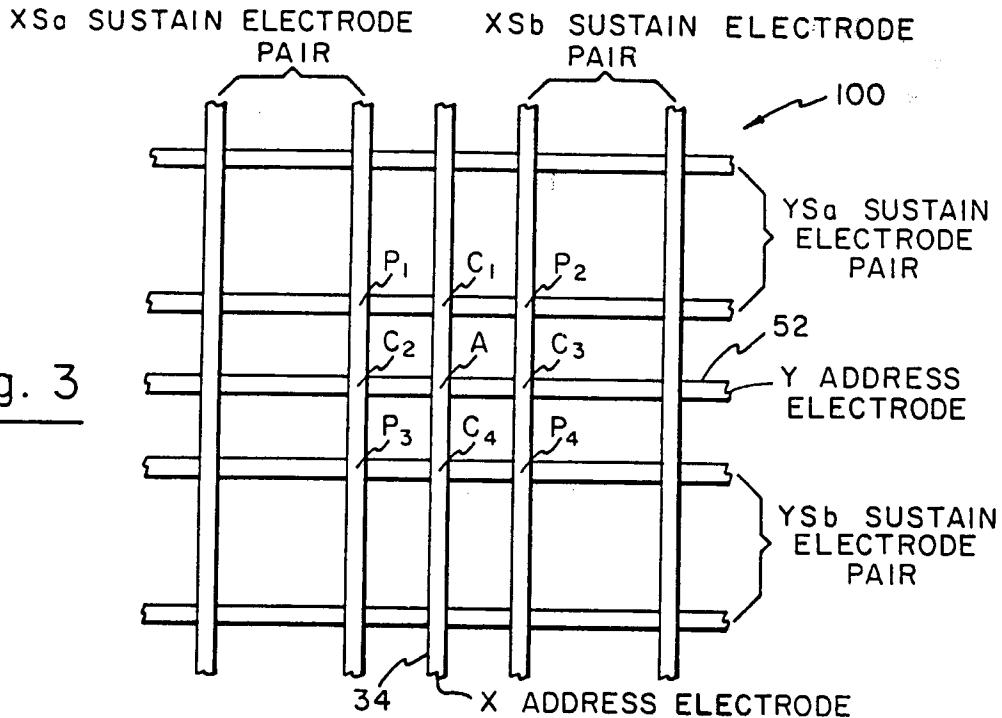


Fig. 3

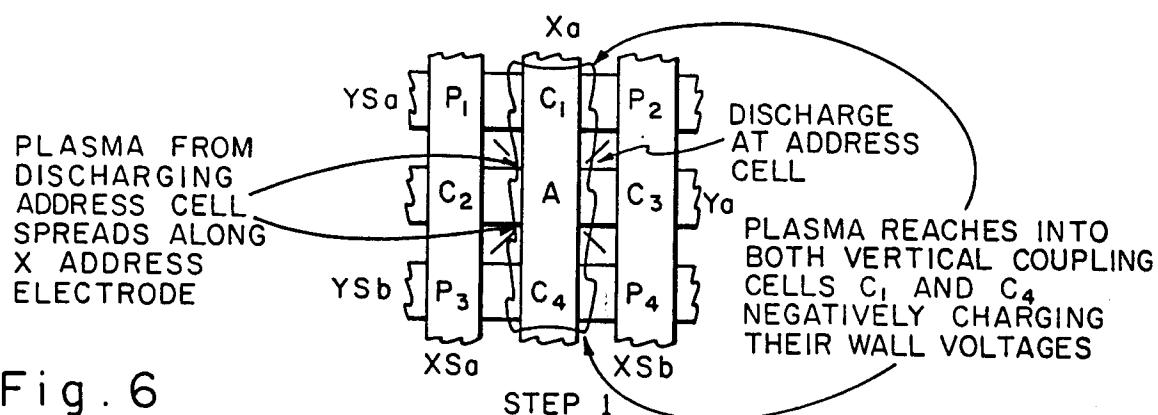
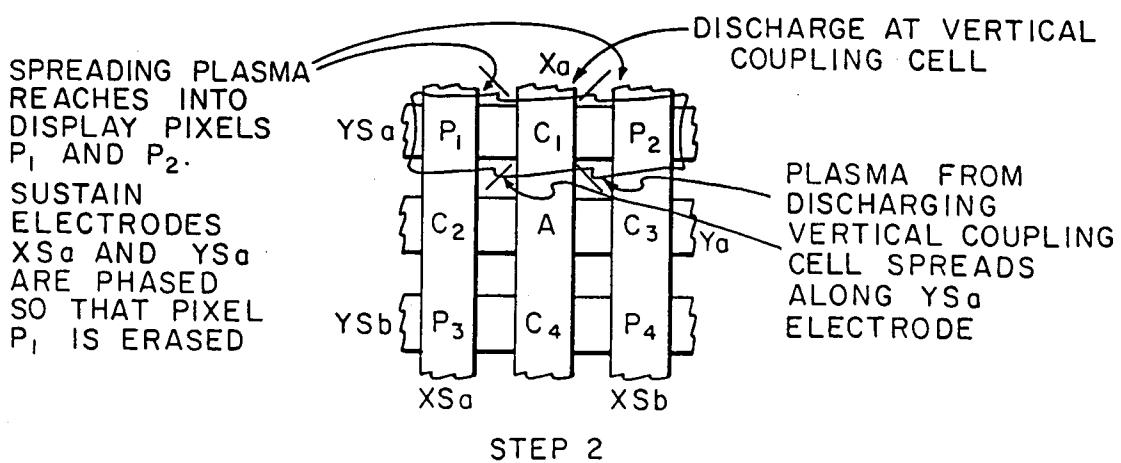


Fig. 6



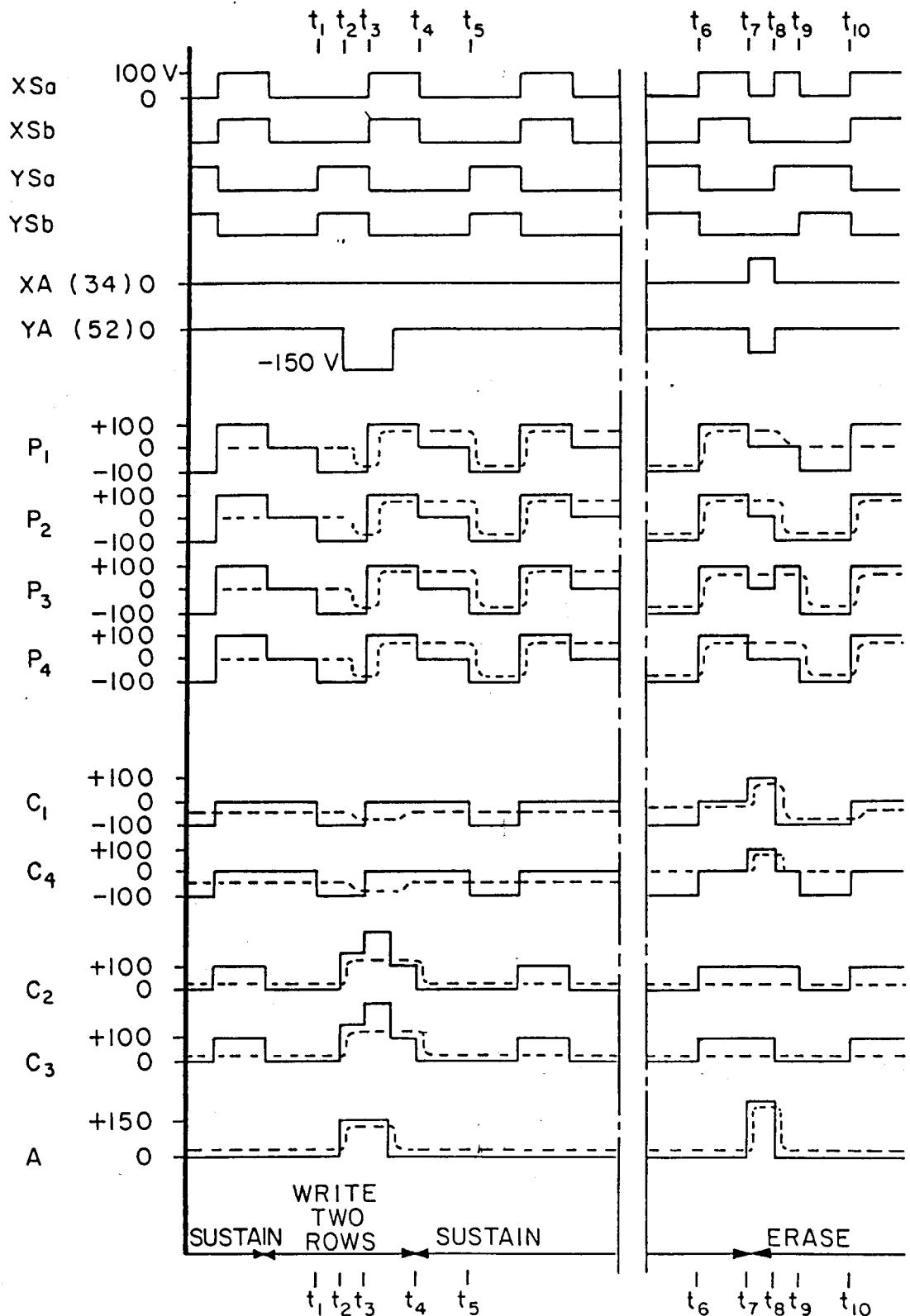
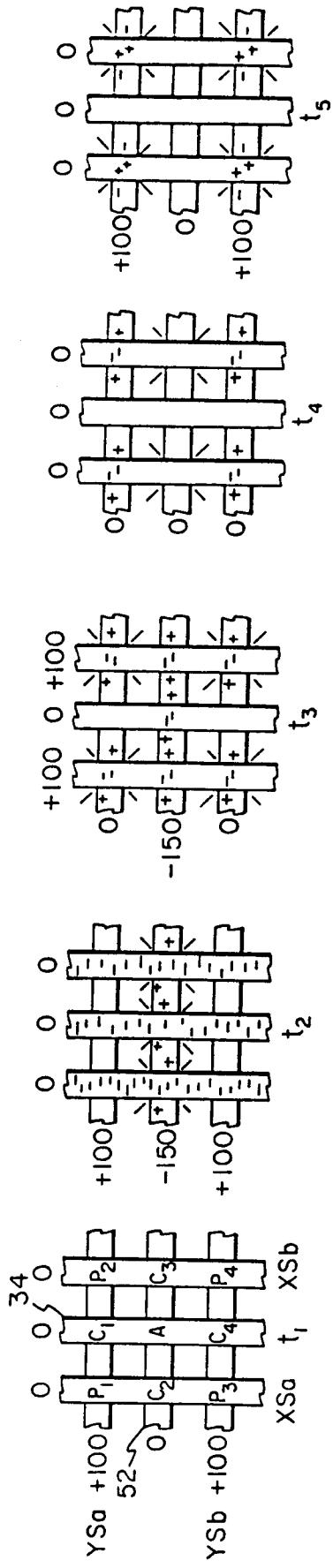


Fig. 4

" WRITE TWO ROWS "



SELECTIVE ERASE

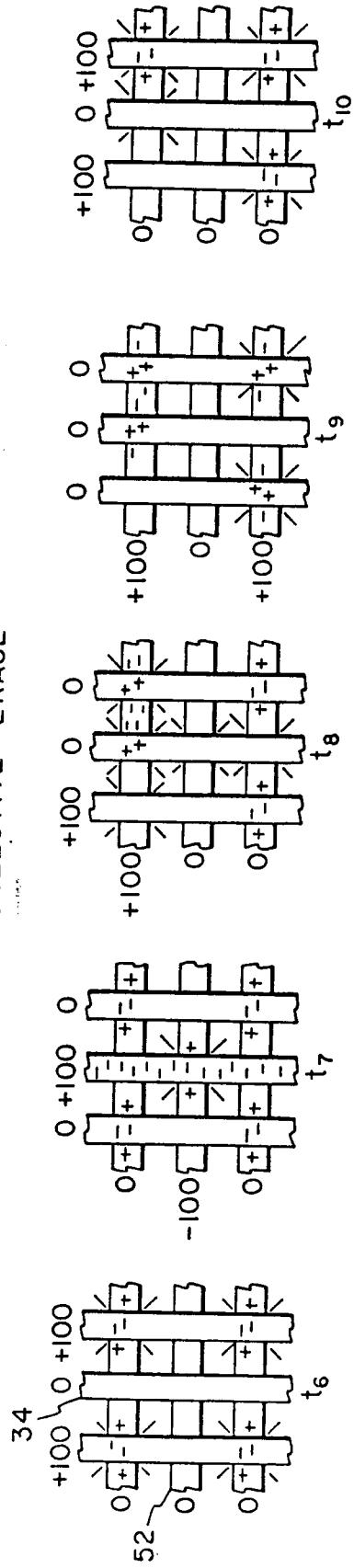


Fig. 5

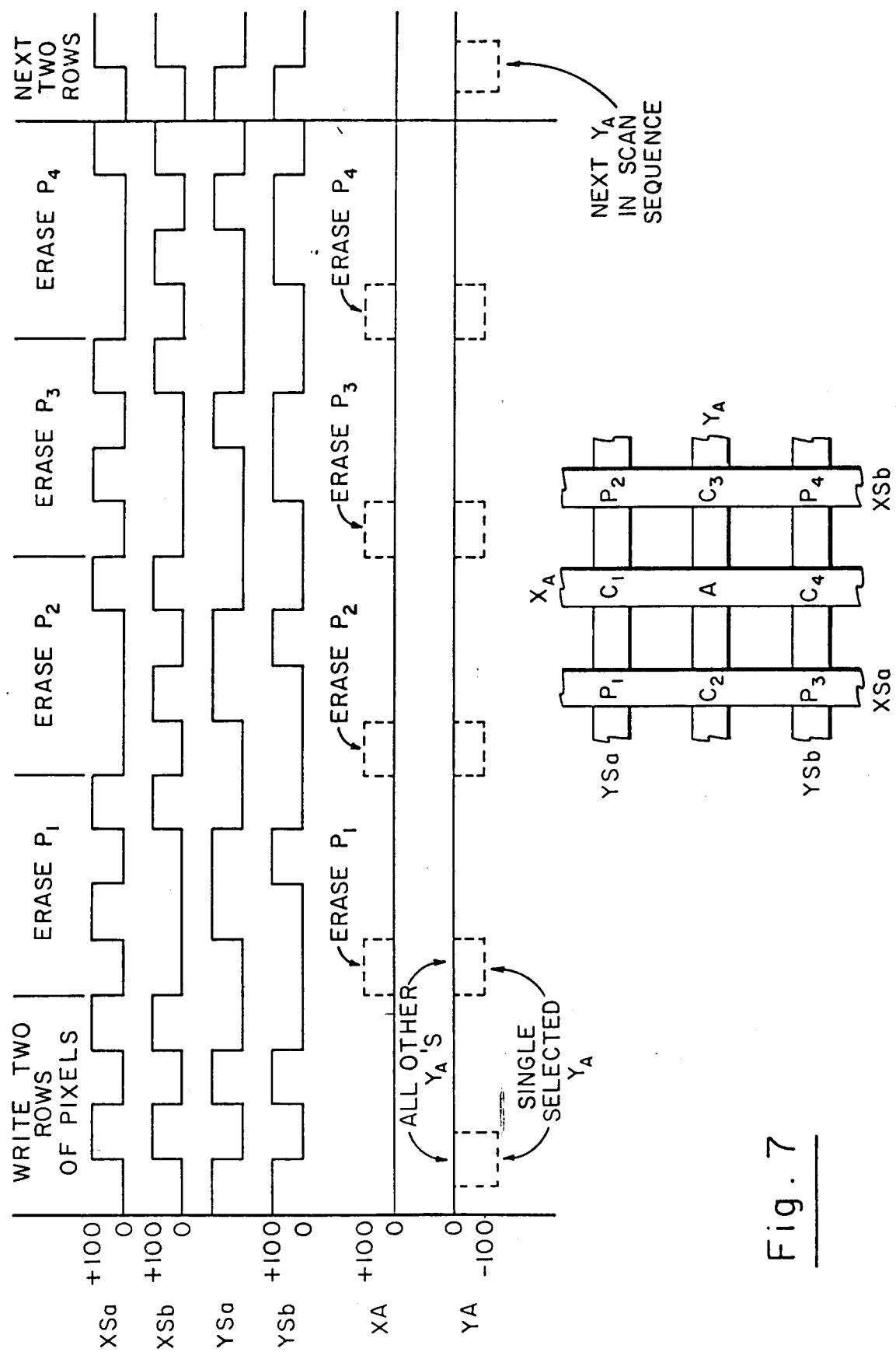
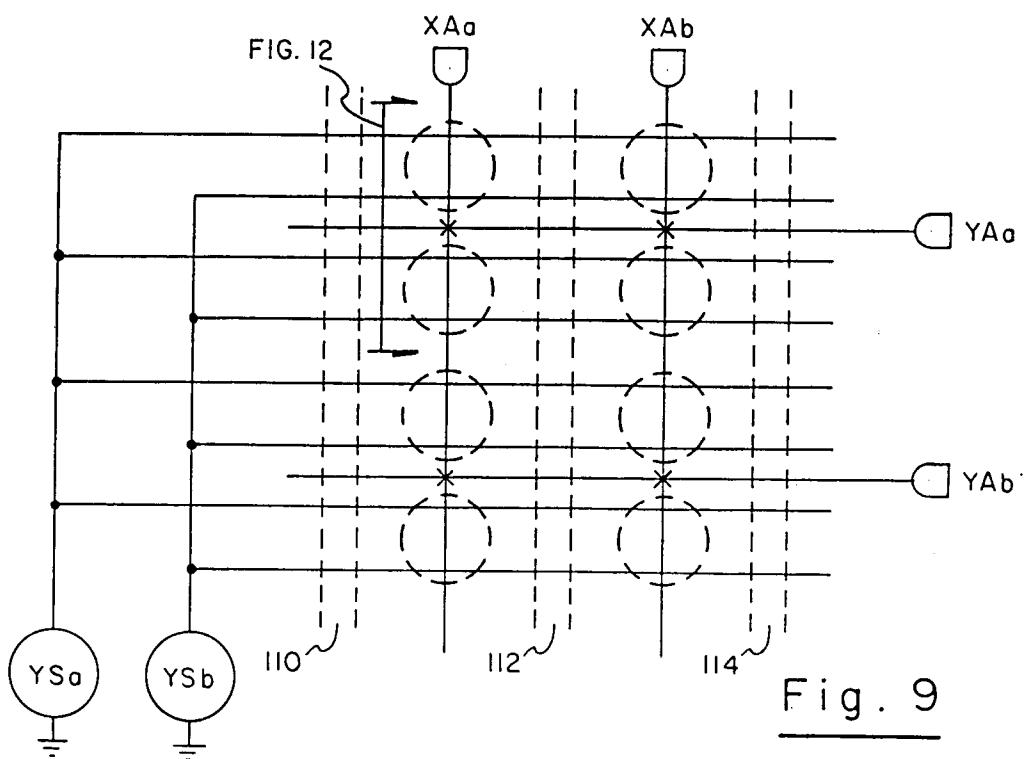
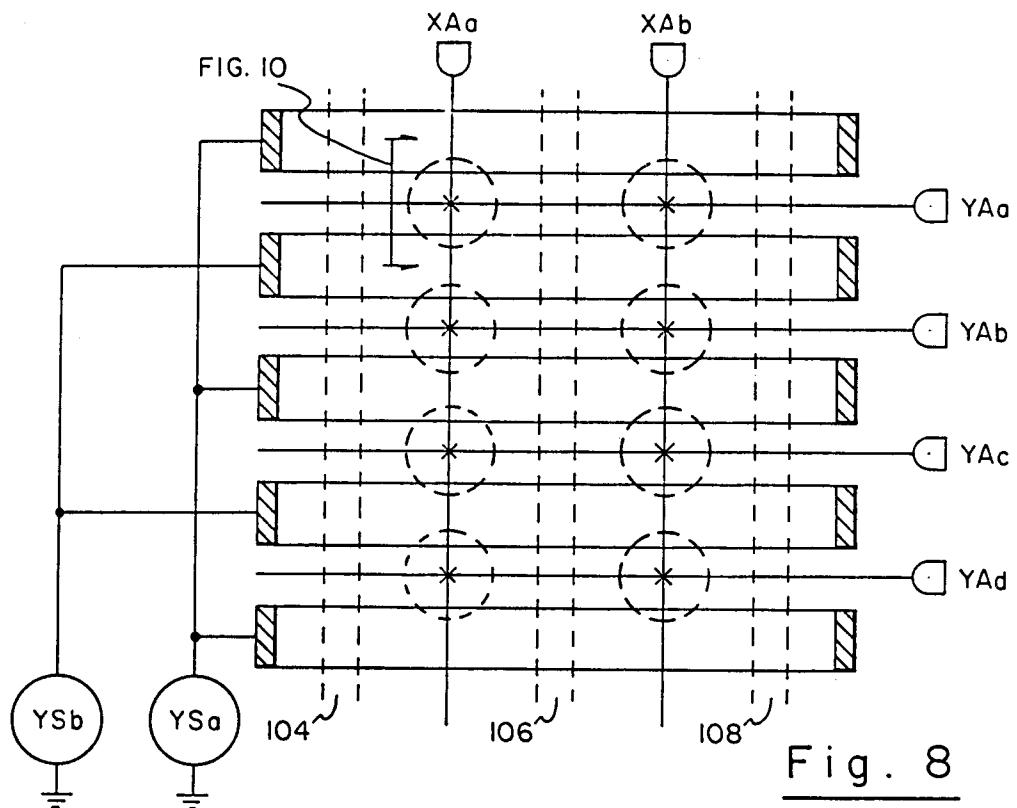


Fig. 7



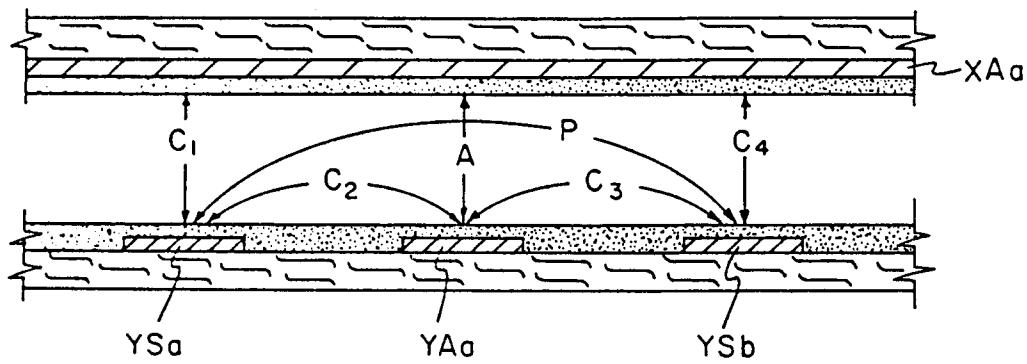


Fig. 10

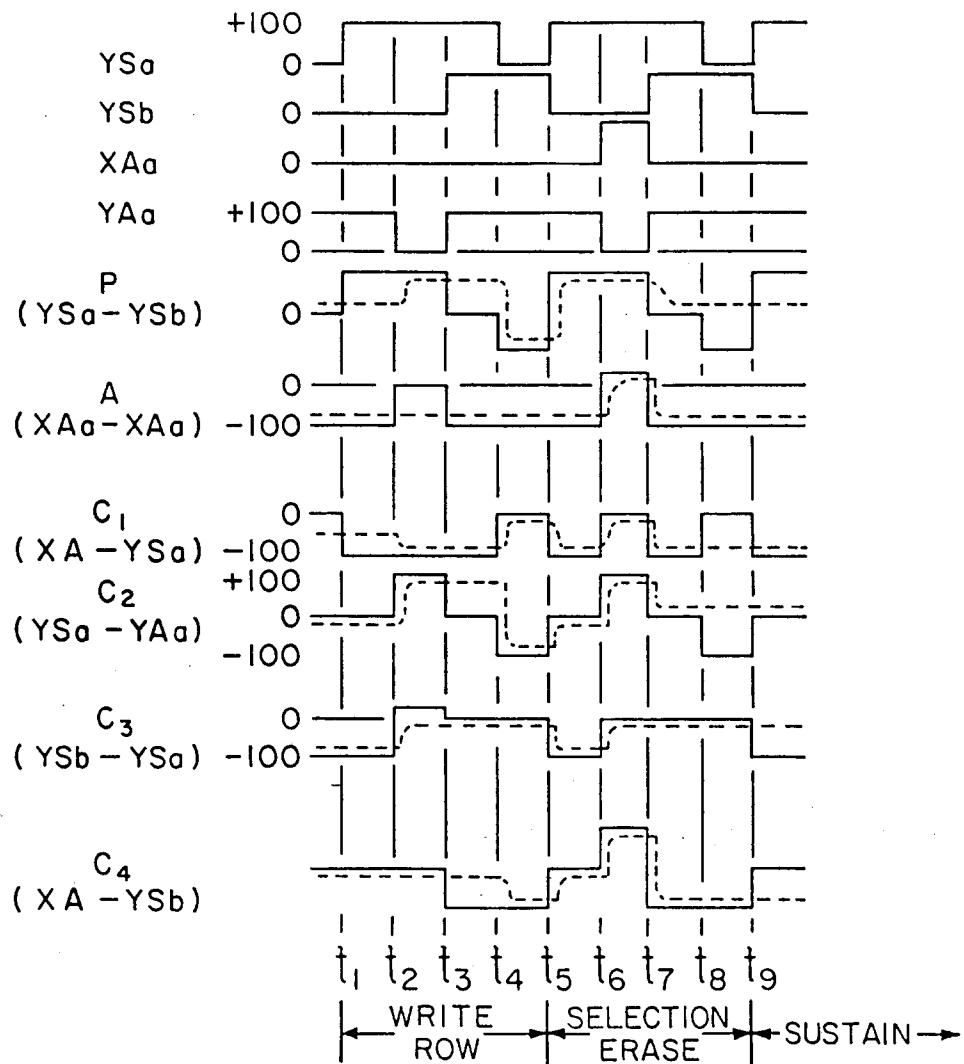


Fig. 11

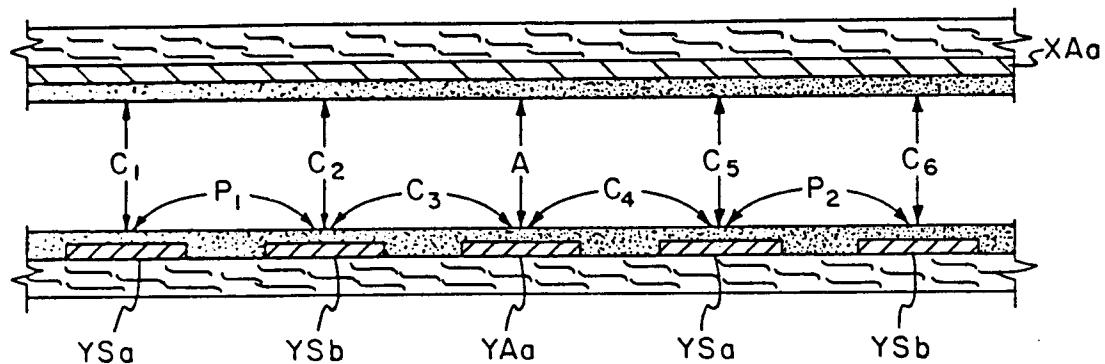


Fig. 12

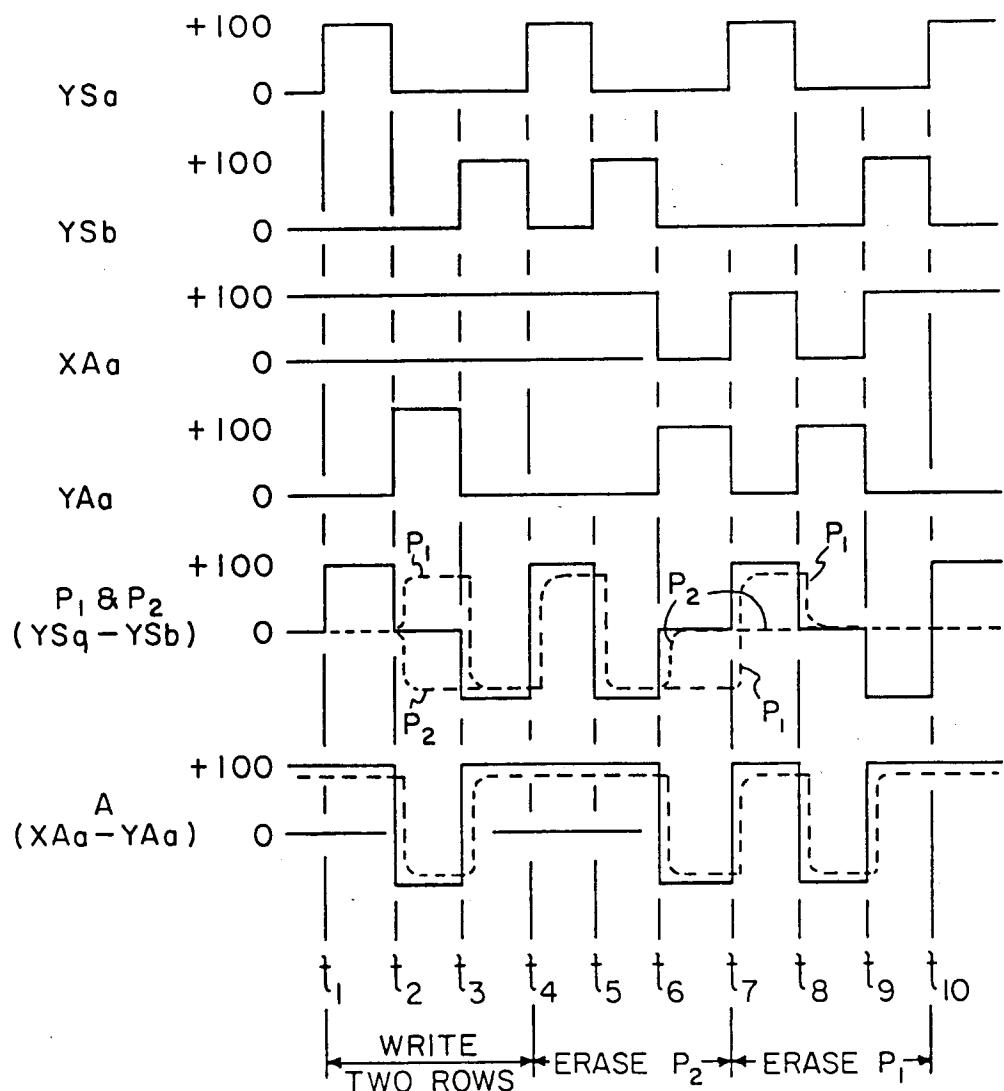


Fig. 13