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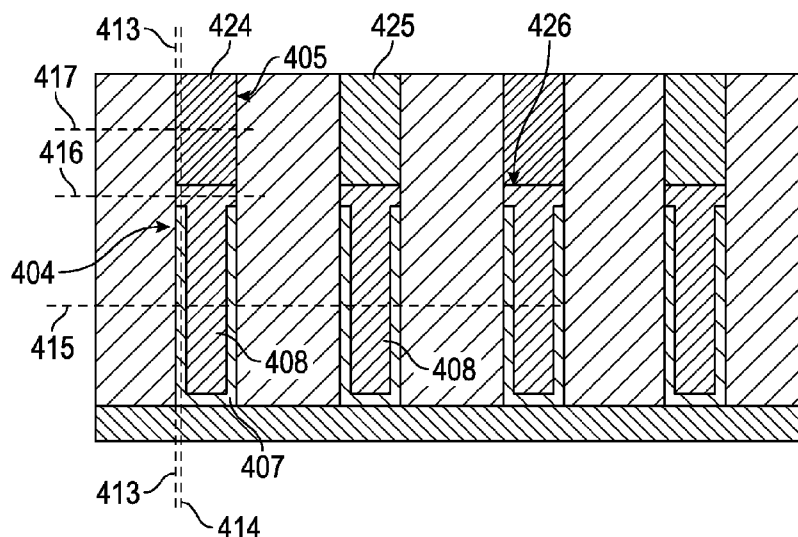


FIG. 3C

(57) Abstract: An embodiment includes a metal interconnect structure, comprising: a dielectric layer on a substrate; an opening, in the dielectric layer, (a) having sidewalls and an aspect ratio of at least 5:1 (height: width), and (b) exposing a conductive region of at least one of the substrate and an additional interconnect structure; a conformal thin film layer on the sidewalls; and a polycrystalline metal within the opening and on the thin film layer; wherein the thin film layer forms an adhesive liner that extends only partially up the sidewalls leaving upper portions of the sidewalls uncovered by the liner. Other embodiments are described herein.

REDUCED HEIGHT LINER FOR INTERCONNECTS

Technical Field

[0001] Embodiments of the present invention relate generally to metal interconnect structures and their methods of fabrication.

Background

[0002] Once semiconductor wafers are prepared, a large number of process steps are still necessary to produce desired semiconductor integrated circuits. In general the steps can be grouped into four areas: Front End Processing, Back End Processing, Test, and Packaging.

[0003] Front End Processing refers to the initial steps in the fabrication. In this stage the actual semiconductor devices (e.g., transistors) are created. A typical front end process includes: preparation of the wafer surface, patterning and subsequent implantation of dopants to obtain desired electrical properties, growth or deposition of a gate dielectric, and growth or deposition of insulating materials to isolate neighboring devices.

[0004] Once the semiconductor devices have been created they must be interconnected to form the desired electrical circuits. This "Back End Processing" involves depositing various layers of metal and insulating material in the desired pattern. Typically the metal layers consist of aluminum, copper, and the like. The insulating material may include SiO₂, low-K materials, and the like. The various metal layers are interconnected by interconnects, which may include a line portion and a via portion. Vias may be formed by etching holes in the insulating material and depositing metal (e.g., Tungsten) in them. The line portion may be formed by etching trenches in the insulating material and depositing metal in them.

[0005] Once the Back End Processing has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. Finally, the wafer is cut into individual die, which are then packaged in packages (e.g., ceramic or plastic packages) with pins or other connectors to other circuits, power sources, and the like.

Brief Description of the Drawings

[0006] Features and advantages of embodiments of the present invention will become apparent from the appended claims, the following detailed description of one or more example embodiments, and the corresponding figures. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

Figures 1(a)-(c) depict non-uniformity in trenches due to recessing of fill material;

Figures 2(a)-(b) depict corrosion of an adhesion liner;

Figures 3(a)-(e) depict recessed liners in various embodiments;

Figures 4(a)-(c) depict recessed liners in various embodiments;

Figure 5 depicts a recessed liner in an embodiment;

Figure 6 includes a method in an embodiment; and

Figure 7 includes a system that includes an embodiment.

Detailed Description

[0007] Reference will now be made to the drawings wherein like structures may be provided with like suffix reference designations. In order to show the structures of various embodiments more clearly, the drawings included herein are diagrammatic representations of semiconductor/circuit structures. Thus, the actual appearance of the fabricated integrated circuit structures, for example in a photomicrograph, may appear different while still incorporating the claimed structures of the illustrated embodiments. Moreover, the drawings may only show the structures useful to understand the illustrated embodiments. Additional structures known in the art may not have been included to maintain the clarity of the drawings. For example, not every layer of a semiconductor device is necessarily shown. "An embodiment", "various embodiments" and the like indicate embodiment(s) so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Some embodiments may have some, all, or none of the features described for other embodiments. "First", "second", "third" and the like describe a common object and indicate different instances of like objects are being referred to. Such adjectives do

not imply objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner. "Connected" may indicate elements are in direct physical or electrical contact with each other and "coupled" may indicate elements co-operate or interact with each other, but they may or may not be in direct physical or electrical contact.

[0008] An embodiment provides a method for selective growth of metals in high aspect ratio (AR) structures. The embodiment enables the creation of interconnect structures as critical dimension (CD) decreases towards 7 nm and beyond. More specifically, an embodiment relates to the use of recessed adhesion liners and the metal fill of trenches and vias with ARs higher than 1:5. The recessed adhesion lines help overcome the limitations of traditional immersion lithography schemes.

[0009] Regarding the above mentioned limitations of traditional immersion lithography schemes, Applicant noted conventional trench fill techniques fill trenches by deposition of a liner followed by a deposition of a conductive metal. The conductive metal is deposited in excess (overflowing the opening that forms the via or trench) and is subsequently planarized (using Chemical Mechanical Planarization (CMP)) and/or recessed. Applicant determined some of the limitations of this "metal deposition and recess" approach include local roughness of the etched material. The local roughness causes metal recess non-uniformity.

[0010] For example regarding this roughness/non-smoothness (and resultant non-uniformity), Figures 1(a)-(c) depict non-uniformity in trenches due to recessing of fill material. Figure 1(a) shows that with challengingly small CDs, trench to trench variation occurs. Note the varying heights 101, 102, 103, 104 of fill material 140, 141, 142, 143 in trenches 111, 112, 113, 114. The trenches are lined with an adhesive liner 140. Figure 1(b) shows that non-uniformity/variation may also occur within a trench (note non-smooth upper surface 121 of fill material 122 within trench 123). Figure 1(c) again shows that variation may occur within a trench (note non-smooth upper surface 131 and varying heights 134, 135 of fill material 132 within trench 133).

[0011] An adhesive liner or adhesion liner helps a fill metal adhere to sidewalls of a trench or via. Such sidewalls may include interlayer dielectric (ILD), Si, or some other material to which certain metals cannot grow from. Thus, the liner adheres to both the fill material and the opening sidewall.

[0012] Another limitation of traditional immersion lithography schemes includes corrosion of the liner due to imperfect etch selectivity to materials in the stack during subsequent processing. For example, Figures 2(a)-(b) depict corrosion of an adhesion liner. Figure 2(a) shows liner 240 and fill metal 222. Figure 2(b) shows liner 240 and fill metal 222 with areas of corrosion 141, 142. Area 241 is the landing via from the upper layer. Liner 240 is representative of liners used in conventional chemical vapor deposition (CVD) and atomic layer deposition (ALD) damascene fills of trenches. Such liners may include metal nitrides. Applicant determined such liners may be incompatible with cleaning stages (and chemicals used therewith) needed to remove excess fill material and/or next layer hard mask. This incompatibility leads to corrosion and potential failure for the interconnect.

[0013] However, embodiments described herein address gap-fill challenges critical to enable 7 nm CD nodes and beyond (such as the challenges identified in Figures 1(a)-(c) and 2(a)-(b)). Moreover, such embodiments offer a way to improve within die recess by relying only on the deposition of the metal. Put another way, the height of the metal fill can be dictated by a more predictable growth of the metal fill along the liner (versus the unpredictable heights on top surfaces of metal fill when the fill is recessed and/or subjected to CMP). Further, embodiments address needs such as filling high AR features and metal recess control for pitch doubling or pitch quartering integration schemes. As used herein, AR refers to the height of a feature (e.g., trench) to a width of the feature.

[0014] More specifically, an embodiment includes a method to deposit metals (e.g., Co or Co alloys) on conductive surfaces using an auto-catalytic chemical technique, such as electroless deposition (ELD), or selective CVD, ALD metal deposition techniques. An embodiment allows a controllable fill of metal trenches by recessing a conductive liner before performing the metal fill.

[0015] Figures 3(a)-(e) depict recessed liners in various embodiments. Figures 4(a)-(c) depict recessed liners in various embodiments.

[0016] An embodiment provides a metal interconnect structure comprising a dielectric layer 401 on a substrate 402. An opening 403 in the dielectric layer has sidewalls 404, 405 and an AR of at least 5:1 (although other embodiments may include AR's of 3:1, 4:1, 6:1, 7:1, 8:1, 9:1, and the like). Opening 403 may expose a conductive region 406 (e.g., source or drain of a switching node) of the substrate. However, in other embodiments element 402 may be just another interconnect structure. Conformal thin film layer 407 is on the sidewalls. Polycrystalline metal 408 is within the opening 403 and on the thin film layer 407. Layer 407 forms an adhesive liner (also referred to as element 407) that extends only partially up the sidewalls (height 409) leaving an upper portion 410 of the sidewalls uncovered by the liner.

[0017] In an embodiment the opening 403 is a damascene trench. As used herein, a damascene trench includes trenches formed using single or double damascene processes. In an embodiment, metal 408 may not include Cu but may include at least one of Co, Ru, W, and Al (although other metals may include Pt, Pd, Rh, Re, and Ir and alloys thereof). As used herein, a "material including A" should be interpreted to encompass, for example, alloys of A. Liner 407 includes a nitride of at least one of Ti, Ta, W, Zr and Mo (e.g., TiN or TaN as TaN, TiN, WN, and MoN), however other materials for liner 407 include borides, carbides and silicides of at least one of Ti, Ta, W, Zr and Mo.

[0018] Liner 407 is on the conductive region 406 and the sidewalls 404, 405 (but in other embodiments liner 407 may be removed from area 406).

[0019] Vertical axis 413 intersects sidewall 404 and vertical axis 414, which is adjacent vertical axis 413. Axis 414 intersects the metal 408 and a portion of the liner 407 adhering to sidewall 404. This is because the metal actually gets wider just above the top of the liner in embodiments where the metal fill extends higher than the liner. Horizontal axis 415 intersects sidewalls 404, 405, the liner 407, and the metal 408. Horizontal axis 416, above horizontal axis 415, intersects the two sidewalls but not the liner. Axis 416 intersects the metal 408. Horizontal axis 417,

above axis 416, intersects sidewalls 404, 405 but not the liner 407 and not the metal 408.

[0020] Figure 3(b) shows how metal 408 can be grown to different heights 418, 419, 420, 421. In an embodiment (see Figure 4(c)) the metal extends from a bottom of the opening to an uppermost edge 422 of the opening with metal. However, in other embodiments the metal extends from a bottom of the opening to a location between an uppermost edge 422 of the opening and an uppermost edge 423 of the liner (see heights 418, 419, 420, 421).

[0021] In Figure 3(c) an additional material 424 is in the opening and on the metal 408. Material 424 fills an upper portion of the opening. In an embodiment material 424 includes a dielectric material, but in other embodiments material 424 includes a metal having a chemical formula unequal to a chemical formula of the metal 408.

[0022] In an embodiment, materials 424, 425 may be different from each other as well as fill 408. For example, materials 424, 425 may form different insulating plug materials that improve shorting margin through etch selectivity with subsequent processing.

[0023] As seen in Figure 3(d) (which is just a very simplistic representation of a dual damascene trench over two vias), in an embodiment an upper surface 426 of the metal is substantially smooth and coplanar with axis 427 and the upper surface extends from a vertical axis 428 intersecting a via 429 to another vertical axis 430 intersecting via 431. This figure just shows how embodiments not only can lead to uniform heights among adjacent trenches (e.g., Figure 3(c)), but also within a single trench (e.g., Figure 3(d)).

[0024] In an embodiment metal 408 is an ELD layer. This may be indicated by the purity of metal 408. For example, the ELD process may produce 99.99% pure Co metal. Such a fill will not have carbon (C) in the film 407 (whereas use of CVD/ALD to deposit the fill metal would lead to C in layer 407). Other embodiments are not so limited and may include, for example, Al, W, Ru, Pt, Pd, Rh, Re, and Ir.

[0025] In an embodiment (Figure 3(e)), metal 408 directly contacts both the liner 407 (see point 433) and the sidewalls (see point 432).

[0026] Figure 4(a) depicts liner 407 etched at point 434. Figure 4(b) is a different image of a different structure from that of Figure 4(a) or 4(c). In Figure 4(b) the fill 408 goes just past the liner (liner ends at point 436) to level 435, whereas in Figure 4(c) the fill 408 goes above and beyond the opening top level 489 (and is subject to CMP to performed later in the process) to level 422.

[0027] Figure 5 depicts a recessed liner in an embodiment. Opening 503 forms a dual-damascene trench 501 and via 502. Adhesion liner 504 lines sidewalls 506, 507 of the via and sidewalls 508, 509 of the trench and bottom surface 510 of the trench 501. The liner extends only partially up the sidewalls of the trench leaving upper portions 511, 512 of the trench sidewalls uncovered by the liner.

[0028] As used herein and as mentioned above, a damascene trench includes trenches formed using single or double damascene processes. A dual damascene trench and via may indicated by the presence of monolithic fill material within the via 502 and the trench 503 (i.e., no seam exists at via/trench interface 513). In an embodiment, liner 504 extends across the bottom edge 514 of the via at the interface between via 502 and conductive region of interconnect 515.

[0029] An embodiment may include a system on a chip with embedded memory including a memory array comprising the metal interconnect structure. Such embedded memory may be located in, for example, Figure 7 (which includes a system that includes an embodiment).

[0030] Figure 6 includes a method 600 in an embodiment. Block 601 includes forming a dielectric layer on a substrate. Block 602 includes forming an opening in the dielectric layer using a damascene process, the opening having sidewalls and an AR of at least 5:1. Block 603 includes forming an opening to expose a conductive region of at least one of the substrate and an additional interconnect structure. Block 604 includes forming a conformal thin film layer on the sidewalls. Block 605 includes etching the conformal thin film layer to form an adhesive liner that extends only partially up the sidewalls leaving upper portions of the sidewalls uncovered by the liner. Block 606 includes forming a polycrystalline metal within the opening using ELD.

[0031] The method may comprise forming the metal at a first height that extends from a bottom of the opening to, but not beyond, a location between an uppermost edge of the opening and an uppermost edge of the liner. Forming the metal at the first height is not based on performing chemical mechanical planarization (CMP) on the metal (because process 600 does not include CMP, but other embodiments may add CMP to process 600). Forming the metal at the first height is not based on etching the metal (because process 600 does not include etching or recessing the metal, but other embodiments may do so). In process 600 forming the metal at the first height is based on a height of the liner that extends only partially up the sidewalls. For example, the metal may use the liner as an adhesive and therefore primarily grow where the liner extends to, although the metal may continue to grow (see, e.g., Figure 4(c)).

[0032] Referring now to Figure 7, shown is a block diagram of an example system with which embodiments can be used. As seen, system 900 may be a smartphone or other wireless communicator or any other internet-of-things (IoT) device. A baseband processor 905 is configured to perform various signal processing with regard to communication signals to be transmitted from or received by the system. In turn, baseband processor 905 is coupled to an application processor 910, which may be a main CPU of the system to execute an OS and other system software, in addition to user applications such as many well-known social media and multimedia apps. Application processor 910 may further be configured to perform a variety of other computing operations for the device.

[0033] In turn, application processor 910 can couple to a user interface/display 920 (e.g., touch screen display). In addition, application processor 910 may couple to a memory system including a non-volatile memory, namely a flash memory 930 and a system memory, namely a DRAM 935. In some embodiments, flash memory 930 may include a secure portion 932 in which secrets and other sensitive information may be stored. As further seen, application processor 910 also couples to a capture device 945 such as one or more image capture devices that can record video and/or still images.

[0034] A universal integrated circuit card (UICC) 940 comprises a subscriber identity module, which in some embodiments includes a secure storage 942 to store secure user information. System 900 may further include a security processor 950 (e.g., Trusted Platform Module (TPM)) that may couple to application processor 910. A plurality of sensors 925, including one or more multi-axis accelerometers may couple to application processor 910 to enable input of a variety of sensed information such as motion and other environmental information. In addition, one or more authentication devices 995 may be used to receive, for example,, user biometric input for use in authentication operations.

[0035] As further illustrated, a near field communication (NFC) contactless interface 960 is provided that communicates in a NFC near field via an NFC antenna 965. While separate antennae are shown, understand that in some implementations one antenna or a different set of antennae may be provided to enable various wireless functionalities.

[0036] A power management integrated circuit (PMIC) 915 couples to application processor 910 to perform platform level power management. To this end, PMIC 915 may issue power management requests to application processor 910 to enter certain low power states as desired. Furthermore, based on platform constraints, PMIC 915 may also control the power level of other components of system 900.

[0037] To enable communications to be transmitted and received such as in one or more IoT networks, various circuitry may be coupled between baseband processor 905 and an antenna 990. Specifically, a radio frequency (RF) transceiver 970 and a wireless local area network (WLAN) transceiver 975 may be present. In general, RF transceiver 970 may be used to receive and transmit wireless data and calls according to a given wireless communication protocol such as 3G or 4G wireless communication protocol such as in accordance with a code division multiple access (CDMA), global system for mobile communication (GSM), long term evolution (LTE) or other protocol. In addition a GPS sensor 980 may be present, with location information being provided to security processor 950 for use as described herein when context information is to be used in a pairing process. Other wireless communications such as receipt or transmission of radio signals (e.g., AM/FM) and

other signals may also be provided. In addition, via WLAN transceiver 975, local wireless communications, such as according to a Bluetooth™ or IEEE 802.11 standard can also be realized.

[0038] Considering the ubiquity of interconnects, interconnects described herein may be found in some or all of the components of Figure 7.

[0039] Please note in some embodiments a seed layer is used. For example, a seed layer may be located between the liner 407 and the metal 408. The seed layer may be deposited using a PVD process. However, in other embodiments ELD is used to deposit fill 408 on liner 407 and no seed layer is needed. For embodiments with a seed layer, such a layer is used to ensure adequate adhesion between materials (e.g., metal fill 407 and ILD 401). The seed layer may include the same metal 408 that is to form metal lines. Alternatively, an alloy of the metal may be used to form the seed layer. The seed layer is generally quite thin. For example, the seed layer may be between about 10 angstroms and about 3,000 angstroms in thickness. By way of comparison, the complete metal lines to be formed may fill photoresist or ILD or silicon/substrate trenches and may be between about 0.06 microns and about 20 microns in height 411 and may be between about 0.01 microns and about 7 microns in width 412. The seed layer may be deposited, for example, by ALD. In this manner, thin and uniform seed layers are formed that adhere to silicon or other materials defining the trenches.

[0040] In an embodiment the dielectric layer (e.g., layer 401) may be composed of any suitable dielectric or insulating material such as, but not limited to, silicon dioxide, SiOF, carbon-doped oxide, a glass or polymer material, and the like.

[0041] Although embodiments may be ideally suited for fabricating semiconductor ICs such as, but not limited to, microprocessors, memories, charge-coupled devices (CCDs), system on chip (SoC) ICs, or baseband processors, other applications can also include microelectronic machines, MEMS, lasers, optical devices, packaging layers, and the like. Embodiments may also be used to fabricate individual semiconductor devices (e.g., an interconnect structure described herein may be used to fabricate a gate electrode of a MOS transistor).

[0042] Thus, embodiments provide many advantages. First, embodiments provide a method for selective deposition of pure metals (e.g., using ELD to form pure or nearly pure Co fill of a trench). Second, an embodiment provides a conductive surface (e.g., liner) to catalyze a deposition and growth of the metal fill within high AR structures. Third, embodiments provide for optimized effective metal area and overall line resistance improvement. For example, a metal nitride liner may be resistive so reducing the amount of liner in an interconnect increases the space available for metal fill, thereby lowering resistance of the interconnect. Fourth, embodiments provide ease of effective metal height control (e.g., just edge the liner to desired height rather than trying to recess the fill metal or subject the fill metal to CMP). In other words, embodiments provide for fill metal height independently of chemical recess (which is not needed in embodiments) or CMP (which is not needed in embodiments). This is important because fill materials, like Ru, are hard to recess by etching and can become volatile during recess attempts. Fifth, embodiments provide for an improved shorting margin. For example, by reducing the amount of metal fill that overflows the interconnect there is less chance for shorting between overflows from adjacent interconnect structures. Sixth, an embodiment reduces the risk of contact to gate or contact to trench shorts by enabling a process independent of metal CMP or wet and/or dry metal recess etch. Both CMP and recess etch processes have oxide loss in vertical and/or horizontal directions associated with them, therefore increasing the risk of within layer shorts. Seventh, embodiments described herein may be used for contact and interconnect gap fill. This may reduce the number of steps and/or tools need to make the contact or interconnect.

[0043] Various embodiments include a semiconductive substrate. Such a substrate may be a bulk semiconductive material this is part of a wafer. In an embodiment, the semiconductive substrate is a bulk semiconductive material as part of a chip that has been singulated from a wafer. In an embodiment, the semiconductive substrate is a semiconductive material that is formed above an insulator such as a semiconductor on insulator (SOI) substrate. In an embodiment, the semiconductive substrate is a prominent structure such as a fin that extends above a bulk semiconductive material.

[0044] The following examples pertain to further embodiments.

[0045] Example 1 includes a metal interconnect structure, comprising: a dielectric layer on a substrate; an opening, in the dielectric layer, (a) having sidewalls and an aspect ratio of at least 5:1 (height: width), and (b) exposing a conductive region of at least one of the substrate and an additional interconnect structure; a conformal thin film layer on the sidewalls; and a polycrystalline metal within the opening and on the thin film layer; wherein the thin film layer forms an adhesive liner that extends only partially up the sidewalls leaving upper portions of the sidewalls uncovered by the liner.

[0046] In example 2 the subject matter of the Example 1 can optionally include wherein the opening is a damascene trench.

[0047] In example 3 the subject matter of the Examples 1-2 can optionally include wherein the metal does not include Cu but does include at least one of Co, Ru, W, Al, Pt, Pd, Rh, Re, and Ir.

[0048] In example 4 the subject matter of the Examples 1-3 can optionally include wherein the liner is on the conductive region and the sidewalls.

[0049] In example 5 the subject matter of the Examples 1-4 can optionally include wherein the liner includes at least one of: (a) a nitride of at least one of Ti, Ta, W, Zr, and Mo, (b) a boride of at least one of Ti, Ta, W, Zr, and Mo, (c) a carbide of at least one of Ti, Ta, W, Zr, and Mo, and (d) a silicide of at least one of Ti, Ta, W, Zr, and Mo.

[0050] In example 6 the subject matter of the Examples 1-5 can optionally include wherein a first vertical axis intersects one of the sidewalls and a second vertical axis, adjacent the first vertical axis, intersects the metal and a portion of the liner adhering to the one of the sidewalls.

[0051] In example 7 the subject matter of the Examples 1-6 can optionally include wherein the metal extends from a bottom of the opening to an uppermost edge of the opening.

[0052] In example 8 the subject matter of the Examples 1-7 can optionally include wherein the metal extends from a bottom of the opening to a location between an uppermost edge of the opening and an uppermost edge of the liner.

[0053] In example 9 the subject matter of the Examples 1-8 can optionally include an additional material in the opening and on the metal; wherein the additional material fills an upper portion of the opening.

[0054] In example 10 the subject matter of the Examples 1-9 can optionally include wherein the additional material includes a dielectric material.

[0055] In example 11 the subject matter of the Examples 1-10 can optionally include wherein the additional material includes a metal having a chemical formula unequal to a chemical formula of the metal.

[0056] In example 12 the subject matter of the Examples 1-11 can optionally include wherein an upper surface of the metal is substantially smooth and the upper surface extends from a vertical axis intersecting a first via to another vertical axis intersecting a second via.

[0057] In example 13 the subject matter of the Examples 1-12 can optionally include an additional opening, in the dielectric layer, (a) having additional sidewalls and an aspect ratio of at least 5:1, and (b) exposing another conductive region; an additional conformal thin film layer on the additional sidewalls; and an additional polycrystalline metal within the additional opening and on the additional thin film layer; wherein the additional thin film layer forms an additional adhesive liner that extends only partially up the additional sidewalls leaving upper portions of the additional sidewalls uncovered by the additional liner; wherein the additional opening is adjacent the opening with no other opening between the opening and the additional opening.

[0058] In example 14 the subject matter of the Examples 1-13 can optionally include a first additional material in the opening and on the metal, the first additional material filling an upper portion of the opening; and a second additional material in the additional opening and on the additional metal, the second additional material

filling an upper portion of the additional opening; wherein the first and second additional materials have differing chemical formulae from one another.

[0059] In example 15 the subject matter of the Examples 1-14 can optionally include wherein: a first upper surface of the metal is substantially smooth and extends a first distance from a first vertical axis intersecting a first via to a second vertical axis intersecting a second via; a second upper surface of the additional metal is substantially smooth and extends the first distance; and the first and second upper surfaces extend equal heights above the substrate.

[0060] In example 16 the subject matter of the Examples 1-15 can optionally include wherein: the opening forms a dual-damascene trench and via and the liner lines sidewalls of the via and a bottom surface of the trench; and the liner extending only partially up the sidewalls leaving upper portions of the sidewalls uncovered by the liner includes the liner extending only partially up sidewalls of the trench.

[0061] In example 17 the subject matter of the Example 1-16 can optionally include a system on a chip with embedded memory including a memory array comprising the metal interconnect structure.

[0062] In example 18 the subject matter of the Examples 1-17 can optionally include wherein: a first horizontal axis intersects two of the sidewalls, the liner, and the metal; and a second horizontal axis, above the first horizontal axis, intersects the two sidewalls but not the liner.

[0063] In example 19 the subject matter of the Examples 1-18 can optionally include wherein the second horizontal axis intersects the metal.

[0064] In example 20 the subject matter of the Examples 1-19 can optionally include wherein a third horizontal axis, above the second horizontal axis, intersects the two sidewalls but not the liner and not the metal.

[0065] In example 21 the subject matter of the Examples 1-20 can optionally include wherein the metal is an electroless deposition (ELD) layer.

[0066] In example 22 the subject matter of the Examples 1-21 can optionally include wherein the metal directly contacts both the liner and the sidewalls.

[0067] Example 23 includes a method comprising: forming a dielectric layer on a substrate; forming an opening in the dielectric layer using a damascene process, the opening (a)(i) having sidewalls and an aspect ratio of at least 5:1, and (a)(ii) exposing a conductive region of at least one of the substrate and an additional interconnect structure; forming a conformal thin film layer on the sidewalls; etching the conformal thin film layer to form an adhesive liner that extends only partially up the sidewalls leaving upper portions of the sidewalls uncovered by the liner; and forming a polycrystalline metal within the opening

[0068] In example 24 the subject matter of the Examples 23 can optionally include forming the metal at a first height that extends from a bottom of the opening to, but not beyond, a location between an uppermost edge of the opening and an uppermost edge of the liner; wherein the forming the metal at the first height is not based on performing chemical mechanical planarization (CMP) on the metal; wherein the forming the metal at the first height is not based on etching the metal; wherein the forming the metal at the first height is based on a height of the liner that extends only partially up the sidewalls.

[0069] In example 25 the subject matter of the Examples 23-24 can optionally include forming the metal on the liner using electroless deposition (ELD); wherein the damascene process includes at least one of a single damascene process and a dual damascene process.

[0070] The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms, such as left, right, top, bottom, over, under, upper, lower, first, second, etc. that are used for descriptive purposes only and are not to be construed as limiting. For example, terms designating relative vertical position refer to a situation where a device side (or active surface) of a substrate or integrated circuit is the "top" surface of that substrate; the substrate may actually be in any orientation so that a "top" side of a substrate may be lower than the "bottom" side in a standard terrestrial frame of reference and still fall within the meaning of the term "top." The term "on" as used herein (including in the claims) does not indicate

that a first layer "on" a second layer is directly on and in immediate contact with the second layer unless such is specifically stated; there may be a third layer or other structure between the first layer and the second layer on the first layer. The embodiments of a device or article described herein can be manufactured, used, or shipped in a number of positions and orientations. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

What is claimed is:

- 1 1. A metal interconnect structure, comprising:
2 a dielectric layer on a substrate;
3 an opening, in the dielectric layer, (a) having sidewalls and an aspect ratio of
4 at least 5:1 (height: width), and (b) exposing a conductive region of at least one of
5 the substrate and an additional interconnect structure;
6 a conformal thin film layer on the sidewalls; and
7 a polycrystalline metal within the opening and on the thin film layer;
8 wherein the thin film layer forms an adhesive liner that extends only partially
9 up the sidewalls leaving upper portions of the sidewalls uncovered by the liner.
- 1 2. The structure of claim 1, wherein the opening is a damascene trench.
- 1 3. The structure of claim 2, wherein the metal does not include Cu but does
2 include at least one of Co, Ru, W, Al, Pt, Pd, Rh, Re, and Ir.
- 1 4. The structure of claim 3, wherein the liner is on the conductive region and the
2 sidewalls.
- 1 5. The structure of claim 3, wherein the liner includes at least one of: (a) a nitride
2 of at least one of Ti, Ta, W, Zr, and Mo, (b) a boride of at least one of Ti, Ta, W, Zr,
3 and Mo, (c) a carbide of at least one of Ti, Ta, W, Zr, and Mo, and (d) a silicide of at
4 least one of Ti, Ta, W, Zr, and Mo.
- 1 6. The structure of claim 5, wherein a first vertical axis intersects one of the
2 sidewalls and a second vertical axis, adjacent the first vertical axis, intersects the
3 metal and a portion of the liner adhering to the one of the sidewalls.
- 1 7. The structure of claim 5, wherein the metal extends from a bottom of the
2 opening to an uppermost edge of the opening.

1 8. The structure of claim 5, wherein the metal extends from a bottom of the
2 opening to a location between an uppermost edge of the opening and an uppermost
3 edge of the liner.

1 9. The structure of claim 5 including an additional material in the opening and on
2 the metal; wherein the additional material fills an upper portion of the opening.

1 10. The structure of claim 9, wherein the additional material includes a dielectric
2 material.

1 11. The structure of claim 9, wherein the additional material includes a metal
2 having a chemical formula unequal to a chemical formula of the metal.

1 12. The structure of claim 5, wherein an upper surface of the metal is substantially
2 smooth and the upper surface extends from a vertical axis intersecting a first via to
3 another vertical axis intersecting a second via.

1 13. The structure of claim 5 comprising:
2 an additional opening, in the dielectric layer, (a) having additional sidewalls
3 and an aspect ratio of at least 5:1, and (b) exposing another conductive region;
4 an additional conformal thin film layer on the additional sidewalls; and
5 an additional polycrystalline metal within the additional opening and on the
6 additional thin film layer;

7 wherein the additional thin film layer forms an additional adhesive liner that
8 extends only partially up the additional sidewalls leaving upper portions of the
9 additional sidewalls uncovered by the additional liner;

10 wherein the additional opening is adjacent the opening with no other opening
11 between the opening and the additional opening.

1 14. The structure of claim 13 comprising:
2 a first additional material in the opening and on the metal, the first additional
3 material filling an upper portion of the opening; and

4 a second additional material in the additional opening and on the additional
5 metal, the second additional material filling an upper portion of the additional
6 opening;

7 wherein the first and second additional materials have differing chemical
8 formulae from one another.

1 15. The structure of claim 13, wherein:

2 a first upper surface of the metal is substantially smooth and extends a first
3 distance from a first vertical axis intersecting a first via to a second vertical axis
4 intersecting a second via;

5 a second upper surface of the additional metal is substantially smooth and
6 extends the first distance; and

7 the first and second upper surfaces extend equal heights above the substrate.

1 16. The structure of claim 1, wherein:

2 the opening forms a dual-damascene trench and via and the liner lines
3 sidewalls of the via and a bottom surface of the trench; and

4 the liner extending only partially up the sidewalls leaving upper portions of the
5 sidewalls uncovered by the liner includes the liner extending only partially up
6 sidewalls of the trench.

1 17. The structure of claim 1 including a system on a chip with embedded memory
2 including a memory array comprising the metal interconnect structure.

1 18. The structure of claim 1, wherein:

2 a first horizontal axis intersects two of the sidewalls, the liner, and the metal;
3 and

4 a second horizontal axis, above the first horizontal axis, intersects the two
5 sidewalls but not the liner.

1 19. The structure of claim 18, wherein the second horizontal axis intersects the
2 metal.

1 20. The structure of claim 19, wherein a third horizontal axis, above the second
2 horizontal axis, intersects the two sidewalls but not the liner and not the metal.

1 21. The structure of claim 18, wherein the metal is an electroless deposition
2 (ELD) layer.

1 22. The structure of claim 18, wherein the metal directly contacts both the liner
2 and the sidewalls.

1 23. A method comprising:
2 forming a dielectric layer on a substrate;
3 forming an opening in the dielectric layer using a damascene process, the
4 opening (a)(i) having sidewalls and an aspect ratio of at least 5:1, and (a)(ii)
5 exposing a conductive region of at least one of the substrate and an additional
6 interconnect structure;
7 forming a conformal thin film layer on the sidewalls;
8 etching the conformal thin film layer to form an adhesive liner that extends
9 only partially up the sidewalls leaving upper portions of the sidewalls uncovered by
10 the liner; and
11 forming a polycrystalline metal within the opening.

1 24. The method of claim 23 comprising:
2 forming the metal at a first height that extends from a bottom of the opening
3 to, but not beyond, a location between an uppermost edge of the opening and an
4 uppermost edge of the liner;
5 wherein the forming the metal at the first height is not based on performing
6 chemical mechanical planarization (CMP) on the metal;
7 wherein the forming the metal at the first height is not based on etching the
8 metal;
9 wherein the forming the metal at the first height is based on a height of the
10 liner that extends only partially up the sidewalls.

- 1 25. The method of claim 23 comprising:
- 2 forming the metal on the liner using electroless deposition (ELD);
- 3 wherein the damascene process includes at least one of a single damascene
- 4 process and a dual damascene process.

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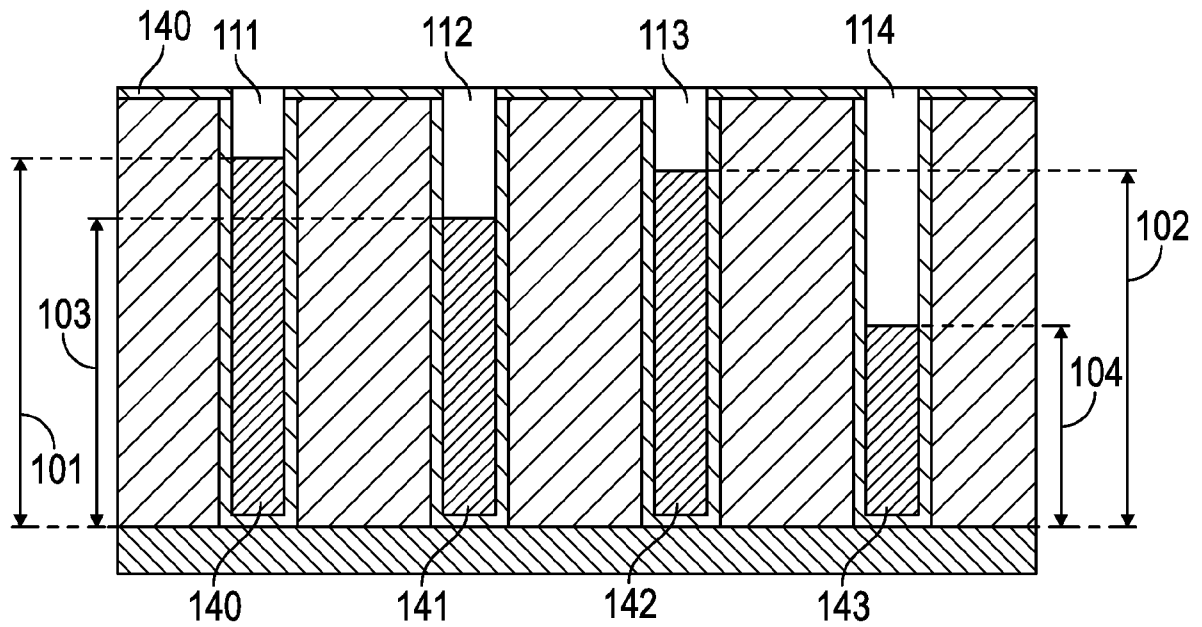


FIG. 1A

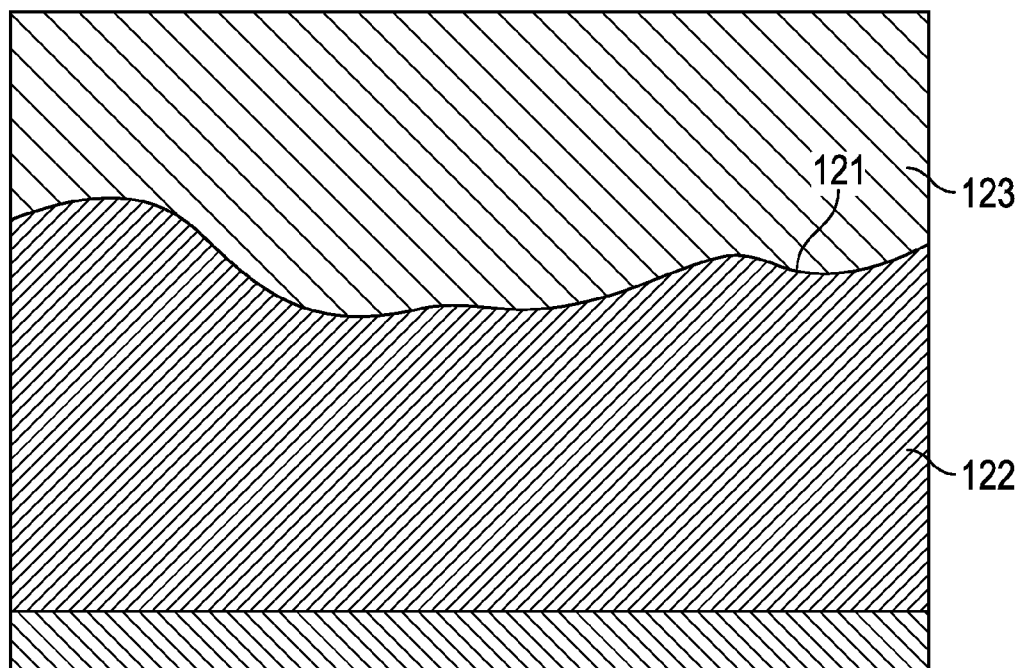


FIG. 1B

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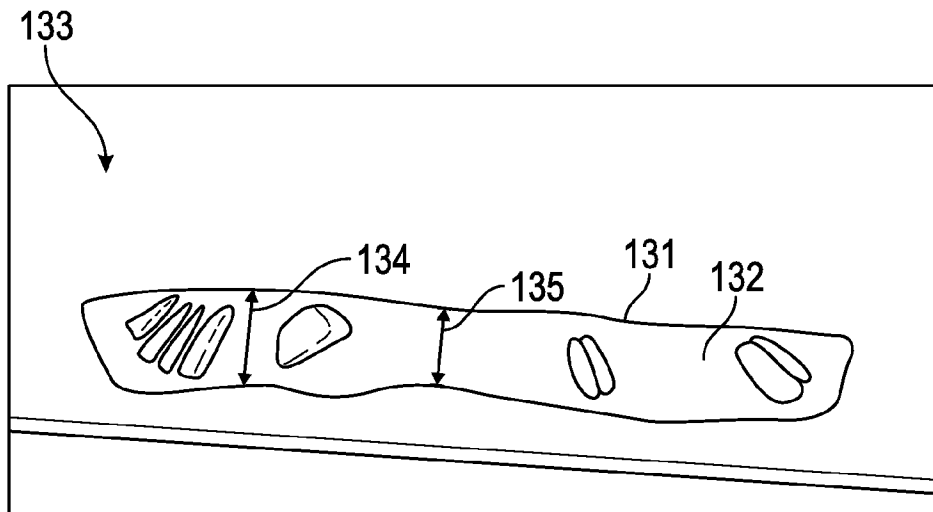


FIG. 1C

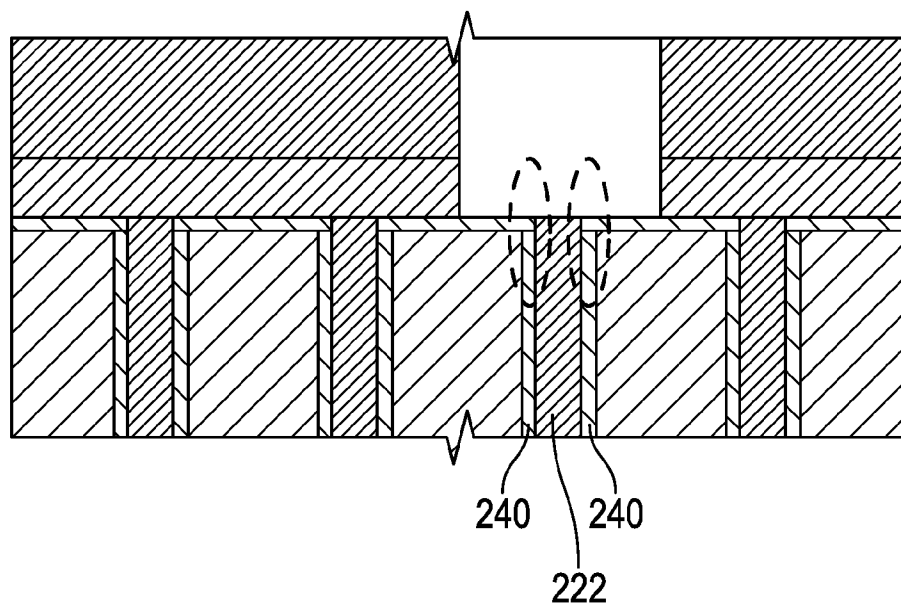


FIG. 2A

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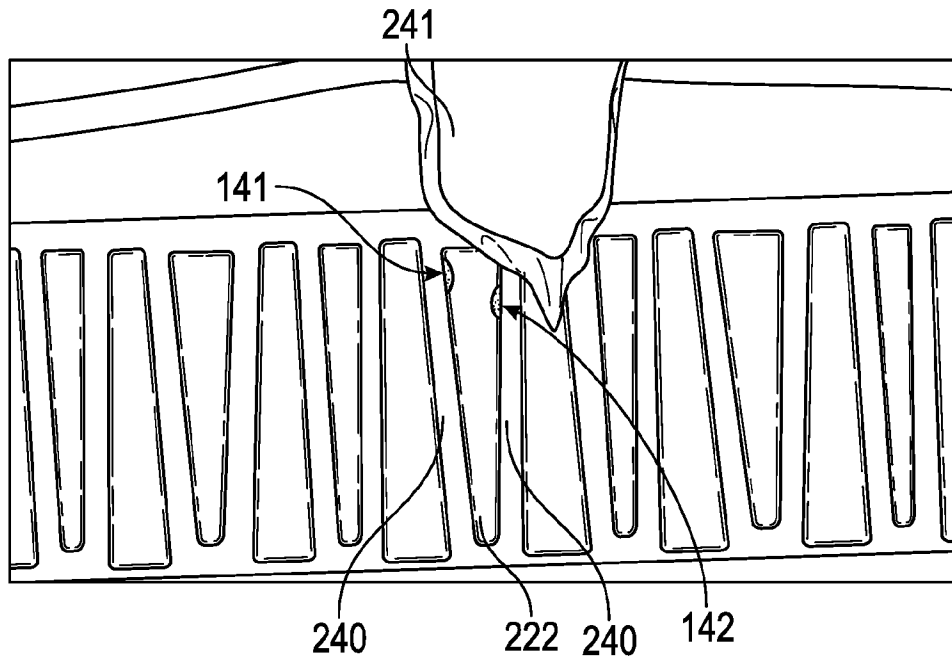


FIG. 2B

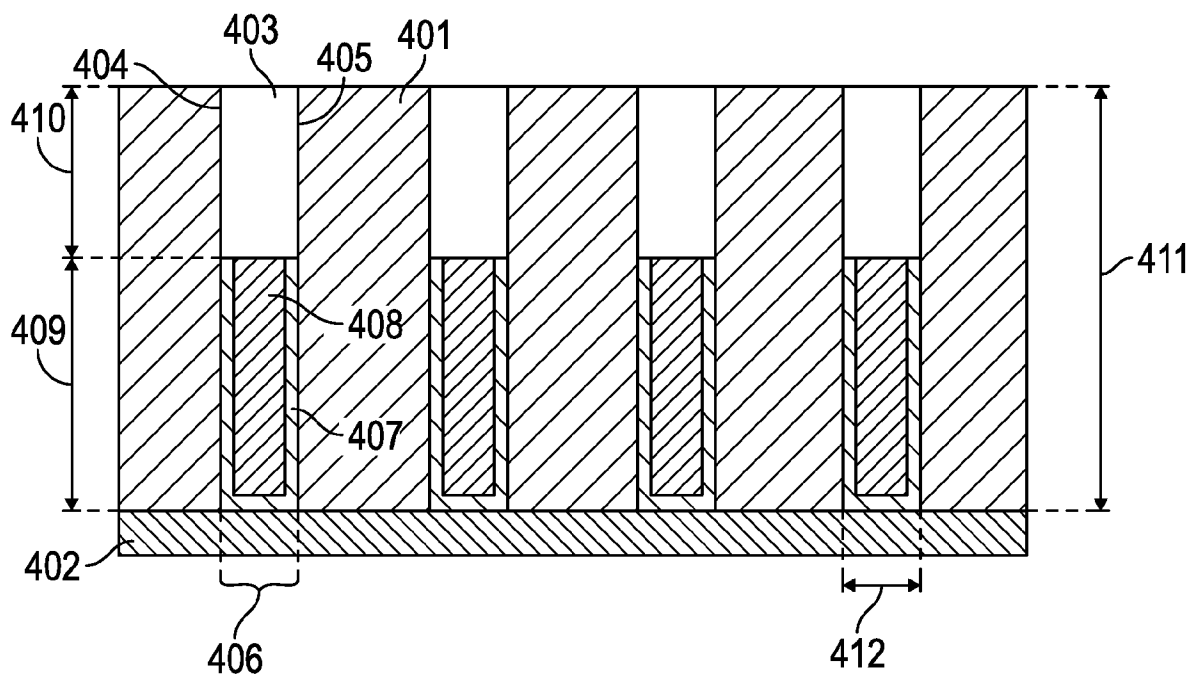


FIG. 3A

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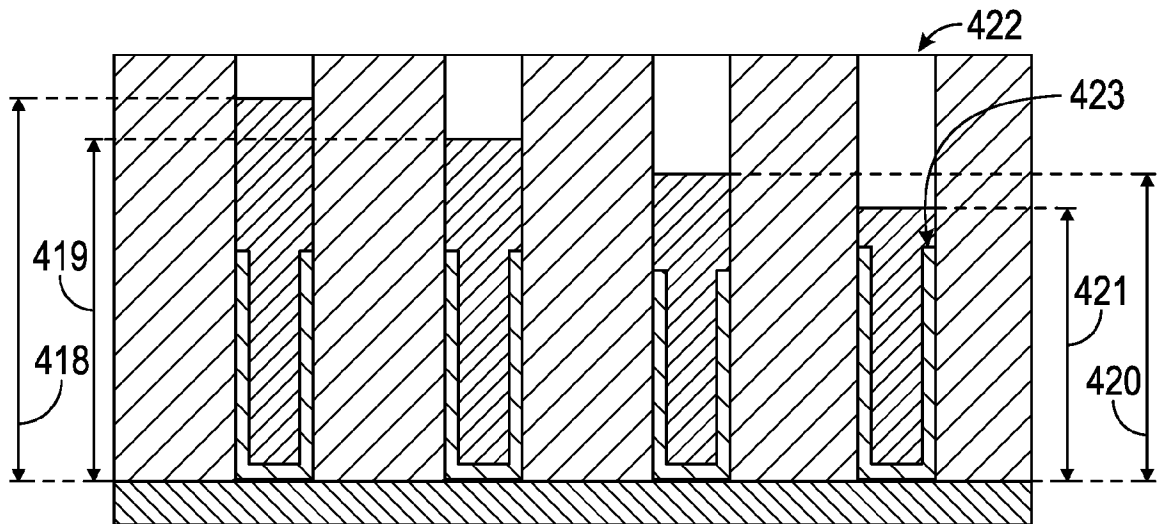


FIG. 3B

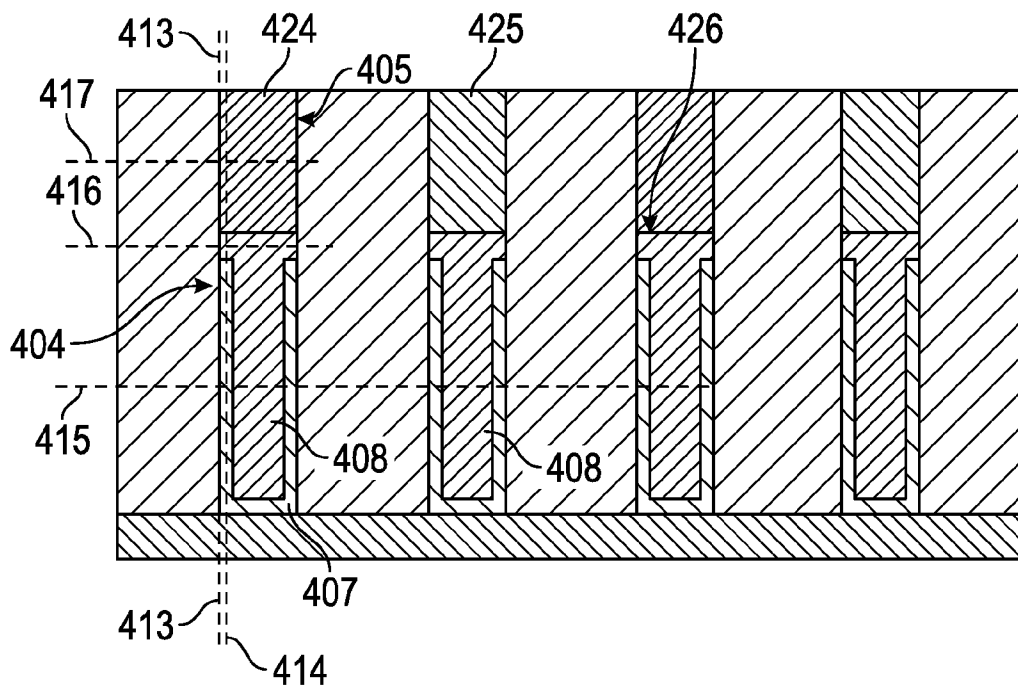


FIG. 3C

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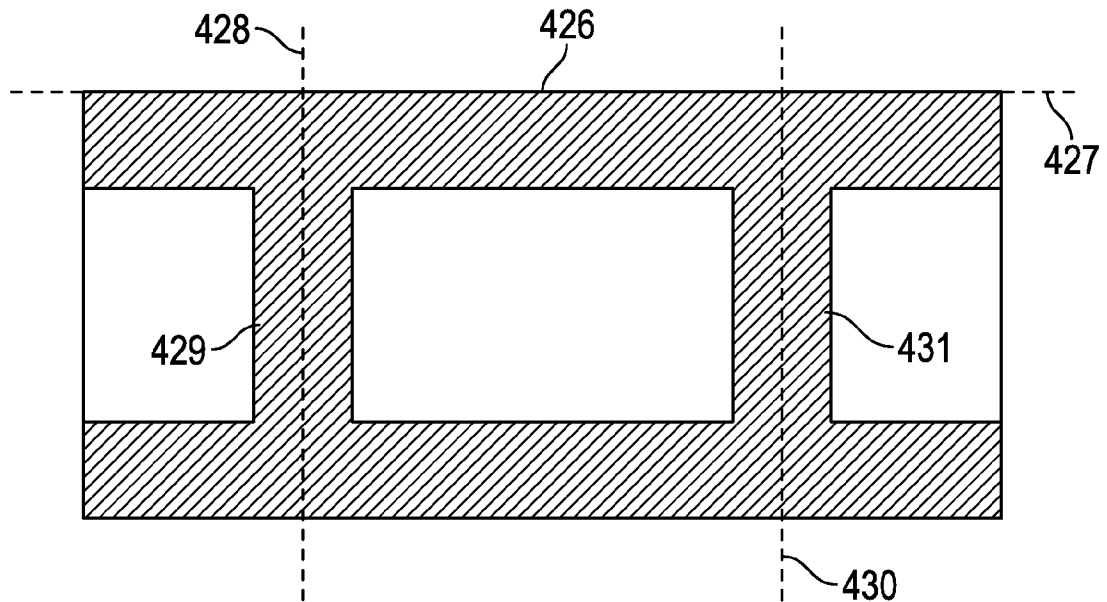


FIG. 3D

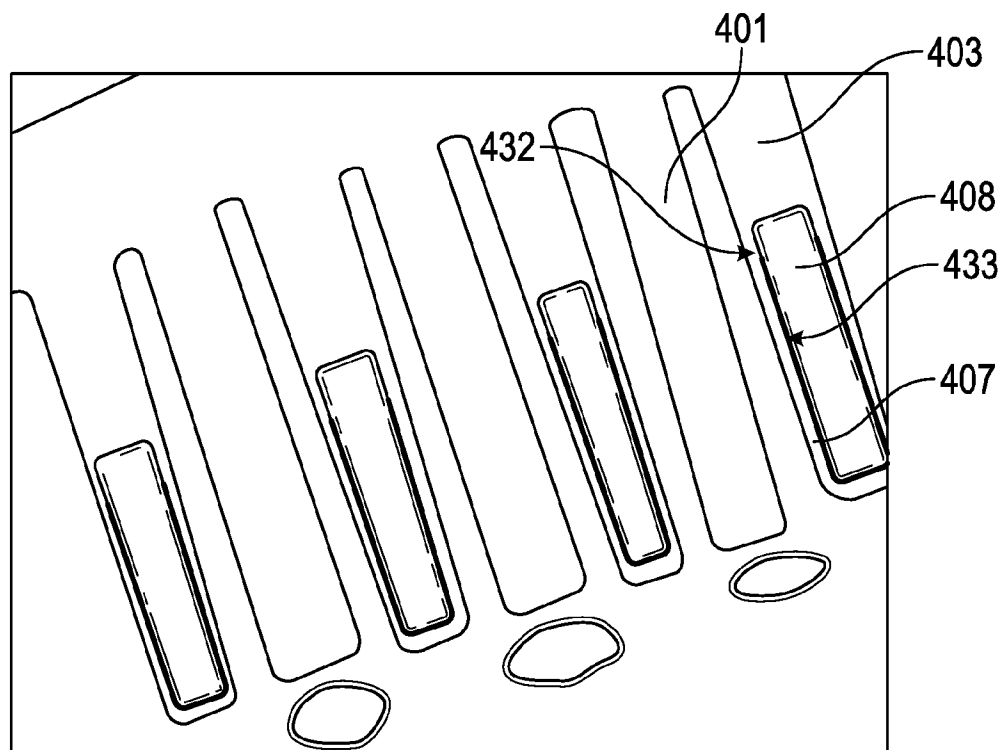


FIG. 3E

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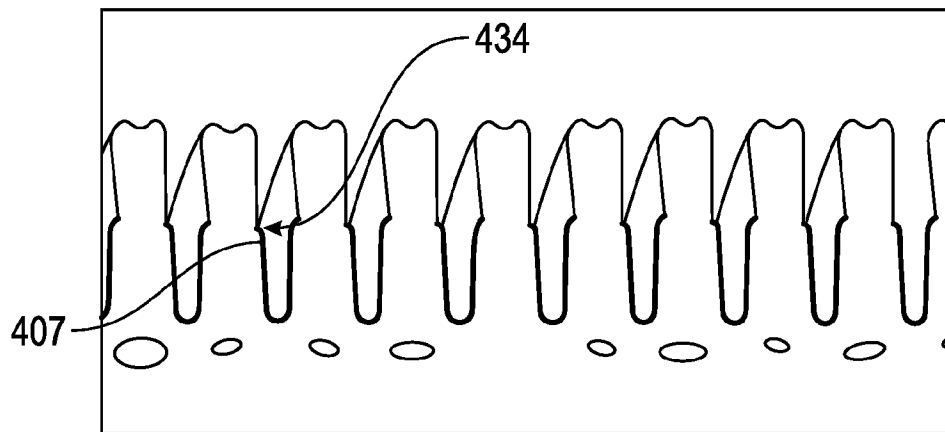


FIG. 4A

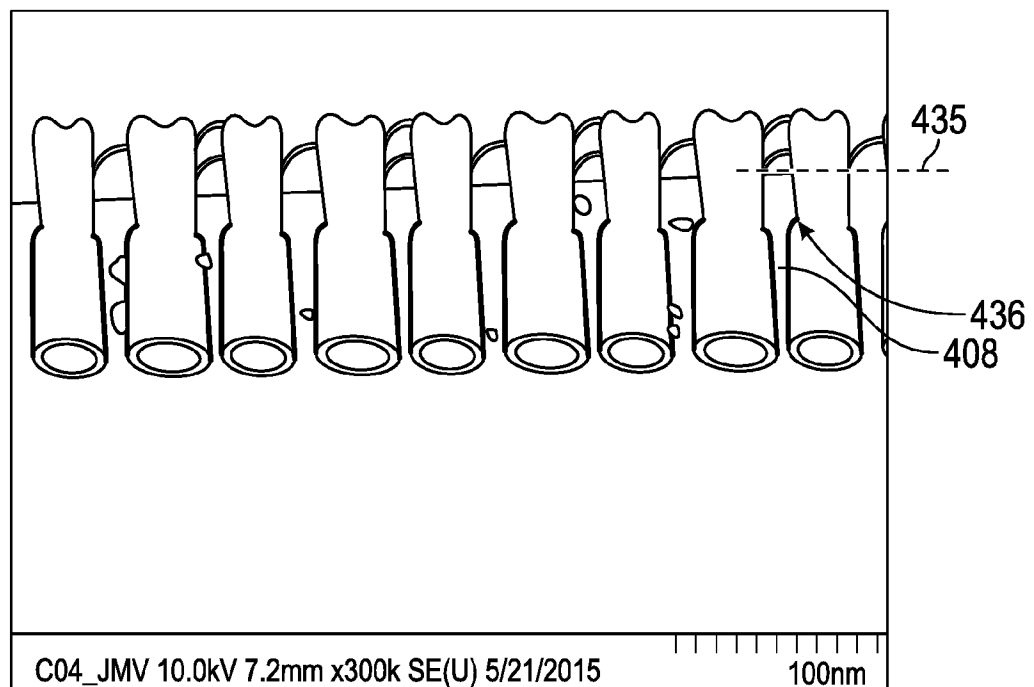


FIG. 4B

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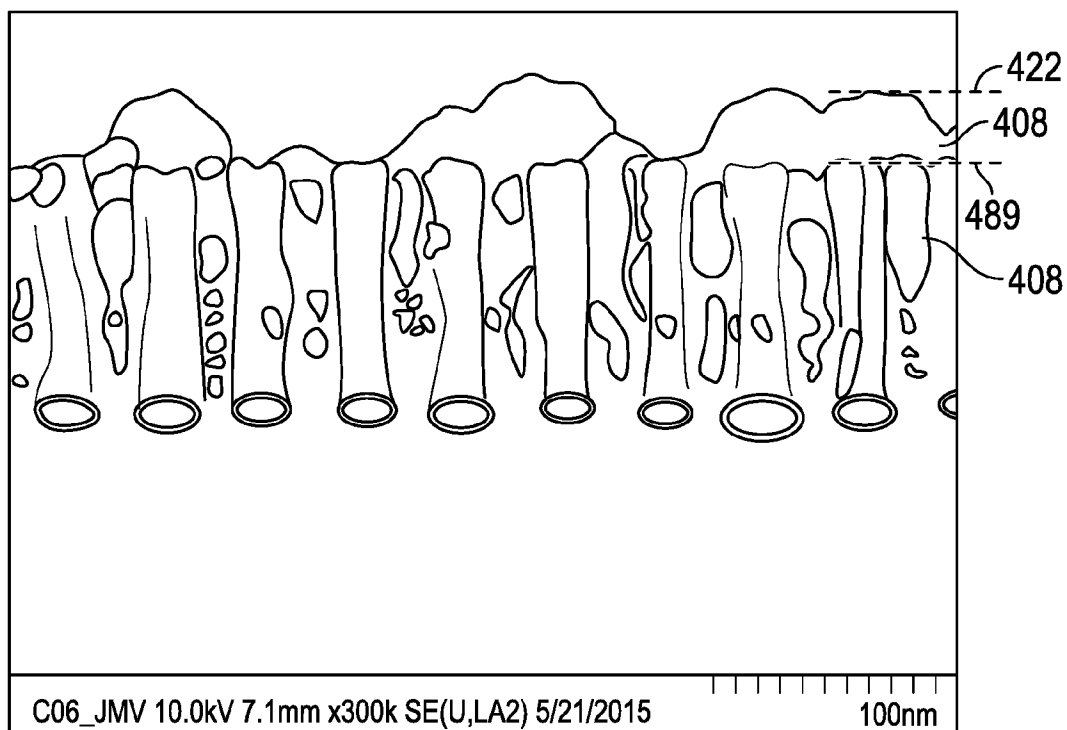


FIG. 4C

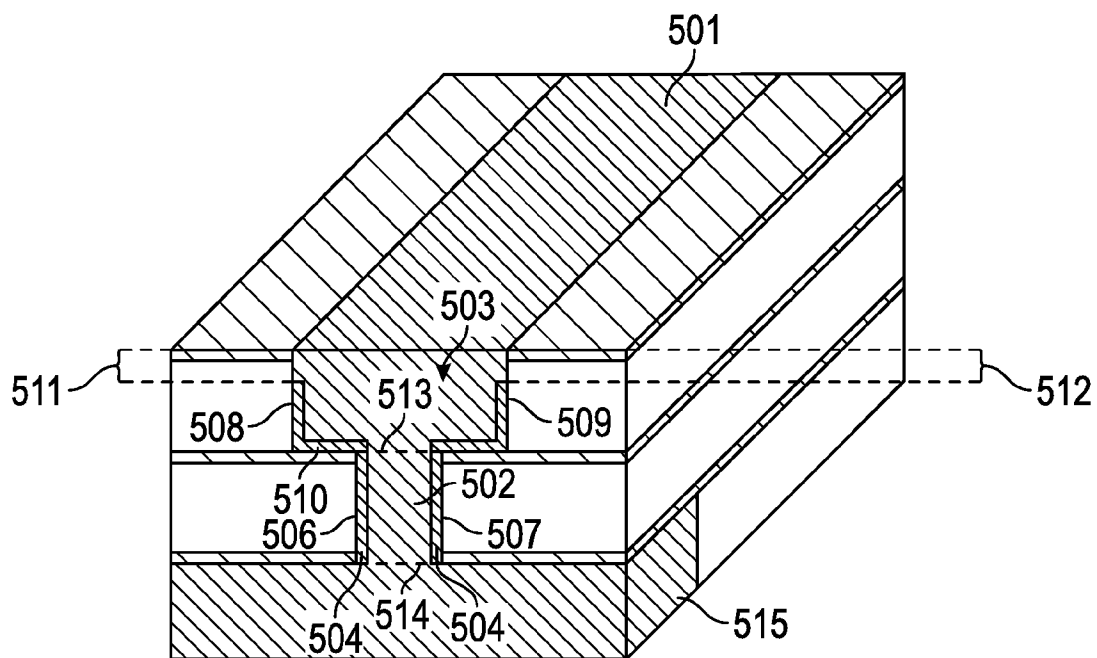
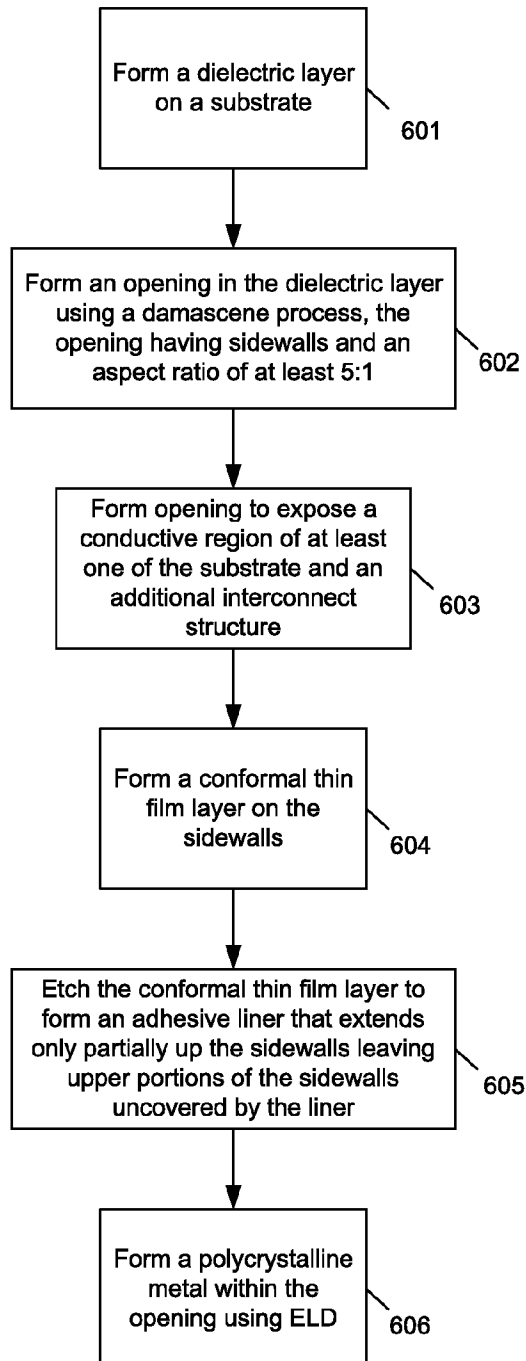


FIG. 5

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600 →**FIG. 6**

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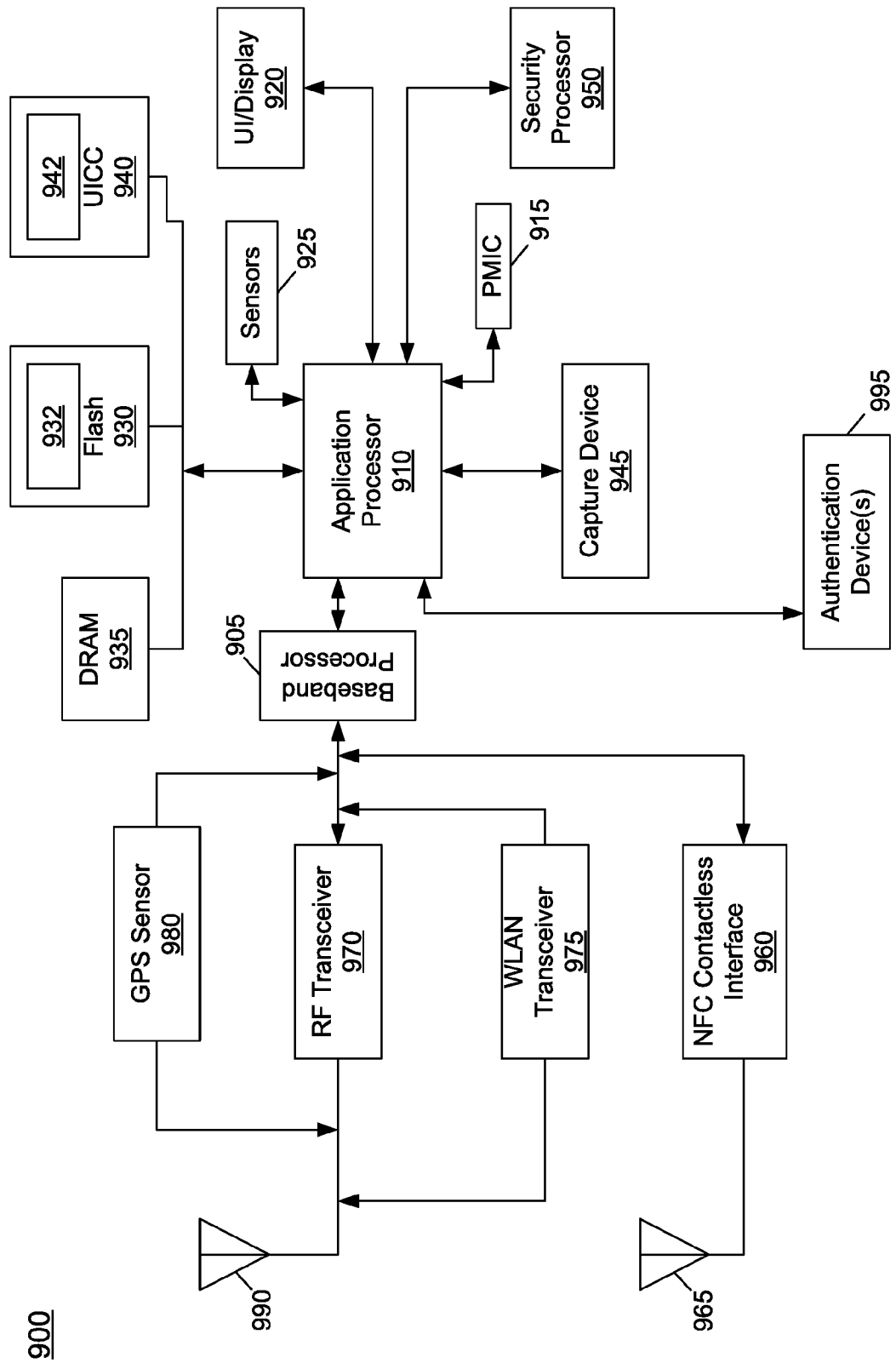


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000378**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/768(2006.01)i, H01L 21/60(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/768; H01L 23/52; H01L 21/302; H01L 21/4763; H01L 29/40; H01L 21/3205; H01L 21/44; H01L 21/48; H01L 21/461; H01L 21/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: interconnect, liner, sidewall, metal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001-0000632 A1 (SHUNICHI YOSHIKAWA) 03 May 2001 See abstract, paragraphs [0005], [0020]-[0043] and figures 1A-2E.	1-8, 13, 17-19, 21-25
Y		9-12, 15-16, 20
A		14
Y	KR 10-2004-0106704 A (SAMSUNG ELECTRONICS CO., LTD.) 18 December 2004 See abstract, page 3 and figures 2a-2e.	9-11, 20
Y	JP 2011-134885 A (PANASONIC CORP.) 07 July 2011 See abstract, paragraphs [0037]-[0042] and figure 1.	12, 15-16
A	US 5427981 A (KYEONG K. CHOI) 27 June 1995 See abstract, column 2, line 49 - column 3, line 44 and figures 2A-2F.	1-25
A	US 6114243 A (SUBHASH GUPTA et al.) 05 September 2000 See abstract, column 3, line 3 - column 4, line 45 and figures 2-10.	1-25
A	US 2003-0119317 A1 (TAKESHI NOGAMI et al.) 26 June 2003 See abstract, paragraphs [0014]-[0030] and figures 1-2F.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 October 2016 (12.10.2016)

Date of mailing of the international search report

12 October 2016 (12.10.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/000378

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