

(51) International Patent Classification:
G05F 1/10 (2006.01)(21) International Application Number:
PCT/US2011/024751(22) International Filing Date:
14 February 2011 (14.02.2011)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/306,822 22 February 2010 (22.02.2010) US
61/306,796 22 February 2010 (22.02.2010) US
61/355,952 17 June 2010 (17.06.2010) US(71) Applicant (for all designated States except US): **MARVELL WORLD TRADE LTD** [BB/BB]; L'Horizon,
Gunsite Road, Brittons Hill, St. Michael, BB14027 (BB).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **VERMA, Ashutosh** [IN/US]; 1700 Halford Ave., Apt 227, Santa Clara, California 95051 (US). **JAMAL, Shafiq** [US/US]; 1575 Eagles Nest Lane, Gilroy, California 95020 (US). **CHO, Thomas B.** [US/US]; 111 Obispo Ct., Fremont, California 94539 (US). **SUTARDJA, Sehat** [US/US]; 27330 Elena Road, Los Altos Hills, California 94022 (US).(74) Agent: **YOUNG, Brian N.**; 900 Lafayette St., Ste. 301, Santa Clara, California 95050 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD,

[Continued on next page]

(54) Title: DUAL OUTPUT DIRECT CURRENT (DC)-DC REGULATOR

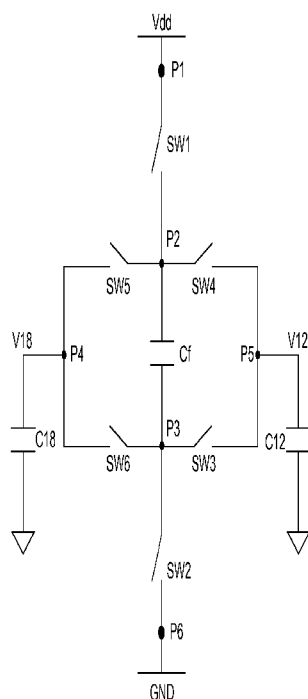


Fig. 1

(57) Abstract: An apparatus includes a first switch coupled to a first voltage reference and a second switch coupled to a second voltage reference. A third switch is coupled to a first terminal of a first capacitor and a first terminal of a second capacitor. A fourth switch is coupled to a second terminal of the first capacitor and the first terminal of the second capacitor. A fifth switch is coupled to the second terminal of the first capacitor and a first terminal of a third capacitor. A sixth switch is coupled to the first terminal of the first capacitor and the first terminal of the third capacitor. The first switch, the second switch, the third switch, the fourth switch, the fifth switch, and the sixth switch are controlled to maintain a first voltage level at a first output and a second voltage level at a second output.



SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR,
TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG,
ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,

EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

Dual Output Direct Current (DC)-DC Regulator

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims priority to U.S. Provisional App. No. 61/306,796 for “Dual Flycap Dual Output DC-DC Regulator” filed February 22, 2010; U.S. Provisional App. No. 61/306,822 for “Dual Output DC-DC Regulator” filed February 22, 2010; and U.S. Provisional App. No. 61/355,952 for “Dual Output DC-DC Switched Capacitor Regulator” filed June 17, 2010, all of which are incorporated herein by reference in their entirety for all purposes.

BACKGROUND

10 [0002] Particular embodiments generally relate to a dual output direct current (DC)-to-DC regulator.

[0003] Unless otherwise indicated herein, the approaches described in this section are not prior art to the claims in this application and are not admitted to be prior art by inclusion in this section.

15 [0004] A charge pump is a DC-to-DC converter that uses capacitors to create either a higher or lower voltage output. Charge pumps use switches to control different connections for the capacitors. For example, in a first phase, a flying capacitor is connected to a voltage supply to charge the flying capacitor. In a second phase, the flying capacitor is disconnected from the voltage supply and connected to a second capacitor at an output. Charge then flows
20 from the flying capacitor to the second capacitor, which increases the voltage across the second capacitor. The above process between the first phase and the second phase continues at a pre-determined frequency. The process regulates the output voltage across the second capacitor to maintain the output voltage a desired level.

[0005] The charge pump regulates the output voltage at a single output. However, if
25 multiple outputs are required, then an additional flying capacitor, an additional output capacitor, and an additional set of switches are needed to regulate the second output. This may be an inefficient use of integrated circuit (IC) chip area.

SUMMARY

[0006] In one embodiment, an apparatus includes a first switch coupled to a first voltage reference and a second switch coupled to a second voltage reference. A third switch is coupled to a first terminal of a first capacitor and a first terminal of a second capacitor. A fourth switch is coupled to a second terminal of the first capacitor and the first terminal of the second capacitor. A fifth switch is coupled to the second terminal of the first capacitor and a first terminal of a third capacitor. A sixth switch is coupled to the first terminal of the first capacitor and the first terminal of the third capacitor. The first switch, the second switch, the third switch, the fourth switch, the fifth switch, and the sixth switch are controlled to maintain a first voltage level at a first output and a second voltage level at a second output.

[0007] In one embodiment, the apparatus includes a seventh switch coupled to the first voltage reference and an eighth switch coupled to the second voltage reference. A ninth switch is coupled to a first terminal of a fifth capacitor and the first terminal of the second capacitor. A tenth switch is coupled to a second terminal of the fifth capacitor and the first terminal of the second capacitor. An eleventh switch is coupled to the second terminal of the fifth capacitor and the first terminal of the third capacitor. A twelfth switch is coupled to the first terminal of the fifth capacitor and the first terminal of the third capacitor.

[0008] In one embodiment, a system includes the first reference voltage; the second reference voltage; the first capacitor; the second capacitor; and the third capacitor.

[0009] In one embodiment, a method includes: coupling a first switch coupled to a first voltage reference; coupling a second switch coupled to a second voltage reference; coupling a third switch coupled to a first terminal of a first capacitor and a first terminal of a second capacitor; coupling a fourth switch coupled to a second terminal of the first capacitor and the first terminal of the second capacitor; coupling a fifth switch coupled to the second terminal of the first capacitor and a first terminal of a third capacitor; coupling a sixth switch coupled to the first terminal of the first capacitor and the first terminal of the third capacitor, and controlling the first switch, the second switch, the third switch, the fourth switch, the fifth switch, and the sixth switch to maintain a first voltage level at a first output and a second voltage level at a second output.

[0010] The following detailed description and accompanying drawings provide a more detailed understanding of the nature and advantages of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Fig. 1 depicts an example of a regulator according to one embodiment.

[0012] Fig. 2a depicts a first case in the switching scheme according to one embodiment.

5 [0013] Fig. 2b depicts a second case for the switching scheme according to one embodiment.

[0014] Fig. 2c depicts a third case in the switching scheme according to one embodiment.

[0015] Fig. 2d depicts a fourth case of the switching scheme according to one embodiment.

[0016] Fig. 3a depicts an example of a critical path according to one embodiment.

[0017] Fig. 3b depicts the resistances in the critical path according to one embodiment.

10 [0018] Fig. 4 depicts an example of a regulator using dual flying capacitors according to one embodiment.

[0019] Fig. 5a depicts an example of using dual flying capacitors Cf1 and Cf2 in the first case of the switching scheme according to one embodiment.

15 [0020] Fig. 5b depicts a second case using dual flying capacitors according to one embodiment.

[0021] Fig. 5c depicts a third case using dual flying capacitors according to one embodiment.

[0022] Fig. 6 depicts a method for maintaining a first voltage level at a first output and a second voltage level at a second output according to one embodiment.

20

DETAILED DESCRIPTION

[0023] Described herein are techniques for a regulator. In the following description, for purposes of explanation, numerous examples and specific details are set forth in order to
25 provide a thorough understanding of embodiments of the present invention. Particular embodiments as defined by the claims may include some or all of the features in these

examples alone or in combination with other features described below, and may further include modifications and equivalents of the features and concepts described herein.

Single Flying Capacitor

[0024] Fig. 1 depicts an example of a regulator 100 according to one embodiment.

5 Regulator 100 maintains output voltages at dual outputs (e.g. output V12 and output V18). A switched capacitor design transfers charge among a flying capacitor (Cf), a first output capacitor (C12), and a second output capacitor (C18). In one example, output V12 is maintained substantially at 1.2 volts, output V18 is maintained substantially at 1.8 volts, and a voltage reference Vdd is at 3.3 volts. Although these voltages are described, other voltages
10 may be used.

[0025] In one embodiment, an IC chip includes switches SW1-SW6. Voltage reference Vdd, voltage reference GND, and capacitors Cf, C12, and C18 are located off chip. In regulator 100, multiple switches, such as switches SW1, SW2, SW3, SW4, SW5, and SW6, are controlled in different switching schemes. Switch SW1 couples reference voltage Vdd to
15 flying capacitor Cf through pins P1 and P2 of the chip. Switch SW2 couples flying capacitor Cf to a second reference voltage, such as ground (GND), through pins P3 and P6. Switch SW3 couples capacitor C12 to a first terminal of flying capacitor Cf through pins P3 and P5. Switch SW4 couples capacitor C12 to a second terminal of flying capacitor Cf through pins P2 and P5. Also, switch SW5 and switch SW6 couple capacitor C18 to the second terminal
20 (through pins P4 and P2) and the first terminal (through pins P4 and P3) of flying capacitor Cf, respectively. Capacitors C12 and C18 are also coupled to ground.

[0026] A switching scheme is performed based on the output voltages at outputs V12 and V18. Each case may include two phases that are switched between according to a reference signal. The switching scheme that is used may be determined based on voltages at outputs
25 V12 and V18 and couple capacitors Cf, C12, and C18 in different paths. A high efficiency is provided and a total resistance of a critical path is less than total resistance restrictions due to characteristics of a layout for the design.

[0027] Fig. 2a depicts a first case in the switching scheme according to one embodiment. The first case may be used when the following high and low voltages for outputs V12 and
30 V18 are found:

V12H < 1.2;

V18H < 1.8;

V12L > 1.15; and

V18L > 1.75,

wherein H denotes the high voltage measured and L denotes the low voltage measured at
 5 outputs V12 or V18. In this case, both the high voltages at outputs V12 and V18 are below
 the desired levels. Thus, the switching scheme attempts to increase the voltages at outputs
 V12 and V18 to maintain them at 1.2 volts and 1.8 volts, respectively.

[0028] In phase 1 (ϕ_1), switches SW1 and SW6 are closed and switches SW2, SW3, SW4,
 and SW5 are open. This couples the second terminal of the flying capacitor Cf to the
 10 reference voltage Vdd and the first terminal of the flying capacitor Cf to output V18. Also,
 capacitor C12 is coupled to output V12.

[0029] The voltage at the second terminal of flying capacitor Cf will be $V_{dd} - V_{18} = 1.5$
 volts. The voltage across flying capacitor Cf starts at 1.2 volts (the starting voltage across
 flying capacitor Cf is from phase 2, which is described below). Thus, there is a voltage
 15 difference ΔV of .3 volts. If capacitor C18 is of a sufficiently large size, then the voltage
 across capacitor C18 remains at 1.8 volts. The current used to charge flying capacitor Cf to
 the voltage of $V_{dd} - V_{18}$ then flows to a load coupled to output V18, which increases the
 voltage at the load (and output V18).

[0030] In phase 2 (ϕ_2), switches SW2 and SW4 are closed and switches SW1, SW3, SW5,
 20 and SW6 are open. Capacitor C18 is coupled to the load at output V18. Also, flying
 capacitor Cf is coupled to capacitor C12. The voltage at the second terminal of flying
 capacitor Cf is $V_{dd} - V_{18}$. If the voltage $V_{dd} - V_{18}$ is greater than the voltage across
 capacitor C12, which is less than 1.2 volts, then charge flows from flying capacitor Cf to
 capacitor C12. Flying capacitor Cf and capacitor C12 will eventually equal the same charge.
 25 For example, if the voltage across flying capacitor Cf is $3.3 - 1.8 = 1.5$ volts, then a voltage
 difference ΔV of .3 volts may be used to charge capacitor C12. This may be enough voltage
 to charge capacitor C12 to the desired level of 1.2 volts. The frequency of the switching
 scheme may switch back to phase 1 at a time around when capacitor C12 is charged to 1.2
 volts.

[0031] The voltages across capacitors Cf, C12, and C18 do not change significantly between phase 1 and phase 2. Thus, the efficiency of regulator 100 is high, such as around 91%. Additionally, both outputs V12 and V18 are charged using flying capacitor Cf and switches SW1-SW6. For example, in phase 1, output V18 is charged, and in phase 2, output V12 is charged.

[0032] Fig. 2b depicts a second case for the switching scheme according to one embodiment. The second case may be used when the following high and low voltages for outputs V12 and V18 are found:

V12H > 1.2;
V18H < 1.8; and
either V18L < 1.75; or
V12L < 1.15.

[0033] In one embodiment, in phase 1, the switches are controlled such that the voltage at output V18 is increased. For example, switches SW3 and SW5 are closed while switches SW1, SW2, SW4 and SW6 are open. This couples capacitor C12 to the first terminal of flying capacitor Cf and to the output V12. Also, capacitor C18 is coupled to the second terminal of flying capacitor Cf and output V18.

[0034] The charge across flying capacitor Cf may be $V_{dd} - V18 = 1.5$ volts. In this case, charge flows to capacitor C18, which is below 1.8 volts. This increases the voltage at output V18.

[0035] Different configurations may be used in phase 2. For example, in phase 2a, switches SW1 and SW6 are closed while switches SW2, SW3, SW4, and SW 5 are open. This circuit configuration is the same as discussed with respect to phase 1 in the first case in Fig. 2a. In this case, flying capacitor Cf is charged and current flows to the load at output V18. This increases the voltage at output V18. Accordingly, the voltage at output V18 is increased in both phases.

[0036] In another embodiment, instead of charging flying capacitor Cf using the configuration in phase 2a, capacitor C12 may be used to charge flying capacitor Cf in a phase 2b. For example, if the voltage across capacitor C12 is greater than 1.2 volts, then the charge from capacitor C12 may be used to charge flying capacitor Cf. However, if the low voltage at output V12 is $V12L < 1.15$, then the configuration shown in phase 2a of Fig. 2a may be used

because the low voltage across capacitor C12 is less than 1.2 volts and it may not be desirable to use capacitor C12 to charge flying capacitor Cf.

[0037] In phase 2b, switches SW2 and SW4 are closed while switches SW1, SW3, SW5, and SW6 are open. The second terminal of flying capacitor Cf is coupled to capacitor C12 at output V12. Also, capacitor C18 is coupled to output V18. The charge from capacitor C12 charges flying capacitor Cf.

[0038] Fig. 2c depicts a third case in the switching scheme according to one embodiment. The third case may be used when the following high and low voltages for outputs V12 and V18 are found:

10 V12H < 1.2;
V18H > 1.8; and
either V18L < 1.75; or
V12L < 1.15.

[0039] In the third case, the high voltage at output V18 is greater than 1.8 and the high voltage at output V12 is less than 1.2 volts. The low voltage for output V18 may be less than 1.75 or the low voltage at output V12 may be less than 1.15 volts. The switching scheme attempts to increase the voltage at output V12. In a phase 1a of the third case, the switches are controlled such that the voltage at output V12 is increased. For example, in phase 1a, switches SW1 and SW3 are closed and switches SW2, SW4, SW5, and SW6 are open. This couples capacitor C18 to output V18. Also, the second terminal of flying capacitor Cf is coupled to voltage reference Vdd. The first terminal of flying capacitor Cf is coupled to capacitor C12 and output V12. This configuration is similar to phase 1 of the first case in Fig. 2a except that flying capacitor Cf is coupled to capacitor C12 instead of capacitor C18.

[0040] The voltage at the second terminal of flying capacitor Cf will be $V_{dd} - V_{12} = 2.1$ volts. The voltage across capacitor Cf is 1.2 volts. Thus, there is a voltage difference ΔV of .9 volts. If capacitor C12 is of a sufficiently large size, then the voltage across capacitor C12 remains at 1.2 volts. The current used to charge flying capacitor Cf to the voltage of $V_{dd} - V_{12}$ then flows to a load coupled to output V12, which increases the voltage at the load (and output V12).

[0041] Other configurations may also be used to charge capacitor Cf, such as a charge across capacitor C18 may be used to charge capacitor Cf as shown in phase 1b. However, if

the low voltage for output V18 is less than 1.75, then it may not be desirable to use the charge from capacitor C18 to charge capacitor Cf. In phase 1b, switches SW2 and SW5 are closed and switches SW1, SW3, SW4, and SW6 are open. This couples capacitor C18 to the second terminal of flying capacitor Cf. The charge across capacitor C18 charges flying capacitor Cf.

5 **[0042]** In phase 2, capacitor C18 continues to be coupled to output V18; however, switches SW2 and SW4 are closed while switches SW1, SW3, SW5, and SW6 are open. This couples the second terminal of flying capacitor Cf to output V12 and capacitor C12. The voltage across flying capacitor Cf is $V_{dd} - V_{12}$, and charge flows from flying capacitor Cf to capacitor C12 because this voltage is greater than the voltage across capacitor C12. For
10 example, the voltage across flying capacitor Cf may be 2.1 volts. As charge transfers from flying capacitor Cf to capacitor C12, the voltage at output V12 is increased. The frequency of the switching scheme may switch back to phase 1 at a time around when capacitor C12 is charged to 1.2 volts.

[0043] Fig. 2d depicts a fourth case of the switching scheme according to one embodiment.
15 The fourth case may be used when the following voltages for outputs V12 and V18 are found:

$$V_{12H} \geq 1.2;$$

$$V_{18H} \geq 1.8;$$

In this case, the voltages at output V12 and output V18 are substantially equal to or slightly
20 above 1.2 and 1.8 volts, respectively. Accordingly, in phase 1 and phase 2, switch SW2 is closed and switches SW1, SW3, SW4, SW5, and SW6 are open. Capacitor C18 is coupled to output V18 and capacitor C12 is coupled to output V12. Flying capacitor is floating. This leaves regulator 100 in a steady state in which the voltages and outputs V12 and V18 are maintained.

25 **[0044]** The above switching schemes are efficient. The efficiency may be a measure of transferring charge from a source to a load, such as from a capacitor to a capacitor coupled to the output. The efficiencies may be high because the amount of charge transferred is low. The efficiency for the first case may be around 91%, the efficiency for the second case around 72.8%, and the efficiency for the third case around 72.8%. These efficiencies may be
30 higher than the conventional charge pump. For a combined efficiency, each case may be multiplied by their expected occurrence and the outcomes added.

[0045] Depending on the design of regulator 100, there may be restrictions with regard to a total resistance within a path in a layout of the IC chip during a switching scheme. For example, for phase 1 of the first case, there is a voltage difference ΔV of .3 volts - 3.3V - 1.8V - 1.2V ($V_{dd} - V_{18} - V_{12}$). Because the voltage difference ΔV is .3 volts, if the total resistance in the path is too high, then the time it takes to charge flying capacitor C_f may become too long or take too many time constants. Assuming the following conditions of a load current (I_L) = 100 mA and a minimum voltage difference (ΔV) = .3 volts, the following resistance total (R_{TOTAL}) may be determined using the following equations:

$$I_L = C_f \times \Delta V \times f_{osc}$$

$$R_{TOTAL} C_f = 1 / 2n f_{osc}$$

$$R_{TOTAL} = 1 / (2n f_{osc} C_f)$$

$$R_{TOTAL} = \frac{\Delta V}{2n * I_L}$$

wherein I_L is a current through the load, C_f is the capacitance of the flying capacitor, f_{osc} is the frequency of the output signal, and n is the number of time constants.

[0046] This provides a resistance total that is $R_{TOTAL} = 03.75$ ohms for four time constants. Four time constants may be desirable because flying capacitor C_f may be charged to 98% of the desired voltage.

[0047] The total resistance takes into account the resistance of switches, metal wires, bond wires, and equivalent series resistance (ESR) of capacitors in the path. Fig. 3a depicts an example of a critical path 302 according to one embodiment. Critical path 302 couples reference voltage V_{dd} to flying capacitor C_f and capacitor C_{18} . The resistances for switches SW1 and SW6, the bond wires, and the ESR of flying capacitor C_f and capacitor C_{18} are in the path. The bond wires are wires that couple from the IC chip to external components. For example, bond wires are needed to couple switch SW1 to reference voltage V_{dd} , a pin P1 to voltage reference V_{dd} , pins P2 and P3 to flying capacitor C_f , and pin P4 to capacitor C_{18} .

[0048] Fig. 3b depicts the resistances in the critical path according to one embodiment. As shown, the resistances for the bond wire to reference voltage V_{dd} (3.3V Bond Wire), switch

SW1 (SW1 Ron), bond wire from pin P2 to flying capacitor Cf (Cf IN Bond Wire), and the ESR resistance for flying capacitor Cf (Cf ESR) are shown. After flying capacitor Cf, resistances for the bond wire from capacitor Cf to pin P3 (Cf OUT Bond Wire), switch SW6 (SW6 Ron), the bond wire from switch SW6 to capacitor C18 (1.8V Bond Wire), and the

5 ESR resistance for capacitor C18 (C18 ESR) are shown. Using a double bond or triple bond wire connection, the total resistance may be below the R_{TOTAL} calculated above of .375 ohms. The resistance may be minimized by maximizing the area of switches SW1 and SW6 and also minimizing the length of the bond wires.

Dual Flying Capacitor

10 [0049] Particular embodiments may use a dual flying capacitor with two outputs. The dual flying capacitors may be used because of the small ΔV in phase 1 of Fig. 2a. If the output current is higher than 100 mA, such as 200 mA, then the total resistance R_{TOTAL} for a path may be lower than desired. The total resistance may be $R = \Delta V / (2 * n * I_a)$, wherein n is a number of time constants and I_a is an output current. The total resistance depends on the

15 voltage difference ΔV and the output current I_a . The output current I_a may be the output current at voltages V18 or V12. If the output current increases, then the total resistance allowed for a path goes down. Also, if Vdd is lower than 3.3V, such as at 3.1V, then the total resistance allowed for a path also goes down. With two switches and four bond wires in a critical path, having a smaller switch resistance may cause design difficulties. Thus,

20 increasing the voltage difference ΔV may be beneficial.

[0050] Fig. 4 depicts an example of a regulator 400 using dual flying capacitors according to one embodiment. The switches of Fig. 1 may be duplicated for two flying capacitors Cf1 and Cf2. For example, flying capacitor Cf1, switches SW1A-SW6A, capacitor C12 and capacitor C18 are similar to the circuit shown in Fig. 1. An additional set of switches SW1B-

25 SW6B and extra pins P7 and P8 are also needed in the chip. Flying capacitor Cf2 is located off chip and coupled to the chip through pins P7 and P8.

[0051] An additional switch SW7 is used when flying capacitors Cf1 and Cf2 are coupled in series. In this case, the second terminal of flying capacitor Cf1 is coupled to the first terminal of capacitor Cf2 via switch SW7. When flying capacitors Cf1 and Cf2 are coupled

30 in parallel, then the corresponding A and B switches are closed, such as if the second terminal

of flying capacitor Cf1 should be coupled to capacitor C18, then switches SW5A and SW5B are closed to couple flying capacitors Cf1 and Cf2 to capacitor C18.

[0052] Fig. 5a depicts an example of using dual flying capacitors Cf1 and Cf2 in the first case of the switching scheme according to one embodiment. In this case, flying capacitor Cf in Fig. 2a is replaced by flying capacitors Cf1 and Cf2. For example, the second terminal for flying capacitors Cf1 and Cf2 are coupled to reference voltage Vdd and the first terminal of flying capacitors Cf1 and Cf2 are coupled to capacitor C18 and output V18.

[0053] The voltage at output V18 is 1.8 volts. As will be described in more detail below, the voltage across flying capacitors Cf1 and Cf2 is .6 volts each. Thus, the voltage at the second terminal of flying capacitors Cf1 and Cf2 is 2.4 volts ($V_{dd} + 0.6V$). A voltage difference ΔV of .7 volts is provided ($V_{dd} - V_{18} - .5 * V_{12} = 3.1V - 1.8V - .6V = .7V$).

[0054] In phase 2, capacitor C12 is coupled to flying capacitors Cf2 and Cf1. The voltage across flying capacitors Cf2 and Cf1 is $V_{dd} - V_{18}$ volts and is transferred to capacitor C12 until the charge across both flying capacitors Cf1 and Cf2 is 1.2 volts. Thus, the charge is .6 volts across each flying capacitor Cf1 and Cf2.

[0055] By having a larger ΔV , the resistance $R_{TOTAL} = \Delta V / (2 * n * I_a) = 438$ milliohms for four time constants. This gives a larger margin for switch sizes, bond wire resistance, and capacitor ESR, if the output current is larger or the reference voltage Vdd is smaller.

[0056] Fig. 5b depicts a second case using dual flying capacitors according to one embodiment. As shown in phase 1, flying capacitor Cf is replaced by flying capacitors Cf1 and Cf2. In phase 2a, flying capacitor Cf is replaced by flying capacitors Cf1 and Cf2. In phase 1, the operation is similar as discussed with respect to Fig. 2b, except the voltage across flying capacitor Cf is split between flying capacitors Cf1 and Cf2. However, in phase 2a, the ΔV is greater because the voltage across flying capacitors Cf1 and Cf2 is split between them. In phase 2b, the operation is similar to that described with respect to phase 2 of fig. 5a.

[0057] Fig. 5c depicts a third case using dual flying capacitors according to one embodiment. In phase 1, a circuit is similar to phase 1a in Fig. 5a except that flying capacitors Cf1 and Cf2 have their second terminal coupled to reference voltage Vdd and their first terminal coupled to capacitor C12 and output voltage V12. In this case, the voltage difference ΔV is increased because the voltage across flying capacitor Cf is split between

5 flying capacitors Cf1 and Cf2. In phase 1b, the flying capacitor Cf is replaced by flying capacitors Cf1 and Cf2 in series. Charge is transferred from capacitor C18 to flying capacitors Cf1 and Cf2. Also, in phase 2, flying capacitor Cf is replaced by flying capacitors Cf1 and Cf2 in series, which is similar to that shown in phase 2 of Fig. 5a. In this case, charge across flying capacitors Cf1 and Cf2 is transferred to capacitor C12.

[0058] In the fourth case, flying capacitors Cf1 and Cf2 are floating and thus the operation is the same as described with respect to Fig. 2b.

10 [0059] Fig. 6 depicts a method for maintaining a first voltage level at a first output and a second voltage level at a second output according to one embodiment. At 602, regulator 100 couples a first switch coupled to a first voltage reference. At 604, regulator 100 couples a second switch coupled to a second voltage reference.

15 [0060] At 606, regulator 100 couples a third switch coupled to a first terminal of a first capacitor and a first terminal of a second capacitor. At 608, regulator 100 couples a fourth switch coupled to a second terminal of the first capacitor and the first terminal of the second capacitor. At 610, regulator 100 couples a fifth switch coupled to the second terminal of the first capacitor and a first terminal of a third capacitor. At 612, regulator 100 couples a sixth switch coupled to the first terminal of the first capacitor and the first terminal of the third capacitor.

20 [0061] At 614, regulator 100 controls the first switch, the second switch, the third switch, the fourth switch, the fifth switch, and the sixth switch to maintain a first voltage level at a first output and a second voltage level at a second output.

25 [0062] As used in the description herein and throughout the claims that follow, “a”, “an”, and “the” includes plural references unless the context clearly dictates otherwise. Also, as used in the description herein and throughout the claims that follow, the meaning of “in” includes “in” and “on” unless the context clearly dictates otherwise.

30 [0063] The above description illustrates various embodiments of the present invention along with examples of how aspects of the present invention may be implemented. The above examples and embodiments should not be deemed to be the only embodiments, and are presented to illustrate the flexibility and advantages of the present invention as defined by the following claims. Based on the above disclosure and the following claims, other

arrangements, embodiments, implementations and equivalents may be employed without departing from the scope of the invention as defined by the claims.

WHAT IS CLAIMED IS:

1 1. An apparatus comprising:
2 a first switch coupled to a first voltage reference;
3 a second switch coupled to a second voltage reference;
4 a third switch coupled to a first terminal of a first capacitor and a first terminal
5 of a second capacitor;
6 a fourth switch coupled to a second terminal of the first capacitor and the first
7 terminal of the second capacitor;
8 a fifth switch coupled to the second terminal of the first capacitor and a first
9 terminal of a third capacitor; and
10 a sixth switch coupled to the first terminal of the first capacitor and the first
11 terminal of the third capacitor,
12 wherein the first switch, the second switch, the third switch, the fourth switch,
13 the fifth switch, and the sixth switch are controlled to maintain a first voltage level at a first
14 output and a second voltage level at a second output.

1 2. The apparatus of claim 1, wherein:
2 the first switch and the sixth switch are closed to couple the first terminal of
3 the first capacitor to the first terminal of the third capacitor,
4 the second switch, the third switch, the fourth switch, and the fifth switch are
5 open, and
6 the second voltage level at the second output is increased.

1 3. The apparatus of claim 2, further comprising a fourth capacitor
2 coupled to the first reference voltage and the first terminal of the third capacitor.

1 4. The apparatus of claim 2, wherein:
2 the second switch and the fourth switch are closed to couple the second
3 terminal of the first capacitor to the first terminal of the second capacitor,
4 the first switch, the third switch, the fifth switch, and the sixth switch are open,
5 and
6 the first voltage level at the first output is increased.

1 5. The apparatus of claim 4, further comprising a fifth capacitor coupled
2 to the second terminal of the first capacitor and the first terminal of the second capacitor.

1 6. The apparatus of claim 1, wherein:
2 the third switch and the fifth switch are closed to (i) couple the first terminal
3 of the first capacitor to the first terminal of the second capacitor and (ii) couple the second
4 terminal of the first capacitor to the first terminal of the third capacitor,
5 the first switch, the second switch, the fourth switch, and the sixth switch are
6 open, and
7 the second voltage level at the second output is increased.

1 7. The apparatus of claim 6, wherein:
2 the first switch and the sixth switch are closed to couple the first terminal of
3 the first capacitor to the first terminal of the third capacitor,
4 the second switch, the third switch, the fourth switch, and the fifth switch are
5 open, and
6 the second voltage level at the second output is increased.

1 8. The apparatus of claim 6, wherein:
2 the second switch and the fourth switch are closed to couple the second
3 terminal of the first capacitor to the first terminal of the second capacitor,
4 the first switch, the third switch, the fifth switch, and the sixth switch are open,
5 and
6 the first voltage level at the first output is increased.

1 9. The apparatus of claim 1, wherein:
2 the first switch and the third switch are closed to couple the second terminal of
3 the first capacitor to the first voltage reference and the first terminal of the first capacitor to
4 the first terminal of the second capacitor,
5 the second switch, the fourth switch, the fifth switch, and the sixth switch are
6 open, and
7 the first voltage level at the first output is increased.

1 10. The apparatus of claim 9, wherein:

2 the second switch and the fourth switch are closed to couple the second
3 terminal of the first capacitor to the first terminal of the second capacitor,
4 the first switch, the third switch, the fifth switch, and the sixth switch are open,
5 and
6 the first voltage level at the first output is increased.

1 11. The apparatus of claim 1, wherein:
2 the first switch and the fifth switch are closed to couple the second terminal of
3 the first capacitor to the first terminal of the third capacitor,
4 the second switch, the third switch, the fourth switch, and the sixth switch are
5 open, and
6 the second voltage level at the second output is decreased.

1 12. The apparatus of claim 1, wherein the first switch, the second switch,
2 the third switch, the fourth switch, the fifth switch, and the sixth switch are open to maintain
3 the first voltage level and the second voltage level.

1 13. The apparatus of claim 1, further comprising:
2 a seventh switch coupled to the first voltage reference;
3 an eighth switch coupled to the second voltage reference;
4 a ninth switch coupled to a first terminal of a fifth capacitor and the first
5 terminal of the second capacitor;
6 a tenth switch coupled to a second terminal of the fifth capacitor and the first
7 terminal of the second capacitor;
8 an eleventh switch coupled to the second terminal of the fifth capacitor and the
9 first terminal of the third capacitor; and
10 a twelfth switch coupled to the first terminal of the fifth capacitor and the first
11 terminal of the third capacitor.

1 14. The apparatus of claim 1, further comprising a thirteen switch coupling
2 the second terminal of the first capacitor with the first terminal of the fifth capacitor.

1 15. The apparatus of claim 14, wherein:
2 the first switch and the sixth switch are closed to couple the first terminal of
3 the first capacitor to the first terminal of the third capacitor,

the second switch, the third switch, the fourth switch, and the fifth switch are open, wherein the second voltage level at the second output is increased.

the seventh switch and the twelfth switch are closed to couple the first terminal of the fifth capacitor to the first terminal of the third capacitor, the eighth switch, the ninth switch, the tenth switch, and the eleventh switch are open, and

the second voltage level at the second output is increased.

16. The apparatus of claim 14, wherein the thirteen switch is closed to couple the second terminal of the first capacitor to the first terminal of the fifth capacitor, wherein the first voltage level at the first output is increased

17. A system comprising the apparatus of claim 1, the system further comprising:

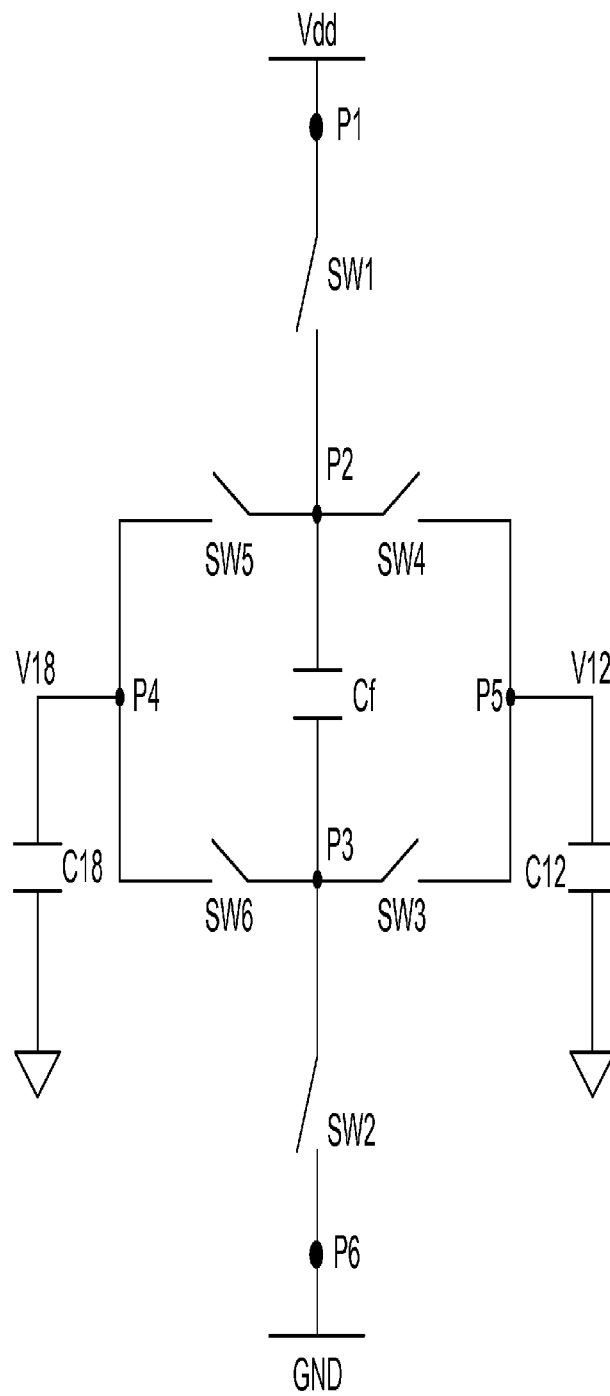
the first reference voltage;
the second reference voltage;
the first capacitor;
the second capacitor; and
the third capacitor.

18. A method comprising:
coupling a first switch coupled to a first voltage reference;
coupling a second switch coupled to a second voltage reference;
coupling a third switch coupled to a first terminal of a first capacitor and a first terminal of a second capacitor;
coupling a fourth switch coupled to a second terminal of the first capacitor and the first terminal of the second capacitor;
coupling a fifth switch coupled to the second terminal of the first capacitor and a first terminal of a third capacitor;
coupling a sixth switch coupled to the first terminal of the first capacitor and the first terminal of the third capacitor; and

12 controlling the first switch, the second switch, the third switch, the fourth
13 switch, the fifth switch, and the sixth switch to maintain a first voltage level at a first output
14 and a second voltage level at a second output.

1 19. The method of claim 18, further comprising:
2 closing the first switch and the sixth switch to couple the first terminal of the
3 first capacitor to the first terminal of the third capacitor; and
4 opening the second switch, the third switch, the fourth switch, and the fifth
5 switch, wherein the second voltage level at the second output is increased.

1 20. The method of claim 18, further comprising:
2 closing the second switch and the fourth switch to couple the first terminal of
3 the first capacitor to the first terminal of the second capacitor; and
4 opening the first switch, the third switch, the fifth switch, and the sixth switch,
5 wherein the first voltage level at the first output is increased.

100**Fig. 1**

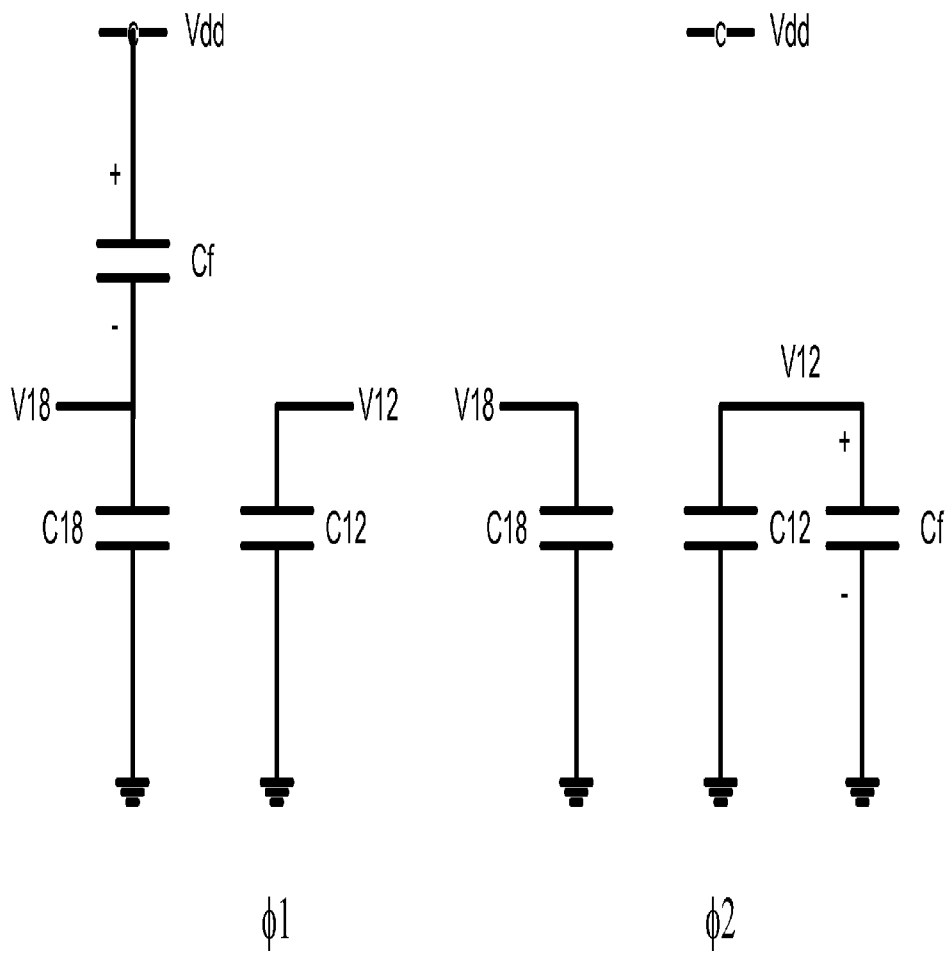


Fig. 2a

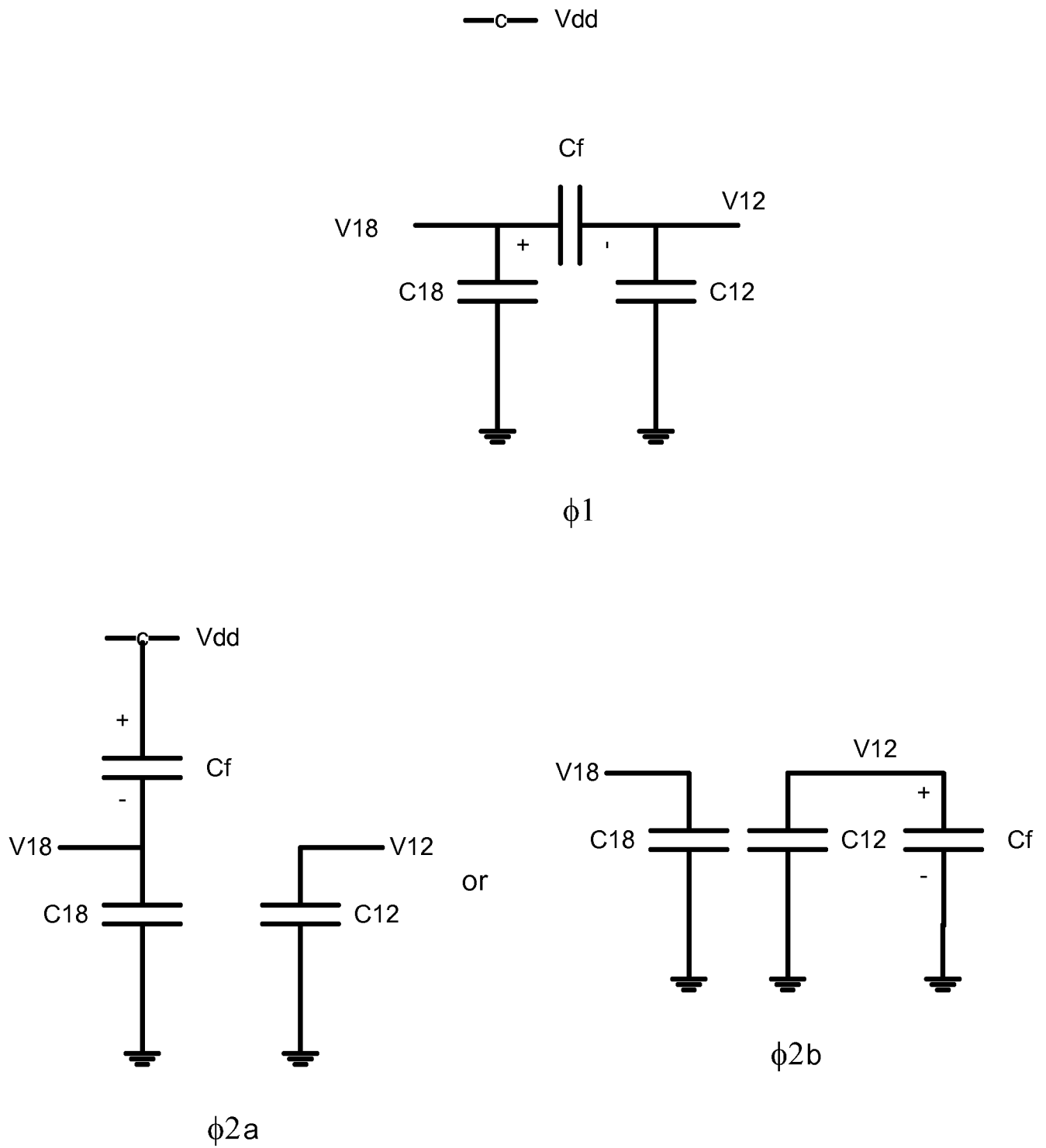


Fig. 2b

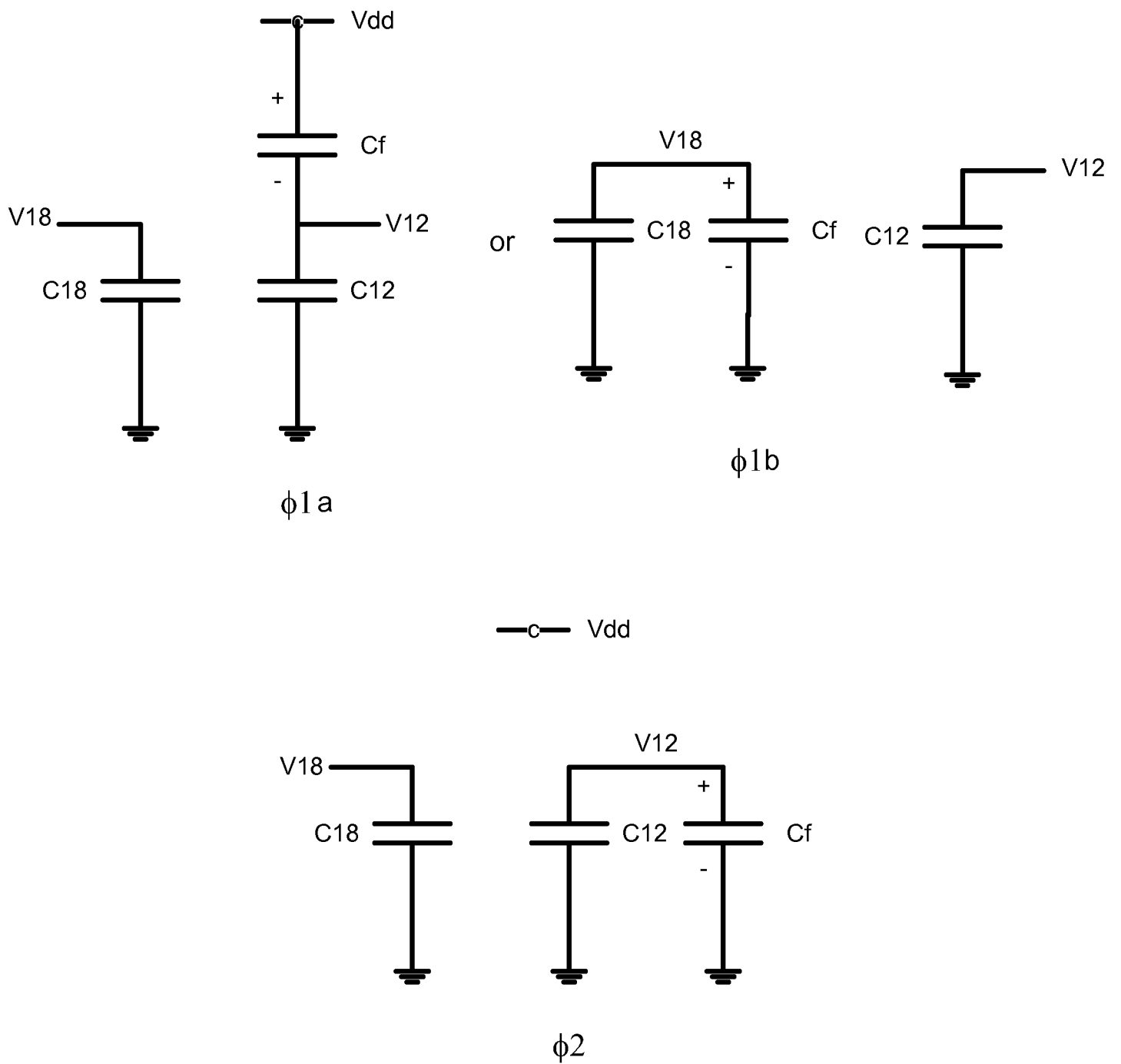


Fig. 2c

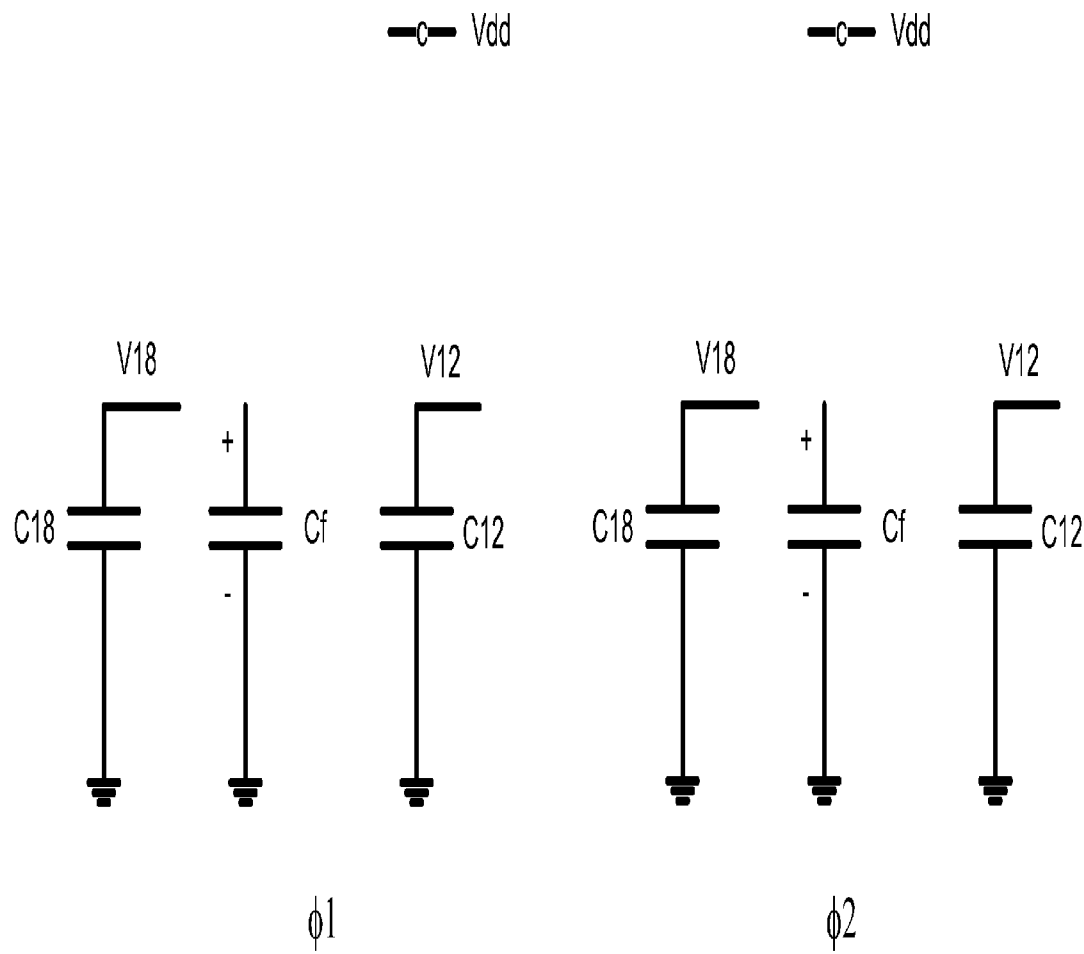


Fig. 2d

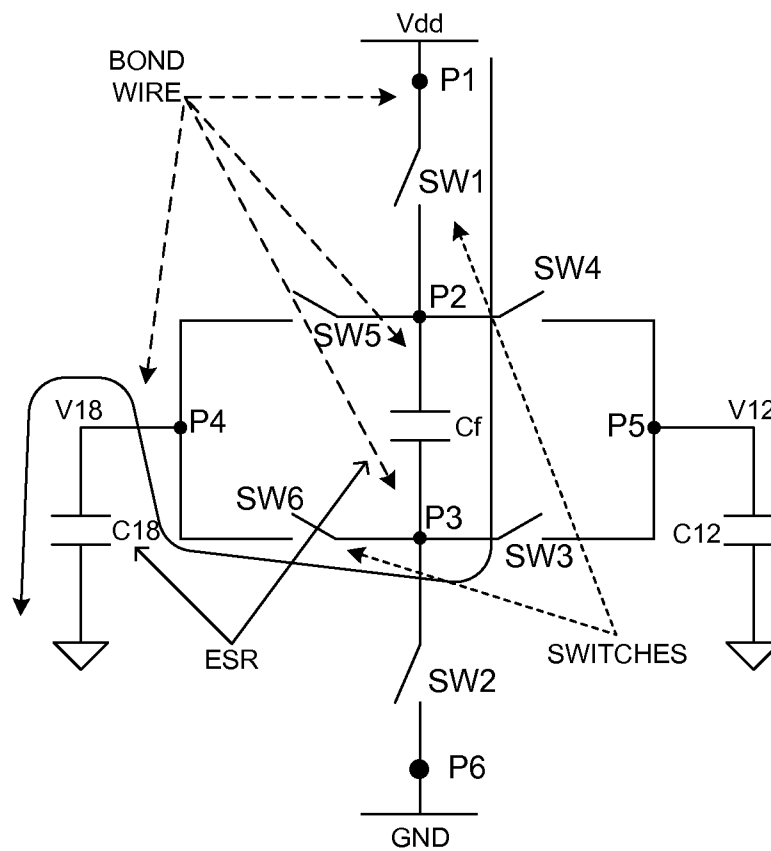


Fig. 3a

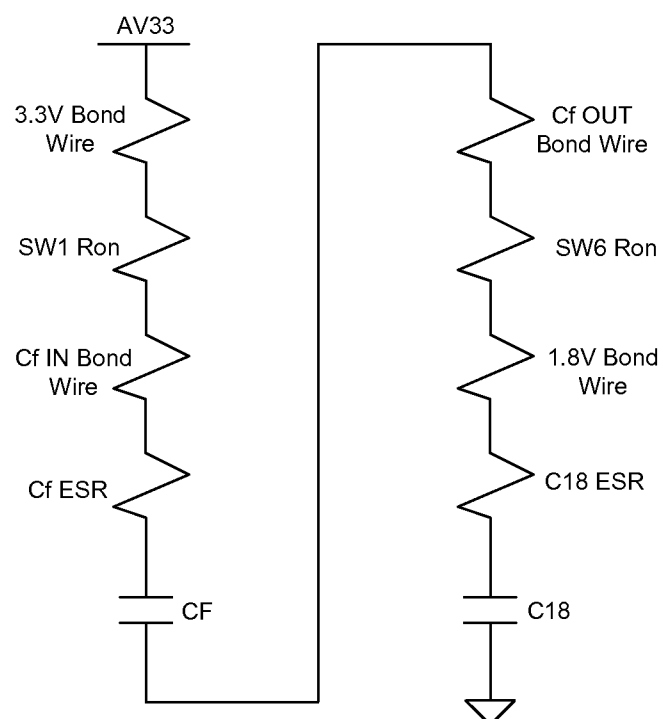
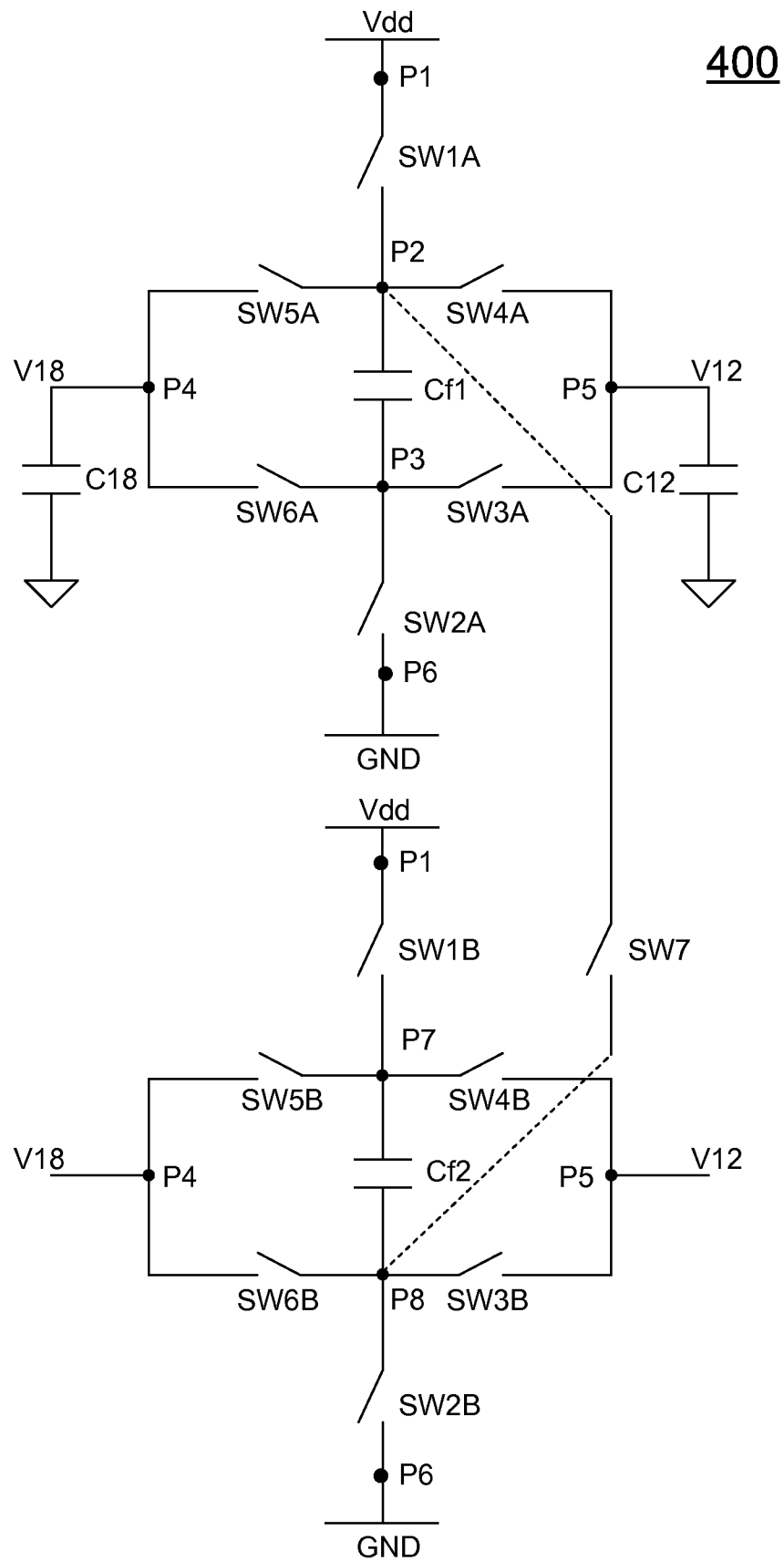


Fig. 3b

**Fig. 4**

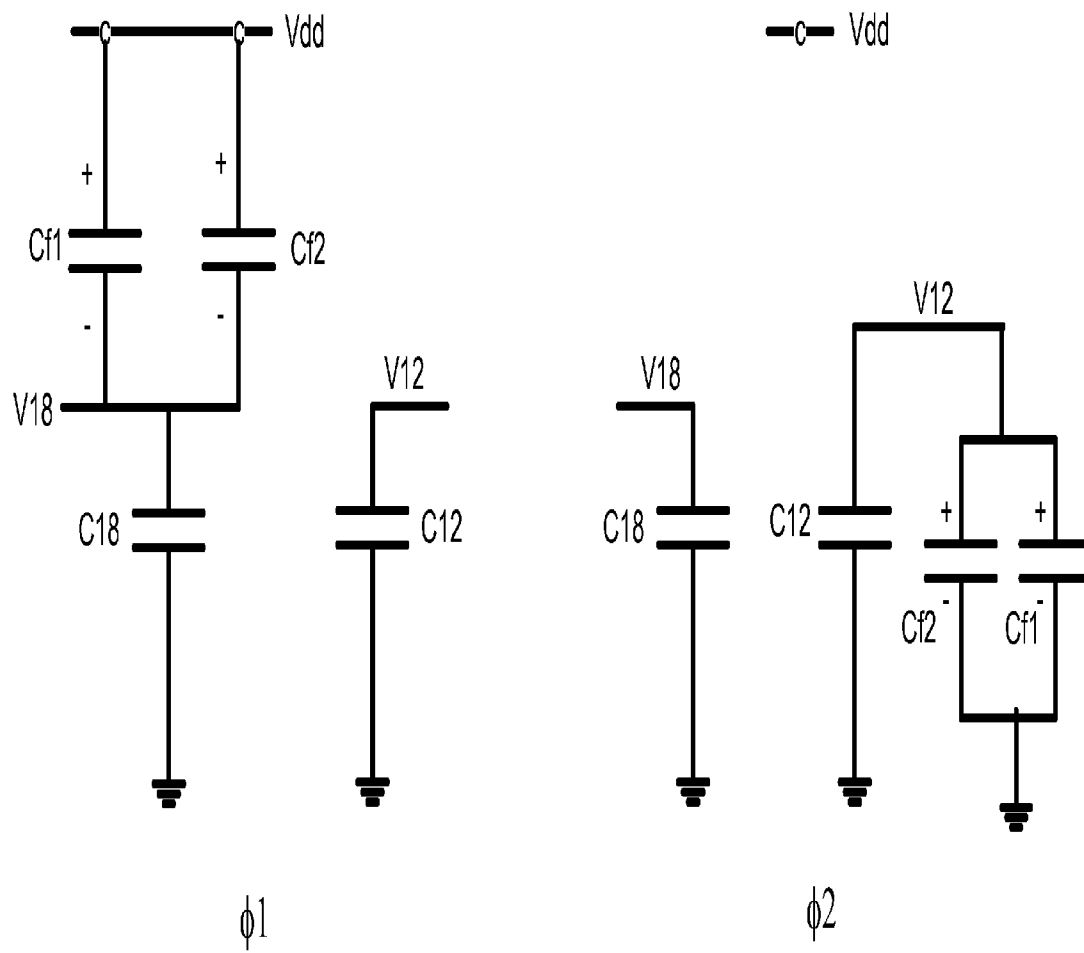


Fig. 5a

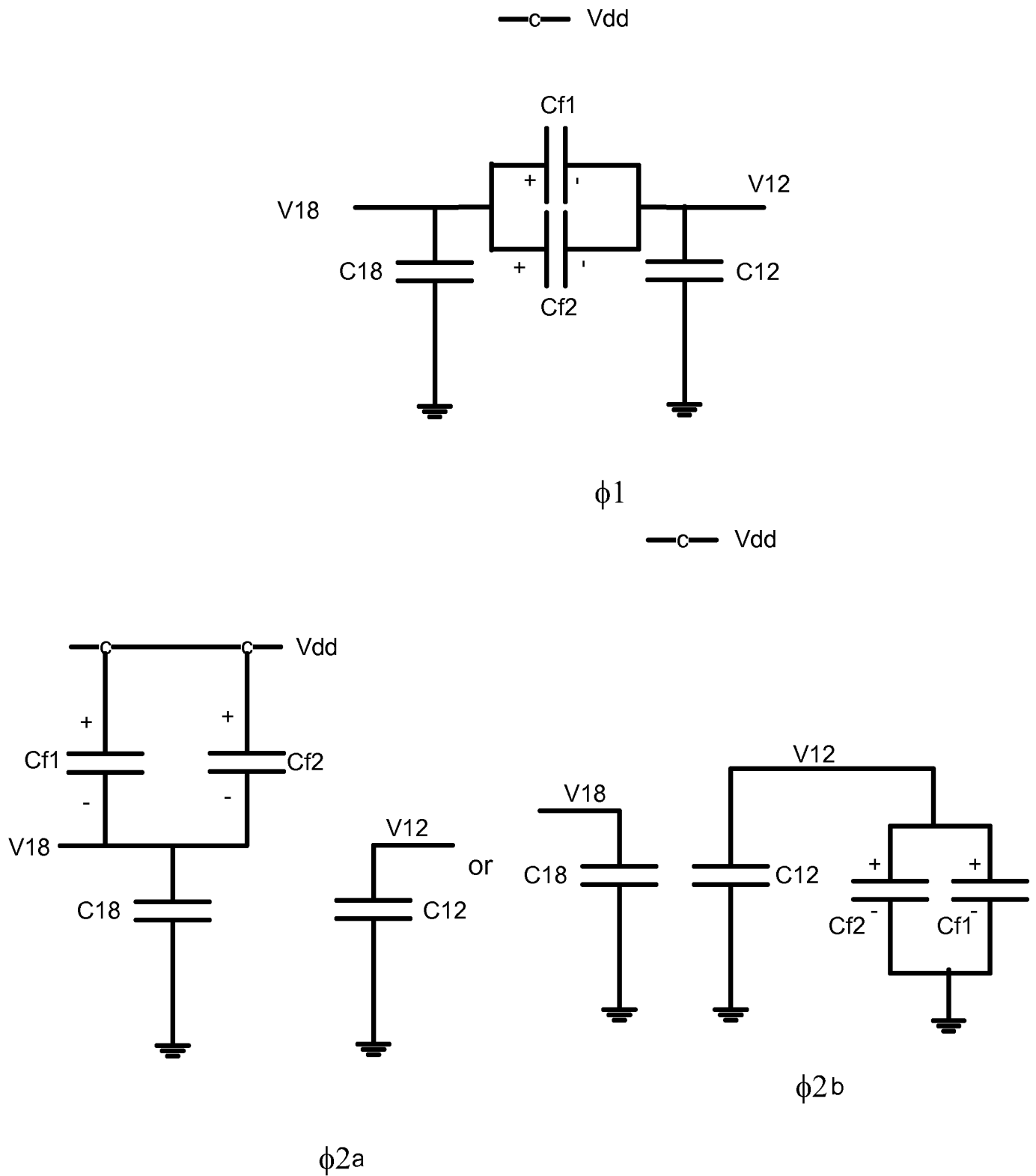
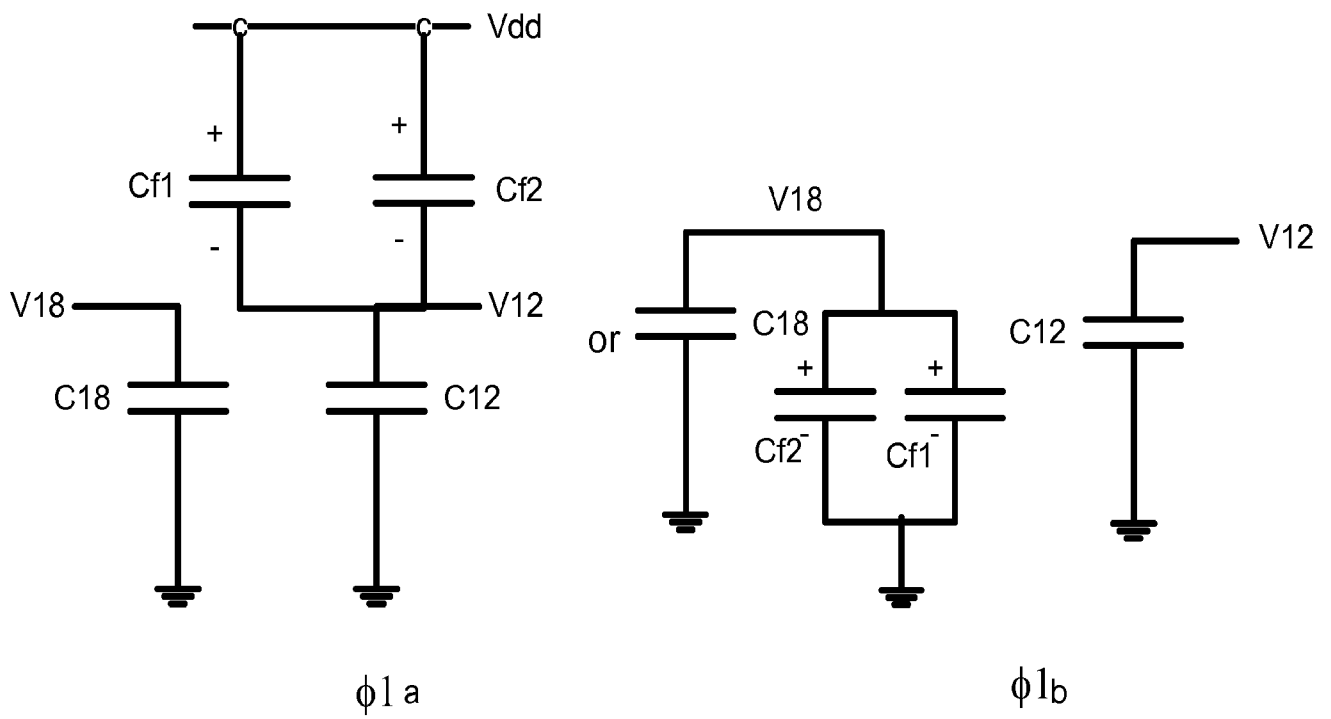


Fig. 5b



—c— Vdd

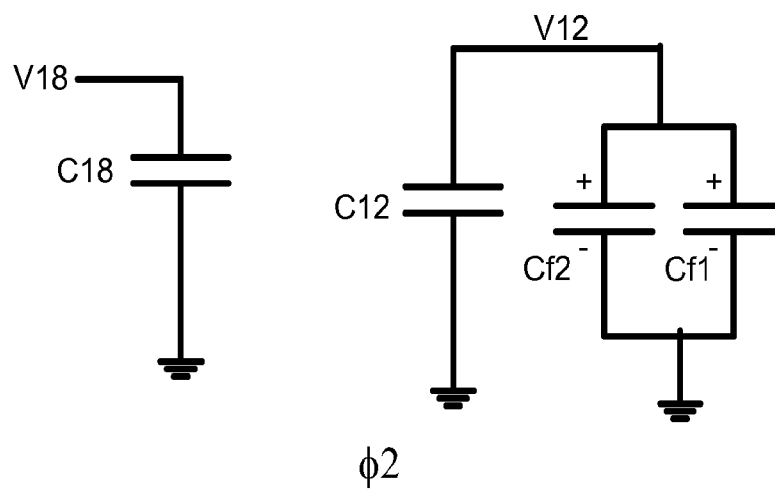
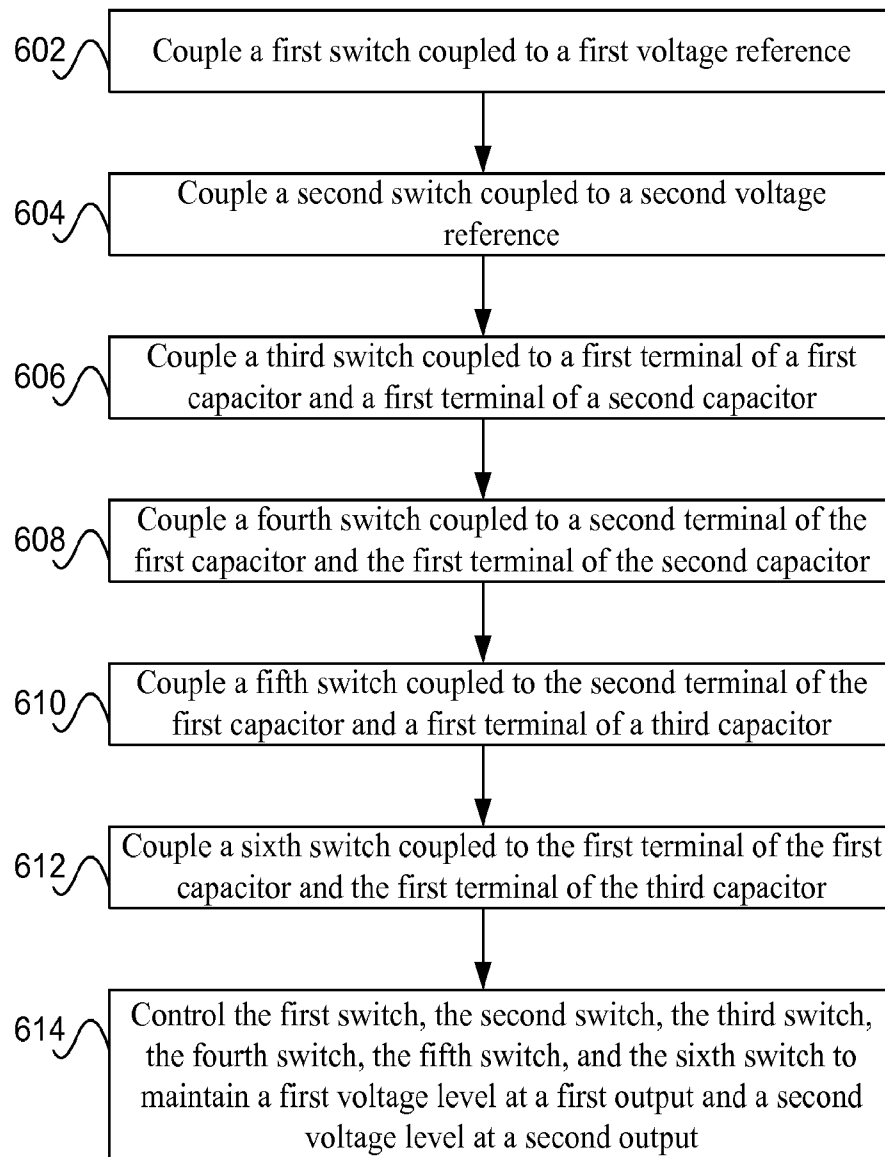


Fig. 5c

600**Fig. 6**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2011/024751

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G05F 1/10 (2011.01)

USPC - 327/536

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) - B41J 2/155, 29/38, 29/393; G05F 1/00, 1/10, 1/445, 1/577, 3/16; H02M 3/00, 3/18 (2011.01)

USPC - 323/225, 267, 271, 282, 288, 350; 327/535, 536, 537, 538; 347/9, 13, 19, 42; 363/30, 59

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

MicroPatent, Questel Orbit, Google Patent, Google

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0150619 A1 (LESSO et al) 26 June 2008 (26.06.2008) entire document	1-20
Y	US 2008/0088179 A1 (OYAMA et al) 17 April 2008 (17.04.2008) entire document	1-20
Y	US 2009/0231176 A1 (CHEN et al) 17 September 2009 (17.09.2009) entire document	3, 5, 13-16
A	US 6,859,091 B1 (NICHOLSON et al) 22 February 2005 (22.02.2005) entire document	1-20
A	US 6,756,772 B2 (MCGINNIS) 29 June 2004 (29.06.2004) entire document	1-20

☐ Further documents are listed in the continuation of Box C.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

10 May 2011

Date of mailing of the international search report

19 MAY 2011

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Blaine R. Copenheaver

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774