Dec. 24, 1968 F. G. SHINSKEY 3,418,486

CURRENT SELECTION AND LIMITING CIRCUITS

Filed Oct. 27, 1966 2 Sheets-Sheet 1

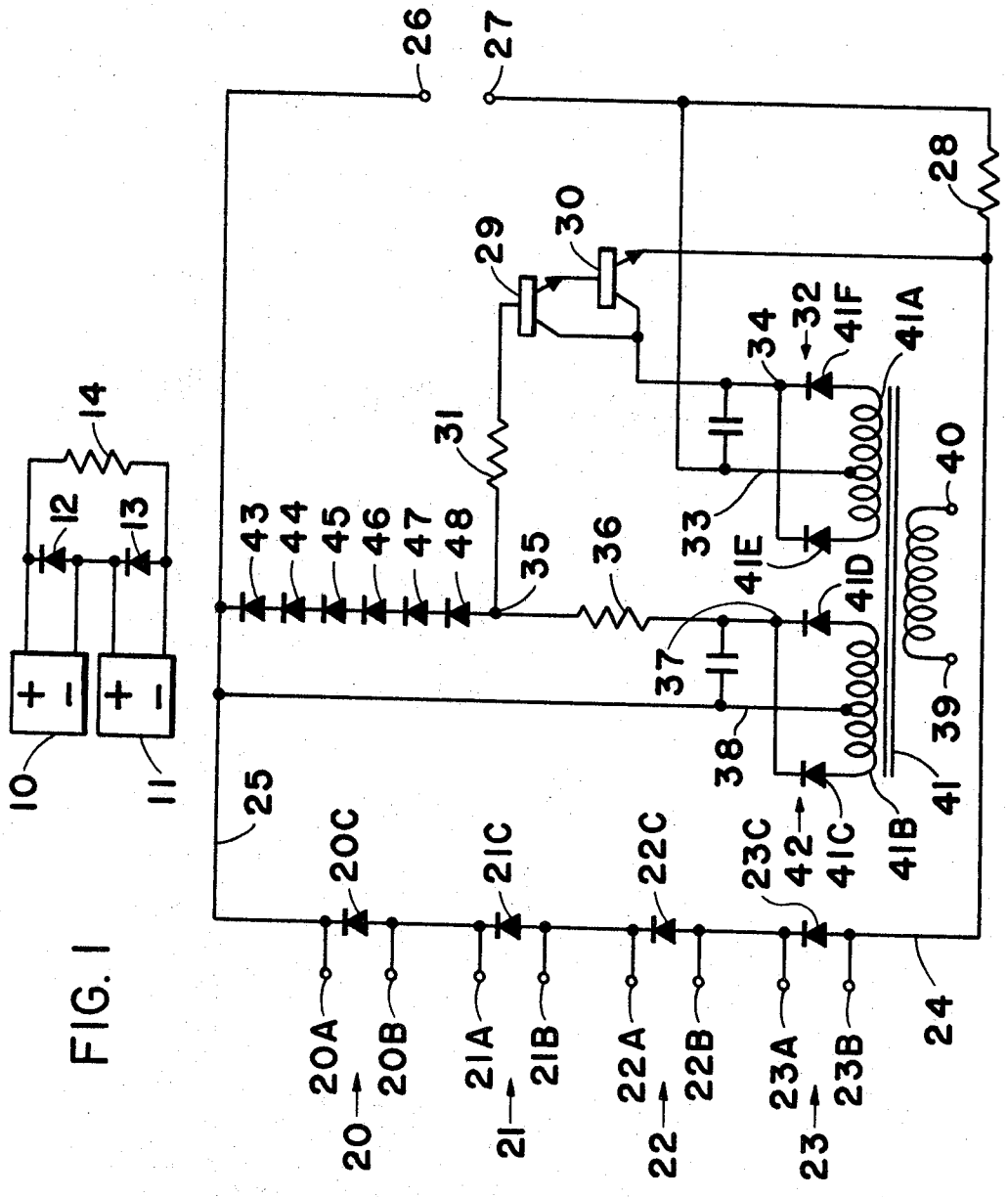


FIG. 1

FIG. 2

INVENTOR.
FRANCIS G. SHINSKEY
BY David E. Hoppe
ATTORNEY

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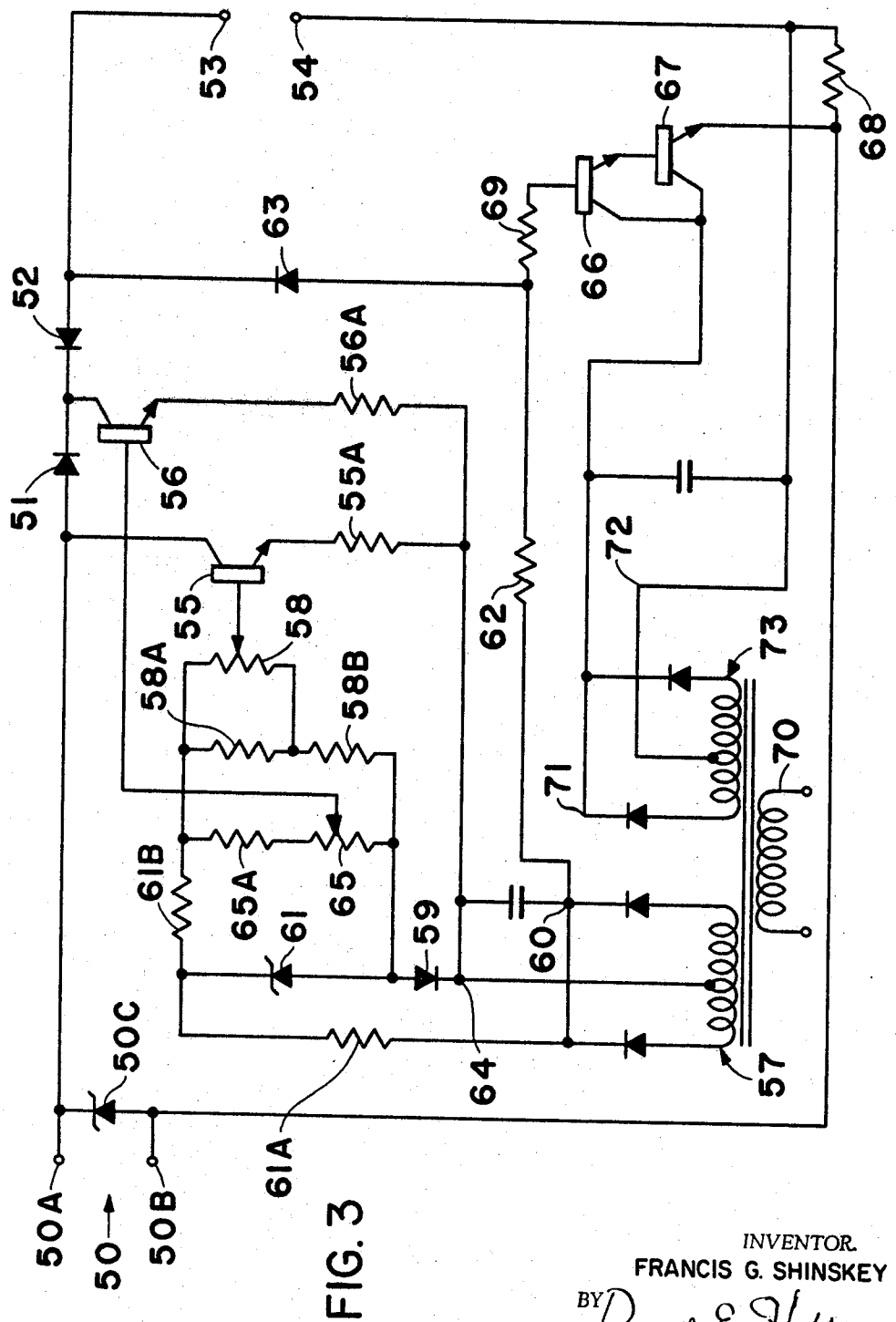


FIG. 3

INVENTOR.
FRANCIS G. SHINSKEY
BY David E. Hoppe
ATTORNEY

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CURRENT SELECTION AND LIMITING CIRCUITS

Francis G. Shinskey, Foxboro, Mass., assignor to The Foxboro Company, Foxboro, Mass., a corporation of Massachusetts

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This invention relates to electrical signal detecting apparatus generally, and more particularly to apparatus adapted to select the one input of a plurality of inputs having an extreme value thereof, and to apparatus adapted to limit a single input within a specified range of values.

Reference is made to U.S. patent to W. H. Howe, No. 3,083,321, disclosing a basic current selecting scheme. The general information specified therein is applicable here. One aspect of the present invention addresses itself to a modification of the Howe disclosure for producing apparatus having an improved selecting function. In addition, the present invention encompasses means for a selection function of the lowest one of a number of current inputs. The present invention also encompasses means for limiting an input current to a preselected maximum and minimum values, and to selecting a median of three input currents.

In process applications where it is desired to operate a single device with a plurality of inputs, the object being to actuate the process device with that input having a maximum current, or in the alternative, a minimum current, it is advantageous and often necessary to provide for high accuracy in the selecting means. It has been found that selection schemes of the prior art require current sources and components of extremely close tolerances in order to provide satisfactory operation. More particularly, difficulties often arise in current selection during transitions among the inputs of the one having the extreme level. Input cross-overs of this nature present difficulties, with the input crossing over to achieve the maximum value tending to interact with the previously extreme input, with the result being a current selection output containing a percentage of error.

Accordingly, it is an object of this invention to provide improved current selection means having a minimum output error throughout the operating conditions anticipated, and requiring a minimum of calibration and adjustment.

It is another object of this invention to provide current selection means for a median current, and that has minimum output error under all operating conditions.

It is another object of this invention to provide current-limiting means for limiting an input current to a predetermined minimum and maximum output level.

It is another object of this invention to provide current selection means that produces an output current corresponding to the maximum current of a plurality of input currents, and in the alternative, may be operated to provide an output current corresponding to the minimum current of a number of input currents.

These and other advantages of this invention may be in part apparent from the following description hereof, and in part pointed out in the accompanying drawings, in which:

FIGURE 1 is a simplified schematic of the selection principle;

FIGURE 2 is a schematic of a high-low current selector;

FIGURE 3 is a schematic of a high-low current limiter.

Referring to FIGURE 1, a simplified schematic illustrating the concept of the basic invention of Patent 3,083,321 is referred to for purposes of explanation. Current sources **10** and **11** are connected in series, with their

polarities in the same direction, and with a diode **12** and **13** being connected across each current source respectively in a back-biased direction. Ideally, the current sources **10** and **11** should have infinite internal impedances. The series configuration of current sources and diodes is applied to a load **14**. When the current from sources **10** and **11** are precisely equal, the current flows serially through the high impedances of both sources and through load **14**, and no current flows through either of the diodes **12** or **13**. Whatever, the current level in this circuit, diodes **12** and **13** will both be backbiased to some extent so long as current from source **10** is the same as the current from the source **11**.

In the event current from source **10** should increase above the current from source **11**, the excess in current must flow through diode **13** in order to complete the circuit. Diode **13** thereby goes from being back-biased to become forward-biased upon a transition from an equal current condition to one of an excess of source **10** current. Under this new condition diode **12** remains back-biased. The current through resistance load **14** is now the highest current of the two respective currents from sources **10** and **11**; in the circuit the higher current from source **10** flows serially through resistor **14** and through the parallel combination of current source **11** and diode **13**, with the excess in current **10** over that of current **11** flowing through diode **13**.

In practice, the circuit of FIGURE 1 has limitations, in that to the extent the current sources have finite impedances and load **14** has an impedance greater than zero, transition errors are introduced. Diodes **12** and **13** are not perfectly linear devices, and in going between a back-biased and a forward-biased condition, tend to introduce errors in the output current level.

Referring to FIGURE 2, a high current selector schematic embodying the present invention is shown. Illustratively, four current inputs **20–23** are shown, but it is to be understood that any number of inputs may be employed with suitable modifications of the circuit as hereinafter pointed out. Current input **20** is particularly described, with current inputs **21**, **22** and **23** being similarly configured. The current source to be connected to input **20** is supplied to terminals **20***a* and **20***b*, with the positive input current polarity being connected to **20***a*. Diode **20***c* is connected in the back-biased direction with respect to the polarity of its associated current input across input terminals **20***a* and **20***b*; that is, the cathode of diode **20***c* is connected to terminal **20***a*. Current sources **21**, **22** and **23** are similarly connected with diodes across them, and the four inputs **20–23** are connected serially so that diodes **20***c* through **23***c* are in series and similarly polarized. The entire set of inputs **20** to **23**, being serially connected, has reference lead **24** leading from the junction of input terminal **23***b* and the anode of diode **23***c*, and has lead **25** leading from the junction of input terminal **20***a* and the cathode of diode **20***c*. Lead **25** is connected directly to output terminal **26** of the current selector circuit, and reference lead **24** is connected to output terminal **27** through resistance **28**.

The circuit as described so far is quite similar to the basic arrangement of FIGURE 1, with the addition of two current inputs and a resistance **28** in series with the output terminals. The remainder of the current selector schematic shown and to be described, is concerned with means to produce a secondary current through resistance **28** opposing the current supplied to output terminals **26** and **27** in order to maintain a specified low back-bias across the input diode associated with the input having the highest current level. This insures that voltage changes in the input circuits will not make the back-biased diode conduct and thus introduce an output cur-

rent error; this specified low back-bias also serves to minimize transition errors.

In this application for selecting the highest among the input currents, the secondary current through resistance **28** is designed to produce a back-bias of 0.5 volt across the particular diode associated with the highest current input. The remaining diodes are forward-biased by the excess current that must flow through them to complete the circuit for the highest input current.

Since the potential drop across the three forward-biased diodes opposes that across the back-biased diode in the input circuits **20–23**, the resultant potential drop between reftrence lead **24** and lead **25** is equivalent to the sum of three forward-biases minus one back-bias. Taking each forward bias to be about 0.5 volt and the desired back-bias to be about 0.5 volt, the forward bias sum is 1.5 volts. Subtracting the back-bias of 0.5 volt, the remainder is 1.0 volt. This potential of 1.0 volt is the desired drop between reference lead **24** and lead **25**, with lead **25** being the more negative owing to the direction of the input diodes **20***c*–**23***c*.

An amplifier comprising transistors **29** and **30** together with associated circuitry operates to maintain the back-bias potential across the non-conducting input diode of the group **20***c*–**23***c* at 0.5 volt by providing sufficient current through resistor **28** to produce a voltage across it opposing the potential output terminals **26** and **27**, with a difference of about 1.0 volt between the flow through series resistance **28** and the output terminal potential to thereby give a potential drop of 1.0 volt between reference lead **24** and lead **25**.

The base of transistor **29** is referred through resistor **31** to the transistor amplifier bias potential appearing at junction **35**. The emitter of transistor **29** is connected to the base of transistor **30** and the emitter of transistor **30** is connected to lead **24**. The amplifier circuit is completed by connection from output terminal **27** back to the negative terminal **33** of power supply **32**, the positive terminal **34** of which is connected to both collectors of transistors **29** and **30**.

The bias potential at junction **35** is derived from bias power supply **42**, which has its negative terminal **38** connected to lead **25**, and its positive terminal **37** connected through current-limiter resistor **36** to junction **35**. Six diodes in series, diodes **43–48** connect junction **35** to lead **25**, the diodes being connected in a forward biased direction. Current-limiting resistor **36** has a value chosen to produce a forward series current through these six diodes at about 30 milliliamps; 30 milliamps is in this application the mid-range of the anticipated input currents from inputs **20–23**. The anticipated input currents illustratively are derived from current sources having a current range of from 10–50 milliamps for this application. The highest of the input currents will have its excess value over the remaining lower inputs flow through the diodes associated with these lower inputs. It is desired to have a forward current through the six diodes **43–48** of the same order as the current through the input diodes **20***c* through **23***c*. The forward current of 30 milliamps through diodes **43–48** produces a voltage drop between junction **35** and lead **25** of about 3.0 volts D.C., with junction **35** being positive with respect to lead **25**. This voltage drop is stable over the operating conditions of the illustrated application. There is a voltage drop across resistor **31** of less than a volt. Resistor **31** has a value selected to provide a current gain for amplifier **29–30** illustratively of a factor of 1200.

The six diodes **43–48** associated with the bias supply **42** serve to establish junction **35** at a desired positive potential with respect to lead **25** so that the base of transistor **29** may be at the proper bias to regulate the current through resistance **28** to a value that determines a regulated 1.0 volt potential difference between reference lead **24** and lead **25**.

Two diodes of the group **43** through **48** serve to contribute to raise the potential at the base of transistor **29** with respect to lead **25** by about 1.0 volt. Note that reference lead **24** is to be regulated at about 1.0 volt positive with respect to lead **25**. Therefore, this two-diode contribution serves to raise the base of transistor **29** above lead **25** by an amount equivalent to the required elevation of the reference level of lead **24** with respect to lead **25**. An additional four diodes are required to further raise the potential at the base of transistor **29** in order to compensate for operating voltage drops in the amplifier circuit. One of these four diodes compensates for the approximately 0.3 to .75 volt drop across resistor **31** and the remaining three diodes compensate for the junction drops across transistors **29** and **30**. The base of transistor **29** must be at a potential sufficiently positive with respect to reference level **24** to overcome the operating junction drops in the two transistors. Two diodes are required to compensate for the junction drop of transistor **30** inasmuch as the output current therefrom is in the range of 0 to 100 milliamps, or twice that of the anticipated input current level. Therefore, the base of transistor **29** is actually made more positive with respect to reference lead **24** by an amount equivalent to the potential drop across three forward-biased diodes.

The raise in potential of the base of transistor **29** over lead **25** by an amount determined by the six series forward bias drop of diodes **43** through **48** effectively places the base above the reference lead **24** required potential by an amount compensating for amplifier operating drops. Any tendency in the potential difference between reference lead **24** and lead **25** to change, results in a corresponding shift in the base-emitter drops of transistors **29** and **30** with a consequent alteration in current supplied from transistors **29** and **30** through resistance **28**. This current alteration serves to maintain the potential at reference lead **24** at the required value with respect to lead **25**.

Typically, current will flow from input circuits **20** through **23** corresponding to the highest current thereof which will be in range of from 10 to 50 milliamps in the illustrated application. This 10–50 milliamp current flows through output terminals **26** and **27** by way of resistance **28**. Transistors **29** and **30** supply current through resistance **28** which opposes current flowing through resistance **28** from the input circuits so that the potential between leads **24** and **25** is stabilized. This potential is held to a value corresponding to the forward drop across input diodes **20***c*–**23***c* minus the back-bias across a non-conducting diode among the input diodes. In order to do this, current in the range of from 0 to 100 milliamps must be supplied from the power supply **32** through amplifier **29–30** and through resistance **28**, thereby providing a resultant bucking voltage across resistor **28** opposing that which would be impressed by the input circuits alone. Resistor **28** must be sufficiently large to produce the maximum desired bucking voltage from the maximum current available from power supply **32**.

The provision of compensating diodes **43** through **48** offers an additional advantage in providing temperature compensation for both the junctions of the amplifier and the input diodes **20***c*–**23***c* of the circuits **20** through **23**; the bias on the base of transistor **29** thereby changes with temperature an amount offsetting the changes resulting from temperature on the input diodes **20***c*–**23***c* and the junctions of transistors **29** and **30**. This temperature compensation is the more accurate as the current through diodes **43** through **48** approximates the current through the input diodes **20***c*–**23***c* and the junctions of transistors **29** and **30**.

The circuit of FIGURE 2 is adaptable to the function of selecting the lowest current among a plurality of input currents by the simple expedient of reversing the connections of each of the input diodes **20***c*–**23***c*, and appropriately adjusting the new required bias potential appearing at junction **35**. The polarity of the current sources re-

mains the same, the positive input terminals being **20***a*, **21***a*, **22***a*, **23***a*. Taking the illustrated situation of four current inputs, the reversal of the four diodes results in a total forward-bias potential drop across three of the diodes of 1.5 volts with reference lead **24** being the negative terminal with respect to such forward-bias drop. The back-bias across the remaining diode, now associated with the lowest input current, thereby subtracts 0.5 volt from this forward-bias sum, with the resultant potential drop between reference lead **24** and lead **25** being 1.0 volt, lead **25** being the positive terminal. As compared with the previous situation described for selecting the highest current among a plurality of current inputs, the change in potential between reference lead **24** and lead **25** is 2 volts, lead **25** now being 1 volt positive where formerly it was 1 volt negative with respect to reference lead **24**. Junction **35** has to be reduced by this 2 volts change to maintain the desired biases across the input diodes **20***c*–**23***c*. This may be accomplished by eliminating four of the diodes of the group **43**–**48** so that only two diodes in series remain, these diodes being in the same forward-biased direction as formerly. Thereby, junction **35** is positive with respect to lead **25** by the forward-bias across two series diodes, or by one volt. Junction **35** is thus 2 volts positive with respect to reference lead **24**, this 2 volts being approximately the value required for establishing transistor amplifier **29**–**30** at its operating level, the junctions of transistors **29** and **30** together with the drop across resistor **31** requiring about a 2 volt bias compensation.

In operation, the lowest input current will have its associated diode **20***c* through **23***c* back-biased, and the remaining diodes of groups **20***c* through **23***c* will be forward-biased, each conducting current from its current source in excess of the lowest current. The lowest current of the current sources flows serially through each of the current sources feeding into inputs **20** to **23**, while the excess current from each current source above the lowest current in the group is thereby shunted through its associated forward-biased diode. In order for lowest current selection to function smoothly between transitions, it is important that the diode associated with the lowest current source be back-biased a small amount; input cross-overs will then cause the back-biased diode to go to a forward-biased condition at a current acceptably close to the actual cross-over.

It is to be understood that any number of current inputs may be employed in the function of selecting the lowest current, with the requirement that the bias be adjusted appropriately to maintain the desired back-bias across the diode associated with the lowest current source.

The circuit of FIGURE 2 is also adaptable to a median selection among three input currents, the highest and lowest currents being effectively rejected, and the median current being passed onto output terminals **26**–**27**. Three inputs are used for median selection, with three Zener diodes being connected in the same direction as the direction of the highest current selection diodes previously described, with the transistor amplifier bias being modified for biasing these series Zeners appropriately. The input diodes for the median selection function are Zener diodes conveniently having low breakdown ratings, illustratively 3.3 volts. In operation the highest input current source will cause reverse conduction in the Zener region of its associated Zener diode, the lowest current source will cause forward-biasing in the normal region of its associated Zener diode, while the median current source has a nonconducting diode owing to a lower back-bias across it.

To obtain the proper low bias, the Zener diode associated with the median current source should have a low back-bias of about 0.5 volt, and the Zener diode associated with the lowest current source forward-biased 0.5 volt. These potentials cancel, so that the total potential across the three series Zeners is equal to the threshold potential required across the conducting Zener diode associated with the highest current source, which is about 2.5 volts back-bias for a 3.3 volt Zener. The regulation of the potential drop between reference lead **24** and lead **25** at a 2.5 volt bias may conveniently be obtained by connecting junction **35** directly to lead **25**. Amplifier **29**–**30** thereby maintains lead **25** 2.5 volt positive with respect to reference lead **24**. With FIGURE 2 altered accordingly, the current from the median source, having a nonconducting diode associated with that source, must flow serially through resistance **28** and output terminals **26** and **27**.

With fixed currents applied to two of the three Zener inputs of the median selector circuit variation of FIGURE 2, the circuit then becomes in effect a current limiter for the variable current input. Ordinary diodes may be used with the fixed current sources instead of the Zeners if the diode across the higher fixed current source is reversed so that it will conduct.

Referring now to FIGURE 3, a schematic of a circuit adapted for high and low current limiting of a variable current is shown. The variable current source has its positive terminal applied to terminal **50***a* and its negative terminal applied to terminal **50***b* of input **50**. Zener diode **50***c*, conveniently 3.3 volts breakdown, has its cathode connected to terminal **50***a* and its anode to terminal **50***b*.

Two diodes **51** and **52** are in series with input Zener diode **50***c* and output terminals **53** and **54**. Diodes **51** and **52** are connected in opposing directions to one another, and are simple diodes that may conduct in one direction only. Each of the diodes **51** and **52** has supplied thereto in its conducting direction a set limit current derived from an adjustable current source.

The connection of the variable input current at **50** with the adjustable set limit currents in series may be considered somewhat analogous to the arrangement described for median selection of an input current in connection with the schematic of FIGURE 2. The circuit of FIGURE 3 is complicated by the arrangement wherein a single power supply **57** effectively supplies the set high limit and set low limit currents. A similar general function obtains in the circuit of FIGURE 3, in that the median current of three currents is passed on to an output, while the highest and lowest currents are not accepted. The lowest and highest currents are specified by adjustments, and the median current of the three currents is supplied to output terminals **53** and **54**. When the input current at terminals **50***a* and **50***b* reaches and crosses either a low set or a high set limit, it is no longer median, and the new median current is the low set or high set limit, as the case may be, which is thereupon passed to output terminals **53** and **54**. The result is a current limiting function in which the input current from terminals **50***a* and **50***b* is passed to output terminals **53** and **54** over a specified range having predetermined upper and lower set limits, and when the input curent exceeds or falls below this range, that particular set limit current is supplied instead to output terminals **53** and **54**.

The collector of low-limit current source transistor **55** is connected to terminal **50***a* and its emitter is connected to negative terminal **64** of power supply **57**. The base of transistor **55** is connected to an adjustable tap on low-limit potentiometer **58**. Low-limit potentiometer **58** is connected serially with temperature compensating **59** and dropping resistor **61***a* between negative terminal **64** and positive terminal **60** of power supply **57**. Zener diode **61** is connected across potentiometer **58** to regulate the voltage drop thereacross at a stable reference level. Low limit potentiometer **58** sets the bias of transistor **55** to regulate the current therethrough to a particular level representing the desired low-limit current.

The base of range limit current source transistor **56** is connected to an adjustable tap on range limit potentiometer **65**, which is connected in parallel with potentiometer **58**. Current flowing through current source

transistor 56 represents the difference between the high current limit and the set low current adjusted by potentiometer 58 and flowing through low limit current source transistor 55.

An amplifier consisting of transistors 66 and 67 and associated circuitry supplies an appropriate current through resistance 68 to maintain the bias across the diodes 50c, 51 and 52 at the requisite level for proper operation. This amplifier functions in much the same manner as transistors 29 and 30 shown and discussed in connection with FIGURE 2. Resistance 68 is connected between terminal 50b of input 50 and output terminal 54. Transistor amplifier 66–67 is supplied from power supply 73, and the base of transistor 66 is referred through gain resistor 69 and diode 63 to the potential at output terminal 53. Note the potential at terminal 53 is about the same as that at input terminal 50a, inasmuch as diodes 51 and 52 are connected in opposite directions, and their biases thereby cancel. Thereby, the potential between input terminals 50a and 50b is regulated to maintain the desired back-bias across diode 50c.

In order to conveniently employ a single current power supply for both the high and low limit currents, current source transistor 55 supplies the set low current therethrough, and current source transistor 56 supplies the difference between the high set current and the low set current therethrough. Both current source transistors 55 and 56 have their emitters connected to the negative terminal 64 of power supply 57. The current flowing from negative terminal 64 to the positive terminal 60 of power supply 57 is the sum of the two currents through the current source transistors 55 and 56, or a current corresponding to the high set limit. This high set current flows through resistor 62 and diode 63 and back to the collectors of transistors 55 and 56 by two parallel paths; the first is through diode 52 which passes the excess current of the set high limit current over the input current of the collector of transistor 56. The second path is through load terminals 53 and 54, resistor 68, the input terminals 50b and 50a, and back to the collector of transistor 55; this path permits the input current to flow therethrough.

Take the case where the input current supplied to terminals 50a and 50b is median between the high set and low set limits. Then the input current flows from terminal 50a through the parallel path transistor 55 makes with the series combination of diode 51 and transistor 56, thence through power supply 57, resistor 62 and diode 63 to output terminal 53 and back therefrom through output terminal 54, resistance 68 and through terminal 50b. Inasmuch as transistor 55 is biased to allocate to itself the low set current, the remaining parallel path through diode 51 must carry the remainder, or the excess input current over the low set current. The excess of the high current over the input current must pass from diode 63 back through diode 52 to current source transistor 56. The remainder, the input current, flows through output terminals 53 and 54. Diodes 51 and 52 are connected in opposite directions, and transistor 56 draws the sum of the currents flowing through diodes 51 and 52, which is equal to the high set current minus the low set current.

Thus diodes 51 and 52 are both conducting when the input current is median between the high set and the low set limits, with the sum of the currents flowing through the two diodes 51 and 52 also flowing through current source transistor 56. This sum is the range between the high set and the low set currents. The current through transistor 56 is again summed with the current through transistor 55 with that sum equal to the high set current.

Take the case of the input current reduced to a level equal to the set low limit current; then the current through diode 51 drops to zero, as current source transistor 55 pulls all the input current therethrough. The input current flows through current source transistor 55, and is a component of the high set current flowing through power supply 57, resistor 62 and diode 63. As the high set current divides between diode 52 and output terminal 53, with the high set current minus the current flowing through current source transistor 55 being drawn back through diode 52 and transistor 56, the remainder, or a current level equal to both the input current and the low set current flows through output terminals 53 and 54.

Now take the case where the input current falls below the low set current. Diode 51 is now back-biased, and the input current is only a component of the low set current flowing through current source transistor 55. The low set current flows therefrom as a component through the power supply 57 and diode 63. The excess in the high current over the low set current now flows through diode 52 and through current source transistor 56 while the low set current component flows to terminal 53 of the output.

Take the case where the input current is higher than the set high level. That portion of the input current equal to the high set current is accepted through power supply 57 to output terminals 53 and 54, while diode 52 becomes back-biased. Under this condition of excess current over that accepted through power supply 57, input Zener diode 50c breaks down under the increased potential across the input terminals 50a and 50b and the excess current over the high set limit flows through Zener diode 50c.

When the input current is in the mid-range between the high set limit current and the low set limit current, the entire bias sensed by transistor amplifier 66–67 appears across Zener diode 50c, as noted above, inasmuch as both diodes 51 and 52 are forward-biased and their potential drops cancel as they are connected in opposing directions. When the input current is equal to or exceeds the high set current, all the high set current flows through power supply 57 serially between the input and output terminals, and diode 52 becomes non-conducting or back-biased. This condition tends to make output terminal 53 become negative with respect to input terminal 50a, where under normal operation these two terminals are substantially at the same potential. So too, when the input current falls to the level or below that of the low set current, the serial current passed between the input and the output flows entirely through transistor 55, and diode 51 becomes non-conducting or back-biased. Under this condition, terminal 53 tends to become positive with respect to input terminal 50a.

Transistor amplifier 66–67 normally maintains terminal 53 in the region of 0.5–1.5 volts positive with respect to input terminal 50b by supplying an appropriate current through resistor 68 opposing the serial current between input and output terminals. When the input current exceeds the high set current, and diode 52 is back-biased, the series combination of diodes 51–52 presents a potential drop across both in a direction opposing the potential drop across Zener diode 50c. As a consequence, the back-bias across Zener 50c increases over the normal back-bias sufficiently to conduct the excess input current over the high set limit. Under this condition, transistor amplifier 66–67 has the same operating bias applied thereto as formerly.

When the input current is low, a potential drop across series diodes 51 and 52 appears in the same direction as that bias appearing across Zener diode 50c, and the back-bias appearing across Zener diode 50c is accordingly reduced.

While there has been shown what is considered to be a preferred embodiment of the invention, it will be manifest that many changes and modifications may be made therein without departing from the essential spirit of the invention. It is intended, therefore, in the annexed claims to cover all such changes and modifications as fall within the true scope of the invention.

What is claimed is:

1. Regulating means for use with electrical apparatus for discriminating among a plurality of electrical current sources on the basis of the relative magnitude of the currents from said electrical current sources so that current is supplied from said plurality of electrical current sources to output terminals of said apparatus in accordance with the discrimination performed by said apparatus comprising,

an electrical component disposed serially between a plurality of electrical current sources and output terminals, and amplifying means responsive to an operating potential derived from the individual potentials associated with each of said electrical current sources and said amplifying means having a regulating current output having a magnitude related to the deviation of said operating potential from a predetermined desired potential and said current output being supplied to said electrical component in a direction making the polarity across said electrical component oppose the polarity appearing at said output terminals so that the difference therebetween appears across said electrical current sources and causes said operating potential to approach said predetermined desired potential whereby the individual potential associated with each of said plurality of electrical current sources are maintained at values appropriate for proper operation of said apparatus.

2. The regulating means of claim 1 wherein each of said current sources are arranged serially with the polarities of each current source disposed in the same direction and including rectifying means interconnected with each current source for facilitating the selection of the current level produced by one of said current sources for transfer to said output terminals.

3. The regulating means of claim 2 wherein a plurality of current sources are arranged serially with rectifying means connected in a back-biased direction across each current source whereby the highest input current is transferred to said output terminals.

4. The regulating means of claim 2 with a plurality of current sources arranged serially with rectifying means connected across each current source in a forward-conducting direction whereby the lowest of the input current is transferred to said output terminals.

5. The regulating means of claim 1 in combination with a current limiter circuit responsive to a variable current source having a back-biased Zener device interconnected therewith and said limiter circuit having an adjustable source of limiting current disposed serially with said variable current source and said output terminals with rectifying means interconnected therewith whereby the current level that may be transferred from said variable current source to said output terminals is restricted by the adjusted current level from said adjustable current source.

6. The regulating means of claim 5 wherein said adjustable source of limiting current is adapted to produce two limiting current levels that bound a restricted range of the current level that may be transferred from said variable current source to said output terminals.

7. The regulating means of claim 2 in combination with a median current selection circuit responsive to three current sources and each said current source having a Zener device interconnected therewith in a back-biased direction with respect to the polarity of its respective said current source whereby the median current level of said three current sources is transferred to said output terminals.

8. The regulating means of claim 1 wherein said amplifying means has compensatory bias for operating voltage drops associated with said regulating means.

9. The regulating means of claim 8 including temperature compensation means for said amplifying means.

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ROBERT K. SCHAEFER, *Primary Examiner.*

H. J. HOHAUSER, *Assistant Examiner.*

U.S. Cl. X.R.

307—80