United States Patent [19]

Stockham

[11] **3,805,940**

[45] **Apr. 23, 1974**

[54] **JUSTIFYING APPARATUS**

[75] Inventor: **William M. Stockham,** Redmond, Wash.

[73] Assignee: **Automix Keyboards, Inc.,** Bellevue, Wash.

[22] Filed: **July 12, 1971**

[21] Appl. No.: **161,714**

[52] **U.S. Cl.** ..... **197/20,** 197/187, 199/18, 95/4.5, 315/8.5, 340/17 SP

[51] **Int. Cl.** **B41j 5/36**

[58] **Field of Search** ..... 197/19, 20, 84 R, 84 A, 197/187; 199/18; 95/4.5; 315/8.5, 8.6; 340/173 SP

[56] **References Cited**

UNITED STATES PATENTS

3,690,231	9/1972	Storch	95/4.5 R
2,751,584	6/1956	Isborn	197/187 UX
3,509,817	5/1970	Sims	197/84 R X
R26,144	1/1967	Robbins et al.	197/20 X
3,529,299	9/1970	Chung et al.	340/173 SP
3,530,976	9/1970	Higgason et al.	199/18
2,379,862	7/1945	Bush	197/84 A
2,402,989	7/1946	Dickinson	315/8.6
2,632,548	3/1953	Ackerman	197/187 X
2,661,899	12/1953	Chromy et al.	315/8.5 X
2,678,713	5/1954	Higonnet et al.	197/84 A
2,682,814	7/1954	Higonnet et al.	197/84 R X
3,028,659	4/1962	Chow et al.	340/173 SP
3,049,210	8/1962	Moyroud	197/19
3,272,306	9/1966	De Witt et al.	197/187
3,350,691	10/1967	Faulis et al.	340/173 SP
3,576,549	4/1971	Hess et al.	340/173 SP
3,618,050	11/1971	Heeren et al.	340/173 SP
3,631,410	12/1971	Velasco	340/173 SP

OTHER PUBLICATIONS

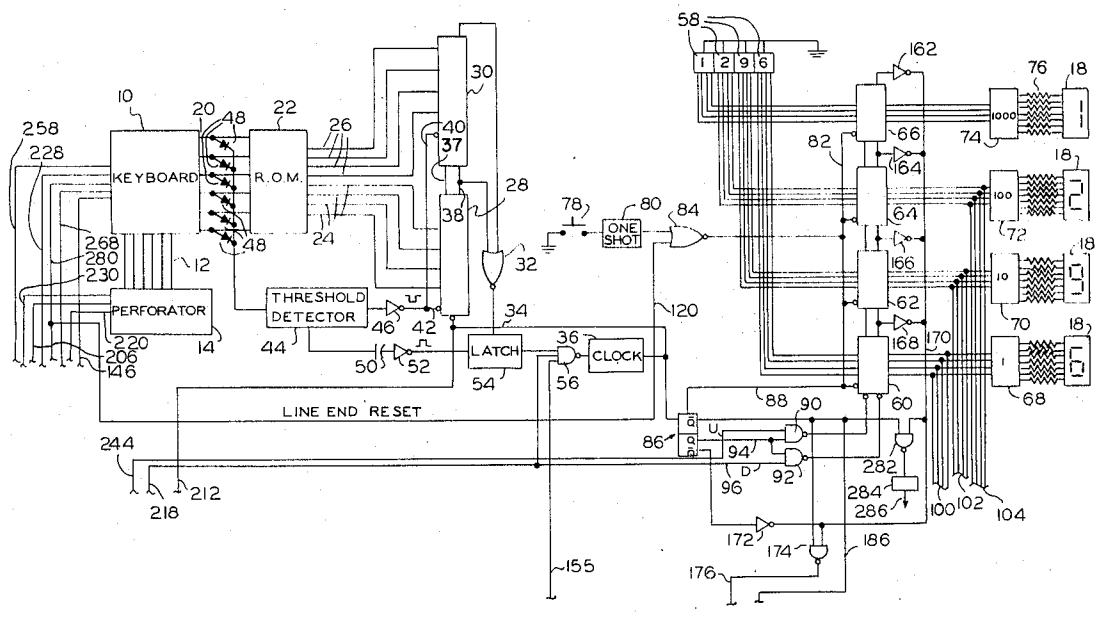
IBM Technical Disclosure Bulletin, Composing Machine, Lincoln et al., Vol. 4, No. 12, May 1962, pp. 67–70.

Primary Examiner—Ernest T. Wright, Jr.
Attorney, Agent, or Firm—Klarquist, Sparkman, Campbell, Leigh, Hall & Whinston

[57] **ABSTRACT**

Apparatus for use in conjunction with a keyboard for operating a typesetter provides an indication when a justifiable line has been entered and continuously supplies a numerical indication of the line length remaining. The keyboard output code accesses incremental width information in a read-only-memory relative to the various characters selected, and this information is entered in an incremental width counter. The incremental width counter is counted down, and an accumulator counter is likewise counted down from an initial line length entry, for digitally outputting the line length remaining. In the event a character or word is deleted, the accumulator counter is accordingly counted upwards.

10 Claims, 4 Drawing Figures



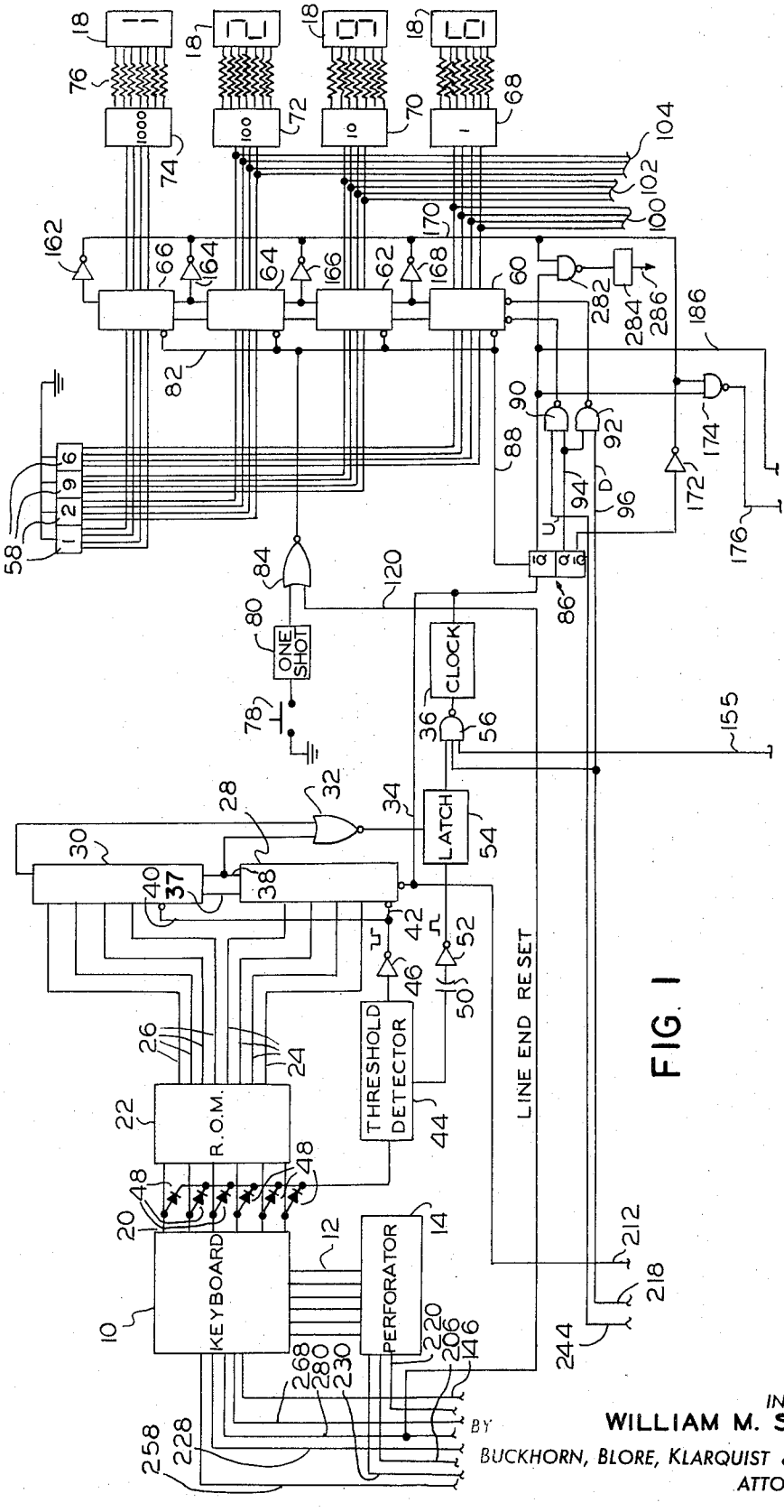


FIG. 1

INVENTOR
WILLIAM M. STOCKHAM
BY
BUCKHORN, BLORE, KLARQUIST & SPARKMAN
ATTORNEYS

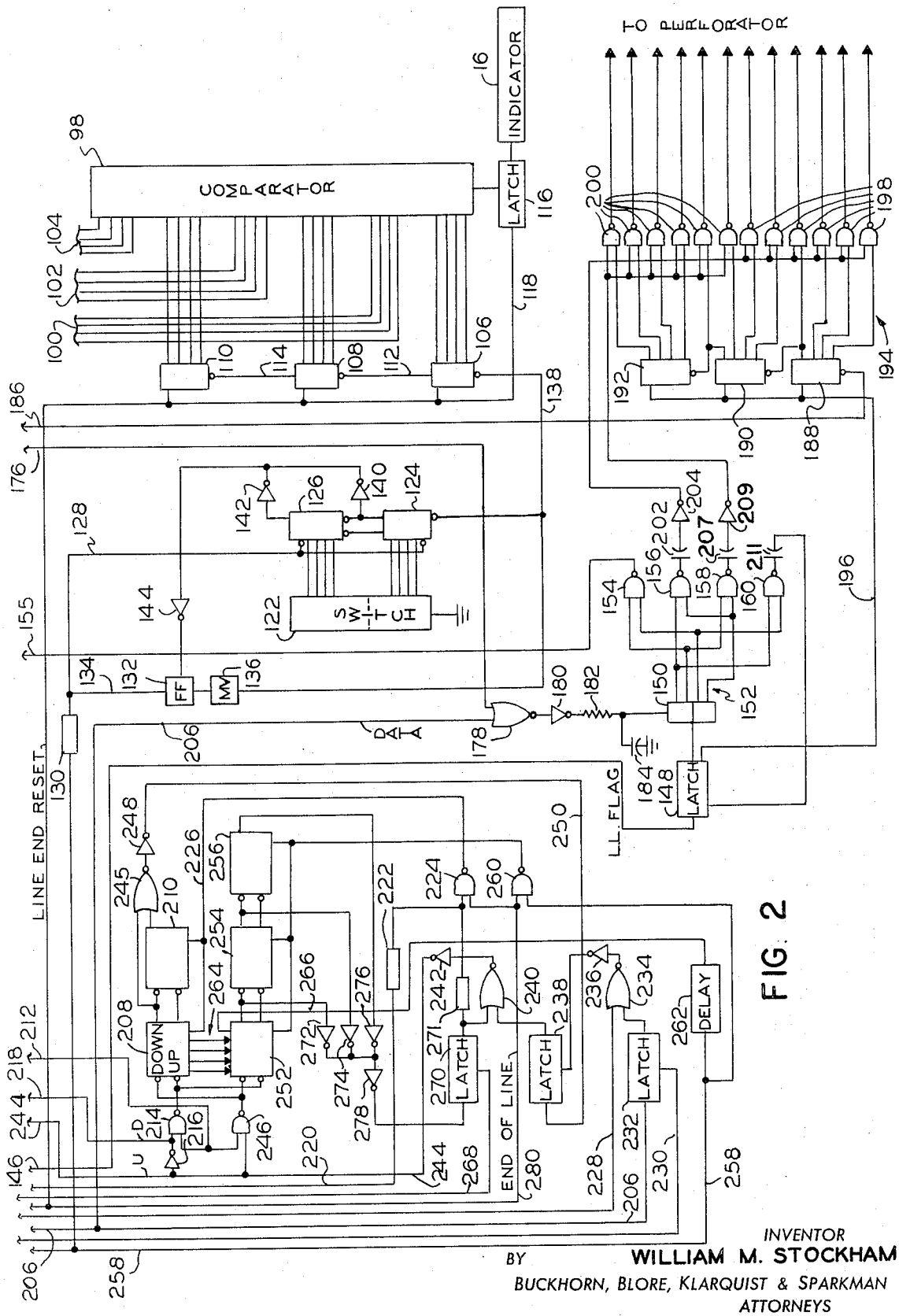


FIG. 2

INVENTOR
WILLIAM M. STOCKHAM

BY
BUCKHORN, BLORE, KLARQUIST & SPARKMAN
ATTORNEYS

FIG. 3

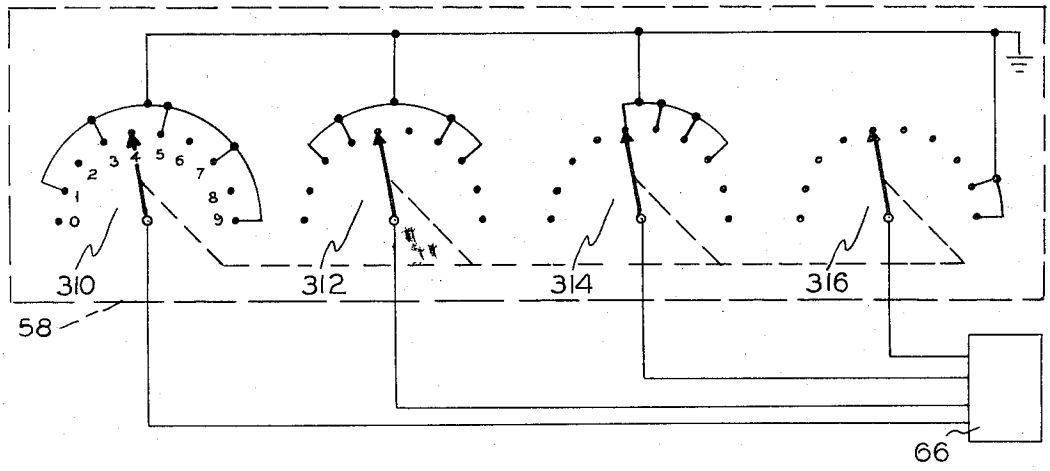
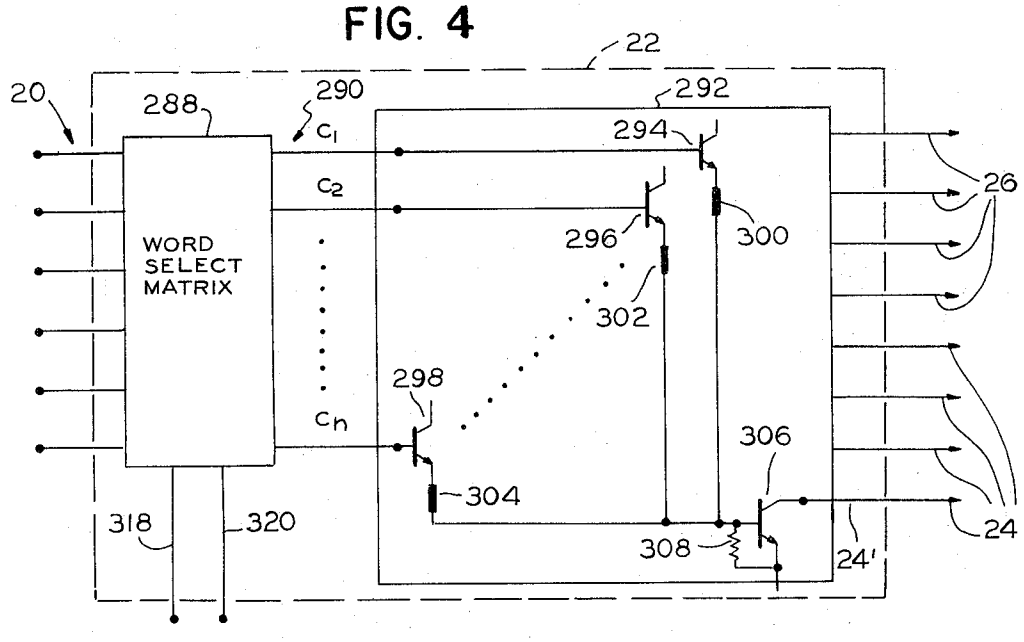


FIG. 4



WILLIAM M. STOCKHAM
INVENTOR

BY
BUCKHORN, BLORE, KLARQUIST & SPARKMAN
ATTORNEYS

JUSTIFYING APPARATUS

BACKGROUND OF THE INVENTION

A keyboard apparatus may be used for generating output information in the form of a punched paper tape which supplies input information for operating a typesetting device such as a phototypesetter or a device which casts solid lines of type. Initially, the length of the line for a given column measure, e.g., pica measure, is determined and information related thereto is entered upon the tape for controlling the typesetter. However, at the end of each subsequent line, the operator must enter a line-end indication, similar to a carriage return on a typewriter, before such line would exceed the predetermined line length. The present invention relates to apparatus which provides the operator some indication that each line is nearly long enough so that awkwardly large spaces are not left between words, as well as some indication of the actual line length remaining. The typesetting device which subsequently receives the punched paper tape will automatically justify each line to fill the column by increasing the spacing between words, with the line length being long enough to fall within a predetermined justifiable range.

Heretofore, relatively complex apparatus has been employed for providing a width indication for each character selected, accumulating the character widths into a line length indication, and providing a notification when the line is nearly filled. A comparatively large number of lines from keyboard keys were employed to operate decoder apparatus for supplying character widths and this decoder apparatus in turn supplied inputs to binary weighting means generating binary output representations of the character widths. These character widths were applied for counting down a line length accumulator. An analog output was frequently produced for operating a meter specifying the line length remaining, and when a predetermined line length was reached a notification was given of a justifiable line.

SUMMARY OF THE INVENTION

According to the present invention, an apparatus for accumulating the width of successive characters selected by a keyboard includes memory means for receiving character codes from the keyboard and for directly accessing the incremental widths of the characters in digital form in the memory means. An incremental width counter directly receives the incremental widths from the memory means and is subsequently counted down, while an accumulator counter, previously preset to a predetermined line length, is simultaneously counted down in a decimal digital manner. Decimal digital readout means continuously supplies a numerical output representing the line length remaining. Also, an indication is given when a justifiable line has been produced.

According to a further aspect of the present invention, a binary counter means is counted in accordance with the predetermined line length entered into the apparatus, and provides a binary output for use by a typesetter device.

In accordance with another aspect of the present invention, circuitry is included for adapting the present apparatus to the deletion of a character or a word. When a character or a word is deleted, the accumulator counter is accordingly counted upwardly by the accumulated width of the portion deleted.

It is therefore an object of the present invention to provide improved and simplified apparatus for accumulating the width of successive characters as selected by a typesetter-operating keyboard for the indication of a remaining line length.

It is a further object of the present invention to provide an improved apparatus for accumulating the widths of successive printing characters wherein the apparatus directly accesses a digital width representation in response to a character code of the type applicable to a perforator or the like.

It is another object of the present invention to provide apparatus for accumulating the widths of successive characters and supplying a continuous indication in a digital decimal manner of the line length remaining.

It is a further object of the present invention to provide an improved and simplified apparatus for accumulating the widths of successive printing characters and indicating when a justifiable line is completed.

It is another object of the present invention to provide apparatus for accumulating the widths of successive printing characters selected by a keyboard, and for adjusting such accumulation in accordance with the deletion of words or characters.

The subject matter which I regard as my invention is particularly pointed out and distinctly claimed in the concluding portion of this specification. The invention, however, both as to organization and method of operation, together with further advantages and objects thereof, may best be understood by reference to the following description taken in connection with the accompanying drawing wherein like reference characters refer to like elements.

DRAWING

FIG. **1** is a block diagram of a first portion of apparatus according to the present invention;

FIG. **2** is a block diagram of a second portion of apparatus according to the present invention;

FIG. **3** is a schematic diagram of a switching device employed with the present invention; and

FIG. **4** is a schematic diagram of a typical read-only-memory employed according to the present invention.

DETAILED DESCRIPTION

Referring to the drawing and particularly to FIGS. **1** and **2**, the apparatus according to the present invention is adapted to be operated from a keyboard **10** which provides outputs on leads **12** for operating paper tape perforator **14** in accordance with the standard "TTS" teletype code or other suitable code structure. Keyboard **10** and perforator **14** are of the standard type employed in the art and will not be described in detail. The punched paper tape produced is then employed as input for a typesetting device such as a phototypesetter or a device which casts solid lines of type from hot metal. The apparatus according to the present invention signals the operator by means of an indicator **16** when a line is almost filled. That is, when a line of characters and spaces accumulate thicknesses as would nearly total a line of type for filling a specified column measure, then the operator is notified by means of indicator **16.** Meanwhile, a continuous numerical represen-

tation of the line length remaining is given upon visible display means **18** in the form of a digital number.

Indicator **16** is actuated at such time as the line of type specified is justifiable to fill the column measure. A minimum space measure (between words) and a maximum space measure are predetermined. When the number of spaces or space bands designated by the keyboard **10** are expandible for filling the remainder of a line, indicator **16** informs the operator, while display means **18** continuously informs him of the remaining line length. A line end designation may be entered at the keyboard **10** at the proper time. The typesetting apparatus receiving the tape will then be capable of justifying the line by positioning of mechanical space bands or the like between words. In this specification, the term "space band" is used synonymously with the term "space" to indicate the designation or entry of a space at keyboard **10.**

Considering the invention in greater detail, the output of keyboard **10** representative of each character or space to be physically presented in the line of type is provided on leads **20** according to the standard "TTS" teletype code or other character code structure. Thus, leads **20** correspond to leads **12** connected to perforator **14** and each lead **20** by the presence or absence of a signal would designate the presence or absence of a paper tape perforation. Leads **20** are connected to read-only-memory **22** and a code on leads **20,** representative of a character or space, accesses a digital output on leads **24** and **26** in the form of a digital representation of the character width. According to the present apparatus, incremental units are employed representing a small linear measure, such as a thousandth of an inch, and fractions of incremental units. The relation between these units and the conventional pica measure or the like is more fully explained hereinbelow.

The memory **22** (See FIG. **4**) is of the type comprising a multiplicity of semiconductor elements **294, 296...298** in a matrix **292** whereby any given character code causes digit indicating outputs, or the inverse thereof, on all of leads **24, 26.** These elements **294, 296 . . . 298** are suitably bipolar transistors or field effect transistors. The memory **22** is programmed for a particular font of characters by disabling selected memory elements **300, 302 . . . 304** (FIG. **4**) whereby a digital output representation in units or fractions of units is supplied when a character code is entered. Thus, selected means are caused to be nonfunctional by the programming. The read-only-memory **22** may be of the programmable type such as devices manufactured by Monolithic Memories Inc., such as the ROM 0512, or may be of the MOS LSI type such as manufactured by Intel Corp. such as the 1601 electrically programmable memory. 256 possible digital outputs are provided, **128** being assigned to each of two fonts or magazines. A switching means (not shown) is employed to switch between the two fonts or magazines. Furthermore, a plurality of such memories **22** are conveniently switched to supply further type fonts, and moreover are removable or exchangeable for providing additional fonts.

In the present embodiment, the character width accessed from memory **22** is provided in binary coded form wherein leads **24** express the first digit in the form of a series of binary digits, while the outputs on leads **26** express the second or higher order digit in the form of binary digits. The binary digits are entered respectively into binary counters **28** and **30,** which together form an incremental width counter. Each of these binary counters **28** and **30** is capable of being counted upwardly or downwardly, e.g., from 0 through 15 to 0, producing a "carry," or in the reverse direction producing a "borrow" output. The borrow output of binary counters **28** and **30** are supplied as an input to NOR gate **32.** The incremental width counter comprising binary counters **28, 30** is operated principally as a down counter, as will hereinafter more fully appear, and consequently a down counting input connection lead **34** receives the output of clock signal generator **36.** The carry and borrow output leads **37** and **38** respectively of binary counter **28** are coupled to the up and down counting inputs of binary counter **30.** Thus, if binary counter **28** were to count in a positive direction and reach zero, a carry would be provided on carry out-put lead **37** for stepping binary counter **30** by one. However, if binary counter **28** is counted downwardly past zero, the output on borrow output lead **38** resets binary counter **30** at one lower count. Counter circuitry of this type is well known in the art and will not be described in detail.

The digital value of character width accessed from read-only-memory **22** is not "counted" into incremental width counter **28, 30,** but is entered directly into incremental width counter **28, 30** when a strobe signal is provided on leads **40** and **42** from threshold detector **44** by way of inverting amplifier **46.** Thus, as a consequence of strobing, the digital outputs on leads **24, 26** are entered directly into incremental width counter **28, 30** operating as a register, and at this time the incremental width counter **28, 30** will contain exactly the numerical output provided on leads **24, 26.** This output is momentarily supplied by the read-only-memory **22,** but will be stored in incremental width counter **28, 30.**

Each time a teletype code is received on leads **20** (which may or may not represent a character), threshold detector **44** is operated through one of the diodes **48.** The threshold detector **44** detects the presence of a code and supplies a positive going pulse which is inverted by amplifier **46** for strobing incremental width counter **28, 30,** and, as the code is representative of a character or space, the outputs on leads **24, 26** will be stored in the incremental width counter **28, 30.** The space width output here indicates the minimum spacing between words.

An output of threshold detector **44** is also coupled via the capacitor **50** to the input of the inverting amplifier **52** for operating latching circuit **54.** Amlifier **52** is biased such that it produces a positive going output pulse at the conclusion of the strobing pulse output supplied from amplifier **46.** This output of amplifier **52** sets latching circuit **54** causing an output thereof supplied to NAND gate **56** to go low. In response thereto the output of NAND gate **56** goes high and enables clock signal generator **36.** Clock signal generator **36** is an astable multivibrator providing a countdown input to incremental width counter **28, 30** on input connection lead **34.** When the incremental width counter **28, 30** counts down to zero from the value initially entered from memory **22,** a borrow signal applied to the two inputs of the NOR gate **32** will cause the output thereof to go high, resetting latching circuit **54** and turning off clock signal generator **36.** In the interim, clock signal generator **36** will have provided a number of counts equal to the digital value initially entered into incre-

mental width counter **28, 30** from memory **22.** Clock signal generator **36** has an output frequency capable of easily counting down the incremental width counter **28, 30** before the next output from keyboard **10** is received.

The line length suitable to fill a desired column measure is entered by means of a plurality of switches **58,** each designed to ground certain switch outputs in a binary coded decimal (BCD) sequence indicative of the desired number. Together, the switches **58** are employed to select or enter into the apparatus the predetermined line length in units. In the present embodiment clock signal generator **36** counts incremental width **28, 30** in quarter units.

The outputs of switches **58** are designed for entry into an accumulator counter comprising decades **60, 62, 64** and **66.** Each of these decades **60, 62, 64** and **66** may comprise counters substantially similar to the hereinbefore described incremental width counter **28, 30.** The decade counters are cascaded to provide an over-all binary coded decimal counter and the outputs of the decimal counter decades **60, 62, 64** and **66** are supplied to decoder circuits **68, 70, 72** and **74.**

In order to enter the selected number from switches **58** into accumulator counter **60–66,** a pushbutton **78** may be initially pressed providing a ground return for one-shot multivibrator **80** which thereupon supplies a strobe pulse on lead **82** via NOR gate **84.** The strobe signal on lead **82** causes a direct entry of information from switches **58** into decades **60, 62, 64** and **66,** in binary coded decimal form. The one-shot multivibrator **80** provides a single positive pulse which causes the output of NOR gate **84** to drop momentarily providing the stroke signal on lead **82.** The same strobe suitably presets a two-stage counter or divider **86** via lead **88.**

The decoder circuits **68, 70, 72** and **74** are adapted to provide seven-segment driver outputs via coupling resistors **76** to display means **18.** Each display means **18** is suitably a light-emitting display such as a Monsanto "Man" No. **1.** The display provides seven horizontal and vertical light-emitter segments which if all energized, would provide a visible representation of the figure **8** in block style. The other numerals are formed from a lesser number of segments. Thus, in the illustrated example, the number **1,296** is entered from switches **58** into the accumulator counter **60–66,** and at the start of each line operation, the number 1,296 will appear on the display means **18.**

The fractional unit pulses generated by clock signal generator **36** are supplied as an input to counter **86,** and the latter provides up and down counting pulses to the accumulator counter **60–66** by way of NAND gates **90** and **92.** As will hereinafter become more evident, NAND gate **92** is normally energized whereby accumulator counter **60–66** counts down from the value initially entered from switches **58.** In the instance of the specific example, clock signal generator **36** provided four pulses for each incremental unit, and consequently a counter or divider **86** is employed comprising two stages, the second stage of which supplies unit counts on lead **94,** supplying inputs for NAND gates **90** and **92.** When both of the inputs upon one of the NAND gates **90** or **92** is energized, the said NAND gates **90, 92** provide an output for stepping the accumulator counter **60–66** in the selected direction.

It should be apparent that since one-quarter unit and one-half unit counts are available at counter **86,** output display means may also be supplied for such half and quarter units. Also, additional switches for half or quarter units may be supplied for use in conjunction with switches **58** and which can be used to preset one or both stages for counter **86.**

Assuming NAND gate **92** is energized, by down lead **96,** it will be seen that as clock signal generator **36** counts incremental width counter **28, 30** down to zero for each new character, the accumulator counter **60–66** will be similarly counted down by a portion of the line length which may theretofore have been entered from switches **58.** With each ensuing character or space, the total in accumulator counter **60–66** becomes less until the line length is reduced to the justifiable level. The line length remaining is displayed by display means **18** so the operator is continuously aware of the approaching line end. Furthermore, the binary coded decimal outputs from decades **60, 62** and **64** are provided as inputs to comparator **98** (see FIG. **2**). The sets of output leads **100, 102** and **104** from the decades **60, 62** and **64** are coupled to the comparator **98** in FIG. **2** as shown, with the signals on each set of four leads of each of output leads **100, 102** and **104** representing a binary coded decimal digit. It is observed only the three lowest order decimal digits are compared.

Comparator **98** receives not only the outputs of decades **60, 62** and **64,** but also comparator **98** receives corresponding binary coded decimal outputs from a register comprising decades **106, 108** and **110.** The register **106, 108** and **110** is employed as an "up" counter and consequently only carry leads **112** and **114** are employed between stages. The respective decimal digits are compared digit for digit in comparator **98,** i.e. a lowest order or one's digit on leads **100** from decade **60** is compared with the output of decade **106,** while the output of decade **62** on leads **102** is compared with the output of decade **108,** and the output of decade **64** on leads **104** is compared with the output of decade **110.** As hereinafter more fully described, the register **106, 108, 110** accumulates the value representative of the maximum allowable expansion for a space band multiplied by the number of space bands. Thus, each time a space band is designated by the operator on keyboard **10,** the count in register **106, 108, 110** is increased by a number of units indicative of the allowable expansion per space band which has been determined in advance. Therefore, as accumulator counter **60–66** counts downwardly from the preset line length, register **106, 108, 110** counts upwardly for designating the maximum total expansion value for spaces thus far specified in the line by the operator. Comparator **98** suitably comprises a number of exclusive-OR function gates for comparing the binary coded decimal BCD inputs provided from decades **60, 62, 64** and from decades **106, 108, 110,** digit for digit, until the outputs become equal or until the outputs of decades **60, 62, 64** "cross over" the outputs for decades **106, 108, 110.** As the comparison takes place, comparator **98** provides a signal for operating latch **116** and latch **116** energizes indicator **16** which may provide a light, an audible tone, or the like. Latch **116** is subsequently reset by a line-end reset signal on lead **118.**

When the operator receives the indication provided by indicator **16,** he may observe the units left in the line from display means **18** and will conclude the line as

soon as practical by providing a proper code from keyboard **10.** This code will be punched on the punched paper tape by perforator **14** for causing the typesetting device to start a new line. The typesetting device will, of course, automatically justify the concluded line to the extent desired. If it is not convenient for the operator to conclude the line immediately, he can determine whether the line length remaining as represented by display means **18** will allow completion of a word, or whether the word should be hyphenated or deleted.

When a line-end code is provided by keyboard **10,** latch **116** is reset via lead **118.** Also, when the line-end code is designated upon keyboard **10,** NOR gate **84** is also operated via lead **120** for again entering the entire line length in accumulator counter **60–66** from switches **58.**

The maximum expansion value for each space band is set into the apparatus by means of switches **122** which are each suitably substantially the same as switches **58.** Thus, each such switch **122** provides a binary coded decimal output for entrance into an up-down counter comprising decade counters **124** and **126.** These decade counters **124** and **126** are interconnected in substantially the same manner as hereinbefore described in reference to binary counters **28** and **30.** When a strobe signal is received on lead **128** from the keyboard **10** via amplifying and shaping circuitry **130,** at the end of a space band indication from the keyboard **10,** the information from switches **122** is inserted into up-down counter **124, 126** operating as a register. At the same time, flip-flop **132** is set via line **134,** which starts astable multivibrator **136** producing a chain of output pulses. Astable multivibrator **136** is suitably the same in construction and frequency of operation as clock signal generator **36.** The output of multivibrator **136** supplies an input for decade counter **124** causing the up-down counter **124, 126** to count downwardly from the maximum expansion value set therein from switches **122.** At the same time, the output of multivibrator **136** is applied to register **106, 108, 110** by way of lead **138** for counting register **106, 108, 110** upwardly. Upon the occurrence of each space band indication from the keyboard **10,** register **106, 108, 110** is counted upwardly and continuously accumulates a value equaling the allowable space band expansion value multiplied by the number of space bands designated from the keyboard **10.** In the instance of each space band, the up-down counter **124, 126** resets flip-flop **132,** turning off multivibrator **136,** when the count in up-down counter **124, 126** reaches zero. For this purpose, a pair of inverting amplifiers **140** and **142** receive the borrow outputs from decade counters **124** and **126,** and their combined output when both decade counters **124, 126** supply such borrow output is provided for resetting flip-flop **132** through inverting amplifier **144.** The up-down counter **124, 126,** together with multivibrator **136** and associated circuitry, comprise means responsive to space band indications transmitted from the keyboard **10** for providing an output signal representative of the incremental count for maximum expansion allowed for a single space band.

For purposes of providing the designated line length to the typesetting device, it is desirable to enter the line length as selected on switches **58** onto the punched paper tape. For this purpose, keyboard **10** is provided with a key or switch supplying a line length flag on lead **146.** At the same time, pushbutton **78** is operated or the same line length flag from keyboard **10** may be connected by an additional lead (not shown) for operating one-shot multivibrator **80.** Therefore, upon the appearance of a line length flag (and before any copy is entered on the keyboard **10**), the line length from switches **58** is initially entered into accumulator counter **60–66.**

The line length flag signal on lead **146** sets latch **148,** the latter suitably comprising a flip-flop circuit. Latch **148** operates a two-stage counter **150,** which comprises a pair of flip-flops providing a series of non-inverted and inverted outputs on output leads **152** indicative of the states of the counter stages. These are successively presented in four different combinations for successively operating NAND gates **154, 156, 158** and **160.** The latch **148,** however, initially sets the counter **150** to operate NAND gate **154** which energizes clock signal generator **36** via lead **155** and NAND gate **56.** As a consequence, clock signal generator **36** produces a series of output pulses which step counter **86,** and accumulator counter **60–66,** downwardly from the value of the line length entered from switches **58.** At this time, accumulator counter **60–66** is counted downwardly to zero, and when the zero value is reached, borrow outputs from the decades **60, 62 64** and **66** provide a joint output via inverting amplifiers **162, 164, 166** and **168,** on lead **170.** Also, the zero condition of the second stage of counter **86** is indicated on the same lead **170** by way of inverting amplifier **172.** Lead **170** provides one input to NAND gate **174** while the other input thereof is derived from the first stage of counter **86.** When both stages of counter **86** as well as all stages of accumulator counter **60–66** have been counted down to zero, an output will be provided from NAND gate **174** on lead **176** which supplies an input to NOR gate **178.** NOR gate **178** thereupon supplies an output, inverted by amplifier **180** and delayed somewhat by the resistor **182** capacitor **184** combination, to step counter **150** to its next count. Thereupon, the appropriate combination of outputs is provided on leads **152** for deenergizing NAND gate **154** and energizing NAND gate **156.** As a consequence, clock signal generator **36** will be shut off.

While accumulator counter **60–66** was counting downwardly, an output was provided from the first stage of counter **86** via lead **186** to supply an input for a binary counter comprising stages **188, 190** and **192.** Counter **188, 190, 192** is connected to operate in true binary fashion rather than in binary coded decimal fashion whereby the outputs on output leads **194** will comprise a binary representation of the line length as theretofore contained in binary coded decimal form in accumulator counter **60–66.** Thus, as accumulator counter **60–66** is counted downwardly, binary counter **188, 190, 192** is counted upwardly to the same value in binary notation. At this time, the binary stages **188, 190, 192** are enabled from latch **148** via lead **196.**

The input from the first counter stage of counter **86** delivered on lead **186** is actually a half-unit count. Thus, two outputs are provided on lead **186** for every output supplied to decade **60** via NAND gate **92.** Consequently, the output leads **194,** starting from the bottom, would indicate the binary values for one-half through **1024.** The binary values from one-half through **16** are supplied to NAND gates **198,** while binary outputs from **32** through **1024** are supplied to NAND gates **200.**

When NAND gate **156** is enabled and NAND gate **154** is disabled from counter **150,** NAND gates **198** are enabled via capacitor **202** and inverting amplifier **204.** Therefore, binary values from one-half unit through **16** units will be provided on the output leads of NAND gates **198.** It is convenient to provide this first set of binary values to the perforator **14** on six leads so that the first part of the line length punching can be punched in a row by the perforator **14.** When such punching takes place, a data signal is provided from the perforator **14** on lead **206.** This merely indicates that the perforator **14** has operated. The output on lead **206** energizes NOR gate **178** and steps counter **150** by one step. Thereupon, NAND gate **158** is energized in place of any of the other NAND gates **154–160.** Therefore, NAND gates **200** are enabled via capacitor **207** and inverting amplifier **209.** Consequently, the higher order binary digits will then be provided to the perforator **14** for another punching. As this is accomplished, lead **206** is energized again for again stepping counter **150.** NAND gate **160** is then energized and resets latch **148** by way of capacitor **211.** The binary counter **188, 190, 192** is reset via lead **196,** and the cycle is complete. Thereupon, the line length may be reentered into accumulator counter **60–66** by means of pushbutton **78,** and the keyboard **10** may be operated in the usual manner for punching the information for a line of type on the paper tape in the perforator **14.**

In a number of instances, it may be desirable to delete a word or a character which has already been punched in the tape by the perforator **14.** Ths is conventionally done, as is well known in the art, by backing up the perforator **14** and punching all holes for each of the character rows where the information is no longer desired. Thus, an incorrect character, word, or the like, can be deleted by reverse feeding the perforator **14** and providing a delete designation from the keyboard **10** to the perforator **14.** Unfortunately, such action would deleteriously affect the operation of the apparatus for indicating the remaining line length or for providing an indication when a justifiable length remains in a line. Therefore, circuitry is provided for altering the remaining length of line count in accumulator counter **60–66,** in accordance with those character and word deletions which are accomplished. Referring again to the diagram, and especially to FIG. **2,** the instance of deletion of a single character will first be considered.

A character counter comprises binary counters **208, 210** connected in substantially the same fashion as the decades of accumulator counter **60–66.** Thus, character counter **208, 210** operates in binary fashion with the lower order digit being counted in binary counter **208** and the higher order digit being counted in binary counter **210.** The counting input for character counter **208, 210** is provided from clock signal generator **36** via lead **212,** and NAND gate **214** is normally enabled from inverting amplifier **216** whereby character counter **208, 210** will count upwardly at the same time accumulator counter **60–66** counts downwardly. It is noted the output of inverting amplifier **216** is also applied for energizing NAND gate **92** by way of lead **218** so that accumulator counter **60–66** normally operates in the down-counting mode as hereinbefore described. Thus, during the execution of a line, the incremental count for each character, actually in quarter units, is entered into character counter **208, 210.** It is also noted that lead **218** is normally high for supplying a remaining input to NAND gate **56.**

Each time perforator **14** operates, a data output indication is provided on lead **220** which resets character counter **208, 210.** The data output on lead **220** brings about a negative going output from amplifying and shaping circuitry **222** whereby the output of NAND gate **224** goes high, resetting character counter **208, 210** via lead **226.** As a consequence, the character counter **208, 210** is normally reset before the next character count is received.

When the operator decides to remove a character, a reverse feed function is first initiated by him which causes a reverse feed signal on lead **230** from the perforator **14.** This signal sets latch **232** which may comprise a flip-flop circuit. A code delete will then be provided by the operator employing keyboard **10** supplying a code delete signal on lead **228.** The code delete signal on lead **228** together with the output of latch **232,** both being negative going signals, bring about a positive going output from NOR gate **234** which is inverted in inverting amplifier **236.** The resulting negative going signal sets character delete latch **238,** the latter suitably comprising a flip-flop circuit. The latch **238** provides one of the signals for NOR gate **240** and when one such signal is present, the output of NOR gate **240** drops. This output is inverted by inverting amplifier **242** providing a positive going signal on lead **244.** The latter energizes NAND gate **246** while at the same time disabling NAND gate **214.** When NAND gate **246** is energized in place of NAND gate **214,** character counter **208, 210** is enabled to count down to zero from the character incremental width indication as resides in character counter **208, 210.** This positive signal on lead **244** is applied to NAND gate **90** in FIG. **1** energizing the same, while NAND gate **92** in FIG. **1** is deenergized as lead **218** goes low. The same negative going signal at NAND gate **56** causes clock signal generator **36** to provide a train of pulses, but instead of counting down accumulator counter **60–66** in the usual manner, such chain of pulses causes accumulator counter **60–66** to count upwardly. Thus, NAND gate **90** is now energized instead of NAND gate **92** and consequently the operation of accumulator counter **60–66** reverses. Inasmuch as the normal character perforated on the tape has the effect of reducing the count in accumulator counter **60–66** so that an indication of the remainder of the line would be given, it is seen that the deletion of such character should have the reverse effect on the accumulated count, i.e., should increase the accumulated count and the indication provided by display means **18.** Counting continues until the character counter **208, 210** in FIG. **2** counts to zero as indicated by two borrow inputs from binary counters **208** and **210** detected by NOR gate **245.** The output of NOR gate **245** is inverted by inverting amplifier **248** for resetting latch **238** via lead **250.** Of course, when latch **238** is reset, the normal level on lead **244** is restored whereby accumulator counter **60–66** can count downwardly, and character counter **208, 210** can count upwardly. At the end of the sequence of events, operation may continue accurately toward a justifiable line indication. The presence of any data, punched by the perforator **14,** resets latch **232** by means of lead **206.**

Considering the circuitry for word deletion, a counter comprising binary counters **252, 254** and **256** parallels the operation of character counter **208, 210,**

receiving the same inputs as character counter **208, 210,** and also operating in a binary manner. However, counter **252, 254, 256** is not reset at the end of every character, but rather is reset at the end of every word. Consequently, a space band signal is received from the keyboard **10** on lead **258.** This signal is negative going and causes a positive output from NAND gate **260** which resets counter **252, 254, 256.** However, after a slight delay provided by delay and shaping circuitry **262,** the incremental width indicated for the space band is entered from the binary counter **208** into binary counter **252** on leads **264** with a strobe input for binary counter **252** being provided on lead **266.** This loads the space band incremental width count into the counter **252, 254, 256** at the start of each word, inasmuch as when a word is deleted, it is considered as including the space at the beginning of the word and it is desired to "back up" accumulator counter **60–66** to the end of the previous word. It is also seen that an end-of-line signal on lead **280** resets both character counter **208, 210** and counter **252, 254, 256.**

In the case of deleting a word, an additional counter, not shown, may be provided for use with perforator **14.** This counter simply counts the number of characters or letters in each word and resets at each space band after which a one is entered. If the operator then wishes to delete a character he may do so automatically by providing a code whereby the perforator **14** backs up the number or rows designated by such counter and punches all holes in the locations of the deleted word. The same function could, of course, be accomplished manually by backing up the perforator **14,** and punching all holes where the word is located. The additional counter does not form a part of the present invention.

When a word delete function, e.g. an automatic word delete as above described, is indicated by the operator on keyboard **10,** a word delete signal is provided on lead **268** from the keyboard **10,** and word delete latch **270** is set thereby. Latch **270** suitably comprises a flip-flop circuit. The output of latch **270** operates NOR gate **240,** as in the case of character delete, whereby counter **252, 254, 256,** and accumulator counter **60–66** are prepared for counting in directions reversed to their usual directing of counting. Character counter **208, 210** is reset via amplifying and shaping circuitry **271** and NAND gate **224.** Also, clock signal generator **36** is again initiated in operation by a signal on lead **218.** Thereupon, counter **252, 254, 256** counts downwardly while accumulator counter **60–66** counts upwardly until counter **252, 254, 256** reaches zero. Then, the borrow signals provided inverting amplifiers **272, 274, 276** together bring about an output via inverting amplifier **278** for resetting latch **270.** Accumulator counter **60–66** will count upwardly until the deleted word is accounted for.

In the event that the operator should attempt to overrun, or provide a line which cannot be set by the typesetter, the accumulator counter **60–66** will run down to zero. This situation is generally to be avoided, and consequently a NAND gate **282** is provided in FIG. **1** which receives the borrow signal on line **170,** as well as a similar indication via inverting amplifier **172** from the second stage of counter **86.** A second input to the NAND gate **282** comprises the output of the first stage of counter **86.** In the event of oversetting, NAND gate **282** detects the presence of a number fractionally less than zero in the line length minus the total accumulated incremental widths and provides an indication via indication means **284.** Also an output is provided on lead **286,** the function of which is to lock up the keyboard **10** and the perforator **14** so that the character that caused overset and further characters cannot be entered in the line by keyboard **10.** However, a new line can be started.

Referring to FIG. **3,** one of the switches **58** is illustrated in greater detail. Such switch **58** may suitably comprise a plurality of ganged switch sections **310, 312, 314** and **316,** with the movable contacts being connected to provide the inputs for decade **66.** Selected of the switch fixed contacts are connected together and are grounded such that in selected switch positions, ones of the inputs to decade **66** are grounded. The arrangement is such that the switches **58** provide a binary coded input to the decade **66,** wherein switch section **310** provides the lowest order digit. For the zero setting of the switch **58,** none of the sections **310, 312, 314, 316** ground any of the inputs to decade **66.** For a "one" setting, section **310** provides a grounded input on the lowest order digit wire. For position two, switch section **312** provides a grounded input to the second order decade counter input wire. For switch position three, both sections **310** and **312** provide grounded inputs on their respective wires connected to decade **66,** and so on in binary fashion. Obviously, this type of switching may be implemented in any similar manner so far as physical structure is concerned.

In operating the present apparatus, the operator first selects the number of units per line by means of switches **58,** as hereinbefore mentioned. The number of units entered for the line length will, of course, be dependent upon the column measure intended, and will be dependent upon the point size of the type. In a particular embodiment of the present invention, the individual incremental unit was selected to be one-eighteenth of an em, i.e., there were 18 units to the em. The units per pica are determined by dividing the number **216** by the point size of the type, the point size being implemented in the present circuit by the read-only-memory **22** selected. Thus, for a particular point size type, the ems per pica will be predetermined. The actual line length in picas per line is determined from actual measurement, with each pica being equal to one-sixteenth inch. The units per line, to be entered by means of switches **58,** are calculated and equal to units per pica (for the particular font of type) multiplied by the picas per line (as actually measured). Thus, suppose there are **36** units per pica in a given instance corresponding to 6-point type. Let us also suppose that the column measure happens to be 18 picas. Then, the number set into switches **58** equals 36×18 or 648 units.

Referring to FIG. **4,** an example of a read-only-memory **22** is illustrated. This memory **22** comprises a word-select matrix **288** receiving a character code on leads **20** and energizing a selected lead **290** in response thereto. Word-select matrix **288** is typically a diode matrix wherein a given input code comprising a given combination of inputs on input leads **20** will select one of the output leads **290.** An additional input **318** is typically provided for shifting between upper and lower case letters, while a further input **320** selects between a pair of type font "magazines." One of the output

leads **290** can be selected by an exclusive-AND function in a conventional manner from an input code. The codes for different characters and for a space band will each select a different one of leads **290.** In the particular instance illustrated, word-select matrix **288** may select one of **256** output leads **290,** designated C_1, C_2 . . . C_n. The word-select matrix **288** is employed for addressing memory matrix **292** which includes transistors **294, 296 . . . . 298** connected at their bases to the respective input leads **290.** It is understood that other transistors are similarly coupled to the remaining, intervening ones of the **256** inputs. The transistor collectors are coupled to a source of voltage, and the emitters are provided with memory elements **300, 302 . . . . 304,** respectively, wherein these memory elements **300, 302 . . . 304** may comprise a fusible link which can be "programmed." The memory elements are connected in common to the base of output transistor **306** having its base returned to its emitter by input resistor **308,** having its emitter coupled to a source of voltage, and having its collector connected to one of the output leads **24,** here numbered **24'**. A similar memory matrix **292** exists for each one of the output leads **24, 26.** In the memory **22** illustrated, the presence of a memory element **300, 302 . . . 304** provides a "zero" output and its absence will provide a "one" output. To eliminate one of the memory elements **300, 302 . . . 304** permanently, for "programming" the unit, a predetermined negative current is applied to the corresponding output terminal where a one output is desired corresponding to a particular input code, which is simultaneously applied on leads **20.** An open circuit will result at the location of a memory element **300, 302 . . . 304** coupled to such output terminal and representing, in binary form, a digit of the character code applied.

It is understood that one of the input leads **290** will connect to corresponding transistors **294, 296 . . . 298** in each memory matrix **292** whereby every output combination is initially possible. Clearly, the read-only-memory **22** can be implemented as one integrated circuit unit including **256** addressing leads **290,** or may alternatively comprise a plurality of smaller integrated circuit memories employed together and selectively enabled.

While I have shown and described a preferred embodiment of my invention, it will be apparent to those skilled in the art that many changes and modifications may be made without departing from my invention in its broader aspects. I therefore intend the appended claims to cover all such changes and modifications as fall within the true spirit and scope of my invention.

What is claimed is:

1. A system for generating output information for presentation to a typesetting device and for accumulating the widths of successive characters as selected by a keyboard for indicating the line length remaining, said apparatus comprising:

a keyboard,

tape producing means for receiving the code for each character from said keyboard for generating a tape for providing the input to said typesetting device,

memory means receiving the code for each character substantially simultaneously with tape production, directly from said keyboard, for accessing the incremental width of the character as a digital output number, said memory means comprising a read-only-memory for supplying digital output numbers in response to character code inputs in at least one font of type,

an accumulator counter comprising a plurality of electronic register stages including means for presetting said stages to a digital value representative of a predetermined line length,

circuitry means responsive to said digital output number of said memory means for changing the digital value in said accumulator counter in accordance with the digital output number representative of each character to establish in said accumulator counter a value representative of the line length as successively reduced by such digital output number from the memory means,

decimal readout means for digitally indicating the value in said accumulator counter, said decimal readout means comprising a plurality of visible digital display units which are respectively responsive to the contents of said register stages,

means responsive to successive space indications from said keyboard for accumulating allowable space band expansion,

comparator means for comparing the accumulated allowable space band expansion and the value in said accumulator counter representative of the line length remaining, and indicator means responsive to equality of the two values compared in said comparator means for indicating a justifiable line.

2. The apparatus according to claim **1** wherein said read-only-memory comprises a semiconductor matrix including memory means rendered inoperative for establishing digital output patterns responsive to character codes entered from said keyboard.

3. In a system for generating output information for presentation to a typesetting device, an apparatus for accumulating the widths of successive characters as selected by a keyboard and for indicating the line length remaining, said apparatus comprising:

memory means receiving each character code directly from said keyboard for accessing the incremental width of the character represented by said code in at least one font of type and for providing said incremental width as a digital output, said memory means comprising a read-only-memory for supplying digital outputs in response to character code inputs,

an incremental width counter directly receiving each said digital output in parallel from said memory means for setting said incremental width counter at a value representative of each digital output,

an accumulator counter comprising a plurality of electronic register stages including means for presetting said stages to a decimal digital value representative of a predetermined line length, signal generator means responsive to the entry of characters from said keyboard for providing an input to both said incremental width counter and said accumulator counter for counting said incremental width counter a number of counts indicative of said incremental width digital output entered therein from said memory means, said signal generator means at the same time counting said accumulator counter for establishing in said accumulator counter a value representative of the predetermined line length as successively reduced by each said digital output,

decimal readout means operated by said accumulator counter for continuously supplying a numerical output indicative of said reduced line length, said decimal readout means comprising a plurality of visible digital display units which are respectively responsive to the contents of said register stages,

means responsive to a space band indication transmitted from said keyboard for providing an output signal representative of the incremental count for the maximum expansion allowed for a single space band,

a register for receiving said maximum expansion incremental count for each space band and accumulating a value representative of such maximum expansion incremental count multiplied by the number of space bands in a line,

comparator means for comparing the value in said register and in said accumulator counter and providing an output when the values in said register and said accumulator counter become equal or the value in said accumulator counter becomes less than the value in said register,

and indicator means responsive to the output of said comparator means for indicating a justifiable line.

4. The apparatus according to claim **3** wherein said memory means comprises a matrix of semiconductor means connected to supply standard digital outputs in response to input codes, ones of said semiconductor means being programmed in accordance with the character widths for a given font or fonts of type to access digital outputs representative of the incremental widths of characters selected.

5. The apparatus according to claim **4** wherein said memory means also includes means responsive to space band indications from said keyboard to provide a digital output in response thereto in accordance with the predetermined minimum space band incremental width.

6. The apparatus according to claim **4** wherein said matrix of semiconductor means includes programmable memory elements, ones of said elements having been programmed to be nonconductive leaving a matrix of elements making connections for providing digital outputs indicative of said font or fonts of type.

7. In a system for generating output information for presentation to a typesetting device, an apparatus for accumulating the widths of successive characters as selected by a keyboard and for indicating the line length remaining, said apparatus comprising:

means responsive to said keyboard for providing as an output incremental width information for each character selected by said keyboard,

an accumulator counter including means for presetting said counter to a value representative of a predetermined line length,

circuitry means responsive to said incremental width information for each character for changing the value in said accumulator counter in accordance with the incremental width of each character to establish in said accumulator counter a value representative of the line length as successively reduced by such incremental width information,

output means for indicating the value in said accumulator counter, and including means for indicating a justifiable line,

separate counter means for also receiving and counting incremental width information at the same time the said value in said accumulator counter is changed, said separate counter means being reset at the end of a character,

means for reverse counting said separate counter means in accordance with copy which it is desired to delete,

and means for simultaneously counting said accumulator counter to remove width information relative to deleted copy.

8. The system according to claim **7** further including additional separate counter means for also receiving incremental width information, said additional separate counter means being reset at the end of a word,

means for reverse counting said additional separate counter means in accordance with copy which it is desired to delete,

and means for simultaneously counting said accumulator counter to remove width information relative to deleted copy.

9. In a system for generating output information for presentation to a typesetting device, an apparatus for accumulating the widths of successive characters as selected by a keyboard and for indicating the line length remaining, said apparatus comprising:

memory means receiving each character code from said keyboard for accessing the incremental width of the character represented by said code in at least one font of type and for providing said incremental width as a digital output,

an incremental width counter directly receiving each said digital output in parallel from said memory means for setting said incremental width counter at a value representative of each digital output,

an accumulator counter comprising a plurality of electronic register stages including means for presetting said stages to a decimal digital value representative of a predetermined line length,

signal generator means responsive to the entry of characters from said keyboard for providing an input to both said incremental width counter and said accumulator counter for counting said incremental width counter a number of counts indicative of said incremental width digital output entered therein from said memory means, said signal generator means at the same time counting said accumulator counter for establishing in said accumulator counter a value representative of the predetermined line length as successively reduced by each said digital output,

decimal readout means operated by said accumulator counter for continuously supplying a numerical output indicative of said reduced line length, said decimal readout means comprising a plurality of visible digital display units which are respectively responsive to the contents of said register stages,

and means for providing an output in binary form indicative of a line length as may be initially preset into said accumulator counter comprising: a binary counter receiving the output of said signal generator means for operating said signal generator means for initially counting said accumulator counter a number of counts indicative of the line length value preset therein, and output gating means for providing the output of said binary counter as an initial part of said output information

for a typesetting device, after said accumulator counter has been counted a number of counts indicative of the line length value preset therein.

10. In a system for generating output information for presentation to a typesetting device, an apparatus for accumulating the widths of successive characters as selected by a keyboard and for indicating the line length remaining, said apparatus comprising:

memory means receiving each character code from said keyboard for accessing the incremental width of the character represented by said code in at least one font of type and for providing said incremental width as a digital output,

an incremental width counter directly receiving each said digital output in parallel from said memory means for setting said incremental width counter at a value representative of each digital output,

an accumulator counter comprising a plurality of electronic register stages including means for presetting said stages to a decimal digital value representative of a predetermined line length,

signal generator means responsive to the entry of characters from said keyboard for providing an input to both said incremental width counter and said accumulator counter for counting said incremental width counter a number of counts indicative of said incremental width digital output entered therein from said memory means, said signal generator means at the same time counting said accumulator counter in a first counting direction for establishing in said accumulator counter a value representative of the predetermined line length as successively reduced by each said digital output,

decimal readout means operated by said accumulator counter for continuously supplying a numerical output indicative of said reduced line length, said decimal readout means comprising a plurality of visible digital display units which are respectively responsive to the contents of said register stages,

and circuitry for altering the count in said accumulator counter in accordance with characters and words deleted under the direction of said keyboard, said circuitry comprising:

separate counter means responsive to said signal generator means for counting the number of increments in each word and character at the same time as said signal generator means provides an input to said accumulator counter, said separate counter means being reset at the end of each such word and character respectively,

means for reverse counting said separate counter means in accordance with the word or character which it is desired to delete,

and means for simultaneously reversely counting said accumulator counter from said first counting direction until said reverse counting of said separate counting means has been accomplished.

* * * * *

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,805,940 Dated April 23, 1974

Inventor(s) William M. Stockham

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 4, line 51, "Amlifier" should be --Amplifier--.

Column 5, line 14, after "width" insert --counter--.

Column 5, line 35, "stroke" should be --strobe--.

Column 12, line 48, "sixteenth" should be --sixth--.

Signed and sealed this 5th day of November 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

FORM PO-1050 (10-69)

USCOMM-DC 60376-P69
* U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,805,940 Dated April 23, 1974

Inventor(s) William M. Stockham

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 4, line 51, "Amlifier" should be --Amplifier--.

Column 5, line 14, after "width" insert --counter--.

Column 5, line 35, "stroke" should be --strobe--.

Column 12, line 48, "sixteenth" should be --sixth--.

Signed and sealed this 5th day of November 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

FORM PO-1050 (10-69)

USCOMM-DC 60376-P69
☆ U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334