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 [21] Appl. No. **20,964**
 [22] Filed **Mar. 19, 1970**
 [45] Patented **Dec. 7, 1971**
 [73] Assignee **Sperry Rand Corporation**

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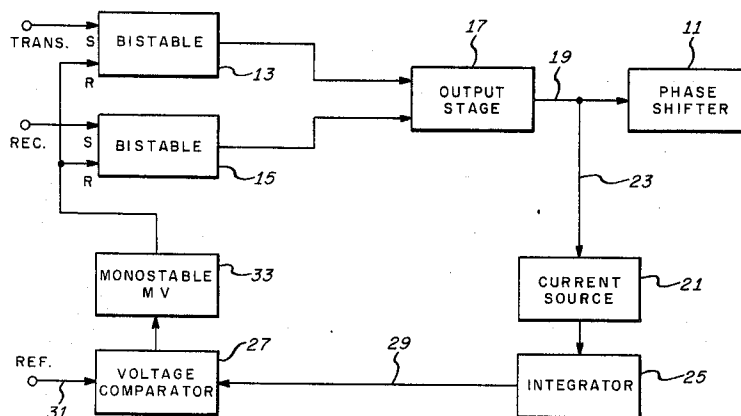
[54] **ELECTRONIC DRIVE CIRCUIT**
5 Claims, 2 Drawing Figs.

[52] U.S. Cl. **307/262,**
307/247, 307/270
 [51] Int. Cl. **H03k 17/00**
 [50] Field of Search. 307/270,
247, 254, 262, 266, 270, 276; 317/75 E

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ABSTRACT: An electronic drive circuit for a microwave ferrite phase shifter includes a single output stage to drive the phase shifter to a specified level of magnetization of either polarity. Bistable circuits permit the output stage to magnetize the phase shifter in one polarity or the other in response to first or second command signals respectively. A signal indicative of the absolute value of the instantaneous voltage being applied to the phase shifter is integrated and compared to a reference voltage. When the integrated signal reaches a prescribed level, a monostable multivibrator is actuated and the magnetization current to the phase shifter is terminated.



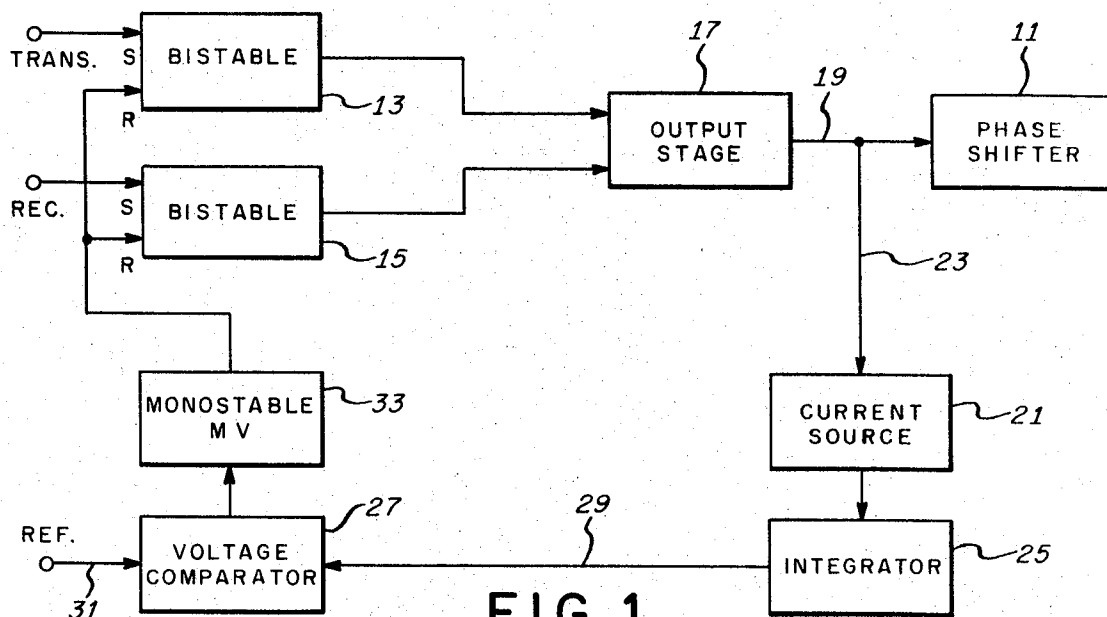


FIG. 1.

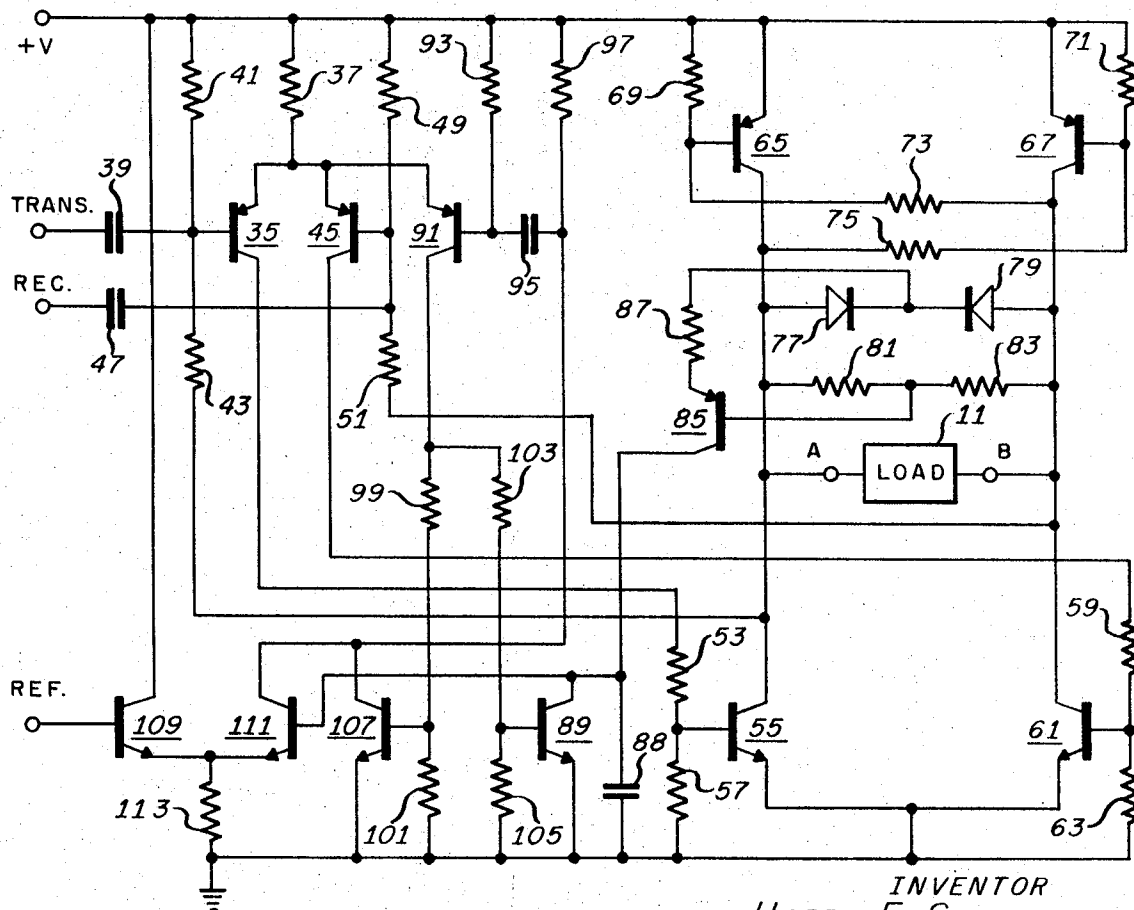


FIG. 2.

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ELECTRONIC DRIVE CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a drive circuit for microwave phase shifters and more particularly to a symmetrical drive circuit for digital nonsaturating ferrite phase shifters.

2. Description of the Prior Art

Microwave phase shifters are well known in the art. Many of these devices employ a ferrite material in conjunction with a section of waveguide. Magnetization of the ferrite causes a desired phase shift in a microwave signal propagating through the waveguide. Such phase shifters have great utility, for instance, in phased array antennas wherein the phase of the signal applied to each element of the array is adjusted in order to "steer" the beam of energy to be transmitted or received.

The accuracy and repeatability of such systems are largely determined by the characteristics of the drive circuit used to magnetize the ferrite material. Typically, the drive circuit must not only drive the microwave load but must also interface with the system command while compensating for otherwise uncompensated load parameters under both transmit and receive conditions.

Both saturating and nonsaturating phase shifters are available. However, the nonsaturating types are frequently preferred since they require minimum switching time and minimum drive power. Furthermore, they have the ability to correct phase shift by varying the drive in order to compensate for ferrite material variations. The phase shift produced in such nonsaturating devices depends critically on the voltage-time product of the switching pulse applied to the shifter. The insertion phase shift is critically dependent upon the equality of the above voltage-time product for both possible directions of switching. If a drive circuit output signal is asymmetrical, the resulting phase shift will be different for the transmit and receive modes and beam "steering" will be impaired.

Conventional drivers for such phase shifters use a single delay circuit, such as a monostable multivibrator which is gated to drive one or another of the two output stages depending upon the polarity desired. Because these systems require two output stages, there is no known practical way for efficiently eliminating the effect of asymmetry in the output stages.

Still other prior art drivers use a separate monostable multivibrator for each polarity of output signal, and adjust these multivibrators for the desired symmetry. However, if the temperature drift characteristics of the monostable multivibrators are not precisely matched, the symmetry is not maintained over a reasonable temperature range.

SUMMARY OF THE INVENTION

The phase shifter driver of the present invention produces highly symmetric drive pulses by utilizing a single timing circuit and a single sensor to sense the absolute value of the actual voltage being delivered to the load. When the voltage-time integral reaches a specified absolute value, the timing circuit is actuated to terminate the drive pulse.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram useful in explaining the principles of the invention, and

FIG. 2 is a circuit diagram illustrating a presently preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, a ferrite phase shifter 11 is actuated in response to a transmit command signal applied to a first bistable circuit 13 or to a receive command signal applied to a second bistable circuit 15. When a command signal of either type is received, the corresponding bistable circuit is triggered into its SET state so as to actuate an output stage 17. The output stage supplies a suitable charging voltage through

a line 19 to the load comprising the phase shifter 11. The voltage applied to the phase shifter is sampled and applied to a current source 21 through a line 23. The current source provides a current having a magnitude proportional to the voltage applied to the phase shifter.

The voltage applied to the phase shifter has a polarity depending upon the type of input signal. Thus, the voltage applied to the phase shifter will have a first polarity in response to a transmit command signal and a second polarity in response to a receive command signal.

The current source 21, however, provides an output current having magnitude indicative of the absolute value of the voltage applied to the phase shifter 11. The current source applies a current to an integrator 25. The polarity of this current is independent of the polarity of the voltage applied to the phase shifter.

The output of the integrator 25 is applied to a voltage comparator 27 through a line 29. A reference voltage is also applied to the voltage comparator through a line 31. The reference voltage may be programmed in a desired fashion or maintained at a steady value depending upon the needs of the particular operation. When the integrated voltage approaches the reference voltage, an output signal is applied to a monostable multivibrator 33, driving the monostable multivibrator into its quasi-stable state. The output of the monostable multivibrator is applied to reset terminals on the bistable circuits 13 and 15 so as to return these circuits to the RESET state.

In this manner, a single timing circuit is used to provide a voltage-time integral of the voltage actually applied to the phase shifter. Since the same timing circuit is used for both the transmit and the receive modes of operation, the drive signal applied to the phase shifter is symmetrical.

The details of the circuit can be better understood by referring to the circuit diagram of FIG. 2. An input transistor 35 has its emitter electrode connected to a positive voltage source through a resistor 37. Transmit command signals are applied to the base of the transistor 35 through a blocking capacitor 39. The base electrode of the transistor 35 is coupled to the positive source of voltage through a resistor 41 and to the output stage of the driver circuit through a resistor 43.

A receive command signal is coupled to a second input transistor 45 through a blocking capacitor 47. The capacitor 47 is connected directly to the base electrode of the transistor 45. The base electrode of the transistor 45 is further connected to the positive voltage source through a resistor 49 and to the output stage of the driver circuit through a resistor 51. The emitter electrode of the transistor 45 is connected to the positive source of voltage through the resistor 37.

The collector electrode of the transistor 35 is connected through a resistor 53 to the base electrode of a transistor 55 and then through a resistor 57 to ground. The transistors 35 and 55, together with their associated resistors, form the first bistable circuit 13 of FIG. 1 that is actuated by a transmit command signal.

The collector of the transistor 45 is connected through a resistor 59 to the base electrode of a transistor 61 and then through a resistor 63 to ground. The transistors 45 and 61, together with their associated resistors, form the second bistable circuit 15 of FIG. 1 that is actuated by a receive command signal.

A pair of output transistors 65 and 67 have their emitter electrodes connected directly to the positive source of voltage and their base electrodes connected to the same source of voltage through the resistors 69 and 71 respectively. The base electrode of the transistor 65 is connected to the collector electrode of the transistor 67 through a cross-coupling resistor 73 and the base electrode of the transistor 67 is connected to the collector electrode of the transistor 65 through a cross-coupling resistor 75.

A first diode 77 and a second diode 79 are connected in series opposition between the collector electrodes of the transistors 65 and 67. First and second resistors 81 and 83 are also connected between the collector electrodes of the

transistors 65 and 67. The ferrite phase shifter load 11 is connected through terminals A and B to these same two electrodes.

The voltage at the junction between the diodes 77 and 79 is applied to the emitter electrode of a current source transistor 85 through a resistor 87. The base electrode of the current source transistor 85 is connected to the junction between the resistors 81 and 83. The collector electrode of the transistor 85 is connected directly to an integrating capacitor 88. A discharge transistor 89 is connected directly across the capacitor 88.

A transistor 91 has its emitter electrode connected directly to the emitter electrodes of the transistors 35 and 45 and its base electrode coupled through a resistor 93 to the positive voltage source and through a capacitor 95 and a resistor 97 to the same positive voltage source. The collector electrode of the transistor 91 is connected through a first pair of resistors 99 and 101 and a second pair of resistors 103 and 105 to ground.

The junction point between the resistors 103 and 105 is connected to the base electrode of the discharge transistor 89.

The junction between the resistors 99 and 101 is connected to the base electrode of a transistor 107. The emitter electrode of the transistor 107 is connected directly to ground and the collector electrode of the transistor 107 is connected directly to the capacitor 95.

A pair of comparator transistors 109 and 111 have their emitter electrodes connected to ground through a common emitter resistor 113. The base electrode of the transistor 109 is connected to receive a reference voltage and the base electrode of the transistor 111 is connected to receive an integrated voltage from the integrator capacitor 88. The collector electrode of the transistor 109 is connected directly to the positive source of voltage whereas the collector electrode of the transistor 111 is connected directly to the collector electrode of the transistor 107, the capacitor 95, and the resistor 97.

The transistors 55, 61, 65 and 67 together with the resistors 69, 71, 73 and 75 form the output stage 17 of FIG. 1.

The diodes 77 and 79 together with the resistors 81, 83 and 87 cooperate with the transistor 85 to form the current source 21 of FIG. 1. This current source delivers a current to the capacitor 88 which is closely proportional to the voltage across the load 11, but independent of the polarity of this voltage.

The integrating capacitor 88 accumulates a charge indicative of the voltage-time integral of the voltage charge applied to the phase shifter load 11.

The discharge transistor 89 serves to discharge the integrating capacitor at the end of a load energizing cycle.

The transistors 109 and 111 together with the resistor 113 form the voltage comparator 27 of FIG. 1.

The transistors 91 and 107 together with the resistors 93, 97, 99 and 101 form the monostable multivibrator 33 of FIG. 1.

The monostable multivibrator is driven into its quasi-stable state when the comparator produces a switching signal. While the monostable multivibrator remains in this state, it clamps the bistable circuits in their RESET state so that any spurious command signals arriving during this time are rendered ineffective.

The transistors 55, 65, 67 and 71, together with their associated components, effectively form a bridge circuit which is balanced in the absence of an input signal so that no current flows through the phase shifter load 11 under these conditions. A command signal causes the bridge to become unbalanced in a direction indicative of the type of command signal.

If, now, a negative-going transmit command pulse is received, the first bistable circuit including the transistors 35 and 55 are forward biased. The collector voltage on the transistor 55 drops, and causes the transistor 67 to increase in conductivity so that current passes through the phase shifter load 11 from terminal B to terminal A.

Under these conditions, the transistor 85 becomes forward biased and delivers a current that is proportional to the voltage across the phase shifter load 11. This current charges the integrating capacitor 88. When the charge on capacitor 88 reaches a value nearly equal to the reference voltage, the comparator transistor 111 is quickly driven into conduction, causing a voltage to suddenly appear across the resistor 97. The voltage change across the resistor 97 is applied to the base electrode of the monostable multivibrator transistor 91 through the capacitor 95 which acts to turn off the bistable circuit, thus terminating the voltage being applied to the phase shifter load 11.

At the same time, the positive pulse developed at the collector electrode of the transistor 91 increases the voltage on the base electrode of the discharge transistor 89 so as to cause the discharge transistor to saturate and discharge the integrating capacitor 88.

At the end of the monostable multivibrator period, the transistors 91 and 107 cease conducting and driver circuit is able to accept another trigger signal.

The foregoing explanation has assumed that a transmit signal was received. It will be understood that a similar sequence of events will occur in response to the reception of a receive command signal except that the second bistable circuit including the transistors 45 and 61 will be triggered and the voltage developed across the load will be of the opposite polarity. By matching the diodes 77 and 79 and the resistors 81 and 83, the voltage-time product of pulses of either polarity are equalized.

Because the circuit of FIG. 2 employs a common timing mechanism for both the transmit and receive modes of operation, the problem of closely matching two delay circuits is eliminated. Furthermore, the derivation of the timing current from the voltage actually applied to the load eliminates errors in symmetry. In prior art circuits such asymmetry was caused by unequal drops across the output transistors.

The length of the drive pulse in the circuit of the invention is controlled by converting the voltage actually developed across the load into an equivalent current.

Since the circuit terminates the voltage applied to the load when the integral reaches the reference value, the drive level is substantially independent of supply voltage and the voltage drop associated with the drive transistors.

The circuit employs direct coupled gates to connect the logic and the output stage so that noise triggers cannot turn on both output stages symmetrically.

The circuit provides accurate control of drive magnitude so as to provide reproducible temperature compensation and greatly reduced power supply voltage sensitivities.

It will be appreciated that although the circuit of FIG. 2 represents the presently preferred embodiment, variations of this circuit will be apparent to those skilled in the art. In some applications, for instance, it is possible to combine the function of the voltage comparator and the monostable multivibrator.

While the invention has been described in its preferred embodiment, it is to be understood that the words which have been used are words of description rather than limitation and that changes may be made within the purview of the appended claims without departing from the true scope and spirit of the invention in its broader aspects.

I claim:

1. A drive circuit for energizing a nonsaturating phase shifter comprising a normally balanced bridge, output terminals on said bridge for connecting an external phase shifter thereto, means to unbalance said bridge including first and second bistable circuits connected to be driven into their SET states in response to first and second command signals respectively, said bistable circuits being further connected to maintain said bridge in an unbalanced condition while the bistable circuit is in the SET state, means to produce an integrated signal indicative of the voltage-time integral of the voltage appearing across said output terminals in response to a command signal, and means to rebalance said bridge when the

magnitude of the integrated signal exceeds a given threshold, said means to rebalance the bridge including means to drive both bistable circuits to the RESET state.

2. The drive circuit of claim 1 wherein the means to produce an integrated signal includes a capacitor and a transistor connected to supply charging current to said capacitor, said transistor being biased in accordance with the absolute value of the voltage across said bridge output terminals.

3. The drive circuit of claim 1 wherein the means to rebalance the bridge includes a comparator circuit for comparing the magnitude of the integrated signal with a reference signal, said comparator further including means to produce a switching signal when the magnitude of the integrated signal approaches the magnitude of the reference signal, and

wherein said means to drive the bistable circuits to the RESET state includes means to couple a switching signal to both bistable circuits.

4. The device of claim 3 wherein the means to couple the switching signal to both bistable circuits includes a monostable multivibrator arranged to be triggered into its quasi-stable state in response to a switching signal, said monostable multivibrator being further arranged to clamp said bistable circuits in their RESET state while the monostable multivibrator remains in the quasi-stable state.

5. The device of claim 2 further including shorting means for shorting out said capacitor when the monostable multivibrator is triggered into its quasi-stable state.

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