United States Patent [19]

Klasing

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[45] **Oct. 2, 1973**

[54] **MONOLITHIC TIMER**

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[21] Appl. No.: **152,085**

Related U.S. Application Data

[63] Continuation of Ser. No. 752,576, Aug. 14, 1968, abandoned.

[52] **U.S. Cl.** ..... **340/384 E,** 340/309.1, 331/155, 307/294

[51] **Int. Cl.** **G08b 3/00**

[58] **Field of Search** ..... 340/384 E, 309.1, 340/309.4, 10; 320/1; 307/109, 253, 294, 297; 331/73, 155

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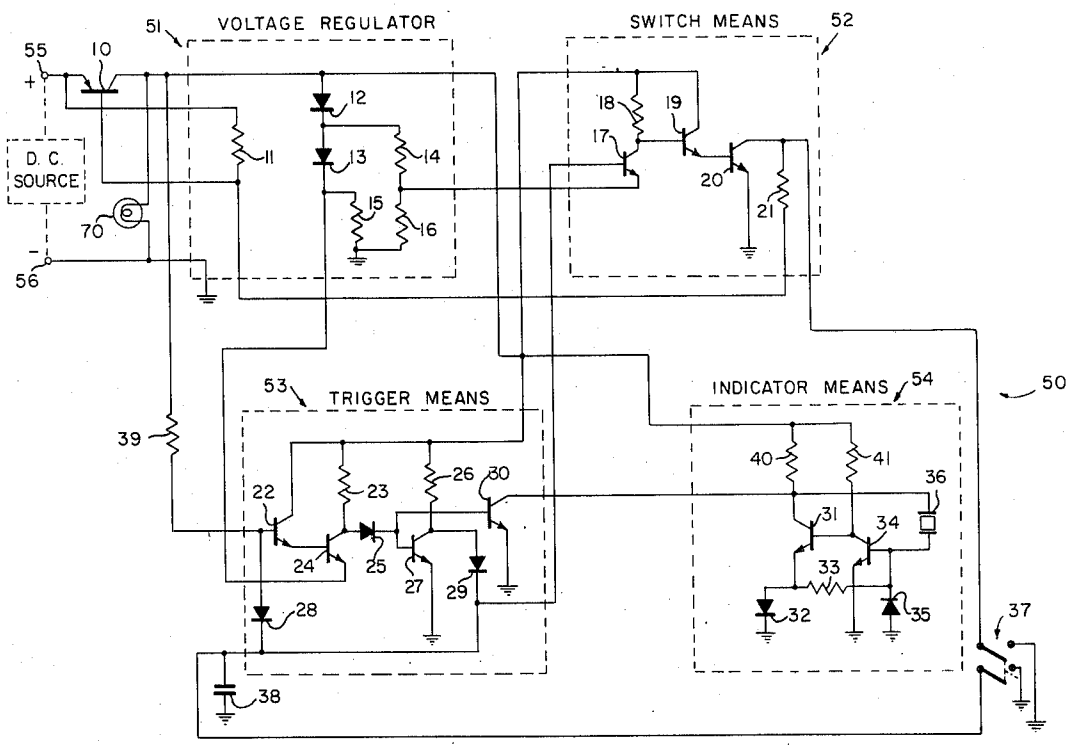
[57] **ABSTRACT**

An electronic timer including a piezoelectric device having a vibratory surface from which an audible sound is radiated. The initiation of the audible sound indicates the termination of a time interval.

29 Claims, 2 Drawing Figures



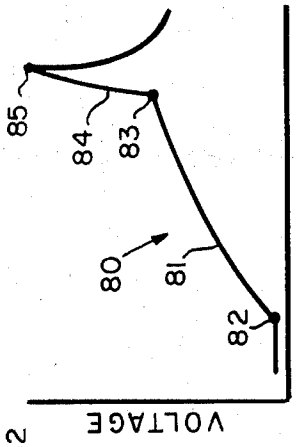


FIG. 2

FIG. 1

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MONOLITHIC TIMER

This is a continuation of application Serial No. 752,576 filed Aug. 14, 1968, now abandoned.

The present invention relates to alarm devices and more particularly to a monolithic or integrated circuit device which indicates the approach of or the end of a timing interval and a method for providing a timed interval.

Electronic timing devices have many uses. For example, electronic timing devices may be used to terminate energization of a device or indicate that the energization should be terminated in electrochemical devices such as appliances, that is, washing machines, dishwashers, dryers, radios, stoves and the like, in electronic devices such as sensing circuits, digital circuits and the like which require that certain functions be performed during a predetermined interval of time on a workpiece or which require that the equipment be allowed to function for a predetermined length of time and then de-energized.

In the processing of photographic materials, it is necessary that once the development of photographic film is initiated that the development of the print be accomplished within a specified time period or undesirable positive prints of the negative print may result. The development time is particularly acute where the solvent-transfer process is used to give direct positive prints in a camera itself. The optical system of the camera is conventional and exposes a negative material in the back of the camera. The negative material is wound into contact with a separate roll of paper material, using pressure rollers which burst a pod or capsule containing a thickened developer-silver halide solvent mixture which is spread as a thin layer between the two materials. The negative is developed in the exposed material, and the undeveloped silver halide is dissolved and transferred to the receiving sheet where it is reduced to silver to form a positive image. The process is used for obtaining black and white pictures in about 10 seconds. If, however, the development time in the camera is terminated by the premature removal of the positive print from the camera, the image on the positive print is pale due to the incomplete chemical action of the developer. If the positive print is permitted to remain in the camera for a period of time beyond that required for proper development of the positive print, the chemical action of the developer may cause the image to deteriorate providing a positive print having a faded image. In color film, if the film is either underdeveloper or overdeveloped, the colors are not precise, that is, one notes a color shift of the colors present on the positive print.

Mechanical timers may be used to indicate the time interval required to provide the proper development time of photographic film, whether black and white or colored, within the camera. Generally, the mechanical timer must be wound to be provided with stored energy sufficient to initiate operation of the timer, set to reflect the desired development time interval and manually released to initiate the timing interval. Either inadequate winding of the timer, improper setting of the timer, or improper release of the timer may have a harmful effect on the timing interval provided by the mechanical timer generally resulting in improper timing. In addition, the mechanical timer is generally separate from the camera and is bulky and inconvenient to carry with the camera.

Accordingly, it is an object of the present invention to overcome the above-enumerated problems.

An object of the present invention is to provide an electronic timer which provides an accurate timing interval and which indicates the approach of or the end of a timing interval.

Another object of the present invention is to provide an electronic timer having an audible alarm and timing means including capacitor means and means for switching the capacitor means in such a manner so as to vary the charging rate of the capacitor means during operation of the electronic timer.

A further object of the present invention is to provide an electronic timer including voltage regulator means compensating for variations in the voltage of a source of energy.

Yet another object of the present invention is to provide an electronic timer having an audible alarm means which is accurate in operation and economical to fabricate.

A further object of the present invention is to provide an electronic timer which is intergral with a camera for timing the interval of time required to develop film within the camera.

Another object of the present invention is to provide an electronic timer which is de-energized automatically at the end of a timing interval thereby conserving the power of the source.

Yet another object of the present invention is to provide an electronic timer which accurately provides intervals of time of about several seconds to several minutes or more.

Yet still another object of the present inventin is to provide an electronic timer which is substantially integrated onto a semiconductor chip.

Another object of the present invention is to provide an electronic timer which is small, lightweight and reliable.

A further object of the present invention is to provide an electronic timer which emits an audible sound from a piezoelectric device at about the end of a timing interval.

Another object of the present invention is to provide an integrated circuit electronic timer which includes a source of illumination which is illuminated at the initiation of a timing interval and extinguished at the end of a timing interval and which electronic timer further includes a means for emitting an audible sound at about the end of the timing interval.

A further object of the present invention is to provide a method for providing a timed interval.

In the accompanying drawing there is illustrated an embodiment of the invention from which these and other objects, features and advantages are apparent.

In the drawings:

FIG. 1 is an electrical schematic of an integrated circuit electronic timer which may be used with a camera which develops exposed film within the camera; and

FIG. 2 is a curve illustrating the charging rate of a timing capacitor connected to a first timing resistor and then to a second timing resistor.

Generally speaking, the present invention relates to an electronic timer means for emitting an audible sound signifying the end of a timing interval and a method for providing a timed interval. A timing means including timing capacitor means connected across a source of energy through a first timing resistor means.

The timing capacitor means is charged at a rate determined by the resistance value of the first timing resistor means. A trigger means, connected to the timing means, electrically disconnects the first timing resistor from the timing capacitor after the passage of a predetermined length of time and electrically connects a second timing resistor thereto thereby charging the timing capacitor at a rate determined by the resistance value of the second timing resistor means. An indicator means having an audible sound means emits an audible sound when the timing capacitor means is electrically disconnected from the first timing resistor and electrically connected to the second timing resistor. A means electrically disconnects the trigger means, the timing means and the audible sound means from the source of energy when the timing capacitor attains a determined charge magnitude thereby terminating the time interval of the electronic timer. The electronic timer may further include a voltage regulator means compensating for variations in the voltage of the source of energy so that the timing interval of the electronic timer is substantially unaffected by the voltage variations, if any.

Referring now to the drawing, and in particular, FIG. 1 of the drawing, an electronic timer which may be used wit and integrally connected to a camera (not shown) is illustrated by reference numeral **50.** The electronic timer includes PNP line switch transistor **10,** voltage regulator means **51,** switch means **52,** trigger means **53,** and indicator means **54** which emits an audible sound after a determined time delay. Input terminals **55** and **56** of the electronic timer are connected across any suitable direct current (DC) source such as a primary cell (not shown) and the like which converts chemical energy into electrical energy. Other DC sources which may be used to provide electrical energy are solar cells, photovoltaic cells and the like. Terminal **55** is illustrated as being the positive input terminal to the electronic timer whereas terminal **56** is shown as being the negative input terminal to the electronic timer. The transistor line switch **10** is a PNP transistor having the emitter connected to the positive terminal **55** and the collector connected to the voltage regulator means **51** and to the trigger means **53** through first timing resistor **39.** The base of the line switch transistor is connected through current limiting resistor **21** of the switch means **52** to a suitable switch such as double pole, single throw switch **37.** The switch **37** may take any one of several acceptable forms such as a push-button switch. When the switch **37** is actuated by any suitable means such as manually by an operator, the transistor **10** has its base connected to ground through the current limiting resistor **21** and the actuated switch thereby driving the base voltage of PNP transistor in a negative direction biasing the transistor to conduction. The collector voltage of the transistor **10** is driven in a positive direction as the transistor is biased to conduction causing the other components of the circuit to be energized in the manner described hereinafter.

Current from the DC source flows through the conducting line switch transistor **10** to lamp **70** connected between the collector of transistor **10** and the negative input terminal **56** (ground) causing lamp **70** to be illuminated visually indicating the energization of the electronic timer. It should be noted that lamp **70** is illuminated at all times during conduction of the line switch transistor thereby indicating that the electronic timer is activated. Current also flows from the DC source through the timing resistor **39,** the series coupled DC blocking diode **28** and double pole, single throw switch **37** to ground. Timing capacitor **38** is connected to ground through the switch **37** when switch **37** is actuated so that residual voltage, if any, carried by the timing capacitor **38** may be discharged to ground through the switch **37.** The initial discharge of any residual voltage carried by the timing capacitor to ground insures that charging of the capacitor is initiated from substantially the same voltage point during each timing interval, i.e., generally about zero voltage.

As the collector voltage of line switch transistor **10** is driven in a positive direction due to the conduction of the transistor, the base voltage of NPN switchig amplifier transistor **19,** connected to the collector of transistor **10** through the load resistor **18,** is driven in a positive direction thereby biasing the transistor **19** to conduction. The collector of transistor **19** is directly connected to the collector of transistor **10.** Biasing transistor **19** to conduction causes the emitter voltage thereof to be driven in a positive direction thereby biasing NPN switching amplifier transistor **20** to conduction. The base of transistor **20** is directly coupled to the emitter of transistor **19.** The emitter of transistor **20** is directly connected to ground and the collector of transistor **20** is connected to the base of transistor **10** through current limiting resistor **21.** It should be seen that the base of transistor **10** is connected to ground through current limiting resistor **21** and transistor **20** as long as transistor **20** is biased to conduction thereby maintaining the line switch transistor **10** conducting regardless of the position of the switch **37,** that is, regardless of whether or not the switch **37** is retained in the actuated position, "closed circuit position", by an operator. Since transistor **20** is biased to conduction soon after the push-button switch is actuated, the operator may release the switch **37** from its actuated position thereby allowing the switch to return to its normal or "open circuit position" without de-energizing the electronic timer.

Upon return of switch **37** to its normal "open" position, the timing capacitor **38** is connected between ground and the collector of the line switch transistor **10** through the DC blocking diode **28** and the first timing resistor **39.** The timing capacitor **38** is charged by the DC source through the PNP line switch transistor, the timing resistor **39** and diode **28** to ground. The charging rate of the timing capacitor is determined by the magnitude of resistance of the timing resistor **29** and the capacitance value of the capacitor. The greater the magnitude of resistance of the timing resistor, the lower the charging rate of the timing capacitor. The charging rate of the capacitor may be varied by varying the resistance value of resistor **39.** The charging rate of the capacitor, when charged through resistor **39,** is illustrated as line **81** between points **82** and **83** of the charging curve **80** in FIG. **2** of the drawing.

NPN amplifier transistor **27** of the trigger means **53** has the base thereof connected to the collector of PNP transistor **10** through diode **25** and load resistor **23.** Transistor **27** is biased to conduction by the collector voltage of transistor **10** being driven positive which, in turn, drives the base voltage of transistor **27** positive thereby biasing transistor **27** to conduction. The emitter of transistor **27** is coupled to ground and the collector thereof is connected through diode **29** to the timing capacitor **38.** The conducting state of transistor **27** substantially prevents the flow of charging current from

the DC source to the timing capacitor through second timing resistor 26 and diode 29. Second timing resistor 26 is connected between the collector of line switch transistor 10 and diode 29.

Driving the collector voltage of transistor 10 in a positive direction causes the base voltage of NPN transistor switch 30 of the trigger means 53 to be driven in a positive direction biasing the transistor 30 to conduction. The base of transistor 30 is directly coupled to the base of transistor 27 and to the collector of transistor 10 through diode 25 and load resistor 23. The emitter of transistor 30 is connected to ground whereas the collector of transistor 30 is connected to the collector of transistor 10 through load resistor 40. Current flowing from the DC source through the line switch transistor to the means 54 is directed through load resistoe 40 and transistor 30 to ground thereby preventing means 54 from emitting an audible sound during the initial phases of the timing interval, that is, during the time required for the timing capacitor to charge from point 82 to point 83 illustrated in FIG. 2.

The return of switch 37 to the normally "open" position connects the capacitor 38 to the DC source through the diode 28, timing resistor 39 and the line switch transistor 10 causing the capacitor to charge at a rate generally indicated by line 81 between points 82 and 83 of FIG. 2. When the magnitude of the charge on capacitor 38 reaches a determined value, which is illustrated by point 83 in FIG. 2, the base voltage of NPN emitter follower transistor 22, connected between the timing resistor 39 and the capacitor 38 through diode 28, is sufficiently driven in the positive direction to bias transistor 22 to conduction. The collector of transistor 22 is directly connected to the collector of transistor 10 and the emitter of transistor 22 is connected to the base of NPN transistor 24. As the emitter voltage of the transistor 22 is driven in a positive direction due to the conducting state of transistor 22, the base voltage of transistor 24 is driven in a positive direction thereby biasing the transistor 24 to conduction. The biasing of amplifier transistor 24 to conduction causes the collector voltage of transistor 24 to be driven in a negative direction thereby driving the base voltage of transistor 27 in a negative direction biasing the orginally conducting transistor 27 to non-conduction. The collector of transistor 24 is connected to the base of transistor 27 through diode 25. After the amplifier transister 27 is biased to non-conduction, the diode 28 is reversed bias when the voltage on capacitor 38 becomes greater than the voltage at the base of emitter follower transistor 22 thereby electrically "disconnecting" resistor 39 from the timing circuit. The flow of current from the DC source to the timing capacitor 38 is now through second timing resistor 26, connected between the collector of the line switch transistor 10 and the collector of amplifier transistor 27, through diode 29, connected between resistor 26 and the timing capacitor, to the timing capacitor. The timing capacitor 38 charges through the resistor 26 and diode 29 at a faster rate as indicated by line 84 between points 83 and 85 shown in FIG. 2 since timing resistor 26 is of a lower magnitude resistance than timing resistor 39. The charging rate of the capacitor may be varied by varying the resistance value of resistor 26.

The time required to charge capacitor 38 to point 83 on the curve 80, which biases transistor 22 to conduction, is governed by the magnitude of voltage at the collector of line switch transistor 10 and the magnitude of voltage at the emitter of transistor 24. The time required to charge capacitor 38 to point 83 on the charging curve 80 is governed by the ratio between the magnitude of voltage at collector of transistor 10 less the voltage drop experienced across diode 28, to the voltage at the emitter of transistor 24 plus the sum of the voltage drops between the base of transistor 22 and the emitter of transistor 24 when transistors 22 and 24 are biased to conduction. If the abovementioned time required to charge capacitor 38 to point 83 on curve 80 is to be substantially constant, the ratio of the voltage magnitudes enumerated above should be substantially constant. The ratio may be rendered substantially constant by using the substantially non-linear voltage-current characteristics of diodes 12 and 13 connected in series between the collector of transistor 10 and the emitter of transistor 24. The non-linearity of the voltage-current characteristics of diodes 12 and 13 may be varied by varying the resistance value of resistor 15 connected between the cathode of diode 13 and ground. The voltage magnitude at the collector of transistor 10 decreases due to, among other things, "aging" of the DC voltage source which results in a decrease in the output voltage thereof. As a result of the decrease in the output voltage of the DC source, the collector voltage of transistor 10 less the voltage drop across diode 28 decreases in a greater percentage than the percentage decrease of the voltage at the collector of transistor 10. At substantially the same time, the current flow through diodes 12 and 13 decreases, causing an increase in resistance of the diodes 12 and 13, which results in a percentage voltage decrease between the cathode of diode 13 and ground which is a larger percentage than the percentage decrease in the voltage at the collector of transistor 10.

It is seen that by proper selection of the magnitude of the resistance value of resistor 15, connected between ground and the cathode of diode 13, the diodes 12 and 13 may be biased so that a variation in current as a result of variation in the voltage of the DC source results in a voltage at the cathode of diode 13 which compensates for variations in the charging rate of capacitor 38 due to variations in voltage at collector of transistor 10 thereby requiring the same length of time to charge the capacitor to point 83 on the curve 80.

When transistor 24 is biased to conduction in the manner described hereinbefore, the collector voltage thereof is driven in the negative direction causing the base current of transistor 30 to be reduced to a magnitude which causes the transistor 30 to be biased to non-conduction. The base of transistor 30 is coupled to the collector of transistor 24 through diode 25. The voltage at the collector of transistor 30 is driven in the positive direction causing the piezoelectric device 36, which has one surface connected to the collector of transistor 30, to deform thereby mechanically stressing the device. The piezoelectric device may be fabricated from any suitable material such as barium titanate which when mechanically stressed emits an audible sound. The deformation of the piezoelectric device causes a current to flow in the base of NPN oscillator transistor 34 which current is of sufficient magnitude to bias the oscillator transistor 34 to conduction. The base of oscillator transistor 34 is connected to a surface of the piezoelectric device opposite the surface to which the collector of transistor 20 is connected. When the piezo-

electric device attains its maximum deformation which is determined to a great extent by its mechanical properties such as the modulus of elasticity and the like and the magnitude of voltage applied thereto, the flow of current in the base of oscillator transistor **34** substantially ceases biasing the transistor to non-conduction. The collector voltage of transistor **34** is driven in the positive direction thereby biasing NPN oscillator transistor **31** to conduction. The collector of oscillator transistor **34** is directly coupled to the base of oscillator transistor **31**. Biasing oscillator transistor **31** to conduction drives the collector voltage of transistor **31** in the negative direction causing the piezoelectric device to be deformed in a direction opposite to the initial direction of deformation of the piezoelectric device causing current to flow in the opposite direction in the piezoelectric device through transistor **31**, diode **32** and diode **35**, The collector of transistor **31** is directly connected to the surface of the piezoelectric device opposite the surface to which the base of transistor **34** is connected. The diode **32** is connected between the emitter of transistor **31** and ground. The diode **35** is connected between ground and the base of transistor **34**. When the piezoelectric device deforms beyond its original position due to momentum and begins to deform in the original deformation direction, current again flows into the base of transistor **34** biasing the transistor to conduction. The transistors **31** and **34** oscillate between conduction and non-conduction in the manner described hereinbefore causing the piezoelectric device to be stressed to its mechanical limit thereby emitting a substantially constant, audible sound. It is seen tha piezoelectric device emits a sound at about point **83** on the curve **80** and the audible sound continues until the electronic timer is de-energized.

Load resistor **40** is connected between the collector of transistor **31** and the collector of line switch transistor **10**. Load resistor **41** is connected between the collector of transistor **34** and the collector of the line switch transistor. Resistor **33** is a bias resistor for the base of transistor **34** and is coupled between the base of transistor **34** and the emitter of transistor **31**.

As described hereinbefore after transistor **27** is biased to non-conduction, the timing capacitor **38** is charged by the DC source through the line switch transistor **10**, the load resistor **26** and the diode **29** at the rate illustrated by line **84** shown in FIG. **2**. After the passage of a determined interval of time, the timing capacitor **38** is charged to a magnitude of voltage, shown as point **85** on the charge curve **80** of FIG. **2**, which is of sufficient magnitude to bias NPN switching amplifier transistor **17** to conduction. The base of transistor **17** is directly connected to the timing capacitor, the emitter thereof is connected to ground through resistor **16** and the collector thereof is directly connected to the base of transistor **19**. The emitter of transistor **17** is connected to a voltage divider including resistors **14** and **16**. The resistors **14** and **16** are coupled between the anode of diode **13** and ground. The voltage divider determines the voltage required to bias transistor **17** to conduction. Biasing transistor **17** to conduction drives the collector voltage of transistor **17** in a negative direction which drives the base voltage of transistor **19** in a negative direction thereby biasing transistor **19** to non-conduction. When transistor **19** is biased to non-conduction, the emitter voltage thereof is driven in a negative direction thereby biasing transistor **20** to non-conduction. Biasing transistor **20** to non-conduction disconnects the base of the line switch transistor **10** from ground thereby driving the base voltage of transistor **10** in a positive direction through resistor **11**, connected between the positive terminal **55** and the base of transistor **10**, thereby biasing transistor **10** to non-conduction. When transistor **10** is biased to non-conduction, the electronic timer is electrically "disconnected" from the source of DC power terminatng the audible sound and extinguishing the lamp signalling the end of the timing interval.

Having thus described my invention, I claim:

1. An electronic timer for indicating a time interval comprising

timing means, including timing capacitor means and a first timing resistor means and a second timing resistor means, adapted to be coupled to a source of DC energy whereby said timing capacitor means is charged to a determined voltage magnitude through said first timing resistor means;

trigger means coupled to said timing means for electrically disconnecting said first timing resistor means from said timing capacitor means and for electrically connecting said timing capacitor means to said second timing resistor means when said capacitor means attains said determined voltage magnitude whereby said timing capacitor means is charged through said second timing resistor means; and

indicator means including a piezoelectric means and a pair of transistors, a base of a first one of said transistors coupled to a first surface of said piezoelectric means, a collector of said first transistor connected to a base of a second one of said transistors, a collector of said second transistor coupled to an opposite surface of said piezoelectric means, the collectors of said transistors coupled to said trigger means, said indicating means biased to conduction by said trigger means when said capacitor means attains said voltage magnitude.

2. The electronic timer of claim **1**, wherein said piezoelectric means is barium titanate.

3. The electronic timer of claim **1**, wherein said trigger means biases said indicator means to conduction upon coupling of said timing capacitor to said second timing resistor.

4. The electronic timer of claim **3**, wherein said second resistor causes said capacitor to be charged at a rate faster than the rate of said first resistor means.

5. The electronic timer of claim **3**, further including a line switch means connected between said DC energy source and said trigger means biased to conduction upon energization of said electonic timer.

6. The electonic timer of claim **5**, wherein said second timing register means further includes means for maintaining said line switch means conducting during charging of said capacitor through said first resistor and said second resistor.

7. The electronic timer of claim **6**, further including manual switch means connected between said line switch means and said timing capacitor for initially energizing siad electronic timer.

8. The electronic timer of claim **6**, further including semiconductor switch means for biasing said line switch means to non-conduction whereby said electronic timer is de-energized upon said capacitor being

charged to a determined value through said second timing resistor.

9. The electonic timer of claim 8, wherein said electronic timer is an integrated circuit.

10. The electronic timer of claim 5, further including a source of illumination coupled to said line switch means and illuminating upon said line switch means being biased to conduction.

11. The electronic timer of claim 5, wherein said source of illumination is a lamp.

12. The electronic timer of claim 1, further including voltage regulator means compensating for variations in voltage of said DC source.

13. The electronic timer of claim 12 wherein said voltage regulator means includes serially connected diodes coupled between said source and said trigger means and resistor means connecting said diodes to ground and said semiconductor switch means.

14. An electronic timer indicating two time intervals comprising an electrical circuit including in combination:

a. first and second switch means, energizing said first switch means completing a circuit to said second switch means to energize same, said second switch means energizing a timing means, said timing means determining the length of said first time interval,

b. trigger means cooperating with said timing means to stop said first time interval and start a second time interval, said timing means determining the length of said second time interval, said trigger means includes a pair of cascaded transistors, the base of the first transistor connected to the said timing means through a first switching means, said cascaded pair of transistors connected to a pair of parallel connected transistor amplifiers through a second switching means, the collector of one of said transistor amplifiers connected to said indicator means, the collector of the other transistor amplifier connected to said second switch means through a second switching means,

c. said second switch means responsive to said timing means to stop said timing means at said second time interval and re-set said timer, and

d. indicator means responsive to said trigger means during said second time interval.

15. An electronic timer according to claim 14 wherein said indicating means is an audible sound emitting means.

16. An electronic timer according to claim 15, wherein said audible sound emitting means is a piezoelectric device.

17. An electronic timer according to claim 16, wherein said indicator means including said piezoelectric device further includes oscillating means for alternatively stressing opposite surfaces of piezoelectric device whereby said piezoelectric device emits an audible sound.

18. An electronic timer according to claim 17, wherein said oscillating means includes at least one pair of transistors alternately biased to conduction.

19. An electronic timer according to claim 18, wherein said pair of transistors includes a base of a first one of said transistors coupled to a first surface of said piezoelectric device, a collector of said first transistor connected to a base of a second one of said transistors, a collector of said second transistor coupled to an opposite surface of said piezoelectric device.

20. An electronic timer according to claim 19, wherein said piezoelectric device is barium titanate.

21. the electronic timer of claim 14, the combination further including voltage regulating means compensating for voltage variations when a DC voltage is applied to said electrical circuit.

22. The electronic timer according to claim 21 wherein said voltage regulating means includes serially connected diodes coupled between a voltage source and said trigger means and resistor means coupled to one of said diodes and to ground.

23. The electonic timer according to claim 21 wherein there are two of said diodes.

24. An electonic timer according to claim 14 wherein said two time intervals are of different length.

25. An electonic timer according to claim 14 wherein said combination further includes a second indicating means responsive to said second switch means.

26. An electonic timer according to claim 14 wherein said timing means includes a timing capacitor means and first and second timing resistors connected to a source of electrical energy, said timing capacitor means charged to a predetermined voltage level through said first timing resistor when said second switch means is energized, said trigger means electrically disconnecting said first timing resistor from said timing capacitor means and electrically connecting said second timing resistor to said timing capacitor means.

27. An electronic timer according to claim 14 wherein said first and second switching means are diodes.

28. An electronic timer according to claim 14 wherein said first switch means is a manual switch opening and closing said electrical circuit.

29. An electronic timer according to claim 14 wherein said second switch means includes first, second and third transistors connected collector to base, emitter to base, the collector of said third transistor connected to said first switch means and to a line switch of said electrical circuit, and its emitter to ground, said trigger means connected to the base of said first transistor, and the collectors of said first and second transistor connected to said line switch.

* * * * *

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,763,488 Dated October 2, 1973

Inventor(s) Charles H. Klasing

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Col. 2, line 33, cancel "inventin" and insert ---invention ---.

Col. 3, line 25, cancel "wit" and insert ---with---.

Col. 5, line 16, cancel "resistoe" and insert ---resistor ---.

Col. 6, line 68, cancel "20" and insert ---30---.

Col. 7, line 18, cancel "," after "35" and insert ---.---.

Col. 7, line 33, cancel "tha" and insert ---that---.

Col. 8, line 56, cancel "register" and insert ---resistor ---.

Col. 8, line 63, cancel "siad" and insert ---said---.

Signed and sealed this 4th day of June 1974.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

FORM PO-1050 (10-69)

USCOMM-DC 60376-P69
* U.S. GOVERNMENT PRINTING OFFICE : 1969 O—366-334.