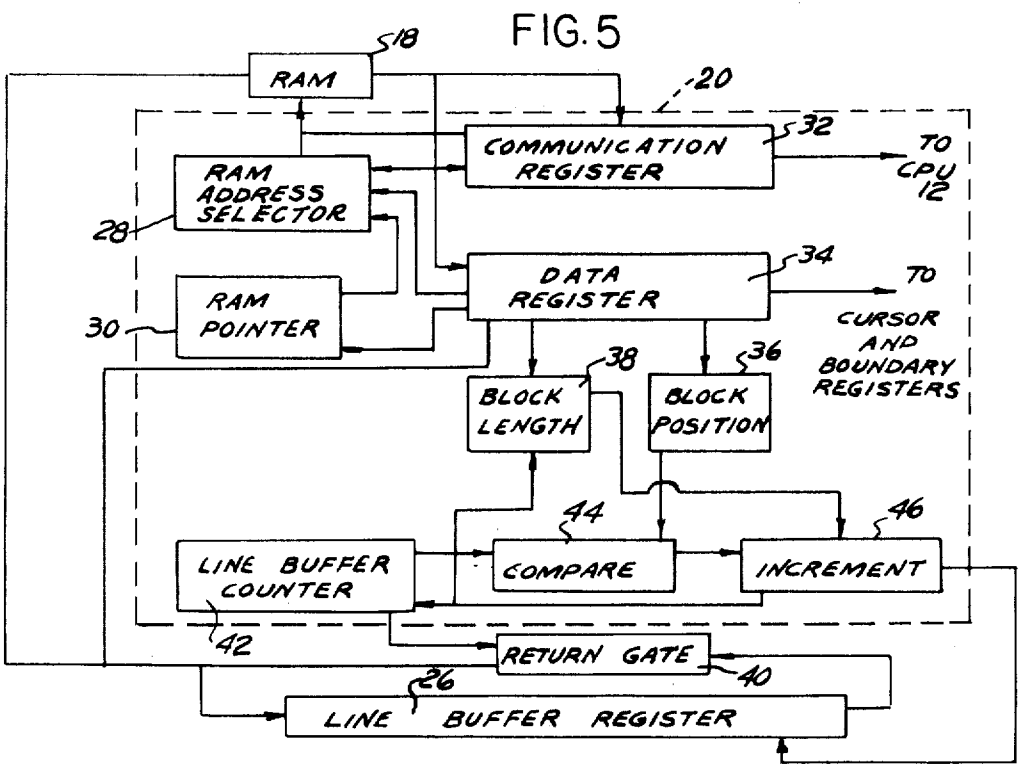
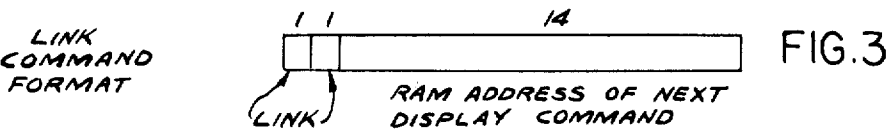
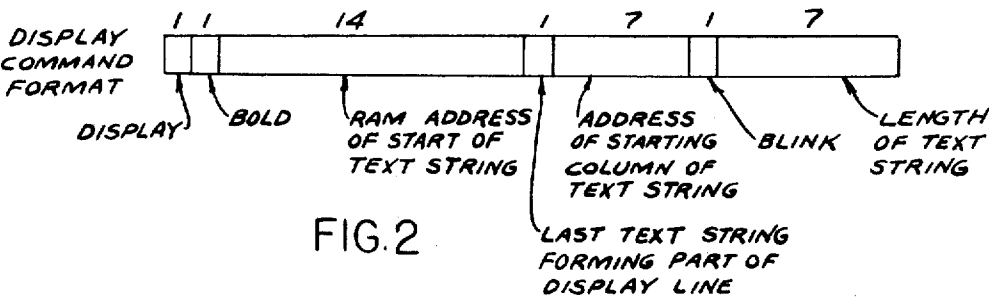
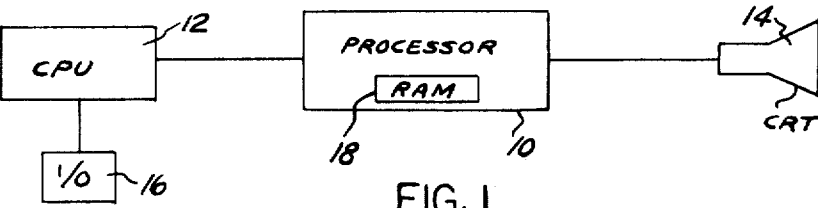




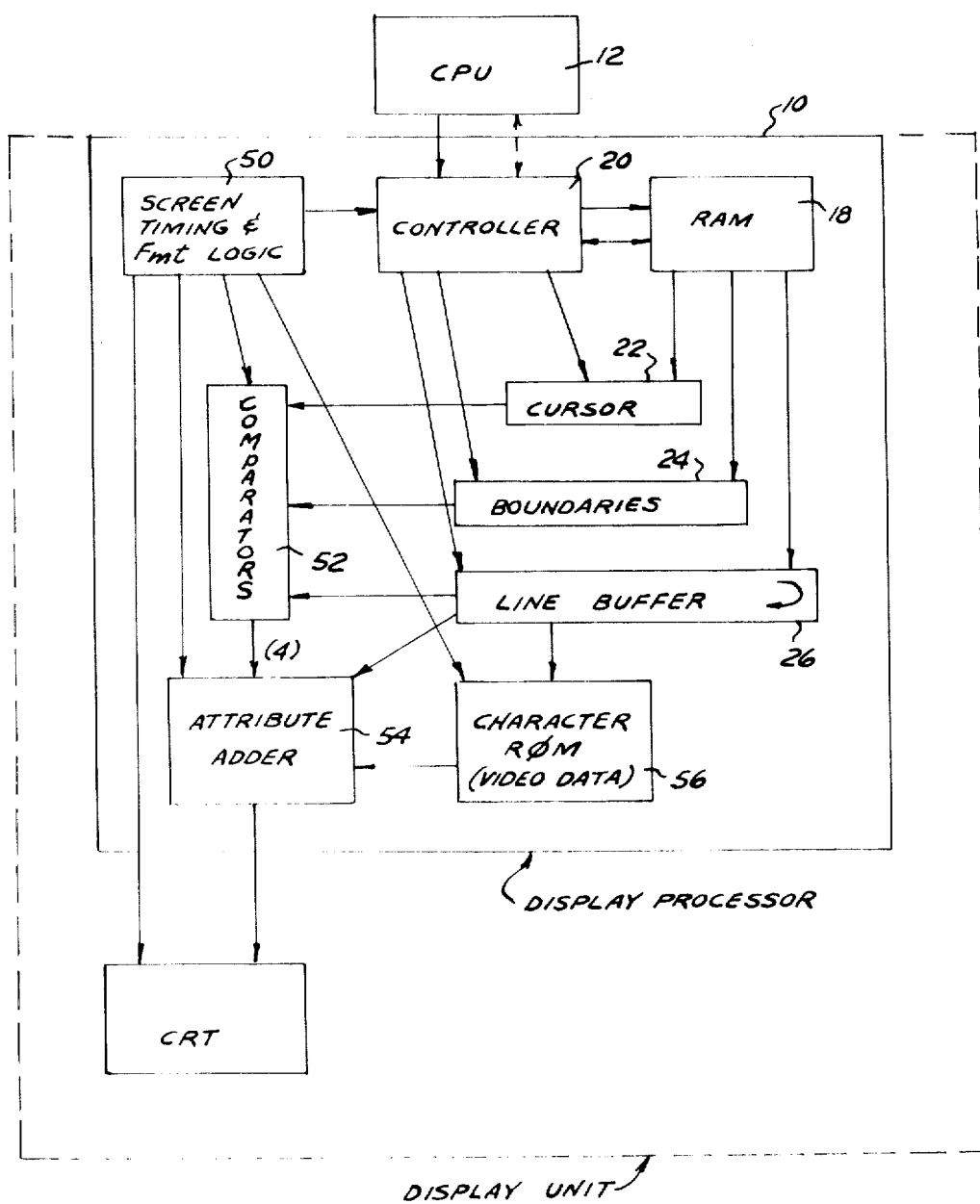
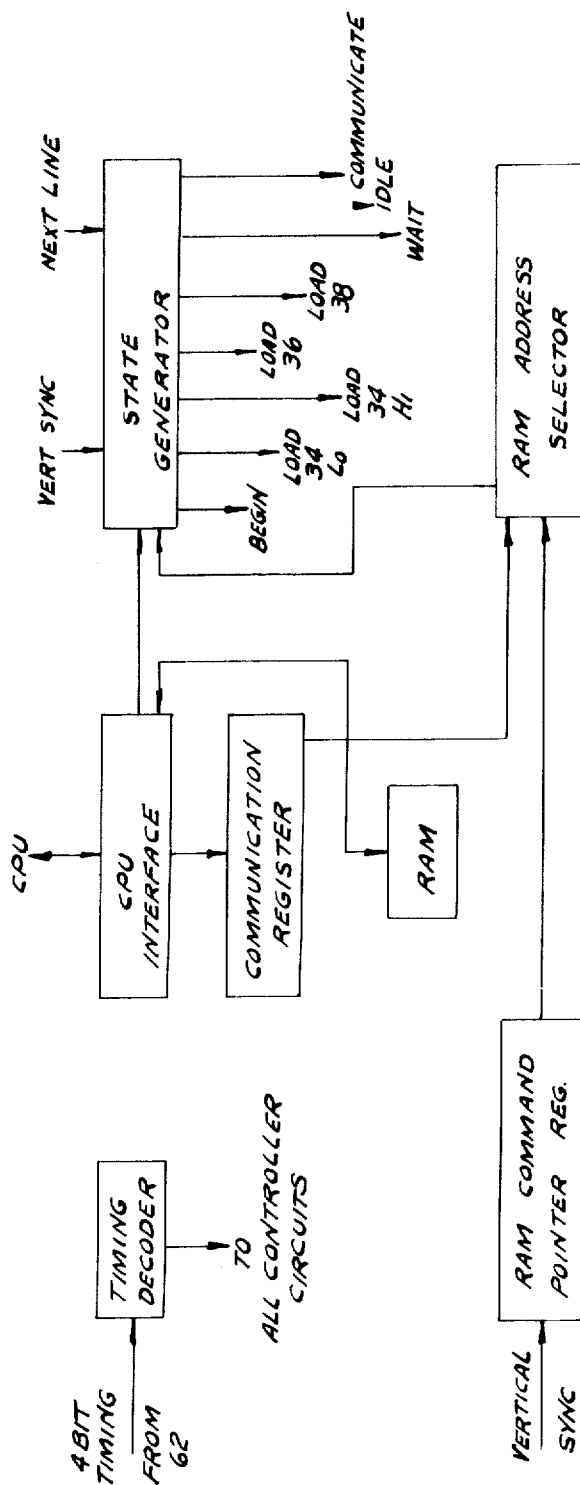
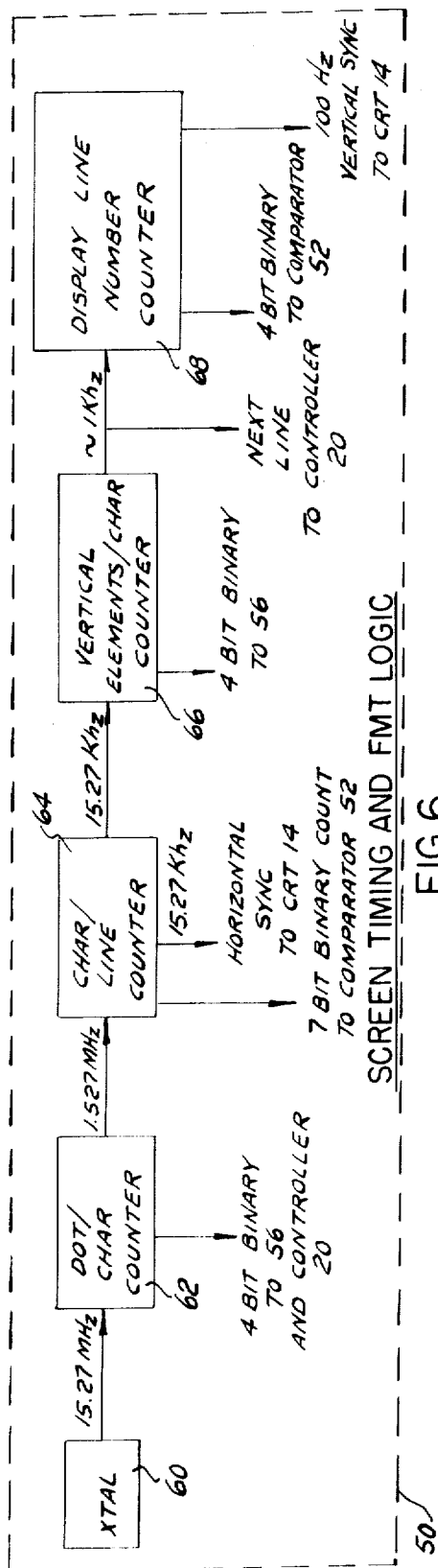


FIG. 4



INTERPRETIVE DISPLAY PROCESSOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a processor for storing digital signals representative of textual material to be written on an output display device and signals for controlling the format of the display and the means for generating a display under the control of these stored signals.

2. Prior Art

Cathode ray tubes, as well as less common forms of alphanumeric displays, such as plasma discharge tubes, are employed as output devices in a variety of systems which operate on digital signals representative of alphanumeric characters and the like to retrieve, compose, and/or edit text composed of strings of such characters. In one typical machine of this class text may be provided to the machine through a keyboard, displayed on a cathode ray tube, and modified, or edited as to content and format by an operator with commands entered through the keyboard. When the edited text displayed on the CRT meets the approval of the operator it may be outputted through a printer, on magnetic or punched tape, or stored within the system for later retrieval.

A suitably programmed general purpose computer may be employed to manipulate the text in the editing process and in large systems the text to be displayed on the output device may be provided directly by the computer in digital form, to digital-analog converters to provide control signals for the CRT deflection circuits. In systems employing relatively small computers the task of continuously generating these control signals would require most or all of the available computer time, leaving no computer capacity for the editing manipulations. Accordingly, processors have been developed which store digital signals representative of a body of text to be displayed and act as a buffer between the computer and the display device. The computer is capable of extracting sections of text from and writing text in the processor storage. The processor acts to provide control signals to the CRT in timed relation to the scan of the cathode ray beam and the processor may also manipulate the text as by scrolling a larger body of text than is capable of being displayed on the tube at any one instant to present different sections of the body for display on the tube. These processors have typically consisted of random access memories connected in the manner of recirculating registers so that the information effectively flows through the memory. The text is arranged in the memory in the order that it is to be displayed on the tube. In an alternate form of processor relatively small text segments are stored in the memory along with information relating to the position that they are to occupy on the final display. The processor includes circuitry for sequentially outputting the segments to the display positions encoded with the information. This arrangement simplifies the process of formatting text on the display surface in blocks, columns or the like.

The present invention is addressed to a processor having a unique configuration which results in a high storage efficiency, a great deal of versatility in formatting and displaying the data and a very simple interface

with the computer or other source of text and editing modifications.

SUMMARY OF THE PRESENT INVENTION

In its broadest form the processor of the present invention stores a body of digital data, representative of text, in some form of addressable memory. The processor also stores data constituting display commands which each define a small portion of the stored text by its storage address, specify attributes relating to the manner in which this text is to be displayed on the output device and define display position coordinates, preferably the horizontal position of the specified text within the display. The processor further includes a buffer register capable of storing a limited section of text to be outputted to the display, typically one horizontal line.

The line buffer is filled with text derived from the text storage section under control of the display commands. The display commands are utilized either in their order of storage or in some different order specified by "link" commands interspersed with the display commands. Initially, the text stored at the address specified by the first display command is written in the buffer at a position specified by the display command. Along with the character codes the line buffer may be filled with data representative of the manner in which that character is to be displayed such as underlined, or blinking, which information may be derived either from the display commands, from codes associated with the stored text or from both. Additional text sections specified by further display commands in the sequence are then added to the line buffer until a display command is reached which signifies that it is the last one to be utilized in filling the buffer. The buffer is then ready to be utilized in writing the line, or other text section, on the display.

When the output device is a cathode ray tube as in the preferred embodiment of the invention, analog signals must be developed to control the deflection or modulation of the cathode beam to generate the appropriate characters. In the preferred embodiment of the invention the alphanumeric characters of the text are generated in dot matrix form and as the cathode ray sweeps horizontally across the display area its intensity is modulated to create the dots for one horizontal line of each of the characters stored in the line buffer. To achieve this conversion a read-only memory matrix encoded to convert digital codes representative of characters into the elements of the dot matrix is employed. As the line buffer is scanned in timed relation to the horizontal sweep of the CRT beam each character code sequentially controls the conversion memory to provide the appropriate dots for the output of one horizontal element of that character. The next beam sweep is one scan line lower on the CRT screen and the next set of dots for the characters stored in the line buffer are outputted by the matrix. Alternatively, an interlaced scan may be used and spaced horizontal elements of a character are generated by consecutive horizontal sweeps of the beam and the intermediate elements of the character are generated as part of the subsequent raster. This requires that the line buffer be filled twice with the same set of characters to generate a single line of display.

When the electron beam has generated an entire line of characters the line buffer is refilled with text for the

next horizontal line using the next group of display commands.

In the preferred embodiment of the invention eighty characters may be written in a horizontal line. From one to eighty display commands may be required to fill the line buffer with text for the display of a line. A single display command could prepare the buffer for the generation of the next line containing from zero to eighty characters. Such a display command would include the address of the first character in a text section containing from zero to eighty characters, and a code indicating that this was the last display command to be used in filling the line buffer. At the other extreme the line buffer could be filled with text sections defined by eighty display commands each calling for one character. A full line, or eighty characters, is the most that can be called for by a single display command. Since each display command also specifies the position in the line buffer that its defined text section is to occupy, the exact formatting of a page is defined by the display commands.

In order for the input unit to the processor to edit the output text it can alter some of the stored text, the display commands or the order in which the display commands are utilized. While in the preferred embodiment of the invention this editing is accomplished by a programmed computer controlled by a keyboard, it could be done in a less automatic manner under control of signals provided by a keyboard suitably connected to the controller memory.

In addition to storing text and display commands, the preferred embodiment of the controller stores information used to control the display of a cursor generated by an intermediate intensity modulation of the CRT beam as well as boundaries on the cathode ray tube. Cursor information defines its vertical and horizontal positions, whether it is to blink, whether it is to have an underline component, and, if underlined, the beginning and end coordinates of the underlining. The boundary information specifies the display of two vertical lines and two horizontal lines which may be selectively written adjacent to any character cell on the display surface. A screen timing unit controls the horizontal and vertical position of the cathode ray beam and contains registers which instantaneously specify its horizontal or vertical position. These are continually compared with registers defining the position of the cursor and the boundary lines. When an identity is recognized signals are added to the character matrix signals which cause the generation of the cursor and/or boundary.

In the preferred embodiment of the invention the string of text defined by each display command, termed a block, is specified in terms of its beginning address in the memory and its length. When a display command to be utilized is selected the block position and block length data are entered into registers used to control the copying of data from the text storage into the line buffer. As successive characters are written into the buffer the contents of the block length register are decremented. When this register reaches zero and if the display command utilized was not the last one to be used in filling the buffer, the next display command in the sequence is selected and the text specified by that command is entered into the buffer. This entry may modify the text previously entered into the buffer under the control of previous display commands; a feature which greatly simplifies the editing since it allows

text to be modified by simply specifying the new parts; the old text need not be deleted from the controller memory.

Preferably the memory capacity will substantially exceed the quantity of text which may be written on the display at a single time. To scroll this larger body of text vertically on the display the identity of the first display command to be utilized in filling the screen is altered between successive displays by alterations, under control of the computer, of the first "link" command in the display command sequence.

Horizontal scrolling is accomplished by altering the part of each display command which specifies the horizontal position it occupies in an output line. Other objectives, advantages and applications of the present invention will be made apparent by the following detailed description of a preferred embodiment of the invention. The description makes reference to the accompanying drawings in which:

FIG. 1 is a block diagram of a text editing system forming a preferred embodiment of the invention;

FIG. 2 is a diagram indicating the format of digital signals constituting display commands;

FIG. 3 is a diagram indicating the format of digital signals constituting a link;

FIG. 4 is a more detailed block diagram of the display processor 10;

FIG. 5 is a more detailed block diagram of those portions of the display processor which cooperate in filling the line buffer register with signals representative of text stored in the RAM;

FIG. 6 is a detailed block diagram of the display timing and format block; and

FIG. 7 is a detailed block diagram of those portions of the display processor involved in the sequence of steps which fill the line buffer. Referring to FIG. 1, the preferred embodiment of the invention constitutes a processor 10 which receives signals representative of text and of commands relating to the display of the text from a central processor unit 12 and acts to display certain sections of that text on a cathode ray tube 14 in a manner prescribed by the commands.

The central processing unit 12 forming part of the preferred embodiment of the invention may be any mini-computer having a suitable input-output device 16. An exemplary use of the preferred embodiment could be as an automatic typewriter wherein the I/O device 16 constitutes a keyboard equipped serial printer such as a teletype device. The operator, using the keyboard of the I/O device 16, would enter text and various information relating to the display of text into the CPU 12. The CPU acts to convert this information into suitable form and provide it to the processor 10 where it would be stored within a random access memory 18 forming part of the processor. On receipt of an appropriate command from the I/O device 16 as relayed through the CPU 12 the processor then would cause the text or certain sections thereof to be displayed on the CRT 14 in a format controlled by information stored within the RAM 18. The operator, observing the display, might then edit the display to change the text or its format by providing appropriate signals from the keyboard to the CPU 12. The CPU, acting under the control of the signals, would modify the contents of the RAM 18 and cause the CRT 14 to display this modified text. After one or more cycles of editing, the text, in its desired final form, could be out-

putted through the printer section of the I/O device 16 in hard copy form.

A variety of alternate uses exist for equipment of this general configuration such as in newspapers for editing text received from a wire service; the completion of prestored forms by the insertion of text in their blanks; as a terminal for interactive conversation with a large computer, and the like.

The preferred embodiment of the processor 10 is capable of displaying up to 128 different alphanumeric symbols in a 32 line, 80 character wide array on the face of the CRT. Each character is written by dots arranged on a 7 × 9 dot matrix. The characters may be displayed in either normal or bold face, either blinking or non-blinking, and either underlined or not.

In addition to displaying text the unit has the capability of displaying a cursor which constitutes a light intensity overlay positionable at any of the character positions and a boundary comprised of two vertical lines and two horizontal lines.

The body of the text to be displayed and the signals for controlling the format and manner of displaying the text are all stored within the RAM 18. The function of the CPU 12 is to load properly formatted information into the RAM, and to fetch information from the RAM for modification. This editing process could be performed by a keyboard suitably interfaced with the RAM but normally and preferably would be performed by a mini-computer in order to simplify the process of editing.

DATA STORAGE WITHIN THE RAM

While the preferred embodiment of the invention utilizes a semi-conductor random access memory, other embodiments of the invention could employ core memories, magnetic discs, addressable tapes or the like to perform the function of the RAM 18. The functional requirements of the RAM are that the information storage be addressable and accessible at a relatively high rate.

While the CRT screen is only capable of displaying 2,560 characters at any one time the capacity of the memory is preferably larger than 2,560 words so that only a portion of the text stored within the memory may be used at one time for display purposes. In the preferred embodiment of the invention, the RAM is capable of storing 8,000 eight bit digital words in word addressable form. Two forms of data are retained in the RAM 18: text data and controller commands.

The text data consists of eight bit words each comprising a seven bit code signifying the encoded character and an eighth bit indicating whether the character is to be underlined when displayed. Normally a plurality of these character codes will be stored at sequential locations within the RAM to form character strings but a string could also consist of only a single character code.

The controller commands determine which parts of the text data are to be written on the CRT, and the format of their display. These commands are used to specify the length and location within the RAM of strings of data to be displayed, the bold and blink attributes of their display and the position in which the data is to be displayed on the CRT. The controller commands are of two forms: "display commands" and "link commands." The display commands each specify the information necessary to display one segment or string of text on

the CRT and define the location of that string within the RAM and the link commands are used to sequence the order of usage of display commands in assembling strings to make up a composite display on the CRT

DISPLAY AND LINK COMMANDS

Each display command supplies all the information necessary to display one string of text data on a CRT. The entire visible display is "drawn" on the CRT under the direction of a series of display commands.

Each display command is 32 bits in length and is stored in four sequential word positions of the RAM. The format of a display command is illustrated in FIG. 2. Starting from the left in FIG. 2 the first bit of the command is a zero. This allows the system to distinguish the start of the display command from the start of a link, which has a one in the most significant bit position. The second bit position contains a one if the text string defined in the command is to be displayed on the screen in bold form and a zero otherwise. The next 14 bit positions define the RAM address of the start of the text string to be utilized in connection with this display command. The next bit contains a one if the display command defines the last text string to be used in forming a single horizontal line of the ultimate display; that is, this bit effectively controls the vertical position on the display raster. The first display commands utilized define the text strings used in generating the uppermost horizontal line on the display. Each time a display command is encountered containing a one in the seventeenth bit position indicating that this is the last display command to be used in generating a line, the display effectively indexes vertically downward one line in utilization of the subsequent display command.

The next seven bits of the display command define the horizontal address across a line of the display at which the first character of the text string defined by the display command is to be positioned. Since there are eighty character positions across a display line this information will contain the address of one of these eighty positions or "columns."

The next (18th) bit position of a display command contains a one if the associated text string is to be displayed in a blinking manner and a zero otherwise. The last seven bits of the four words constituting a display command define the length of the text string in terms of word addresses in the RAM. Thus between the 14 bits which define the beginning address of a text string and the seven bits which define the length of a string a total definition is provided for the address of a string stored at one or more sequential positions in the RAM. If the final seven bits contain 0000001 the text string consists of the single character stored at the RAM address defined by the 14 bits.

A single display command always refers to text to be displayed on one horizontal line of the CRT.

As will subsequently be described a series of one or more display commands are used to organize a body of text to be displayed across one full line of the CRT. The number of display commands to be used in filling one line is determined by the use of the bit which indicates that a particular display command defines the last text string to form part of a display line.

The display command may be arranged in sequential order within the RAM and when a text string associated with one display command has been properly assembled for use in generating the encoded characters on

the CRT the display command at the next sequential RAM address is utilized. Alternatively, "link commands" may be interspersed with the display commands in the RAM. A link command defines a modification of the sequential use of display commands. As illustrated in FIG. 3, a link command is 16 bits or two RAM words in length. The first two bits contain a one and a zero respectively to distinguish a link command from a display command. The next 14 bits contain the RAM address of the next display command to be utilized by the system in generating a display. This next display command may be located anywhere within the RAM. There are no boundary or alignment constraints for the containment of the display commands and link commands within the RAM. The link command is an effective jump or branch command which allows successive display commands to be scattered throughout the RAM and connected by links, and allows the sequence of display of the text to be altered without moving stored text.

CURSOR SPECIFICATION AND CONTROL

In addition to the text data and controller commands which are stored at variable addresses in the RAM, the RAM contains eight words of information which are stored in fixed locations; preferably, the first eight words of the RAM, that is the RAM locations having the addresses 000 - - 001 to 000 - - 007.

The first four of these locations are reserved for data specifying the nature and location of a cursor which may be displayed along with the text. The cursor includes a normal middle intensity character mask and a unique, full intensity, underline component, located on the same line as the character mask but having a controllable width.

The first word, having an address of 000 . . . 000 contains a one in the most significant bit position if a cursor is to be blinked on and off and the five least significant bits specify the line number vertically on which the cursor is to be located.

The word in location 000 . . . 000 contains a zero in its first bit position if a cursor is to be displayed; a one in that bit position indicates that no cursor is to be displayed. The next seven bits of the first word specify the column number across the width of the display surface at which the character mask component is to appear.

The third word, 000 . . . 002 determines by its first bit position whether the cursor shall include an underline component. The next seven bits specify the column number of the beginning of that underline component if it is to be employed.

The fourth word, at RAM location 000 . . . 003 specifies the column number of the end of the underline component of the cursor in its last seven bit positions. Accordingly, a cursor will normally be drawn from the column number specified by the address contained in the third word and ending at the column number the address of which is contained in the fourth word.

When the address specified in the fourth word for the column number of the end of the underline component is less than the address specified in the third word as the beginning of the underline component two underline components will be generated on the screen, the first, extending from the zero column position on the far left end of the screen, to the column address specified in the third word, and the second component extending

from the column address specified in the fourth word to the far right hand end of the screen or column eighty.

BOUNDARY SPECIFICATION AND CONTROL

The fifth through eighth words of the RAM, those having addresses 000 . . . 004 to 000 . . . 007 are reserved for the specification of a boundary or outline to be displayed on the CRT. The boundary consists of (at most) two vertical lines and two horizontal lines. Any combination of components of the boundary may be selectively enabled or disabled.

The fifth word in the RAM contains a zero in its first bit position if a top boundary is to be displayed and its least significant five bits specify the vertical line number at which the top boundary is to be displayed.

The sixth word contains a zero in its most significant bit position if a left boundary is to be displayed and the balance of the word contains the column number of the left boundary.

The seventh word in the RAM contains a zero in its first bit position if bottom boundary is to be displayed and the least significant five bits of the word contain the line number of the bottom boundary.

The eighth word in the RAM contains a zero in its first bit position if a right boundary is to be displayed and the balance of the word contains the column number of the right boundary.

With the control information contained in these four words, a boundary can be displayed which consists of a left, right, top and/or bottom line on any columns or lines of the CRT. If desired, all boundary display can be disabled. If the value specified in the fifth RAM word for the left boundary exceeds the address specified in the sixth RAM word for the right boundary, and the top and/or bottom boundaries are enabled, then the top and/or bottom boundaries will be displayed as two segments extending from column zero to the left boundary and from the right boundary to the far right. If the value specified for the top boundary exceeds that specified for the bottom boundary, no boundary at all will be displayed on the CRT.

THE EDITING PROCESS; RAM - - CPU INTERACTION

The data outlined above as being resident in the RAM controls the display generated on the CRT in a manner which will be subsequently described. The editing process, therefore, consists of simply modifying the contents of the RAM to a state which will achieve the desired display. This process simply consists of the specification of a RAM address by the CPU and the generation of a signal which will either write new words in the specified RAM location destructively, or non-destructively read out the contents of the specified location. To assist in the editing process means may be provided for automatically incrementing or decrementing the memory address as successive words are written in or read from the RAM.

THE DISPLAY PROCESS

Referring to FIG. 4 which discloses the display processor 10 in more detail the transfer of information within the processor for purposes of either accessing the RAM 18 by the CPU 12 during the editing process, or during the display of information on the CRT 14 under control of data in the RAM, is achieved by a con-

troller 20. The display process begins in response to a timing signal from the timing unit 50 which will be subsequently described in detail. The first step in the display process involves the controller transferring the data resident in the first eight words of the RAM into a cursor register 22 and a boundary register 24. This is done by the controller starting at the first word of the RAM and transferring the information relating to the line number on which the cursor is to be located into register 22. Sequentially the addresses contained in the next three words are transferred into registers for later use.

Addresses contained in the fifth through the eighth words of the RAM are then loaded into the boundary register 24. Next the controller utilizes the text data and controller commands contained in the RAM 18 to fill a line buffer 26 with all of the text necessary for the generation of one horizontal line of text on the CRT, in the manner specified by the display commands. This loading process will be described in connection with FIG. 5 which illustrates only the pertinent sections of the controller and the line buffer in more detailed block form.

Access to a particular word in the RAM 18 is controlled by a RAM address selector 28 and three associated address registers contained within the controller 20. A RAM command pointer 30, one of the three selectable RAM address registers, controls the sequential utilization of display commands under control of the link commands and provides its output to the RAM address selector 28. A display data address register, the second of these three registers, is loaded with data from the RAM at locations specified by the command pointer 30 and is used to control the movement of data from RAM to the line buffer register 26 and of link addresses to the pointer register 30. A communication register 32 acts as an address buffer between the RAM and the CPU 12 and is capable of controlling the RAM address selector 28 in order to gain access to any storage area within the RAM.

As has been noted, at the beginning of the display cycle the RAM command pointer 30 is set to all zeros and controls the address selector 28 to cause the contents of the first word position in the RAM to be provided to the cursor register 22 and the pointer 30 is incremented by one to cause the address selector 28 to provide the contents of the second word storage area to the boundary register 24.

This procedure is continued until the contents of the first eight word storage areas have been transferred to the cursor and boundary registers.

The display data address register 34 is two words in length and when the RAM pointer 30 reaches a count of nine it causes the memory address register to load the ninth RAM word into the first word of the display data address register 34 and then automatically indexes to cause the tenth RAM word to be loaded into the second word position of the data register.

The controller 20 examines the first bit position of the first word contained in the address register 34 to determine whether the two data words constitute a "link" or part of a display command. If the words constitute a link the data register loads the link address into the RAM command pointer 30. This causes the RAM address selector to extract the two words beginning at that RAM address and place them into the display data address register 34. This process continues until the

display data address register contains a display command. When a display command is recognized the command pointer 30 is incremented twice and the address of the starting column of the text string is loaded into a block position register 36 and the length of the text string, the last word of the display command, is loaded into a block length register 38. The RAM address of the start of the text string referred to by that display command is then provided by the display data address register 34 to the RAM address selector 28.

The line buffer register 26 is an eighty character, twelve bit wide recirculating register having a gate 40 in its recirculating path. A line buffer counter 42 contained within the controller 20 contains an address signifying the position of the line buffer contents within the register, or the column number of the 12 bit word emerging from the line buffer at any time.

At the beginning of the filling process the line buffer counter is at zero. The return gate 40 is open so that the contents of the buffer are effectively not recirculated. The line buffer register 26 is then incremented to the position stored in the block position register 36 under control of a comparator unit 44 which receives the contents of the block position register 36 and the line buffer counter 42 and causes the unit 46 to generate increment signals which are used to advance the line buffer register contents and increment the line buffer counter 42. Assuming that the block position is something other than zero, since the return gate 40 is opened null or zero signals are entered into those stages of the line buffer register which precede the block start position contained in the register 36. When the counter reaches that start position the comparator 44 detects the identity between the contents of the counter 42 and the block position register 36 and disables the increment generator 46.

At this point the eight bits of the first word stored in the RAM address identified as the start of the text string by the display command contained in the display data address register are loaded in parallel into the line buffer register. Along with these eight bits the block length and block position registers enter one bit each into the line buffer indicating whether the display of the character so stored is to be bold and whether it is to blink. These signals were derived from the second bit of the first word and the first bit of the fourth word of the display command then stored in the appropriate registers. Accordingly, ten bits are stored in the line buffer register defining the character to be generated at that column of the display and the blink, bold and underlined attributes of that character.

At the time a data word is read out of the RAM into the line buffer the block length register 38 is decremented by one count and the display data address register 28 and the block position register 36 are each incremented by one count. If, after the block length register 38 is decremented it still contains a positive number the data word located at the position indicated by the display data address register is loaded into the next stage of the line buffer as are the same bold and blink bits from the block length and block position registers which were loaded with the last word. Thus these bold and blink registers are redundantly loaded into the line buffer with all of the characters associated with a single display command. Again the block length register 38 is decremented and the display data address register 28 and block position registers 36 are incremented. This

process is continued until the block length register reaches zero indicating that all of the characters associated with the present display command have been loaded into the line buffer register.

If the display command contains a one in its eighteenth bit position signifying that its associated text string is the last one to be used in filling the line buffer, the increment generator 46 sends a series of signals to the line buffer register causing it to index its contents until the line buffer counter 42 returns to zero. During this time the return gate 40 is open and nulls are generated so that the stages of the line buffer register following the one containing the last character loaded from the display command are filled with null signals. At this point the line buffer would be completely filled and ready to generate a line of display in a manner which will be subsequently described.

Alternatively if the display command being utilized is not the last one to be used in filling the line buffer the contents of the command pointer 30 are incremented and are fed into the address selector so that the next display command in the sequence may be fetched. Again the contents of that designated address in the RAM are placed into the display data address register until a display command is recognized and the process is repeated.

If the block position associated with the next display command to be utilized immediately follows the line buffer stage in which the last word identified by the previous display command was entered, the text string identified by that subsequent display command is simply entered into the line buffer. If there is a gap between the two, the line buffer counter is indexed until its contents identify with the block position as stored in register 36 in the manner previously described and nulls are entered into the positions of the line buffer intermediate the end of the first text string and the start of the second.

A subsequent string to be used in filling the line buffer may have its first character positioned in a lower position of the line buffer than the start of a previously entered string. In this case the line buffer counter will pass through a zero state in its transition between those two positions. When this occurs the return gate 40 is closed so that thereafter the content of the line buffer are recirculated and no more nulls are generated.

When one string overlaps a string previously entered in the line buffer it acts to supersede that data. This simplifies the editing process since text overlays can be made without deleting the material that it replaces.

This process is continued until a display command is encountered containing a bit indicating that its associated text string is the last to be used in filling a line buffer. The line buffer contents are then advanced until the line buffer register reaches zero. At this point the line buffer is ready to be used in generating one line of characters across the face of the CRT.

WRITING A SINGLE TEXT LINE ON THE CRT UNDER CONTROL OF THE LINE BUFFER

Referring again to FIG. 4 the scan of the CRT 14 is controlled by a screen timing and format logic control 50 to produce a 480 line scan. This provides fifteen horizontal lines for the display of each character. The preferred embodiment of the invention employs a seven bit wide, one bit high character generating matrix drawn on a 10 dot wide, 15 dot high square. An extra

dot column on each side of the character is used for boundary generation and the square left open provides the horizontal spacing between characters. Nine vertical rows are required for character generation and an extra two rows at the bottom are reserved for lower case descenders. One row at the top of the character is reserved for boundary and rows at the bottom of the character are reserved for underlines and boundary. The last bottom row is left as a space between lines and to provide time during the raster generation for the contents of the line buffer to be changed between the display of two contiguous lines of characters.

In the preferred embodiment of the invention the actual horizontal and vertical deflection circuits are associated with the CRT 14 and the screen timing of unit 50 provides sync signals to the CRT to assure timing control. Alternatively, the screen timing unit could generate the deflection signals. In either event the screen timing unit 50 contains registers which store the instantaneous horizontal and vertical positions of the CRT scan. As has been previously described the cursor register 22 and the boundary register 24 are loaded with the horizontal and vertical addresses of the cursor and boundaries. During the scan these addresses are provided to a comparator 52 which also examines the registers contained in the screen timing unit 50 indicating the horizontal and vertical positions of the scan. When identity is recognized between cursor or boundary address registers and the scan position a signal is provided to an attribute adder unit 54 which constitutes a matrix which generates video modulation signals at the proper time in the scan to generate the necessary matrix dot for the particular attribute. The attribute adder 54 has an input from the screen timing unit 50 for this purpose.

The contents of the horizontal position register in the screen timing logic are also provided to the controller 20 which recirculates the contents of the line buffer 26 in timed relation to the horizontal scan of the CRT so that the column of the line buffer containing a character to be generated in any particular column is presented just as the scan reaches that column. The seven bits of each line buffer column representing the character are provided to a character read-only-memory 56 which constitutes a matrix. The character read-only-memory also has an input from the screen timing logic unit 50 indicating which horizontal line of the fifteen lines allotted to each character the scan is in, and the horizontal register signal. The read-only-memory is encoded so that for each character input at each particular horizontal and vertical position, within that character, it provides either a zero or a one output to the attribute adder 56, depending upon whether the inputted character has a dot in that particular position of the matrix. The attribute adder also receives the three bits of each line buffer word which control whether the character is to be bold, blinked, or underlined and effectively generates appropriate video signals for modulation of the CRT scan.

When a line constituting the characters contained in one line stored in the line buffer is completed the contents of the RAM pointer are provided to the RAM address register and the line buffer is refilled in the manner previously described.

The generation of lines may be terminated when a special display command containing all zeros is encountered or the screen timing logic 50 indicates that

the last available line in the raster has been scanned, whichever event occurs first. In either event the cycle of operation begins again upon receipt of an appropriate timing signal at that point with the contents of the first eight words in the RAM being provided to the cursor register 22 and the boundary register 24.

The screen timing and format logic unit 50 is disclosed in more detail in FIG. 6. The basic timing for the system derives from signals generated by a crystal controlled oscillator 60 preferably having an output frequency of 15.27MHz. This output is provided to a Horizontal Dot within Character Counter 62 constituting a ten state counter which times the generation of the dots forming the horizontal elements of the character matrix. This unit provides a four bit binary signal signifying the 1-10 count to the character read-only-memory 56 to control the selection of signals for the generation of the appropriate dots for the generation of a character inputted to the matrix from the line buffer 26. This four bit binary signal is also provided to the controller 20 wherein it is decoded to control the timing of the various operations of the controller.

A pulse signifying each tenth change of state of the Dot within Character Counter 62 and preferably having a frequency of about 1.52 MHz, is provided to a Character within Line Counter 64 which counts up to 100. The counter 64 provides a seven bit binary output representing its count to the comparator 52 for comparison with the horizontal addresses stored in the cursor register 22 and the boundary register 24. Once in each cycle the character within line counter 64 provides an output to the CRT 14 which acts as a horizontal sync signal to initiate the scan of a horizontal line. The same 15.27 KHz signal is provided to a Vertical Element within Character Counter 66 which counts to 16 and provides a four bit binary signal representing its count to the character read-only-memory 56 to control the vertical position of the horizontal line within the dot matrix which is then being generated.

The output signal of the counter 66 having a frequency of slightly less than 1 KHz is provided to controller 20 and is termed NEXT LINE signify that all of the data stored in the line buffer has been utilized to generate a line and the line buffer must be refilled.

This same output signal of the vertical elements within character counter 66 is provided to a display line number counter 68 which essentially counts the number of character rows displayed during a raster. It is a scale of 32 counter and its five bit binary output, signifying the vertical line number, is provided to the comparator 52 for comparison with the vertical addresses contained in the cursor register 22 and the boundary register 24. Once a cycle it provides an output constituting a vertical sync signal to the CRT 14.

Thus, based on the various outputs from the screen timing and format logic unit 50, generation of a raster on the CRT 14 is controlled by the horizontal sync signal from the counter 64 and the vertical sync signal from the counter 68. Also, the operation of the controller 20 and the line buffer 26 are synchronized to that raster generation; the character ROM 56 is informed as to the particular dot position within the matrix to be generated; and the comparator 52 receives information used to control the addition of attributes stored in the registers 22 and 24 to the character signals at the positions.

FIG. 7 illustrates certain of the elements of the controller 20 which cooperate with the timing circuitry to control the sequence of the system.

The four bit timing signal from the dot within character counter 62 is provided to a timing decoder 70 within the controller to generate various timing signals that are provided to all of the controller circuits.

The initiation of a sequence of filling the line buffer is initiated by the vertical sync signal from counter 68. This signal is provided to the RAM command pointer register 30 to reset it to zero and also to a state generator 72 to place it in an initial state. The state generator 72 is also connected to CPU interface 74 which can provide a signal which changes the condition of the state generator 72 in response to a request signal received from the CPU. The state generator 72 also receives the NEXT LINE output from the counter 66 which initialize its state.

In the absence of an overriding signal from the CPU interface 74, when the state generator 72 receives a VERTICAL SYNC signal, which will coincide with a NEXT LINE signal, it provides an output denominated BEGIN which causes the RAM address selector 28 to go to the RAM address indicated by the RAM command pointer register 30 which has also been initialized by the VERTICAL SYNC signal. Under control of appropriate logic set by these signals, the contents of the first word position in the RAM are loaded into the cursor register 22. This occurs during the time required to generate one character, or the time between two identical states of the timing decoder 70. During the next character time the RAM command pointer register 30 is incremented and the contents of the second RAM word are loaded into the cursor register. This cycle continues until the contents of the first eight RAM positions have been loaded into their appropriate registers.

The state generator 72 receives an output from the RAM address selector 28 and when the first eight words have been loaded the state generator enters its second state entitled LOAD 34 LO. During this state, which occupies one character time, the contents of the ninth word in the RAM are loaded into the lower half of the two word display data address register 34. This requires one character time and the RAM command pointer register 30 is incremented at the end of that time. At the beginning of the tenth word time the state generator 72 is controlled to enter a new state termed LOAD 34 HI. During this single character state the contents of the RAM command pointer register 30 are loaded into the upper half of the register 34.

The next condition of the state generator is controlled by whether the two words loaded into the register 34 previously, represent a link or a command. If they represent a link they are loaded into the RAM command pointer register 30 and the state generator 72 reverts to LOAD 34 LO. This process is repeated until a display command is encountered whence the state generator enters a state entitled LOAD 36 from LOAD 34 HI. During the next character time the subsequent RAM word is loaded into block position register 36 and the RAM command point register 30 is again incremented. Then the state generator enters a state termed LOAD 38 wherein the word then contained in the RAM command pointer register 30, the next subsequent word in RAM, is loaded into the block length register 38.

The state generator 72 next enters the state term WAIT wherein the buffer memory increment control 46 repeatedly generates increment signals for the line buffer register 26 until the contents of the line buffer counter 42 equate with the contents of the block position register 36 as determined by the comparator 44. When this occurs a repeated cycle begins wherein the contents of the RAM at the address obtained in the display data address register 34 are loaded into the then available state of the line buffer along with the associated bold and blink bits from the registers 36 and 38; the display data address register 34 is incremented; and the block length register 38 is decremented. This continues until the block length register reaches zero, indicating that all of the characters of the associated display command have been loaded. If the last display command did not contain a signal indicating that it was the last one to be used in filling a line, the state generator 72 then returns to the LOAD 34 LO state and the cycle repeats. When the last display command to be used in filling a line has been utilized the state generator enters a state termed IDLE.

At any time during this cycle a request from the CPU to the state generator can cause the state generator to enter the COMMUNICATE state wherein access to the RAM is controlled by the communication register. After this request signal has been removed the state generator returns to the state at which the interruption occurred. If the COMMUNICATE request occurs while characters are being loaded from the RAM into the line buffer register the state generator waits until the next character has been fully loaded before responding to the request.

Having thus described our invention we claim:

1. A text display processor comprising: means for storing a plurality of digital signals representative of a plurality of strings of text characters in addressable form; means for storing a plurality of digital signals representative of display commands each defining a section of said stored strings of text characters by address and the position of said characters are to occupy in the display in addressable form; a register for storing signals representative of contiguous sections of text to be displayed; means for filling said register with certain of said digital signals representative of strings of text characters from said means for storing text character signals under control of a plurality of said stored display commands; a display means; and means for writing characters on said display means under control of the contents of said register.

2. The text display processor of claim 1 wherein the display means operates to display a plurality of horizontal lines of alpha-numeric characters and said register operates to store sufficient signals for the generation of a single line of text of said display.

3. The text display processor of claim 1 wherein said means for writing characters on said display means under control of the contents of said register includes a matrix for converting digital signals representative of text characters into analog signals for the control of the display means.

4. The text display processor of claim 3 wherein said display means constitutes a cathode ray tube and said analog signals constitute signals capable of writing alpha-numeric characters on said cathode ray tube in dot matrix form.

5. The text display processor of claim 4 wherein each character dot matrix has a vertical dimension of N dots and a line of characters is written by N horizontal sweeps of the the cathode ray tube beam across the cathode ray tube, all N sweeps being controlled by one set of signals stored in said register.

6. The text display processor of claim 1 wherein said plurality of stored display commands utilized to fill said register are stored in consecutive storage areas within said means for storing a plurality of digital signals representative of display commands.

7. The text display processor of claim 6 wherein said means for storing a plurality of digital signals representative of display commands also stores digital signals operative to alter the normal sequence of utilization of display commands in filling said register.

8. The text display processor of claim 1 wherein said means for storing a plurality of digital signals representative of text characters and said means for storing a plurality of digital signals representative of the display commands both constitute a single random access memory.

9. The text display processor of claim 8 wherein said means for filling said register with certain of said digital signals representative of text characters under control of a plurality of said stored display commands derives display commands from sequential storage areas of said random access memory and further including a plurality of digital signals representative of commands for altering the normal sequence of utilization of said display commands, stored in said random access memory, interspersed with said display commands.

10. The text display processor of claim 1 including means for storing signals relating to the sequence of utilization of said display commands in filling said register, and means for utilizing the last said signals to control said means for filling the register.

11. The text display processor of claim 1 wherein said means for filling said register with certain of said digital signals representative of strings of text characters under control of a plurality of said stored display commands includes means operative to utilize said plurality of display commands sequentially and at least certain of said display commands contain signals indicating they constitute the last display commands to be utilized in filling said register.

12. The text display processor of claim 1 wherein said register is operative to store signals representative of a line of text to be displayed and each display command includes a signal defining the position that the section of stored text characters which that display command defines is to occupy within said display line.

13. The text display processor of claim 1 including means for altering the digital signals representative of strings of text characters and the digital signals representative of display commands connected to said means for storing said digital signals representative of strings of text characters and the digital signals representative of display commands.

14. A text display processor comprising: a random access memory for storing digital signals representative of strings of text characters, digital signals representative of display commands each defining a section of said stored text characters strings by address within the memory and further defining the position said characters are to occupy in the display, and digital signals relating to the sequence of utilization of said display com-

mands; a register for storing signals representative of contiguous sections of text to be displayed; means for filling said register with certain of said digital signals representative of strings of text characters from said random access memory under control of a sequence of said stored display commands, said sequence being determined by said digital signals relating to the sequence of utilization.

15. The text display processor of claim 14 wherein said display means constitutes a cathode ray tube, and further including means for deflecting the beam of the cathode ray tube vertically and horizontally so as to generate a sequence of rasters; means for digitally storing the instantaneous position of said beam; and connections between said means for digitally storing the instantaneous position of said beam, and said means for writing characters on said display means under control of the contents of said register.

16. The text display processor of claim 14 wherein said means for filling said register with certain of said digital signals representative of strings of text characters under control of a sequence of said stored display commands includes means for examining sequential signals stored within said memory, using such signals which are representative of display commands to fill the register with the strings of text characters defined by said display commands and utilizing said digital signals relating to the sequence utilization of said display commands to locate successive display commands in said sequence.

17. The text display processor of claim 14 wherein said digital signals representative of display commands each define a section of said stored strings of text characters by address within the memory, further define the position said characters occupy in the display and further include signals representative of the manner of display of each of said text characters; and said register is filled with both of said aforesaid signals relating to the manner of display of the text characters as well as the text characters.

18. The text display processor of claim 15 further including a plurality of digital signals stored in said random access memory relating to the display of material other than alphanumeric characters on the display, and the position said material is to occupy on the display; and means for comparing such signals representative of the positions with the contents of said means for digitally storing the instantaneous position of said beam within said raster; and means for generating said material on said display means under control of said comparator.

19. The text display processor of claim 18 wherein said means for generating said material on said display means under control of said comparator includes a digital-analog convertor connected to the output of the comparator and connections between said digital-analog convertor and said display means.

20. A system for editing data comprising: a keyboard, a random access memory adapted to receive signals generated by said keyboard; a register; means for writing in said register the contents of a plurality of positions in said random access memory containing digital

codes representative of alpha-numeric characters under the control of digital codes stored in other sections of the memory, each of which code specifies a memory address and the position which the contents of that memory address is to occupy in the register; display means; and means for controlling the display means so as to write the alpha-numeric characters representative of the signals stored in the register under control of the contents of the register.

21. The data editing system of claim 20 wherein the display means constitutes a cathode ray tube, the register constitutes a recirculating register, and including means for recirculating said register in timed relation to the generation of the raster on the cathode ray tube.

22. The data editing system of claim 21 wherein each line of alphanumeric characters on display is generated by a plurality of horizontal scans of the cathode ray tube beam across the cathode ray tube and the contents of the register are modified under control signals stored in the random access memory between the generation of display of two consecutive lines on the cathode ray tube.

23. A text display processor including: means for storing a plurality of first digital signals representative of text characters; a display means; means for writing certain text characters defined by certain of said stored first digital signals on said display means; means for storing second digital signals defining the position and length of lines to be drawn on said display means; and means for drawing lines on said display means under the control of said second signals.

24. The text display processor of claim 23 wherein the display means constitutes a cathode ray tube and means for controlling the beam of the cathode ray tube to cause it to generate a raster consisting of a plurality of horizontal lines vertically spaced from one another, and further including: comparator means for comparing the position of the cathode ray beam in said raster with the contents of said means for storing second digital signals relating to the position and length of lines to be drawn on said display means; and means for modulating the intensity of the cathode ray beam in accordance with the output of said comparator means.

25. In a text display processor including means for storing a plurality of first digital signals representative of text characters, display means, and means for writing text characters by certain of said stored first digital signals on said display means at a first intensity level, means for storing second digital signals defining the character position of a cursor to be drawn on said display means; and means, under control of said second digital signals, for causing a cursor to be displayed at a second lower intensity level in the character position defined by said second digital signals.

26. In the text display processor of claim 25 means for storing third digital signals defining the beginning and end of an underline component to be associated with said cursor, and means for drawing said underlined component on said display means under the control of said third signals.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,848,232

Dated November 12, 1974

Inventor(s) Jerome E. Leibler et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 4, line 49 "oeprator" should read --operator--.
Column 5, line 27 "inferfaced" should read --interfaced--.
Column 6, line 65 "command" should read --commands--.
Column 7, line 41 "000...000" should read --000...001--.
Column 12, line 51 "posi" should be deleted.
Column 15, line 56 "of" (second occurrence) should read --on--.
Column 18, line 48 --defined-- should be inserted between
"characters" and "by".

Signed and sealed this 4th day of March 1975.

(SEAL)

Attest:

RUTH C. MASON
Attesting Officer

C. MARSHALL DANN
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