US 20170041018A1

(19) United States
(12) Patent Application Publication
KUO et al.
(10) Pub. No.: US 2017/0041018 A1
(43) Pub. Date: Feb. 9, 2017

(54) **DIGITAL TO ANALOG CONVERTER WITH OUTPUT IMPEDANCE COMPENSATION**

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(21) Appl. No.: **14/676,227**

(22) Filed: **Apr. 1, 2015**

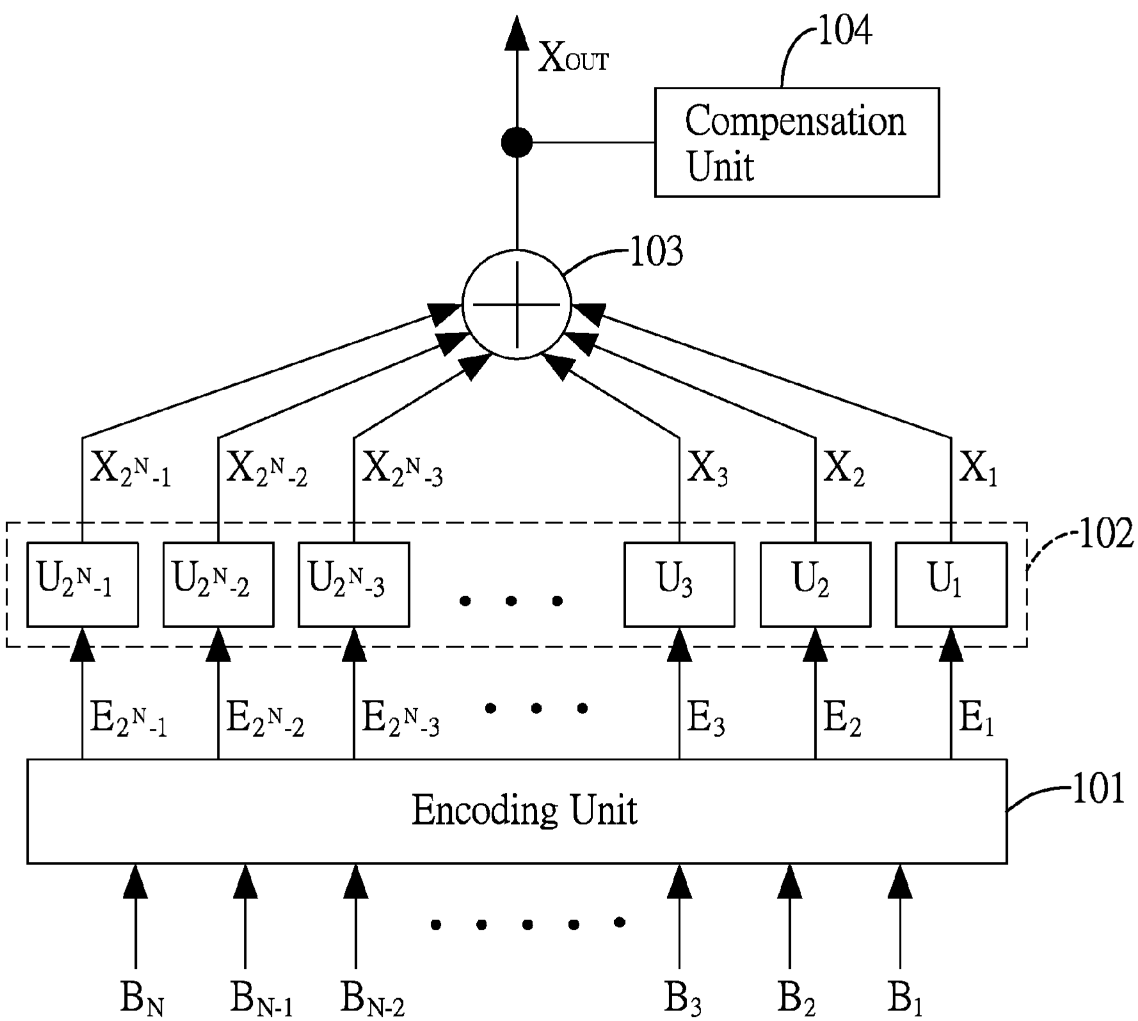
Publication Classification

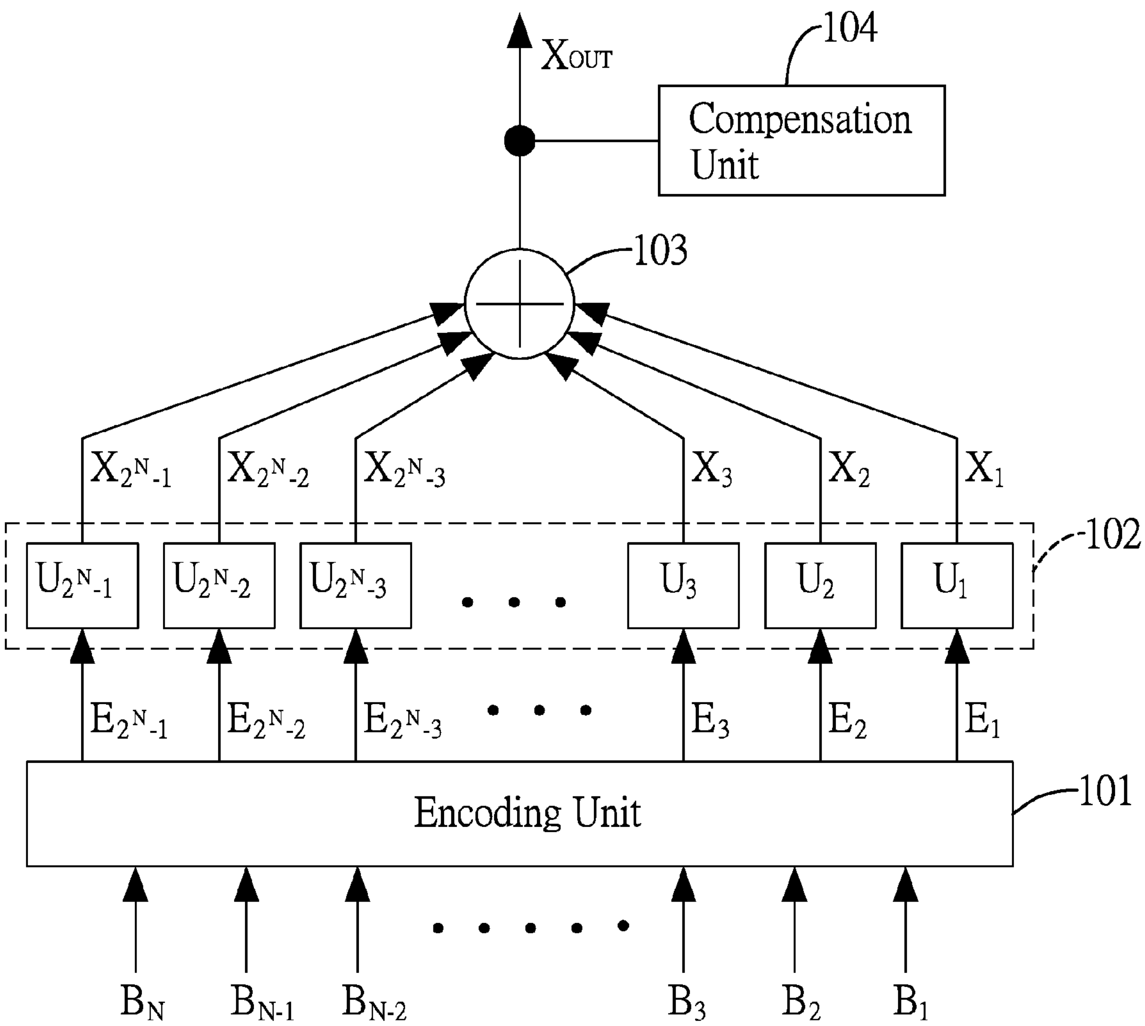
(51) **Int. Cl.**
H03M 1/80 (2006.01)
H03M 1/66 (2006.01)
H03M 1/06 (2006.01)

(52) **U.S. Cl.**
CPC ***H03M 1/808*** (2013.01); ***H03M 1/0602*** (2013.01); ***H03M 1/664*** (2013.01)

(57) **ABSTRACT**

A digital to analog converter with output impedance compensation has an encoding unit, a current cell array, a summing unit and a compensation unit. The compensation unit is connected to output terminals of the DAC and provides a nonlinear impedance to compensate an original output impedance of the DAC. With the compensated output impedance, the SFDR performance and the linearity of the DAC are improved to obtain a superior input-to-output transfer curve.





XOUT
104
Compensation Unit
103
X_{2^N-1}
X_{2^N-2}
X_{2^N-3}
X_3
X_2
X_1
102
U_{2^N-1}
U_{2^N-2}
U_{2^N-3}
U_3
U_2
U_1
E_{2^N-1}
E_{2^N-2}
E_{2^N-3}
E_3
E_2
E_1
Encoding Unit
101
B_N
B_{N-1}
B_{N-2}
B_3
B_2
B_1

FIG.1

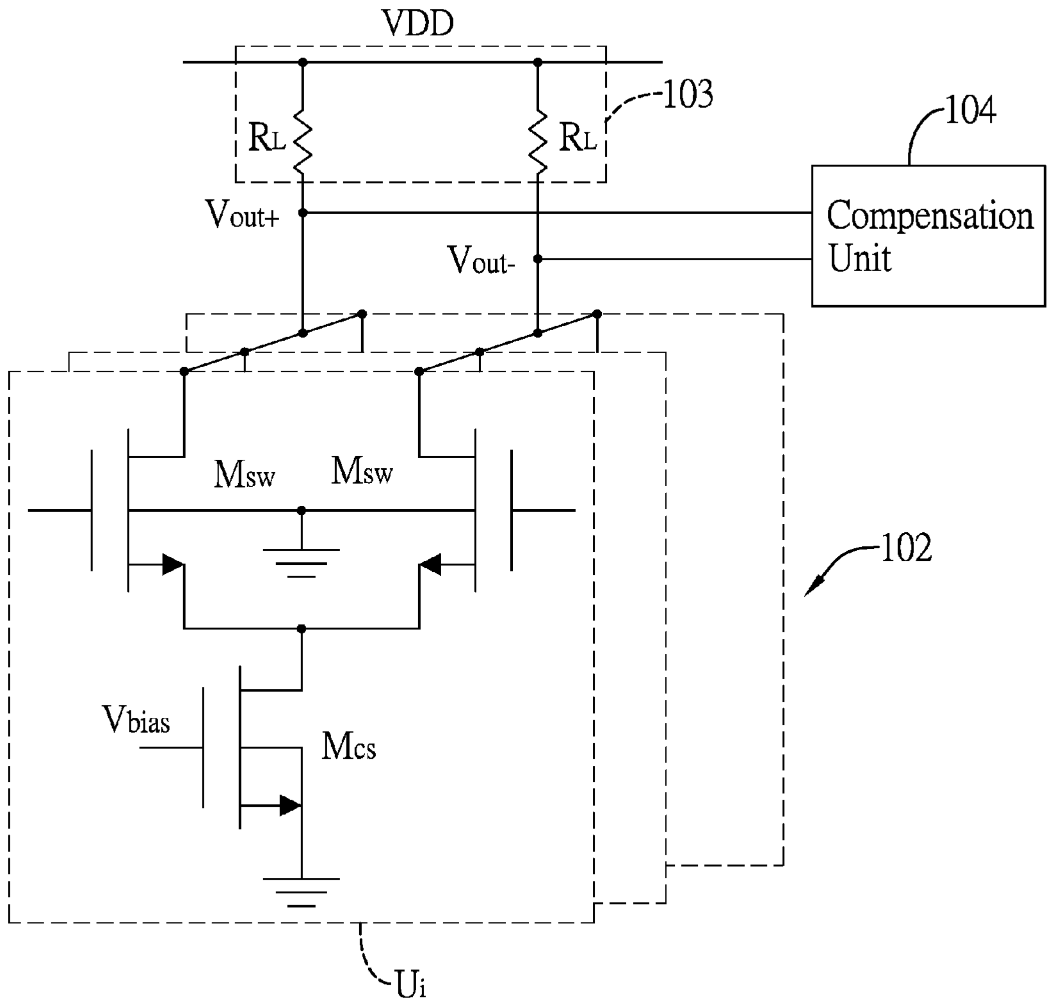

VDD
103
104
RL
RL
Compensation Unit
Vout+
Vout-
Msw
Msw
102
Vbias
Mcs
Ui

FIG.2

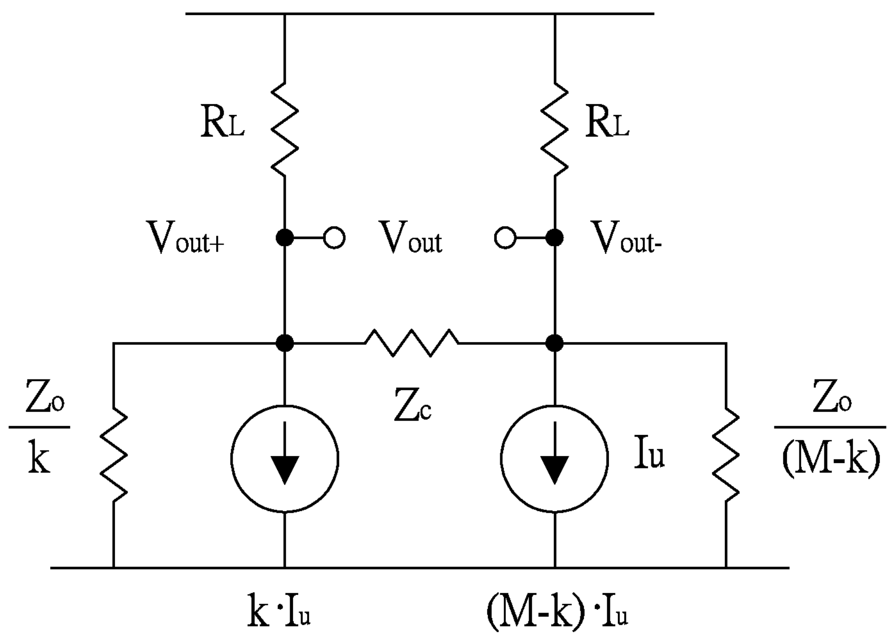


FIG.3

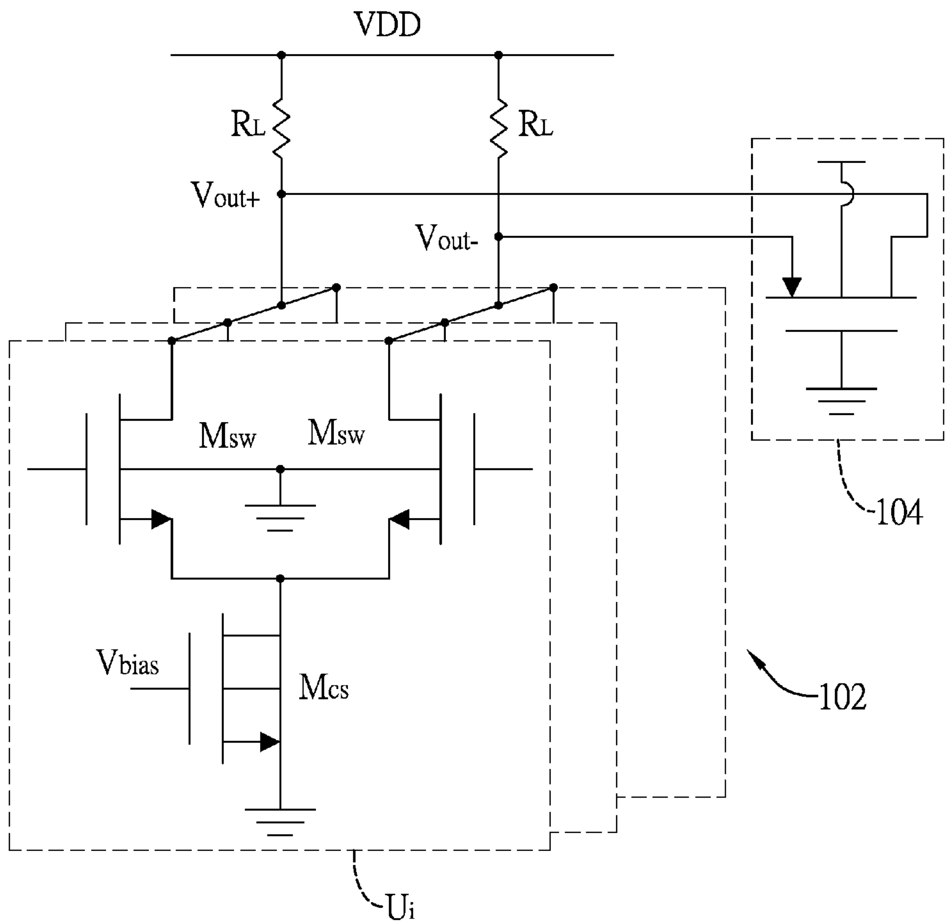


FIG.4

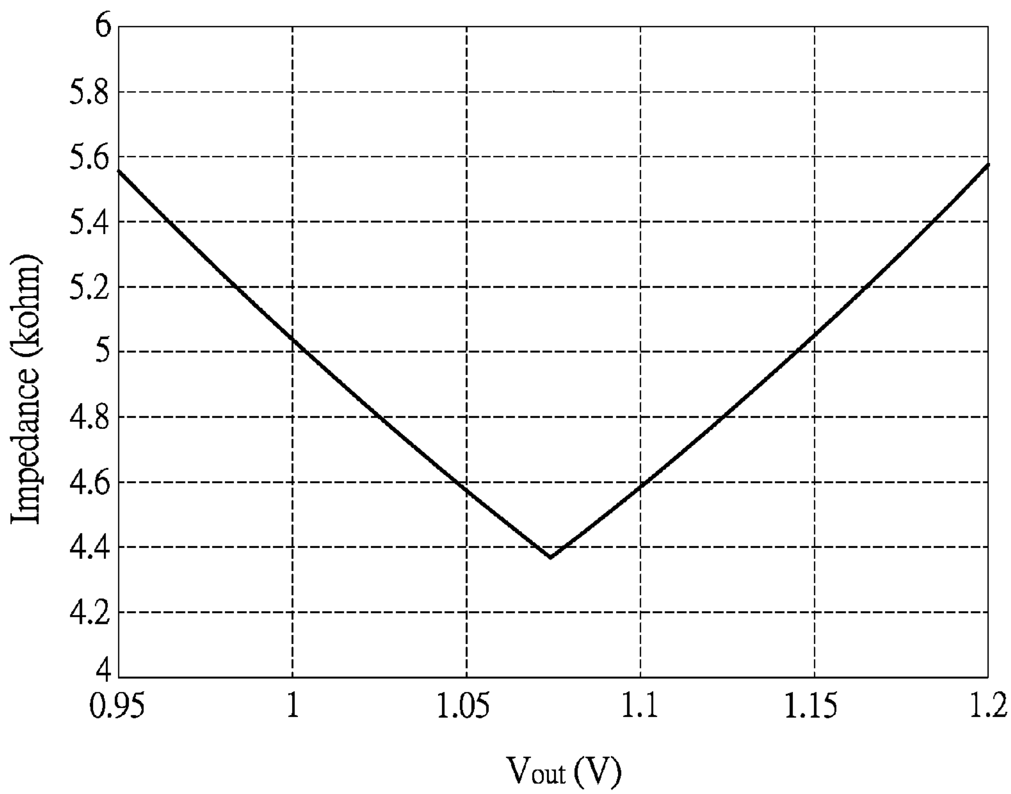
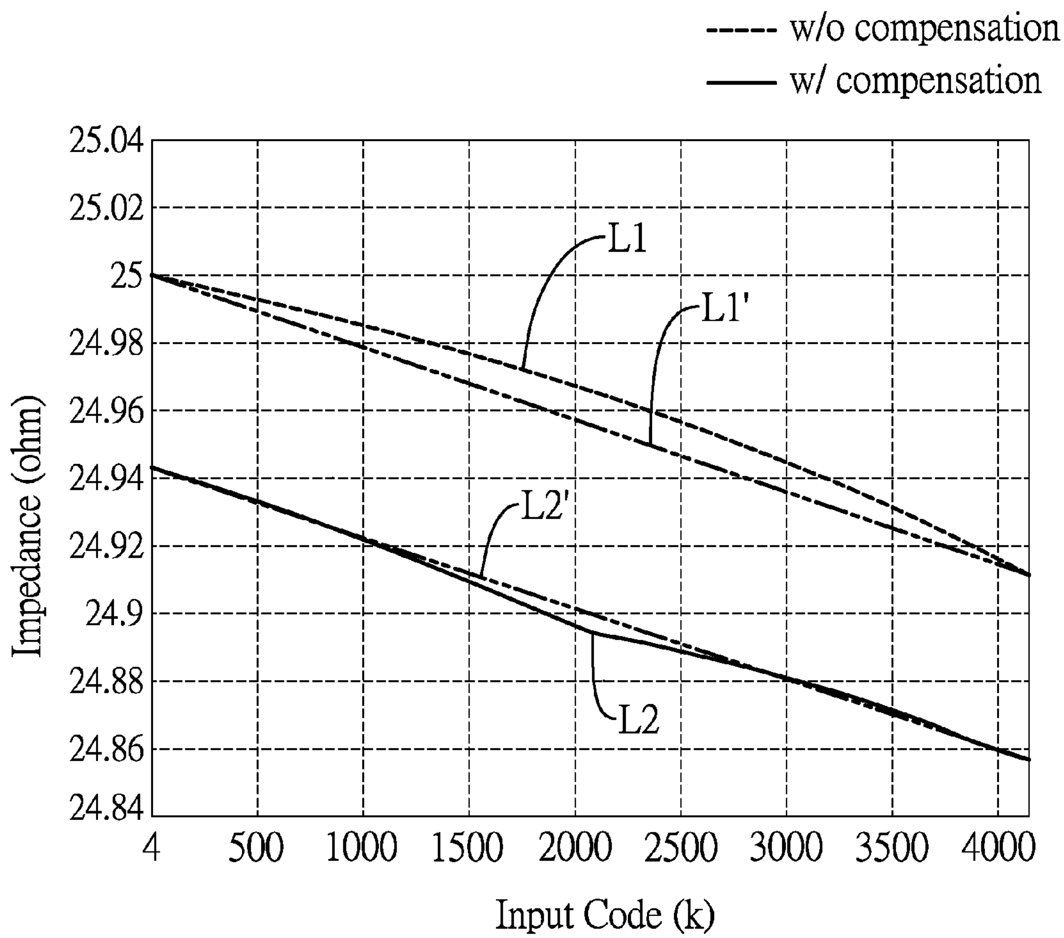

6
5.8
5.6
5.4
5.2
5
4.8
4.6
4.4
4.2
4
Impedance (kohm)
0.95
1
1.05
1.1
1.15
1.2
Vout (V)

FIG.5



w/o compensation
w/ compensation
25.04
25.02
25
24.98
24.96
24.94
24.92
24.9
24.88
24.86
24.84
Impedance (ohm)
L1
L1'
L2'
L2
4
500
1000
1500
2000
2500
3000
3500
4000
Input Code (k)

FIG.6

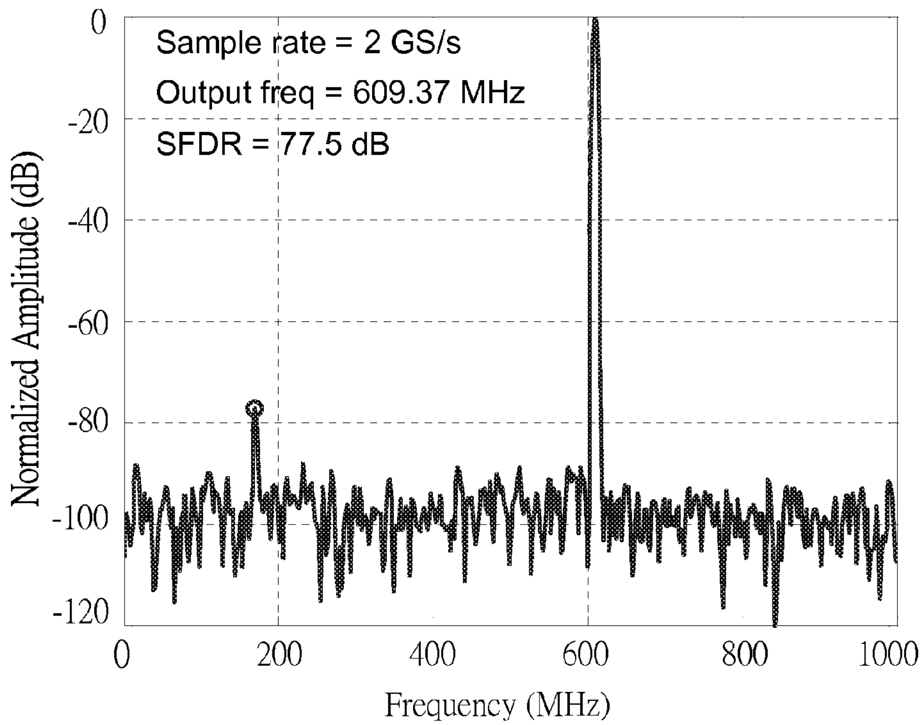


FIG.7A
PRIOR ART

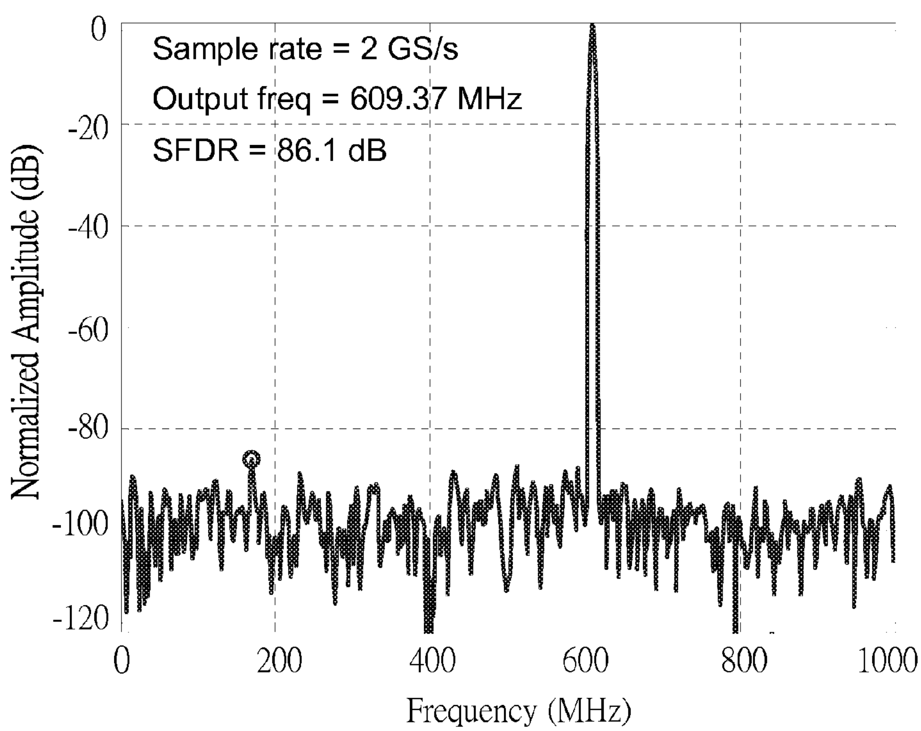
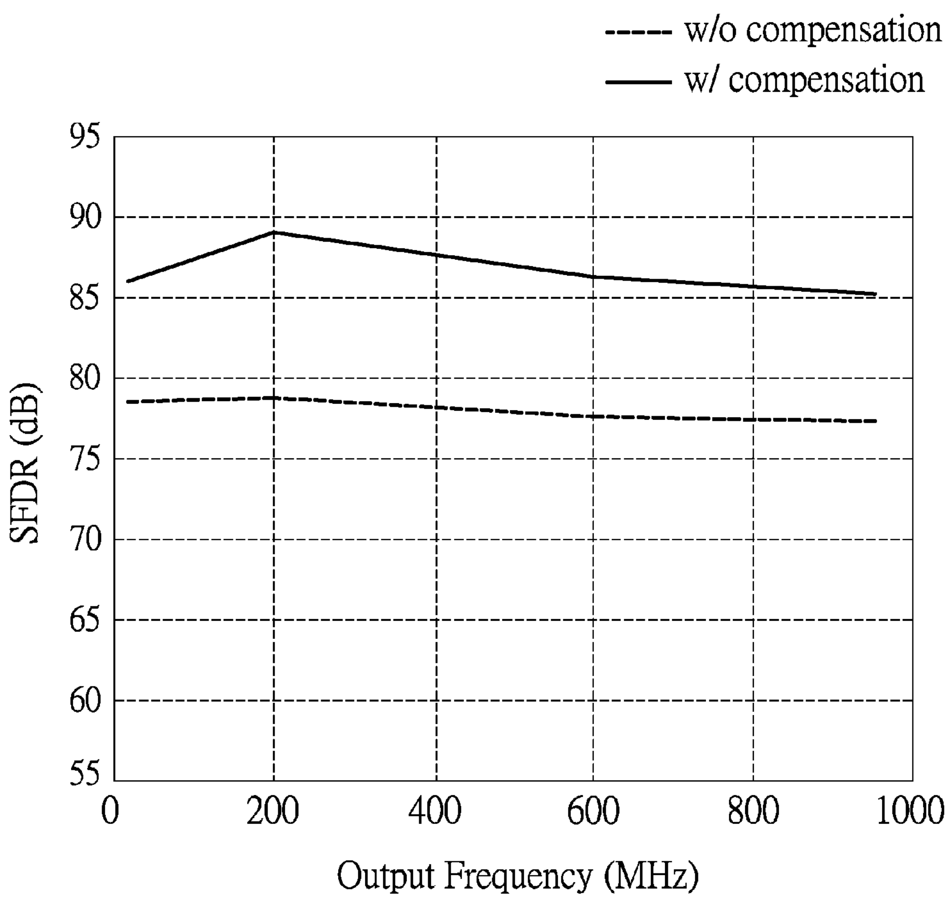


FIG.7B



w/o compensation
w/ compensation
95
90
85
80
75
70
65
60
55
SFDR (dB)
0
200
400
600
800
1000
Output Frequency (MHz)

FIG.8

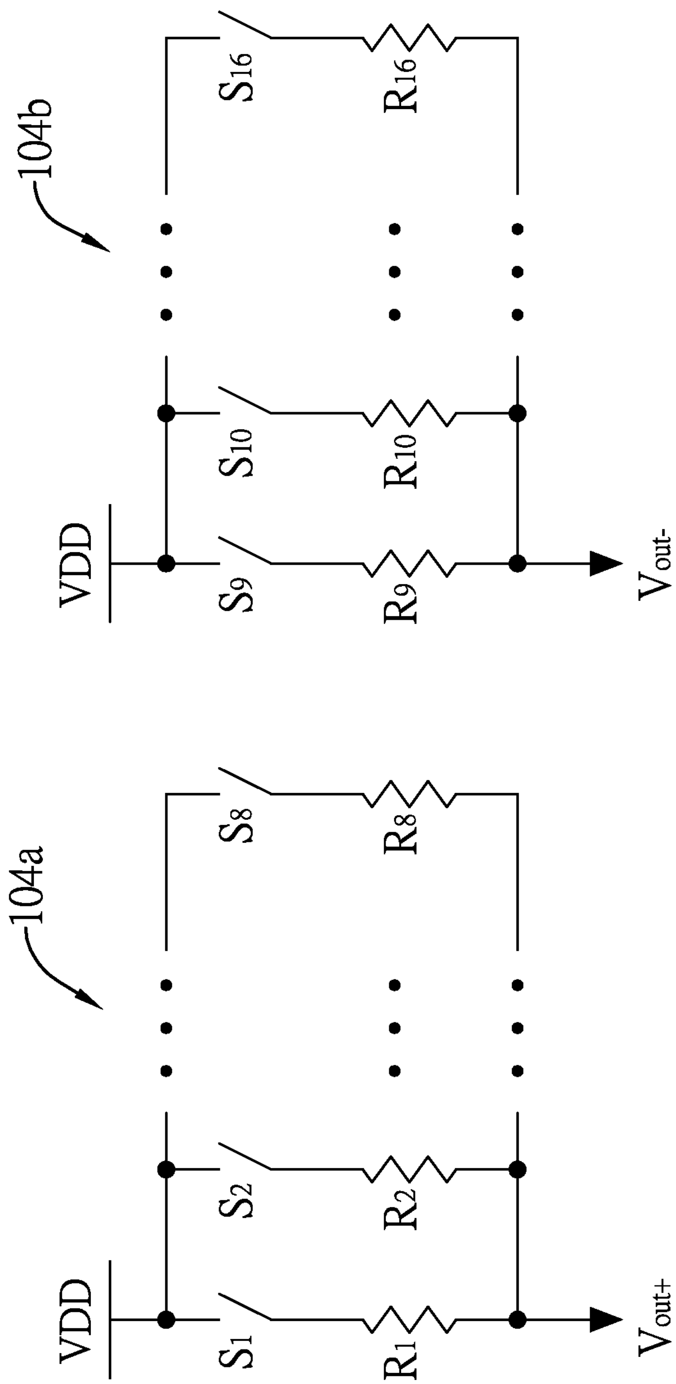

104a
VDD
S_1
S_2
S_8
R_1
R_2
R_8
V_{out+}
104b
VDD
S_9
S_{10}
S_{16}
R_9
R_{10}
R_{16}
V_{out-}

FIG.9

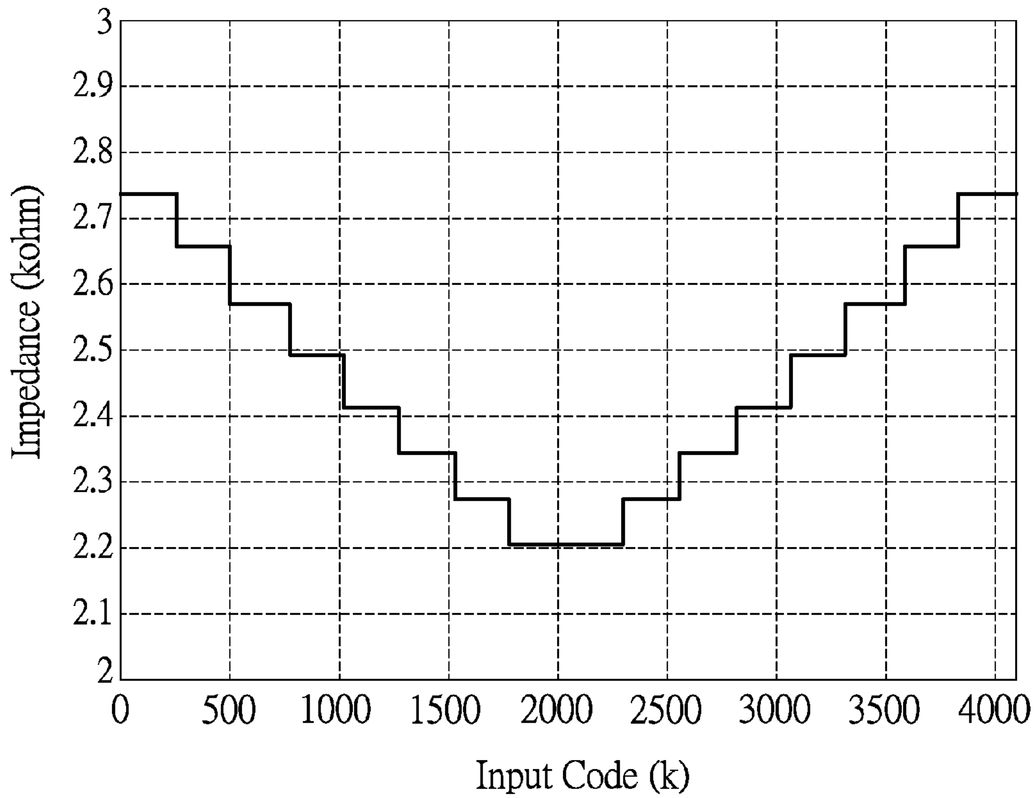

Impedance (kohm)
3
2.9
2.8
2.7
2.6
2.5
2.4
2.3
2.2
2.1
2
0
500
1000
1500
2000
2500
3000
3500
4000
Input Code (k)

FIG.10

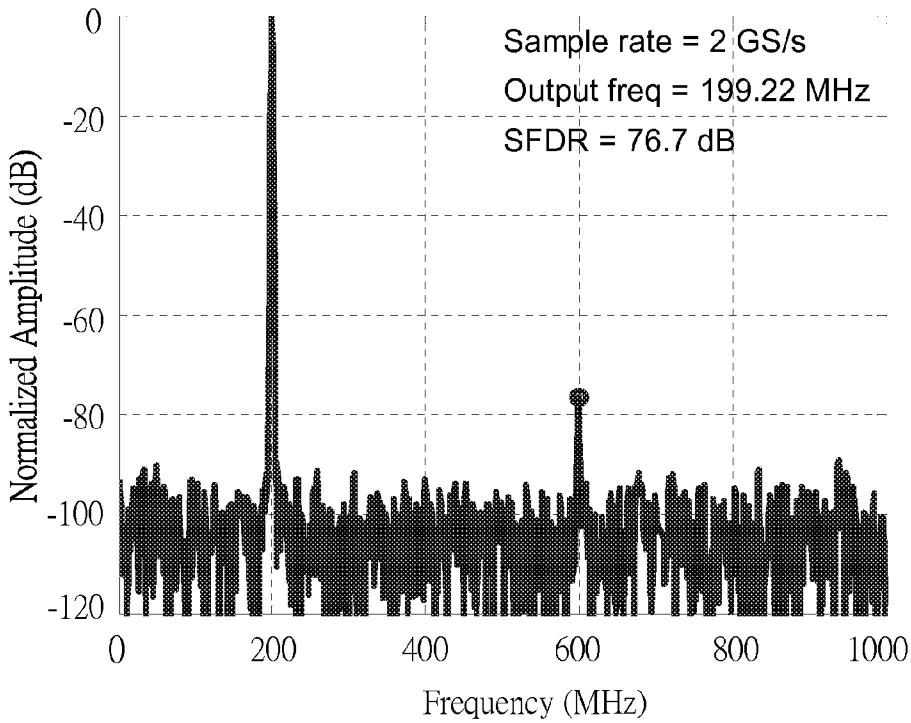


FIG.11A
PRIOR ART

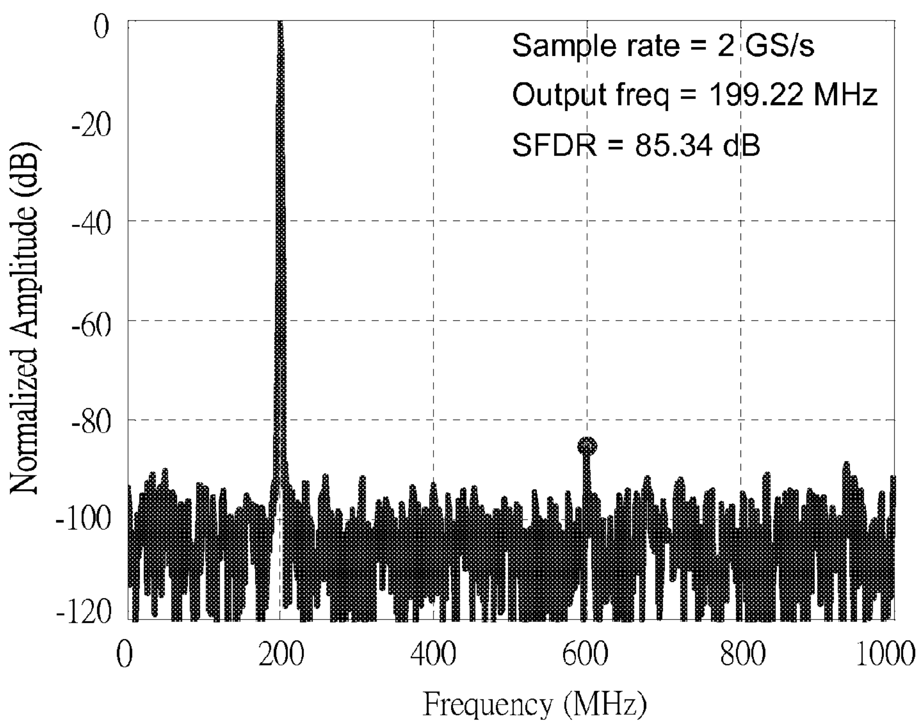


FIG.11B

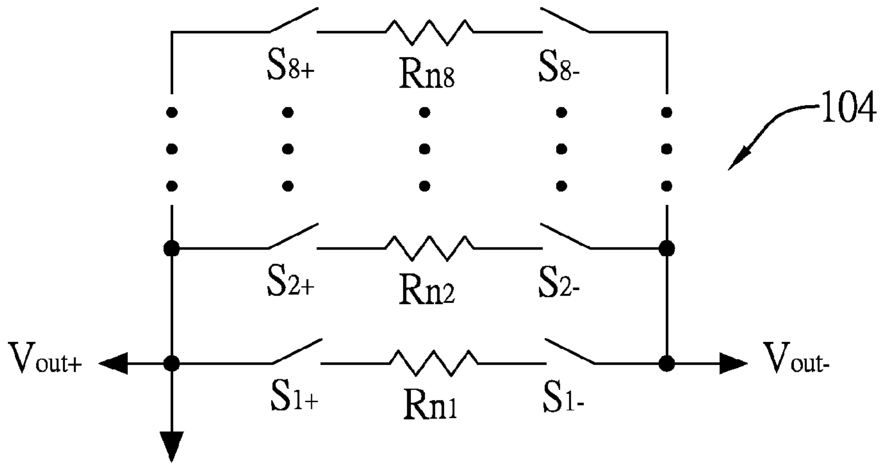


FIG.12

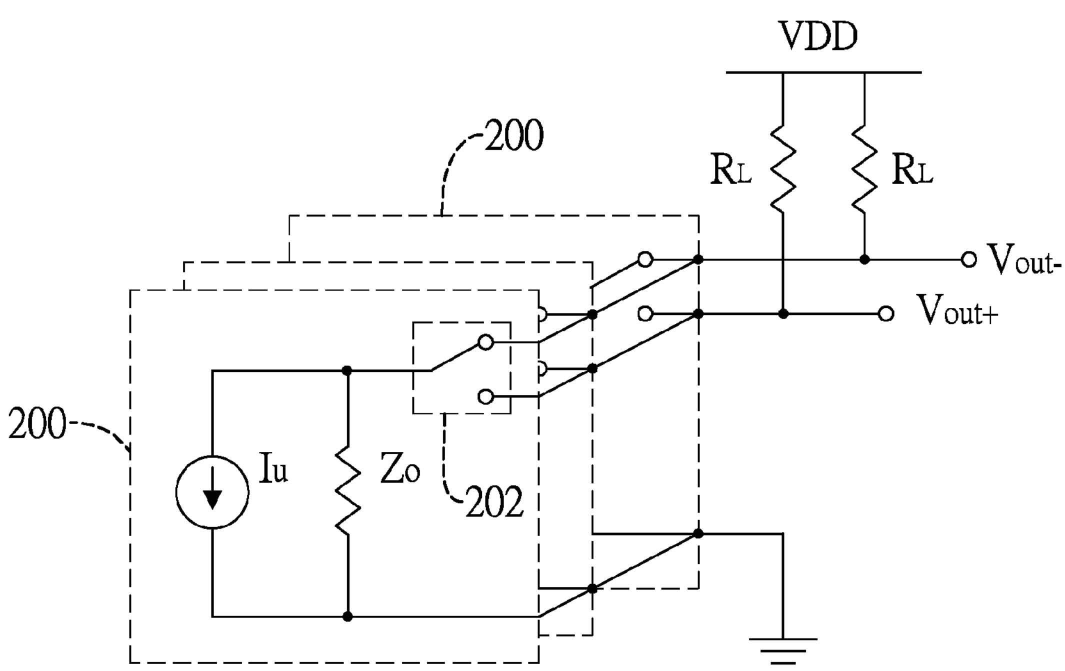


FIG.13
PRIOR ART

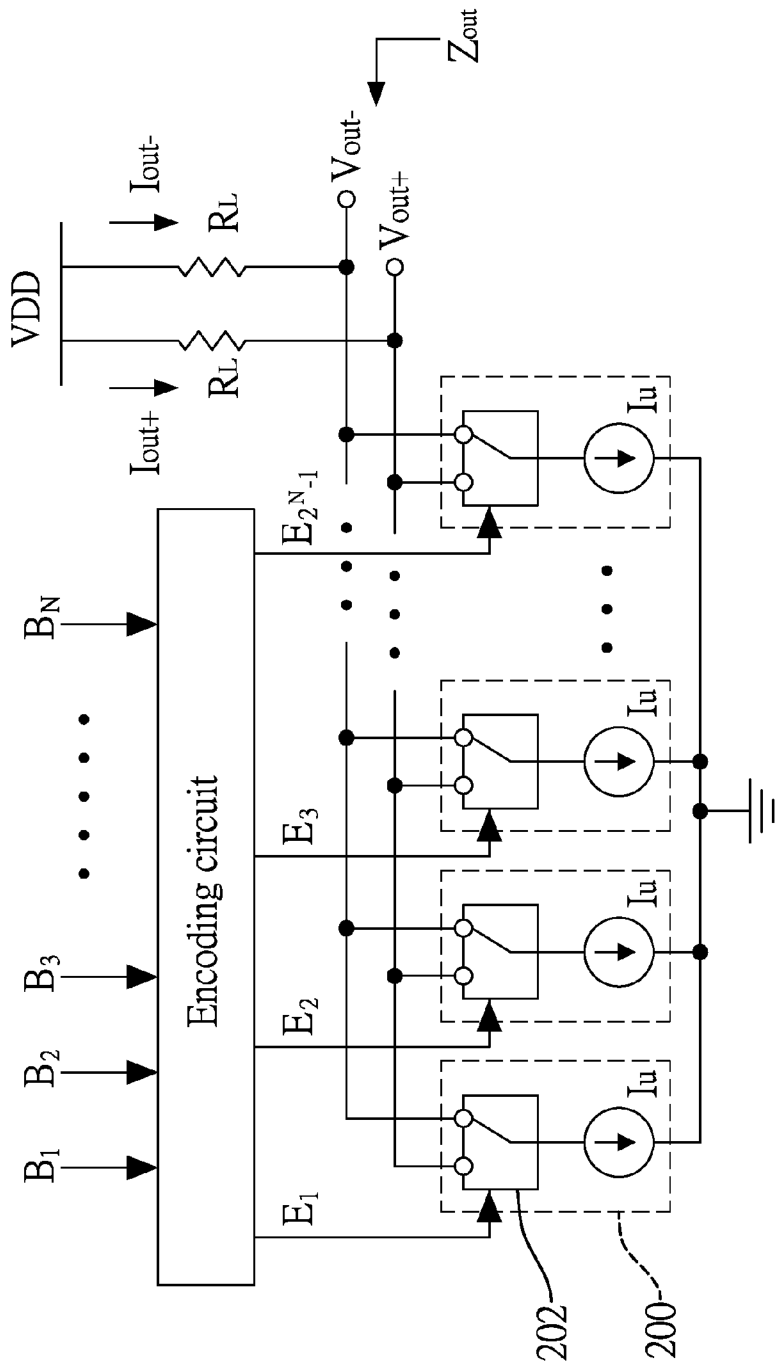


FIG.14
PRIOR ART

DIGITAL TO ANALOG CONVERTER WITH OUTPUT IMPEDANCE COMPENSATION

BACKGROUND OF THE INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a digital to analog converter (DAC), and more particularly to a digital to analog converter with output impedance compensation for enhancing performance of digital to analog conversion.

[0003] Description of the Prior Art

[0004] With reference to FIG. **13**, a multi-bit current-steering digital-to-analog converter (DAC) is composed of multiple current cells **200**. Each of the current cells **200** includes a current source I_u, with an output impedance Z_o of the current cell **200** in parallel and a pair of current switches, wherein the pair of current switches is simplified as a single switching element **202** with two output ends in FIG. **13**. Ideally, the output impedance Z_o of the current cell **200** should be infinitely large, so the current from the current source I_u, can fully flow to an output load R_L instead of flowing to the output impedance Z_o. However, the output impedance of any practical device is finite. As a result, the output current of the current source I_u does not fully flow to the output load R_L, causing some non-ideal effects.

[0005] For a single current cell **200**, the finite output impedance Z_o will only cause gain error rather than nonlinear distortion if the value of the output impedance Z_o is constant. However, the number of all the current cells **200** in the multi-bit current-steering DAC is much more than one. For an N-bit current-steering DAC, there are 2^N-1 current cells **200**. All of the current cells **200** are connected in parallel to sum their output currents at two output terminals V_{out+}, V_{out-} of the DAC.

[0006] With reference to FIG. **14**, considering an N-bit current-steering DAC, there are 2^N-1 current cells **200** connected in parallel at the output terminals of the DAC. An overall output impedance Z_{out} seen from the output terminals V_{out+}, V_{out-} of the DAC is correlated to the number of the current cells **200** connected at the output terminals V_{out+}, V_{out-}. The connection of each current cell **200** to any one of the output terminals V_{out+}, V_{out-} is determined by its respective current switch, which is controlled by digital input signals $B_1, B_2 \ldots B_N$. As a result, the overall output impedance Z_{out} is nonlinear and varies with the digital input signals $B_1, B_2 \ldots B_N$. The nonlinear overall output impedance Z_{out} will cause harmonic distortion tones in frequency domain.

[0007] In addition to the input signals-dependent nonlinearity, the output impedance Z_o of each current cell **200** is also affected by an output voltage at the output terminals V_{out+}, V_{out-}. The output voltage dependency of the output impedance further degrades the linearity of the DAC.

SUMMARY OF THE INVENTION

[0008] An objective of the present invention is to provide a digital to analog converter (DAC) with output impedance compensation, wherein the linearity and the spurious free dynamic range (SFDR) performance of the DAC can be improved.

[0009] The DAC comprises an encoding unit, a current cell array, a summing unit and a compensation unit. The encoding unit receives and encodes a plurality of binary-weighted digital inputs to generate a plurality of encoded controlling signals. The current cell array comprises a plurality of conversion units that respectively receive the encoded controlling signals to generate analog output signals. The summing unit receives the analog output signals from the current cell array and sums the analog output signals to generate an accumulated analog output signal. The compensation unit provides a nonlinear impedance to compensate an output impedance seen from the current cell array and the summing unit of the DAC.

[0010] By incorporating the compensation unit in the DAC, the output impedance is compensated and improved. As a result, the linearity of an input-to-output transfer curve of the DAC is improved, and the SFDR performance of the DAC can also be enhanced.

[0011] Other objectives, advantages and novel features of the invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** shows an N-bit digital to analog converter (DAC) of the present invention;

[0013] FIG. **2** shows a current cell array comprised of multiple conversion units of the DAC of FIG. **1**;

[0014] FIG. **3** shows a simplified impedance model of the current cell array connected with an impedance model Z_c of a compensation circuit;

[0015] FIG. **4** is a circuit diagram showing the current cell array connected to the compensation unit implemented by a single PMOS transistor of the present invention;

[0016] FIG. **5** shows an impedance curve of the PMOS transistor of FIG. **4**;

[0017] FIG. **6** shows output impedance curves of a 12-bit exemplary DAC without and with output impedance compensation;

[0018] FIGS. **7**A and **7**B respectively show SPICE-simulated output spectrums of the 12-bit exemplary DAC without and with the compensation unit of FIG. **5**;

[0019] FIG. **8** shows the SPICE-simulated SFDR curves of the 12-bit exemplary DAC without and with output impedance compensation;

[0020] FIG. **9** is a circuit diagram showing the compensation unit implemented by two compensation circuits of the present invention;

[0021] FIG. **10** shows an impedance curve of the two compensation circuits of FIG. **9**;

[0022] FIGS. **11**A and **11**B respectively show SPICE-simulated output spectrums of the 12-bit exemplary DAC without and with the compensation unit of FIG. **9**;

[0023] FIG. **12** is a circuit diagram showing a third embodiment of the compensation unit of the present invention;

[0024] FIG. **13** shows a current cell array of a conventional N-bit current-steering DAC;

[0025] FIG. **14** shows an architecture of the conventional N-bit current-steering DAC.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] With reference to FIG. **1**, an N-bit digital to analog converter (DAC) according to the present invention comprises an encoding unit **101**, a current cell array **102** comprised of multiple current cells U_i, where i is from 2^N-1 to

1, a summing unit **103** and a compensation unit **104**, wherein each current cell U_i is a conversion unit.

[0027] The encoding unit **101** receives a plurality of binary-weighted digital inputs B_N to B_1. The encoding unit **101** generates a plurality of encoded controlling signals E_i, where i is from 2^N-1 to 1, based on the received binary-weighted digital inputs B_N to B_1 for the current cells U_i respectively. The encoded controlling signals E_i may be thermometer-coded signals, direct binary-coded signals, or the combination of the both. The current cells U_i respectively receive the encoded controlling signals E_i and generate respective analog output signals X_i, where i is from 2^N-1 to 1. The summing unit **103** receives the analog output signals X_i from all of the current cells U_i and generates an accumulated analog output signal X_{OUT}. The compensation unit **104** is provided to compensate an output impedance seen from outputs of the summing unit **103** and the current cell array **102**.

[0028] The DAC may have two differential output terminals or a single-end output terminal. In one embodiment, the compensation unit **104** comprises two separated compensation circuits connected to the differential output terminals of the DAC respectively. In another embodiment, the compensation unit **104** is a single compensation circuit connected between the differential terminals. In yet another embodiment, the compensation unit **104** is a single compensation circuit connected to the single-end output terminal.

[0029] With reference to FIG. **2**, for an N-bit current-steering DAC, a number of the current cells U_i of the N-bit DAC is 2^N-1. In this embodiment, the DAC has differential output terminals V_{out+}, V_{out-} at which the current cell array **102** and the summing unit **103** are connected together. All of the current cells U_i are connected to the differential output terminals V_{out+}, V_{out-}. Each current cell U_i comprises a current source M_{CS}, and a pair of current switches M_{SW}. The current switches M_{SW} direct an output current of each current cell U_i to one of the differential output terminals V_{out+}, V_{out-}. The compensation unit **104** provides a nonlinear compensating impedance Z_C between the differential output terminals V_{out+}, V_{out-} of the DAC.

[0030] With reference to FIG. **3**, a simplified impedance model of the current cell array **102** with an impedance model of the compensation unit **104** is shown. By providing the nonlinear compensating impedance Z_C between the differential output terminals of the DAC, the original nonlinear output impedance of the DAC is compensated. With the compensated output impedance, the linearity of the DAC's output signal can be increased. Therefore, the spurious free dynamic range (SFDR) performance of the DAC will be improved. The nonlinear compensating impedance Z_C can be designed to be simple or complex according to the desired performance and implementation complexity.

[0031] In the impedance model of FIG. **3**, M is the number of total current cells U_i, i.e. $M=2^N-1$, k is the decimal value of the received binary-weighted digital inputs B_N to B_1, and R_L is a loading resistor. Each current cell U_i is modeled as an output impedance Z_o connected in parallel with an ideal current source providing an output current I_u. The output current of each current cell flows to one of the differential output terminals V_{out+}, V_{out-} under the control of the current switches. Since the current cells U_i are connected at the differential output terminals V_{out+}, V_{out-}, all of the output impedances of the current cells U_i are connected in parallel and can be denoted by Z_o/k and $Z_o/(M-k)$. Therefore, the total output impedances of the DAC seen from the output terminals vary with the input signal.

[0032] With reference to FIG. **4**, the compensation unit **104** in accordance with a first embodiment is implemented by a P-type metal-oxide-semiconductor (PMOS) transistor operated in a linear region and having a source, a drain and a gate. The drain and the source of the PMOS transistor are respectively connected to the differential output terminals V_{out+}, V_{out-}, and the gate is grounded. With reference to FIG. **5**, due to the non-ideal effects of the PMOS transistor and the symmetric voltages at the differential output terminals V_{out+}, V_{out-} of the DAC, the impedance curve of the PMOS is symmetrically v-shaped. The Y-axis represents the impedance value and the X-axis represents an output voltage of one of the differential output terminals V_{out+}, V_{out-}.

[0033] With reference to FIG. **6**, two output impedance curves of a 12-bit exemplary DAC are shown, wherein the broken lines indicate the original output impedance curve without compensation L1, and the solid line indicates the output impedance curve with compensation L2 of the present invention. Comparing the output impedance curve without compensation L1 with a first ideal linear line L1', it is noted that the difference between the linearity of the output impedance curve without compensation L1 and the first ideal linear line L1' is very obvious especially when the input code is about at the middle value, i.e. 2048. The linearity of the output impedance curve without compensation L1 is not good.

[0034] By adding the compensation unit **104** that provides a small impedance corresponding to the middle input code as shown in FIG. **5**, the output impedance curve with compensation L2 will be more closer to a second ideal linear line L2'. The difference between the output impedance curve with compensation L2 and the second ideal linear line L2' is reduced. The v-shaped impedance curve of the PMOS can improve the original output impedance of the DAC and accordingly make the curve of the compensated output impedance have superior linearity.

[0035] With reference to FIGS. **7**A and **7**B, two output spectrums of the 12-bit exemplary DAC are generated by Simulation Program with Integrated Circuit Emphasis (SPICE) software. FIG. **7**A shows the output spectrum without output impedance compensation. FIG. **7**B shows the output spectrum with output impedance compensation of the present invention. The harmonic distortion is reduced by the impedance compensation. The sample rate of the DAC is 2GS/s, the output frequency is 609.37 MHz, and the SFDR performance is improved from 77.5 dB to 86.1 dB.

[0036] With reference to FIG. **8**, the SPICE-simulated SFDR curves without and with the output impedance are shown. The broken lines indicate the original SFDR without compensation, and the solid line indicates the SFDR with compensation of the present invention. The compensation unit **104** can improve more than 8 dB for SFDR performance at any output frequencies.

[0037] With reference to FIG. **9**, the compensation unit **104** in accordance with a second embodiment is implemented by two compensation circuits **104***a*, **104***b* for connecting to the differential output terminals V_{out+}, V_{out-} of the DAC respectively. Each compensation circuit **104***a*, **104***b* comprises multiple selectable resistors R**1** to R**8**, R**9** to R**16** connected in parallel, wherein each selectable resistor is connected with a respective controllable switch S**1** to S**8**, S**9** to S**16** in series. The resistors R**1**-R**8** of the same compensation circuit **104***a* have different resistances. The controllable switches S**1** to S**8**, S**9** to S**16** are selected and turned on depending on the received binary-weighted digital inputs B_N to B_1. For a DAC with a single-end output terminal, a single compensation circuit **104***a* can be connected to the output terminal DAC as the compensation unit **104**.

[0038] With reference to the following table for a 12-bit DAC with two differential output terminals, relationships between the received binary-weighted digital inputs B_N to B_1 and the selected resistors are shown. The binary-weighted digital inputs B_N to B_1 are represented in decimal values 0 to 4095 of an input data range. For example, if the binary-weighted digital inputs B_N to B_1 correspond to any one of the decimal values 0 to 255, the corresponding controllable switches S**1** and S**9** of the two compensation circuits **104***a*, **104***b* will be turned on to select the resistors R**1** and R**9**. Preferably, both of the selected resistors in the two compensation circuits **104***a*, **104***b* have the same resistance, i.e. R**1**=R**9**, R**2**=R**10**, R**3**=R**11**, R**4**=R**12**, R**5**=R**13**, R**6**=R**14**, R**7**=R**15**, and R**8**=R**16**.

Input code (decimal value)	Turn-on switches	Selected resistors
0-255, 3840-4095	S1, S9	R1, R9
256-511, 3584-3839	S2, S10	R2, R10
512-767, 3328-3583	S3, S11	R3, R11
768-1023, 3072-3327	S4, S12	R4, R12
1024-1279, 2816-3071	S5, S13	R5, R13
1280-1535, 2560-2815	S6, S14	R6, R14
1536-1791, 2304-2559	S7, S15	R7, R15
1792-2047, 2048-2303	S8, S16	R8, R16

[0039] With reference to FIG. **10**, the impedance curve of the two compensation circuits **104***a*, **104***b* is formed by different impedance values contributed by the resistors R**1** to R**16**. The impedance curve has a highest impedance value corresponding to a lowest input value and a highest input value of the input data range, and has a lowest impedance value corresponding to a middle input value of the input data range. Therefore, the impedance curve of is substantially and symmetrically v-shaped.

[0040] With reference to FIGS. **11**A and **11**B, two output spectrums of the 12-bit exemplary DAC are generated by SPICE software. FIG. **11**A shows the output spectrum without output impedance compensation. FIG. **11**B shows the output spectrum with output impedance compensation of the present invention. The harmonic distortion is reduced by the impedance compensation. The sample rate of the DAC is 2GS/s, the output frequency is about 200 MHz, and the SFDR performance can be improved from 76.7 dB to 85.3 dB.

[0041] With reference to FIG. **12**, a third embodiment of the compensation unit **104** is connected between the differential output terminals V_{out+}, V_{out-} of the DAC respectively. The compensation unit **104** comprises multiple selectable resistor unit R_{n1} to R_{n8} connected in parallel, wherein each selectable resistor unit R_{n1} to R_{n8} is connected to two respective controllable switches S_{1+} to S_{8+}, S_{1-} to S_{8-} in series. The resistor units R_{n1}–R_{n8} have different resistances. If the $R_{n1-}=2\times R_1=2\times R_9$ and so on, the compensation unit **104** will have the same output impedance curve as shown in FIG. **10**.

[0042] With reference to the following table for a 12-bit DAC with two differential output terminals, relationships between the received binary-weighted digital inputs B_N to B_1 and the selected resistors are shown.

Input code (decimal value)	Turn-on switches	Selected resistors
0-255, 3840-4095	S_{1+}, S_{1-}	R_{n1}
256-511, 3584-3839	S_{2+}, S_{2-}	R_{n2}
512-767, 3328-3583	S_{3+}, S_{3-}	R_{n3}
768-1023, 3072-3327	S_{4+}, S_{4-}	R_{n4}
1024-1279, 2816-3071	S_{5+}, S_{5-}	R_{n5}
1280-1535, 2560-2815	S_{6+}, S_{6-}	R_{n6}
1536-1791, 2304-2559	S_{7+}, S_{7-}	R_{n7}
1792-2047, 2048-2303	S_{8+}, S_{8-}	R_{n8}

[0043] By adding a nonlinear impedance compensation unit **104** at the output terminals of the DAC, the compensated output impedance of the DAC will have superior linearity and the SFDR performance of the DAC is improved. Further, because the output impedance of the DAC is improved by connecting a relative simple compensation unit **104** at the output terminal instead of modifying the structures of the current cells U_i, the fabricating cost of the DAC is relative low. With the simple structure, the compensation unit **104** is suitable to be applied to high-speed DACs.

[0044] Even though numerous characteristics and advantages of the present invention have been set forth in the foregoing description, together with details of the structure and features of the invention, the disclosure is illustrative only. Changes may be made in the details, especially in matters of shape, size, and arrangement of parts within the principles of the invention to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

1. A digital to analog converter (DAC) with output impedance compensation, the DAC comprising:

an encoding unit receiving and encoding a plurality of binary-weighted digital inputs to generate a plurality of encoded controlling signals;

a current cell array comprising a plurality of conversion units that respectively receive the encoded controlling signals to generate analog output signals;

a summing unit receiving the analog output signals from the current cell array and summing the analog output signals to generate an accumulated analog output signal; and

a compensation unit providing a nonlinear impedance to compensate an output impedance seen from the current cell array and the summing unit of the DAC;

wherein the plurality of binary-weighted digital inputs is capable of expressing an input data range; and

an impedance curve of the nonlinear impedance provided by the compensation unit has

a highest impedance value corresponding to a lowest input value and a highest input value of the input data range; and

a lowest impedance value corresponding to a middle input value of the input data range.

2. (canceled)

3. The DAC as claimed in claim **1**, wherein the DAC has two differential output terminals at which the current cell array and the summing unit are connected together, and the compensation unit is connected between the differential output terminals to compensate the output impedance of the DAC.

4. The DAC as claimed in claim **3**, wherein the compensation unit is a PMOS transistor operated in a linear region and having a source, a drain and a gate, wherein the drain and the source of the PMOS transistor are respectively connected to the two differential output terminals, and the gate is grounded.

5. The DAC as claimed in claim **3**, wherein the compensation unit comprises two separate compensation circuits respectively connected to the differential output terminals.

6. The DAC as claimed in claim **5**, wherein each of the compensation circuits comprises multiple resistors connected in parallel and each resistor is connected with a controllable switch in series, wherein the resistors of the same compensation circuit have different resistances.

7. The DAC as claimed in claim **6**, wherein the controllable switches are selectively turned on according to the binary-weighted digital inputs.

8. The DAC as claimed in claim **3**, wherein the compensation unit comprises multiple resistor units connected in parallel and each resistor unit is connected with two controllable switches in series, wherein the resistor units have different resistances.

9. The DAC as claimed in claim **1**, wherein the DAC has a single-end output terminal, and the compensation unit is connected to the single-end output terminal to compensate the output impedance of the DAC.

10. The DAC as claimed in claim **9**, wherein the compensation unit comprises multiple resistors connected in parallel, and each resistor is connected with a controllable switch in series, wherein the resistors have different resistances.

11. The DAC as claimed in claim **10**, wherein the controllable switches are selectively turned on according to the binary-weighted digital inputs.

12. The DAC as claimed in claim **3**, wherein each conversion unit comprises a current source and a pair of current switches.

13. The DAC as claimed in claim **5**, wherein each conversion unit comprises a current source and a pair of current switches.

14. The DAC as claimed in claim **9**, wherein each conversion unit comprises a current source and a pair of current switches.

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