PATENT SPECIFICATION (11) 1 558 937

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(21) Application No. 25783/77 (22) Filed 21 Jun. 1977 (19)
(31) Convention Application No. 2627855 (32) Filed 22 Jun. 1976 in
(33) Fed. Rep. of Germany (DE)
(44) Complete Specification Published 9 Jan. 1980
(51) INT. CL.[3] H01L 29/30 29/70
(52) Index at Acceptance
H1K 1AA9 2S1B 2S20 2S2D 2S2P 9D1 9D2 9N3 9R2 KB



(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR COMPONENTS

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the

invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

The present invention relates to semiconductor components having two zones of different conductivity types separated by a p-n junction, one of said zones being formed by at least a part of a monocrystalline semiconductor body, and the other of said zones being produced in the semiconductor body by a doping process, for example, implantation or diffusion.

In double-diffused silicon planar transistors, for example, having an emitter produced by the diffusion of phosphorus, the so-called emitter dip occurs in the base zone below the emitter; this effect renders control of the base width and current amplification difficult and increases the internal base track resistance. In addition, the emitter efficiency is well below the expected theoretical value corresponding to the doping used. When arsenic is used for doping the emitter, although no emitter-dip effect usually occurs, in this case also, the theoretical value of the emitter efficiency is nowhere near reached.

Both effects have their origin in the high surface doping concentration usually used for the emitter, because, on the one hand, of the production of crystal faults, and on the other hand, of the increased recombination of the minority carriers and reduction in the effective emitter doping due to the reduction in the band spacing.

In order to avoid these disadvantages, the so-called polysil emitter has been proposed. This makes use of the idea of screening the silicon monocrystal from the harmfully high doping concentration during production of the emitter. For this purpose, on the completion of the conventional processes in producing a transistor by the planar technique, including the base diffusion, an emitter window is opened in the surface oxide layer and a thin layer of polycrystalline, undoped silicon is then deposited in the window in a conventional manner. Phosphorus, for example, is then diffused into the monocrystal through the polycrystalline silicon layer. This disturbingly high doping concentration thus occurs at the surface of the polycrystalline silicon layer, and it is possible to set the concentration of the dopant in the monocrystal by controlling the diffusion time.

Transistors produced in this way exhibit no emitter-dip effect at high current amplification. The penetration depth is extremely small, and the layer resistance of the base zone below the emitter is only slightly increased.

However, when this polysil technique is used, the polysilicon deposition parameters and the boundary properties between the polysilicon layer and the monocrystal have a strong influence on the electrical characteristics of the transistor.

It is an object of the present invention to provide a semiconductor component of the kind referred to above which does not suffer from these disadvantages and which has properties which are better than corresponding conventional components.

According to the invention, there is provided a semiconductor component having two zones of different conductivity types in a monocrystalline semiconductor body and separated by a p-n junction, one of said zones being formed in the other of said zones by doping and containing a region in which the lattice structure of the semiconductor body has been damaged during production of the component, said p-n junction surrounding and being spaced from said region. The region having a damaged lattice structure may

be at least partially healed.

The semiconductor components of the invention can conveniently be produced by first producing a localised region in a monocrystalline semiconductor body or a zone thereof of one conductivity type, the lattice structure of which region is damaged, and doping that part of the semiconductor body which contains the region having the damaged lattice structure to form therein a zone of the other conductivity type, in such a way that the p-n junction formed by the doped part of the semiconductor body lies deeper within the semiconductor body than the damaged region and therefore surrounds and is spaced from the latter.

If desired, the region having a damaged lattice structure can be thermally treated during or after the doping step so as to bring about an at least partial recrystallisation and healing of the region.

The invention will now be further described with reference to the drawing, in which:-

Figure 1 is a schematic side-sectional view of part of a semiconductor body to illustrate one stage in the production of a transistor according to the invention;

Figure 2 is a similar view to that of Figure 1 showing the transistor after the production of the emitter;

Figure 3 is a diagram of the doping concentration as a function of the depth from the surface in a semiconductor structure corresponding to that of Figure 1;

Figure 4 is a diagram of the doping concentration as a function of the depth in a semiconductor structure which is modified form of that shown in Figure 1.

Referring to Figure 1, in a monocrystalline semiconductor body 1 the collector zone 2 and a base zone 3 of a planar transistor have been formed. On the surface of the body 1, there is arranged in conventional manner a layer 5 consisting of oxide or other insulating material, for example, in the case of a body 1 made of silicon, a silicon dioxide layer. This oxide layer 5 is itself covered by a photolacquer layer 6. A window 7 is provided in the two layers 5 and 6 in the conventional manner for the production of the emitter of the transistor.

In accordance with the invention, a region 4 having a damaged lattice structure is now produced in the surface of the semiconductor substrate body 1 within the base zone 3. The lattice damage here is produced by the implantation of particles of suitable energy and mass directly into the monocrystal through the window 7 using a particle beam.

Preferably, ions of the host lattice, i.e. ions of the material of the semiconductor body 1 are used to produce the region 4. If the semiconductor body 1 consists of silicon, the implanted ions are preferably silicon ions. However, the implantation can also be carried out using particles which are different from the material of the semiconductor body, such as protons, oxygen ions or ions of an inert gas.

The region 4 does not necessarily have to directly adjoin the surface of the semiconductor body 1 as shown in Figure 1. As will be further explained below with reference to the diagram of Figure 4, the region 4 can also be located at a specific distance beneath the surface of the semiconductor body 1, i.e. within the latter. Either of the two possibilities for the situation of the region 4 can be effected by suitable choice of the particle type and energy used in the implantation step. The distance of the region 4 from the surface of the semiconductor body 1 may, for example, be 1 to 2 pm.

The lateral extent of the region 4 is determined by the window 7 in the masking layers 5 and 6.

The lateral extent of the region 4 is determined by the window 7 in the masking layers 5 and 6.

The region 4 can alternatively be produced by implantation through a covering layer, e.g. an oxide or nitride layer, such as SiO_2 or Si_3N_4.

The semiconductor body 1 can, of course, consist of materials other than silicon.

In a practical example, the region 4 is produced adjacent to the surface by silicon implantation using an energy of at most 300 keV and a dosage of between 10^{14} and 10^{17} cm^{-2}. If the thickness of the oxide layer 5 is enough to serve as an implantation mask, the photo-lacquer layer can be removed before the implantation.

After or before the production of the region 4, an emitter zone 20 is produced in the semiconductor body 1 by a doping process, as shown in Figure 2.

The doping of the region 4 can be effected by diffusion, by implantation or by a combination of both processes, and the region 4 can be heated to produce an at least partial healing by recrystallisation.

When doping is carried out by diffusion, it is possible to proceed in known manner. It is expedient to divide the diffusion process into two stages, an initial deposition stage (which may be carried out either prior to or after the production of the region 4) and a subsequent drive-in stage, in order to set the emitter-base p-n junction 21 at the desired position. The diffusion process is carried out through the region 4 in such a way that the p-n junction 21 is formed in a region having an undamaged crystal structure. Generally, the p-n junction 21 will be spaced at a distance of from a few 100 to a few 1000 Å from the region 4. The initial deposition stage can be carried out before or after the production of the region 4.

The process can be used both for n-diffusion, using phosphorus, for example, as dopant, or for p-diffusion, e.g. using boron as dopant.

As previously mentioned, the region 4 can extend to the semiconductor surface or can be located within the semiconductor body 1.

These conditions are illustrated in Figures 3 and 4, in which the doping concentration N is in each case plotted as a function of the depth x in the semiconductor body 1. In Figures 1 and 2, the x-direction is that direction which runs vertically downwards in the plane of the drawing, the zero point lying in the semiconductor surface. In Figure 3, that region shown in cross-shading lies at the semiconductor surface and extends to a depth of x_1 into the semiconductor body 1. A dash-dotted vertical line indicates that the p-n junction 21 is to lie at a depth x_2 in the body 1. The horizontal line N_0 indicates the basic doping of the semiconductor body 1 or of a corresponding doping profile.

When the emitter zone 20 is produced by implantation doping, the implantation energy is so selected that the maximum of the implantation doping profile represented by a curve 30 lies within the region 4. In a heating step which follows the implantation (which may be effected either before or after the production of the region 4), the doping atoms diffuse out of the region 4 which has a damaged lattice structure into the monocrystal, so that the final p-n junction 21 lies at a depth x_2, i.e. surrounds at a distance the region 4 which originally possessed a damaged structure but which, however, as a result of the heating may have partially recrystallised and thus been partially healed. The aforementioned distance can, as mentioned above, be from a few 100 to a few 1000 Å.

Figure 4 illustrates the situation in which the region 4 lies below the surface of and within the semiconductor body 1. Its dimensions are governed by the values of the depth x_3 and x_4. The theoretical depth of the final p-n junction 21 has a value x_5. For this situation, the maximum of the implantation curve may lie either in the region 4 (indicated by the solid curve 41) or in the region 4 (indicated by the solid curve 41) or in the region of the crystal between the damaged region 4 and the surface (indicated by the broken curve 40). Here again, the implantation is followed by a heating process, so that the doping atoms diffuse out of the region 4 or through the region 4 further into the monocrystal, so that the p-n junction 21 is formed at a depth x_5. (The same applies to that part which is close to the surface, i.e. the p-n junction between the region 4 and the surface).

When doping is effected with arsenic, the implantation may be effected, for example, at an energy of less than 300 keV, and in a dosage of between 10^{13} and 10^{17} cm^{-2}. The maximum of the implantation profile in this case also can be formed in the manner explained with reference to Figures 3 and 4.

During a succeeding diffusion step carried out, for example, for 30 mins at 1000°C, the implanted arsenic diffuses out to produce the p-n junction 21. Simultaneously, during this heating process, a recrystallisation and thus a partial healing of the structure of the region 4 can occur.

The semiconductor components of the invention are particularly suitable for use in integrated circuits.

WHAT WE CLAIM IS:-

1. A semiconductor component having two zones of different conductivity types in a monocrystalline semiconductor body and separated by a p-n junction, one of said zones being formed in the other of said zones by doping, and containing a region in which the lattice structure of the semiconductor body has been damaged during production of the component, said p-n junction surrounding and being spaced from said region.

2. A semiconductor component as claimed in Claim 1, wherein said region has been at least partially healed by recrystallisation.

3. A semiconductor component as claimed in Claim 1 or Claim 2, wherein said region extends from the surface of the semiconductor body to a given depth in said body.

4. A semiconductor component as claimed in Claim 1 or Claim 2, wherein said region lies at a given depth below the surface of said semiconductor body.

5. A semiconductor component as claimed in Claim 4, wherein the distance of said p-n junction from said region is from a few 100 to a few 1000 Å.

6. A semiconductor component as claimed in any one of the preceding Claims, wherein the doped zone containing said region forms the emitter of a transistor.

7. A semiconductor component substantially as hereinbefore described with reference to Figures 1 to 3, or Figure 4 of the drawings, and as shown in Figure 2 thereof.

8. A process for the production of a semiconductor component as claimed in Claim 1, comprising the steps of locally producing a region having a damaged lattice structure in a monocrystalline semiconductor body or a zone thereof of one conductivity type, doping a part of the semiconductor body which contains said region to produce a zone therein of the other conductivity type, in such a way that the p-n junction thus formed lies deeper inside the semiconductor body than does said region and surrounds and is spaced from said region.

9. A process as claimed in Claim 8, wherein said region is thermally treated to

effect an at least partial healing of the region by recrystallisation during or after the said doping step.

10. A process as claimed in Claim 8 or Claim 9, wherein said region is produced by implantation.

11. A process as claimed in Claim 10, wherein the implantation is effected using ions of the same material as that of the semiconductor body.

12. A process as claimed in Claim 10, wherein the implantation is carried out using particles which are different from the material of the semiconductor body.

13. A process as claimed in Claim 12, wherein said particles are protons, oxygen ions, or ions of an inert gas.

14. A process as claimed in any one of Claim 10 to 13, wherein the implantation is effected through a covering layer on the surface of said body.

15. A process as claimed in Claim 14, wherein said covering layer is of SiO_2 or Si_3N_4.

16. A process as claimed in any one of Claims 10 to 15, wherin the implantation energy is such that said region lies at the surface of said semiconductor body.

17. A process as claimed in any one of Claims 10 to 15, wherein the implantation energy is such that said region lies below the surface of said semiconductor body.

18. A process as claimed in any one of Claims 8 to 17, wherein said doping step is effected by diffusion.

19. A process as claimed in Claim 18, wherein the diffusion step is carried out in a preliminary deposition stage followed by a drive-in stage.

20. A process as claimed in Claim 19, wherein said preliminary deposition stage is carried out prior to the production of said region.

21. A process as claimed in Claim 19, wherein said preliminary deposition stage is carried out after the production of said region.

22. A process as claimed in any one of Claims 8 to 17, wherein said doping step is carried out by implantation followed by a heat treatment.

23. A process as claimed in Claim 22, wherein said doping implantation is carried out prior to the production of said region.

24. A process as claimed in Claim 22, wherein said doping implantation is carried out after the production of said region.

25. A process as claimed in any one of Claims 8 to 24, wherein said doping step is carried out in a first stage in which the doping front is moved to the desired position of the p-n junction outside said region.

26. A process for the production of a semiconductor component substantially as hereinbefore described with reference to Figures 1 and 2, and Figures 3 or 4, of the drawings.

27. An integrated circuit including a semiconductor component as claimed in any one of Claims 1 to 7.

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Printed for Her Majesty's Stationery Office,
by Croydon Printing Company Limited, Croydon, Surrey, 1980.
Published by The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.

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1 SHEET
This drawing is a reproduction of the Original on a reduced scale

Fig.1

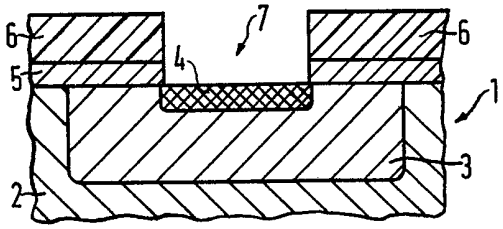

Fig.2

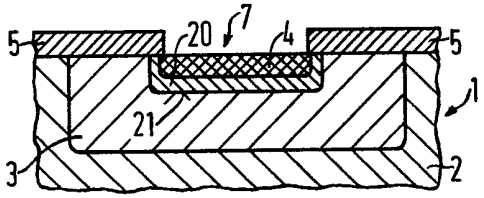

Fig.3

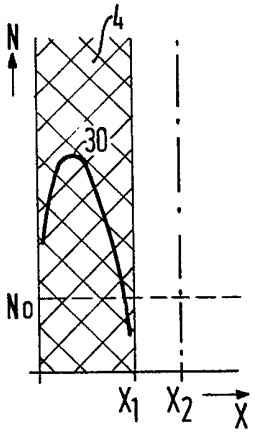

Fig.4

