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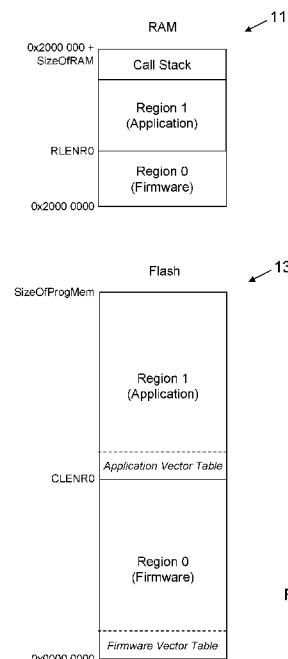
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(57) Abstract: An integrated-circuit radio communication device (1) comprises a processor (7), memory (13), and radio communication logic (17). The memory (13) has a firmware module (23) stored at a firmware memory address, the firmware module (23) comprising instructions for controlling the radio communication logic (17) according to a predetermined radio protocol. The processor (7) is configured to receive supervisor call instructions, each having an associated supervisor call number, and to respond to a supervisor call instruction by (i) invoking a supervisor call handler in the firmware module (23), and (ii) making the supervisor call number available to the call handler. A software application (27) is loaded into the memory (13) of the device (1), and stored at a predetermined application memory address. It is arranged to invoke a radio communication function from the firmware module (23) by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.

Integrated-Circuit Radio

This invention relates to integrated-circuit radio-communication devices and methods of configuring such devices.

5

Integrated-circuit radio-communication devices typically integrate a processor, memory and radio communication logic on a silicon chip. An antenna may be fabricated on the silicon or may be connecting externally. The device will have pins for connecting to a power supply, clock source and any external peripherals such 10 as sensors, timers, digital-to-analog converters and output devices. The processor interfaces with the radio communication logic in order to supervise the sending and/or receiving of radio messages.

Such radio-communication devices, or chips, can be used in a wide range of

15 wireless products, such as wireless mice and keyboards, controllers for game consoles, bicycle speedometers, remote controls, garage-door openers, wireless loudspeakers, etc.

The processor on such a device may run software directly from non-volatile

20 memory in order to control the radio communication logic according to a predetermined radio protocol, such as Bluetooth (RTM) or ZigBee (RTM).

The manufacturing of a complete product, such as a wireless mouse, that

incorporates such a radio-communication chip typically involves the manufacturer of 25 the radio chip supplying it to a product manufacturer, who will integrate the chip into the rest of the product. The chip manufacturer may also provide a development kit, containing tools, such as a cross compiler, loader and debugger, and

documentation that allow the product manufacturer to develop, install and debug

custom application software for the radio device. The custom application software

30 may, for instance, include routines for receiving input from a movement sensor on a wireless mouse and for transmitting suitable radio messages according to a desired protocol.

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A development kit may additionally include source code for a software library and/or operating system, written by the chip manufacturer. The product manufacturer can then compile and link the supplied source code with its own custom software application, to create a single object file for loading to a predetermined address in

5 the memory of each chip.

The library or operating system may contain instructions that implement a particular radio protocol. It could include other functions, such as memory management, processor scheduling, inter-process communication, etc. The application developer

10 can call these supplied functions from its application code, rather than having to write them from scratch. This can make development of the application software simpler and quicker. It can also ease portability between different models of the radio chip.

15 The applicant has come to realise, however, that such traditional approaches can be improved upon.

From one aspect, the invention provides a method of configuring an integrated-circuit radio communication device, wherein:

20 the device comprises a processor, memory, and radio communication logic; the memory has a firmware module stored at a firmware memory address, the firmware module comprising instructions for controlling the radio communication logic according to a predetermined radio protocol; and the processor is configured to receive supervisor call instructions, each

25 having an associated supervisor call number, and to respond to a supervisor call instruction by (i) invoking a supervisor call handler in the firmware module, and (ii) making the supervisor call number available to the call handler, the method comprising loading a software application into the memory of the device, such that the application is stored at a predetermined application memory

30 address, wherein the software application is arranged to invoke a radio communication function from the firmware module by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.

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Thus it will be seen by those skilled in the art that, in accordance with the invention, a software application can be loaded onto a radio-communication chip so as to interface via supervisor call instructions with a firmware module that provides radio control functions.

5

This removes the need for the software application developer to link the application code with a library or operating system supplied by the chip manufacturer, thereby resulting in a simpler and more efficient development process. By avoiding the need for link-time dependencies, the chances of bugs arising during development of 10 the software application can be reduced. Because there is no need to keep re-linking the firmware module that provides radio control functions at successive development stages, the location of member objects in memory can remain unchanged during the development process. This continuity in memory location can avoid bugs occurring and can also aid debugging if errors do arise.

15

In preferred embodiments, the firmware module, stored at the firmware memory address, is a linked binary. Thus no linking between the firmware module and the software application is required, or is even possible. It is envisaged that the firmware module will usually be a compiled binary module (e.g. compiled from the C 20 programming language), although it is possible that it could be assembled directly from machine code.

In order to develop the software application, the only non-standard information (i.e. not determined by the processor or device architecture) that the application 25 developer need know is: the predetermined software-application memory address; information relating to the amount of any data memory (e.g. in RAM) available for the software application to use, and the predetermined correspondence between supervisor call numbers and radio communication functions in the firmware module. This information can be sufficient to write, compile and load a software application 30 for the device. It is envisaged that the application developer could conveniently be provided with a header file (e.g. in the C programming language) which would contain this information. (Such a header file may, of course, optionally contain other, additional features to provide further assistance to the application developer.)

Another advantage of configuring a device according to methods of the invention is that the device manufacturer need not reveal confidential source code in its firmware module to the application developer.

5 The integrated-circuit device may be provided to a developer of the software application with the firmware module already pre-loaded on the device. This can further increase the security of any confidential information contained in the firmware module. However, this is not essential. The application developer may instead receive the firmware module as a binary image of pre-compiled instructions
10 and load the firmware module onto the device.

Thus, from a further aspect, the invention provides a method of configuring an integrated-circuit radio communication device, wherein the device comprises a processor, memory, and radio communication logic, the method comprising:

15 loading a software application into the memory of the device, such that the application is stored at a predetermined application memory address; and
loading a firmware module into the memory of the device, such that the firmware module is stored at a predetermined firmware memory address, the firmware module comprising instructions for controlling the radio communication
20 logic according to a predetermined radio protocol,
wherein:
the processor is configured to receive supervisor call instructions, each having an associated supervisor call number, and to respond to a supervisor call instruction by (i) invoking a supervisor call handler in the firmware module, and (ii)
25 making the supervisor call number available to the call handler; and
the software application is arranged to invoke a radio communication function from the firmware module by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.

30 The firmware module and the software application may be loaded onto the device in any order or substantially simultaneously. It will be appreciated that loading the two simultaneously is still fundamentally different from loading a single, linked software application and library as the skilled person might have done in the past. As before,

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the firmware module is preferably a compiled and linked binary module (but without being linked to the software application).

The invention also extends to an integrated-circuit radio communication device
5 itself.

Thus, from a third aspect, the invention provides an integrated-circuit radio communication device, wherein:

the device comprises a processor, memory, and radio communication logic;
10 the memory has a firmware module stored at a firmware memory address, the firmware module comprising instructions for controlling the radio communication logic according to a predetermined radio protocol; and
the processor is configured to receive supervisor call instructions, each having an associated supervisor call number, and to respond to a supervisor call
15 instruction by (i) invoking a supervisor call handler in the firmware module, and (ii) making the supervisor call number available to the call handler;
the memory has a software application stored at a predetermined application memory address, the software application being arranged to invoke a radio communication function from the firmware module by issuing a supervisor call
20 instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.

From further aspects, the invention provides a firmware module, and a transitory or non-transitory medium storing the same, for loading on an integrated-circuit radio

25 communication device comprising a processor, memory, and radio communication logic, at a firmware memory address, the firmware module comprising:

instructions for controlling the radio communication logic according to a predetermined radio protocol; and
a supervisor call handler arranged to respond to a supervisor call instruction
30 being issued by a software application by performing a radio communication function corresponding to a supervisor call number associated with the supervisor call instruction.

The firmware module is preferably a linked binary module.

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From still further aspects, the invention provides a software application, and a transitory or non-transitory medium storing the same, for loading on an integrated-circuit radio communication device comprising a processor, memory, and radio communication logic, at a predetermined software application memory address, the 5 software application being arranged to invoke a radio communication function by issuing a supervisor call instruction having an associated, predetermined supervisor call number corresponding to the function to be invoked.

In preferred embodiments of any of the above aspects, the firmware module is 10 arranged so that all the radio communication functions provided by the firmware module are invoked by supervisor call instructions having respective supervisor call numbers according to a predetermined correspondence between numbers and functions. In this way, no other mechanism for invoking firmware functions need be supported by the device, thereby avoiding substantial static or run-time link 15 dependencies, and simplifying the device and development of the software application.

It will be appreciated that the firmware module may provide other functions, not necessarily related to radio communication, which the software application can 20 invoke; for example, an encryption algorithm. Preferably the device is configured so that the invoking of all such functions is carried out by the issuing of supervisor call instructions.

Because embodiments of the device need not contain a traditional, full operating 25 system, the application developer can be free to develop the software application as a native application for the processor architecture, without having to learn how to interface with a proprietary operating system supplied by the chip manufacturer. Especially when the processor is well-known in the art, this is a particularly attractive feature for the application developer.

30 If the device has a hardware abstraction layer in addition to the firmware module, the software application may interface directly with this layer. Application-specific drivers may also be loaded onto the device.

Configuring the device may comprise using the correspondence between supervisor call numbers and radio communication functions when compiling the software application. Compiling or loading the software application may make use of the predetermined software-application memory address. In some embodiments,

5 configuring the device may comprise receiving the correspondence between supervisor call numbers and radio communication functions and/or receiving the predetermined software-application memory address, e.g. as a header file. Such information may then be used when compiling the software application.

10 The device is preferably configured so that no run-time linking is required when executing the software application on the device.

The processor may implement the supervisor call instructions in any appropriate way. In one set of preferred embodiments, the processor is an ARM Ltd. (RTM) processor, such as a processor from the Cortex-M family, and the supervisor call instructions are then SVC instructions, supported by the processor.

15 The software application may issue a supervisor call instruction by executing a dedicated SVC processor instruction. Such an instruction may be generated by a compiler when compiling the software application, e.g. by the developer including a specific pre-processor directive in the source code for the software application.

20 The number associated with the supervisor call may be made available to the call handler via a register or via the call stack or via any other appropriate mechanism.

25 Preferably, the processor and/or software application are configured to make the values of one or more arguments available to the supervisor call handler. In this way, the software application can pass arguments to a radio communication function, such as data to be transmitted. The call handler may be able to pass a return value from the radio communication function to the software application.

30 The processor is preferably configured to handle a supervisor call instruction from the software application as an exception (software interrupt). In this way, the software application can interrupt less time-critical processing when a time-critical radio communication function needs to be invoked.

The processor preferably supports a plurality of interrupt priorities. In some embodiments, some event-driven functions in the firmware module are assigned a relatively high priority, while others are assigned a relatively low priority. Preferably, 5 functions associated with time-critical radio communication operations are assigned the relatively high priority.

The software application may be arranged to handle interrupts (forwarded by the firmware module, as explained below) and may have a relatively high priority for 10 some event-driven functions and a relatively low priority for others. The software application priorities are preferably interleaved with those of the firmware module. The highest firmware priority level is preferably higher than the highest software-application priority level, so that critical radio communication operations, implemented in the firmware module, can always take precedence over the 15 software application. This can provide protection against careless programming in the software application.

The firmware module is preferably configured to invoke a function in the software application in response to the firmware module receiving an interrupt. Such an 20 interrupt may arise, for example, from a peripheral, such as a movement sensor.

The firmware module and the software application may each have a respective interrupt vector table. The two tables preferably use the same interrupt-vector-address offsets as each other. The offsets of interrupt vector addresses in the 25 firmware module's vector table (and hence the software application's vector table, when the two use the same offsets) are typically fixed by the processor architecture. The device is preferably configured to use the firmware module's vector table when processing an interrupt (i.e. as the system interrupt vector table).

30 However, the firmware module is preferably configured so that all interrupts that the firmware module is not programmed to handle itself are passed on to the software application. This may be implemented by the firmware module causing execution to branch to the address contained in the corresponding offset in the software application's vector table whenever it is not configured to handle a particular 35 interrupt. This is possible because the software application is loaded to a

predetermined memory address, so that the firmware module can know, in advance, where to find the software application's vector table once the application has been loaded onto the device.

5 For example, in some embodiments the RESET interrupt handler address is always placed at offset = 0 by the compiler. Therefore, the RESET handler address in the firmware module's vector table will be at address 0x0000 0000 + 0 = 0x0000 0000 in the memory. The RESET handler address in the software application's vector table is at address CLENR0 + 0 = CLENR0, where CLENR0 is the predetermined
10 base memory address at which the software application is located.

This interrupt forwarding mechanism conveniently allows the software application to be programmed to handle hardware interrupts in substantially the same way as if no firmware module were present on the device. I.e. the firmware module can be
15 invisible to the software application for the purposes of receiving interrupts. The forwarding is preferably implemented in such a way that it adds latency of fewer than about 30 instructions or less than about 3 microseconds, compared with a direct hardware interrupt to a software application.

20 The firmware module may be arranged to be substantially disabled. Such disabling may be carried out via a call to the firmware module (preferably using the SVC mechanism). Disabling the firmware module may cause the firmware module to reset the protocol stack and to disable any memory protection (if present) in order to give resources back to the software application. When disabled, the firmware
25 module preferably forwards all interrupts to the software application (even those which it might otherwise have handled itself).

The processor preferably supports seamless transitions from one interrupt priority level to another. This is sometimes referred to as tail-chaining. This provides an
30 elegant means of transferring control between the software application and the firmware module (and vice versa) so as to allow time-critical radio communication functions to take precedence when necessary.

35 The device preferably comprises memory protection logic arranged to intercept memory access instructions. This logic may be located between the processor and

- 10 -

the memory. It may use the location of a memory-access instruction (i.e. where the processor has read the instruction from) to determine whether to allow access. The memory protection logic is preferably configured to prevent the software application from reading or overwriting the firmware module (or both).

5

Such memory protection can provide benefits in protecting sensitive information in the firmware module from being read by the developer of the software application. It can also minimise potential damage from programming errors in the software application, as well as aiding the detection and correction of bugs in the software application.

10

The memory protection logic may be configured to protect RAM associated with the firmware module from being read or written to by the software application (or both).

15 The processor, memory, and radio communication logic are preferably integrated on a single silicon chip. However, they may alternatively be integrated in a multi-chip module.

20 The memory is preferably a non-volatile memory such as EEPROM or flash. It preferably supports random-access reading, so that the firmware module and software application can be executed directly from the memory.

25 The skilled person will appreciate that the device will typically also comprise volatile memory. It may additionally comprise one or more peripherals. It may have connections for receiving power and a clock signal. It may have a connection for an antenna. It may have one or more input and/or output interfaces such as a serial connection.

30 Optional or preferred features of one aspect or embodiment described herein may, wherever appropriate, be applied to any other aspect or embodiment.

Certain preferred embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

35 Figure 1 is a schematic drawing of a microcontroller embodying the invention;

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Figure 2 is a schematic drawing showing major software components within the microcontroller architecture;

Figure 3 is a schematic memory map for the microcontroller;

Figure 4 is a figurative diagram of different processor interrupt priority levels;

5 Figures 5a - 5c are figurative diagrams illustrating various interrupt scenarios;

Figure 6 is a figurative diagram of source code elements illustrating the software application calling a function in the firmware module;

10 Figure 7 is a figurative diagram of source code elements illustrating the software application using a system call to invoke an internal function; and

Figure 8 is a figurative diagram of source code elements illustrating the software application receiving a hardware interrupt.

15 Figure 1 shows an integrated-circuit microcontroller 1, sometimes known as a system-on-chip, which comprises clock logic 3, which may include a resistor-capacitor oscillator and/or may receive an input from an off-chip crystal oscillator (not shown), power management circuitry 5, a processor 7 (e.g. an ARM (RTM) Cortex-M0), memory protection logic 9, RAM 11, non-volatile flash memory 13, one or more peripherals 15, radio communication logic 17 and input/output circuitry 19.

20

These components are interconnected in a conventional manner, e.g. using lines and buses (not shown). The memory protection logic 9 is situated so as to intercept instructions from the processor 7 to the RAM 11 and flash memory 13. When installed in a product, the microcontroller 1 may be connected to a number of 25 external components such as a power supply, radio antenna, crystal oscillator, sensors, output devices, etc.

30 Figure 2 shows the microcontroller 1, above which sits an optional hardware abstraction layer 21, such as the ARM (RTM) Cortex Microcontroller Software Interface Standard. The architecture also includes a firmware module 23, drivers 25 and software application 27. The drivers 25 may be specific to the software application 27.

35 The firmware module 23 is a binary application comprising a number of embedded software blocks. A radio protocol block 31 implements one or more wireless

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protocol stacks. A radio event manager 33 provides access scheduling for the radio communication logic 17 and event multiplexing. A library 35 provides shared hardware resource management and functions such as random number generation, configuring interrupts and priority, power management (e.g. for enabling and 5 disabling peripherals), encryption functions, etc. A firmware manager 37 supports enabling and disabling the firmware module, and enabling and disabling the wireless protocol stack.

10 The firmware module 23 owns the system vector table and is the entry point for the program on all resets.

An application programming interface (API) 29 for the firmware module 23 allows the software application 27 to invoke functions in the firmware module 23. It is implemented entirely using system calls. When using an ARM (RTM) processor, 15 each API function prototype is mapped to a firmware function via an associated supervisor call (SVC) number at compile time. This mapping can be provided to the developer of the software application 27 to allow the functions to be called correctly.

20 The firmware module 23 can communicate events to the software application 27 as software interrupts, the content of which is buffered until read (polled) by the software application 27. The reading is done through an API call (e.g. event_get()).

25 The software application 27 can access the microcontroller (1) hardware directly or via a hardware abstraction layer 21, e.g. by means of application-specific drivers 25, in addition to being able to use the firmware module 23 to use the hardware indirectly.

30 Figure 3 shows how the RAM 11 and flash 13 are shared between the firmware module 23 and the software application 27 (including any application-specific drivers 25). When using an ARM (RTM) Cortex-M0 processor 7, the flash 13 is assigned addresses from zero (0x0000 0000) upwards, to its capacity, SizeOfProgMem and the RAM 11 is assigned addresses from 0x2000 0000 upwards to (0x2000 0000 + SizeOfRAM). Different address values may be used if a different type of processor is used.

The flash 13 comprises two distinct regions either side of address CLENR0 (code length region 0). Region 0, between zero and CLENR0, is where the firmware module 23 is loaded. Its interrupt vector table is stored at address zero. Region 1, extending upwards from CLENR0, is where the software application 27 is loaded. It

5 too has an interrupt vector table, at address CLENR0, the purpose of which is explained below. It will be appreciated that the device 1 may have other non-volatile memory (not shown) which may be used for other purposes, such as storing configuration information or flags.

10 The RAM 11 similarly has a Region 0, from the base address 0x2000 000 to RLENR0, and a Region 1, extended upwards from RLENR0. RAM Region 0 provides data storage for the firmware module 23 while RAM Region 1 provides data storage for the software application 27. A call stack is shared between the firmware module 23 and the software application 27 and grows downwards, e.g.

15 from 0x2000 0000 + SizeOfRAM. The memory allocated to the call stack must be big enough for the needs of both the software application 27 and the firmware module 23.

20 The firmware module 23 call-stack usage requirement may be published for the device 1 by the chip manufacturer. The developer of the software application 27 must then define an initial stack pointer and reserve sufficient stack memory for both the firmware module 23 and his software application 27. The firmware module 23 will initialize the main stack pointer on reset.

25 The memory protection logic 9 is arranged to intercept all memory access requests (e.g. read requests) from the processor 7 to the flash 13 and the RAM 11. It determines the source of the access request instruction (e.g. whether the request is from the firmware module 23 or from the software application 27). It also accesses memory protection configuration data (e.g. stored in one or more dedicated

30 registers) which specifies respective access permissions for the various sources, and allows or denies the access request accordingly.

35 In some preferred embodiments of the invention, the software application 27 is denied read and/or write access to flash Region 0 and to RAM Region 0. This protects confidentiality for the firmware module 23 and can prevent inadvertent or

malicious writing by the software application 27 to memory locations allocated to the firmware module 23, thereby increasing robustness and security. The software application flash Region 1 may also be protected from read access, e.g. to protect against read back via an external debugging interface.

5

This means that the initial stack pointer cannot be in RAM Region 0 as the software application 27 does not have write access to this region. In other embodiments of the invention, the call stack may be in two parts, where the firmware module 23 call stack is located in RAM Region 0 and the software application 27 call stack is located in RAM Region 1.

10 Figure 4 shows the different interrupt levels 41 provided by an ARM (RTM) Cortex-M0 processor, with increasing priority in the direction of the arrow, and how these levels are mapped to the interrupt levels 43 used by the firmware module 23 and 15 software application 27.

Above the Main background context are four interrupt priorities which are used as follows, in increasing order of priority: software application low priority, firmware module low priority, software application high priority and firmware module high 20 priority. The high-priority software application interrupt is used for critical interrupts where low latency is required.

Figures 5a - 5c show various examples of possible changes in priority level.

25 Figure 5a illustrates a background main process being interrupted by the software application at low priority, e.g. by a serial driver. The software application 27 then makes an API call to the firmware module 23 (by triggering an supervisor call (SVC) exception). The firmware module 23 handles the call at the low-priority firmware level before returning to the application low-priority level. Finally, the software 30 application 27 completes its operation and execution returns to the main background level.

Figure 5b illustrates an API call to the firmware module 23 being made from the main context (by triggering an SVC exception). The execution of the API function in 35 firmware low-priority is interrupted by a high-priority software application exception.

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This may be to service a sensor input, for example. Once the software application finishes its high-priority execution, the firmware API call can continue at the lower priority level, before finally returning to the background main process.

5 Figure 5c illustrates a high-priority interrupt of a background main process by the firmware module 23. This could be due to a time-critical radio communication interrupt, such as an incoming radio packet, to which the radio event manager 33 must respond. The interrupt service routine in the firmware module 23 sets a low-priority firmware exception flag to signal to the higher levels of the radio protocol
10 stack. On completion of the high-priority routine, the low-priority routine is executing immediately due to the tail-chaining capabilities of the processor 7 (i.e. without having to revert to the background main level in between). The low-priority firmware routine in turn sets an exception flag to signal the software application 27 that a radio data packet has been received. This exception is chained after
15 completion of the low-priority firmware module routine. In this example, the software application 27 then makes an API call to the firmware module 23 via an SVC which completes and returns context from the SVC to the software application 27. Finally, the software application low-priority operation completes and execution returns to the main level.

20

Figures 6 - 8 illustrate by example how control can pass between the software application 27 and the firmware module 23. Uncompiled C language code extracts are used for illustration. Of course, in reality, binary instructions from the flash memory 13 are executed by the processor 7. The numbered arrows indicate
25 successive execution steps.

Figure 6 shows the software application 27 calling a function through the API 29 of the firmware module 23. The application 27 calls a function with a prototype imported from the firmware API 29 using a firmware header file supplied to the
30 software-application developer by the chip manufacturer. The __SVC(x) pragma causes the compiler to insert an instruction in the object code which causes a supervisor call (SVC) exception when the function is called by the software application 23.

The processor 7 invokes the SVC handler via the firmware module's interrupt vector table (which acts as the system interrupt vector table). The SVC number associated with the function called by the software application 27 is passed to the SVC handler, along with any arguments. Such arguments may be passed via

5 registers or via the call stack, depending on the processor. The SVC handler uses the SVC number to call the correct firmware module function. This could be a radio control function (e.g. an instruction to transmit data by radio), or a firmware management function (e.g. to disable the firmware module), or a library function (e.g. to generate a random number). The function executes and then returns to the

10 software application 27. A return value may be available in a register or on the call stack.

Figure 7 shows the software application 27 invoking one of its own functions via a system call. It might do this in order to change from a low priority to a high priority

15 execution level. Similarly to the situation in Figure 6, the software application 27 triggering a SVC so as to cause execution to pass to an SVC handler in the firmware module 27. However, in this case, the instruction uses an SVC number in a range that is reserved for the software application's own use. The firmware module 23 thus causes execution to branch to a handler function

20 (app_systemcall_function()) in the software application 27, potentially at a different priority level to that of the preceding operation.

Figure 8 shows how a hardware interrupt can be received by the software application 27. The firmware module 23 is arranged to forward interrupts to the

25 software application 27 by default, unless they are interrupts that the firmware module 23 is configured to handle. Additionally, if the firmware module 23 has been disabled by the software application 27 (e.g. via a suitable API call to the firmware manager 37), then the firmware module will forward all interrupts to the software application 27.

30 On receiving an interrupt, e.g. from a motion sensor, an interrupt handler in the firmware module 23 is vectored to. This checks whether the firmware module 23 is enabled and whether it is an interrupt that the firmware module 23 is set up to deal with. If so, the firmware module 23 handles the interrupt. If not, it branches

35 execution to an interrupt handler routine in the software application 27. The

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firmware module 23 can know where to find this routine because the location of the software application vector table (at CLENR0) is predetermined, and the offsets into this vector table are the same as the offsets into the firmware module's vector table.

- 5 In this way, a firmware module implementing radio control logic, programmed to a firmware memory address on an integrated radio communication chip, can be configured and used both securely and conveniently.

Claims

1. A method of configuring an integrated-circuit radio communication device, wherein:
 - the device comprises a processor, memory, and radio communication logic;
 - 5 the memory has a firmware module stored at a firmware memory address, the firmware module comprising instructions for controlling the radio communication logic according to a predetermined radio protocol; and
 - the processor is configured to receive supervisor call instructions, each having an associated supervisor call number, and to respond to a supervisor call
 - 10 instruction by (i) invoking a supervisor call handler in the firmware module, and (ii) making the supervisor call number available to the call handler,
 - the method comprising loading a software application into the memory of the device, such that the application is stored at a predetermined application memory address, wherein the software application is arranged to invoke a radio
 - 15 communication function from the firmware module by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.
2. A method of configuring an integrated-circuit radio communication device, 20 wherein the device comprises a processor, memory, and radio communication logic, the method comprising:
 - loading a software application into the memory of the device, such that the application is stored at a predetermined application memory address; and
 - loading a firmware module into the memory of the device, such that the
 - 25 firmware module is stored at a predetermined firmware memory address, the firmware module comprising instructions for controlling the radio communication logic according to a predetermined radio protocol,
 - wherein:
 - the processor is configured to receive supervisor call instructions, each
 - 30 having an associated supervisor call number, and to respond to a supervisor call instruction by (i) invoking a supervisor call handler in the firmware module, and (ii) making the supervisor call number available to the call handler; and

the software application is arranged to invoke a radio communication function from the firmware module by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.

5

3. A method as claimed in claim 1 or 2, wherein the firmware module is a linked binary module.

4. A method as claimed in any preceding claim, wherein the firmware module 10 is arranged so that all radio communication functions provided by the firmware module are invoked by supervisor call instructions having respective supervisor call numbers, according to a predetermined correspondence between numbers and functions.

15 5. A method as claimed in any preceding claim, further comprising compiling the software application and using the correspondence between supervisor call numbers and radio communication functions in said compiling.

20 6. A method as claimed in any preceding claim, further comprising using the predetermined software-application memory address when compiling and/or loading the software application.

25 7. A method as claimed in any preceding claim, wherein the software application is arranged to issue a supervisor call instruction by executing a dedicated SVC processor instruction.

8. A method as claimed in any preceding claim, wherein the firmware module and the software application each has a respective interrupt vector table, wherein the device is configured to use the vector table of the firmware module when 30 processing an interrupt, and wherein the firmware module is configured so that all interrupts that the firmware module is not programmed to handle itself are passed on to the software application.

- 20 -

9. A method as claimed in claim 8, wherein the interrupt vector tables of the firmware module and the software application use the same interrupt-vector-address offsets as each other.
- 5 10. A method as claimed in any preceding claim, wherein the device comprises memory protection logic arranged to intercept memory access instructions and being configured to prevent the software application from reading or overwriting the firmware module.
- 10 11. An integrated-circuit radio communication device, wherein:
 - the device comprises a processor, memory, and radio communication logic;
 - the memory has a firmware module stored at a firmware memory address, the firmware module comprising instructions for controlling the radio communication logic according to a predetermined radio protocol; and
 - 15 the processor is configured to receive supervisor call instructions, each having an associated supervisor call number, and to respond to a supervisor call instruction by (i) invoking a supervisor call handler in the firmware module, and (ii) making the supervisor call number available to the call handler;
 - the memory has a software application stored at a predetermined application memory address, the software application being arranged to invoke a radio communication function from the firmware module by issuing a supervisor call instruction having an associated predetermined supervisor call number corresponding to the function to be invoked.
 - 20
- 25 12. A device as claimed in claim 11, wherein the firmware module is arranged so that all radio communication functions provided by the firmware module are invoked by supervisor call instructions having respective supervisor call numbers, according to a predetermined correspondence between numbers and functions.
- 30 13. A device as claimed in claim 11 or 12, wherein the firmware module is arranged so that all functions provided by the firmware module are invoked by the issuing of supervisor call instructions.
- 35 14. A device as claimed in any of claims 11 to 13, configured so that no run-time linking is required when executing the software application on the device.

15. A device as claimed in any of claims 11 to 14, wherein the software application is arranged to issue a supervisor call instruction by executing a dedicated SVC processor instruction.

5

16. A device as claimed in any of claims 11 to 15, wherein the processor and/or software application are configured to make the values of one or more arguments available to the supervisor call handler.

10 17. A device as claimed in any of claims 11 to 16, wherein the processor is configured to handle a supervisor call instruction from the software application as an exception, wherein the processor supports a plurality of interrupt priorities, and wherein some functions in the firmware module are assigned a relatively high priority, with other functions in the firmware module having a relatively low priority.

15

18. A device as claimed in claim 17, wherein the software application is arranged to handle interrupts, assigning a relatively high priority to some event-driven functions, and a relatively low priority to other event-driven functions.

20 19. A device as claimed in claim 18, wherein the high and low software application priorities are interleaved with the high and low firmware module priorities.

25 20. A device as claimed in claim 18 or 19, wherein the highest firmware priority level is higher than the highest software-application priority level.

21. A device as claimed in any of claims 11 to 20, wherein the firmware module is configured to invoke a function in the software application in response to the firmware module receiving an interrupt.

30

22. A device as claimed in any of claims 11 to 21, wherein the firmware module and the software application each has a respective interrupt vector table, wherein the device is configured to use the vector table of the firmware module when processing an interrupt, and wherein the firmware module is configured so that all

interrupts that the firmware module is not programmed to handle itself are passed on to the software application.

23. A device as claimed in claim 22, wherein the interrupt vector tables of the
5 firmware module and the software application use the same offsets as each other.

24. A device as claimed in any of claims 11 to 23, wherein the firmware module
can be substantially disabled via a call to the firmware module, so as to cause the
firmware module to reset the protocol stack and to disable any memory protection
10 in order to give resources back to the software application, and wherein, when
disabled, the firmware module will forward all interrupts to the software application.

25. A device as claimed in any of claims 11 to 24, wherein the processor
supports seamless transitions from one interrupt priority level to another.
15

26. A device as claimed in any of claims 11 to 25, comprising memory
protection logic arranged to intercept memory access instructions and being
configured to prevent the software application from reading or overwriting the
firmware module and/or from reading or writing to RAM associated with the
20 firmware module.

27. A firmware module for loading on an integrated-circuit radio communication
device comprising a processor, memory, and radio communication logic, at a
firmware memory address, the firmware module comprising:
25 instructions for controlling the radio communication logic according to a
predetermined radio protocol; and
a supervisor call handler arranged to respond to a supervisor call instruction
being issued by a software application by performing a radio communication
function corresponding to a supervisor call number associated with the supervisor
30 call instruction.

28. A firmware module as claimed in claim 27, being a linked binary module.

29. A software application for loading on an integrated-circuit radio
35 communication device comprising a processor, memory, and radio communication

- 23 -

logic, at a predetermined software application memory address, the software application being arranged to invoke a radio communication function by issuing a supervisor call instruction having an associated, predetermined supervisor call number corresponding to the function to be invoked.

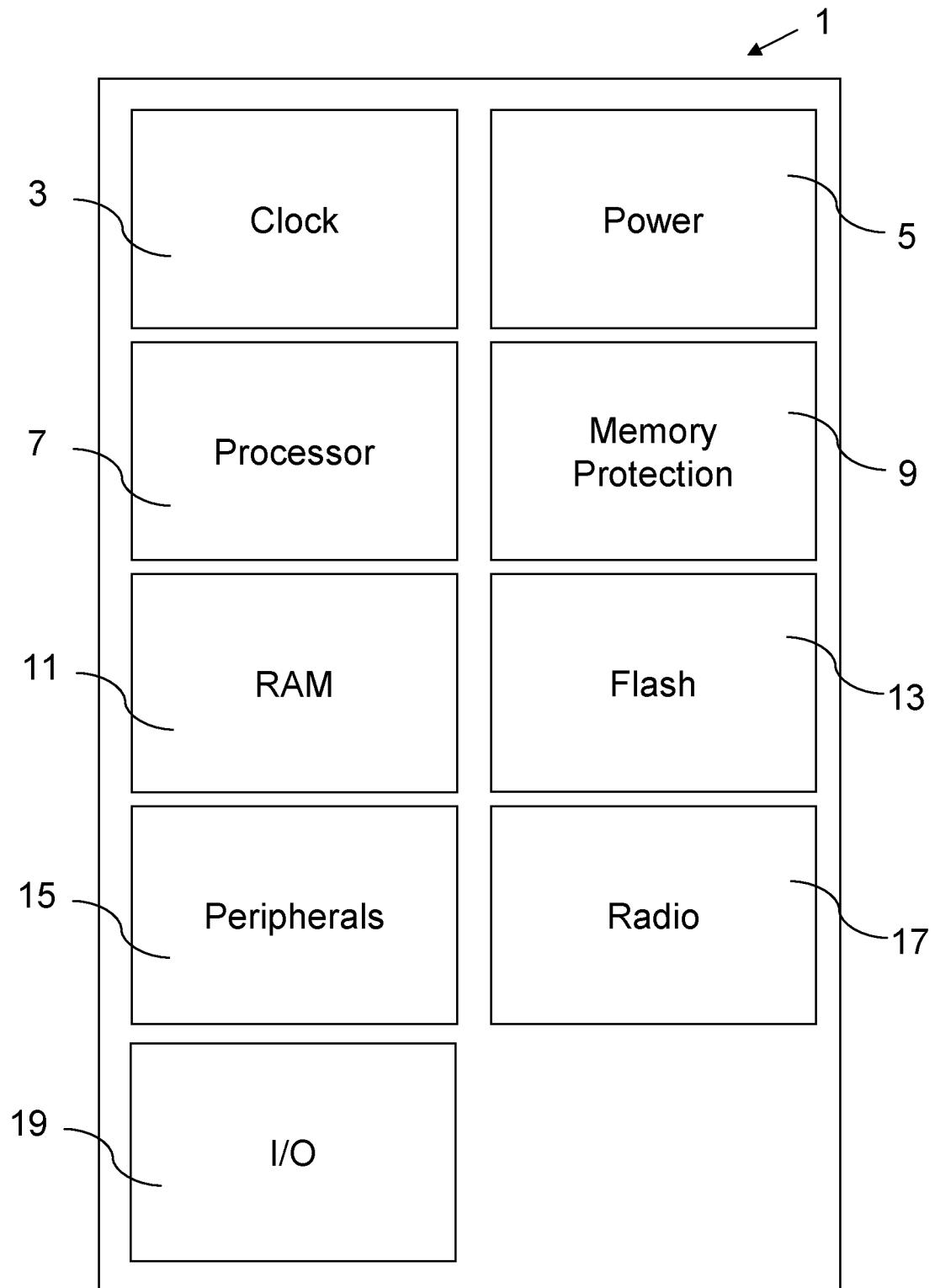


Figure 1

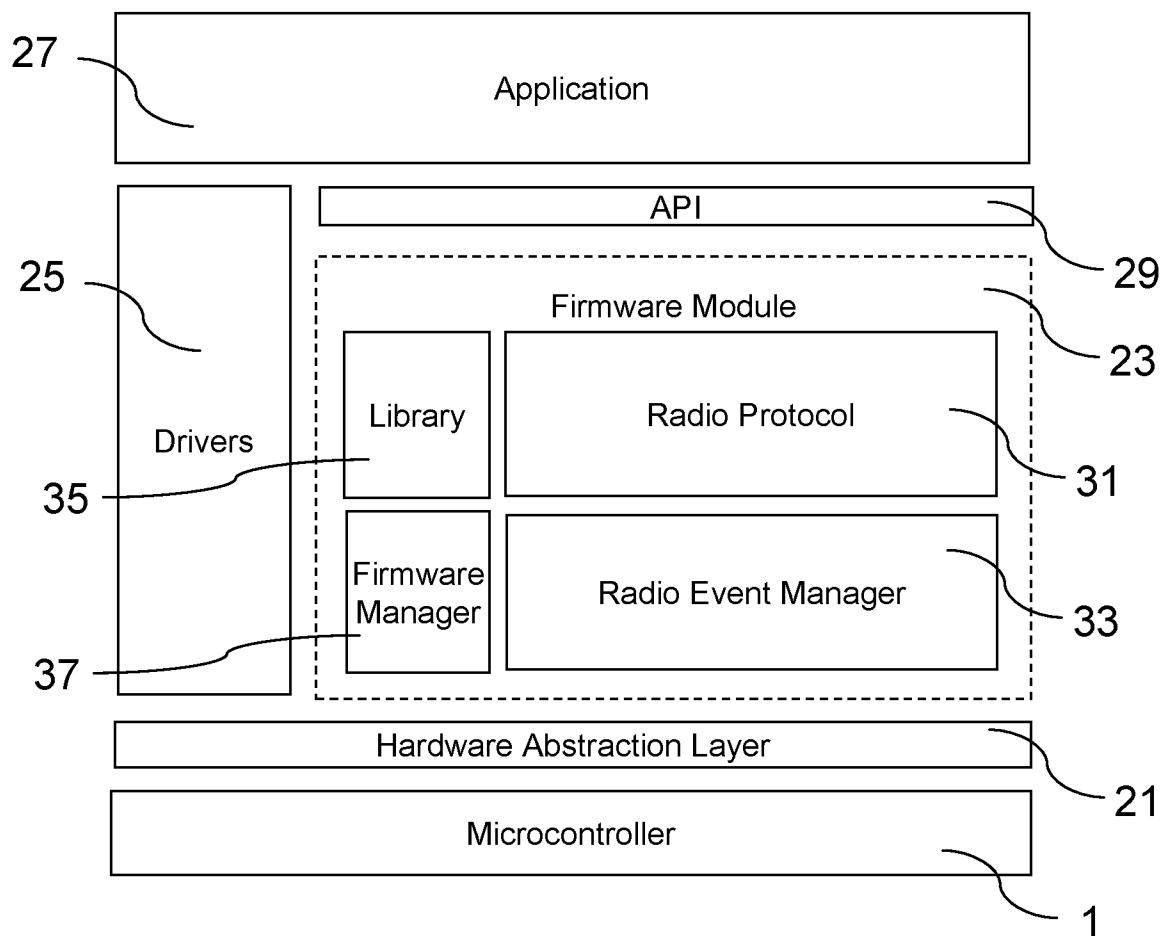


Figure 2

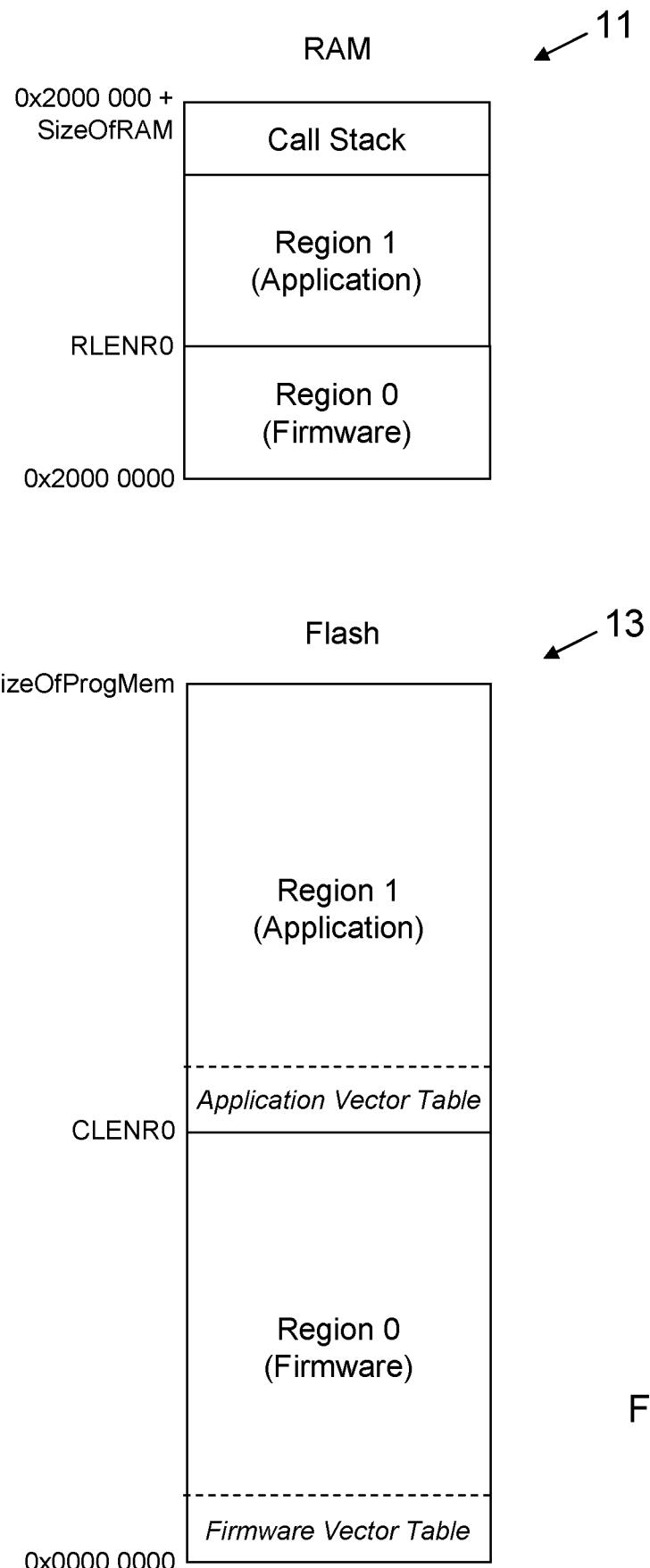


Figure 3

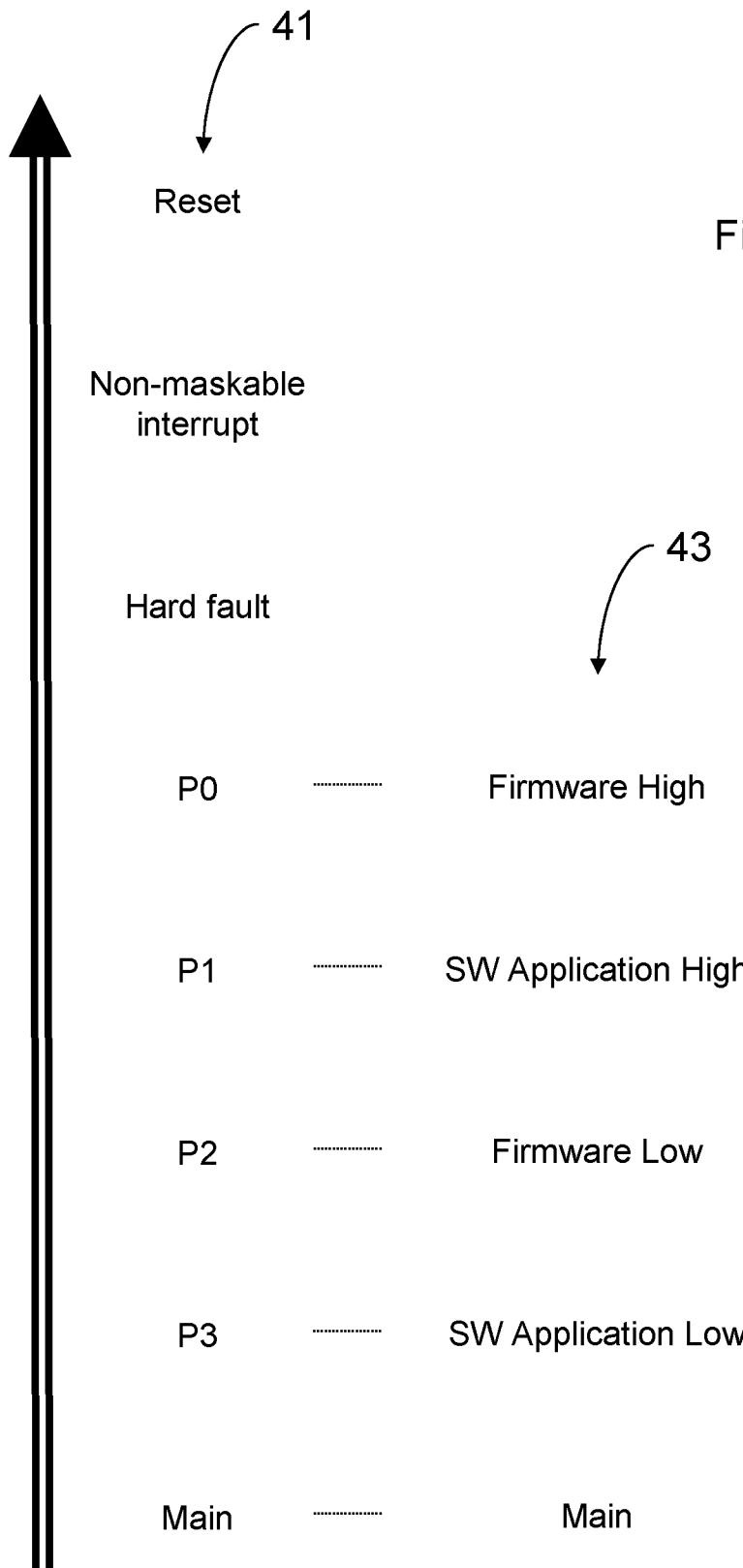


Figure 4

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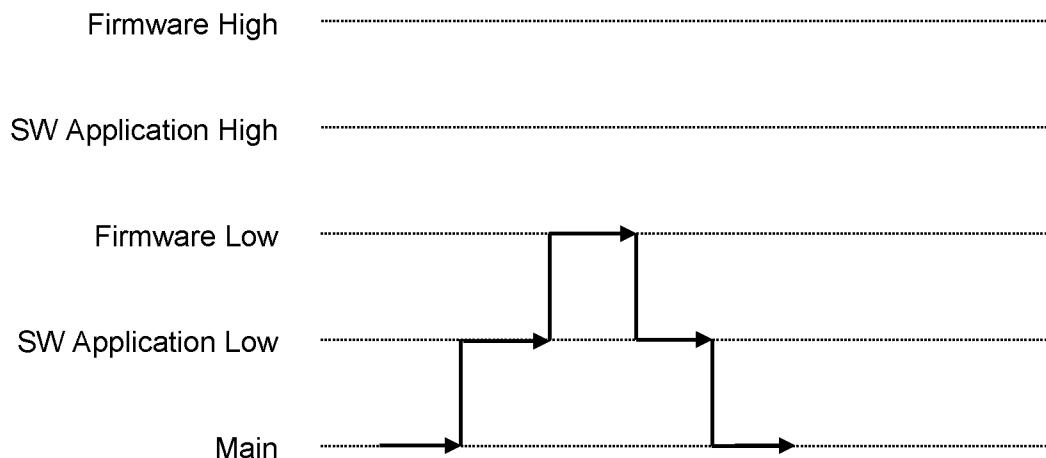


Figure 5a

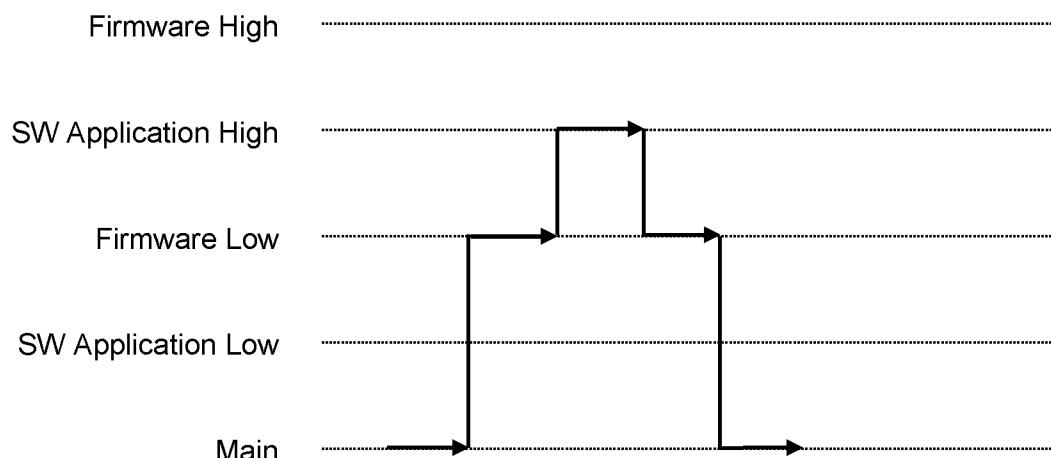


Figure 5b

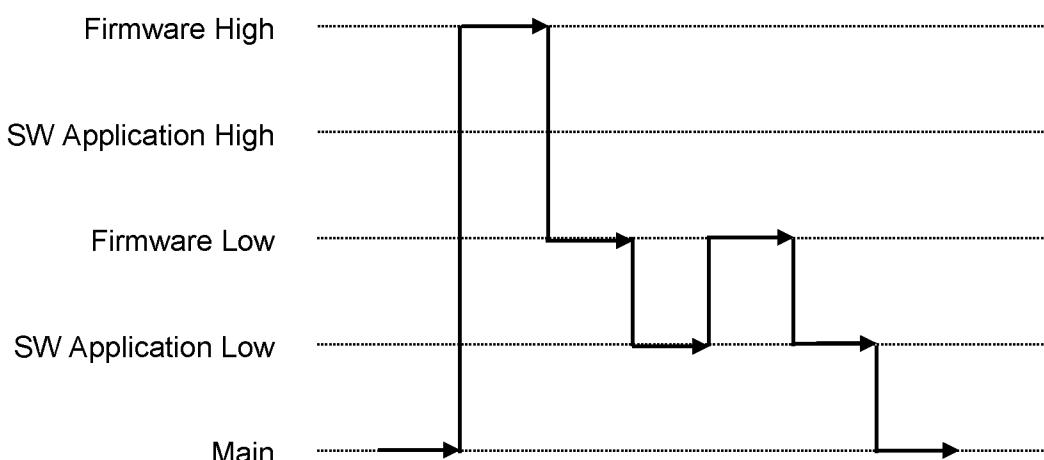


Figure 5c

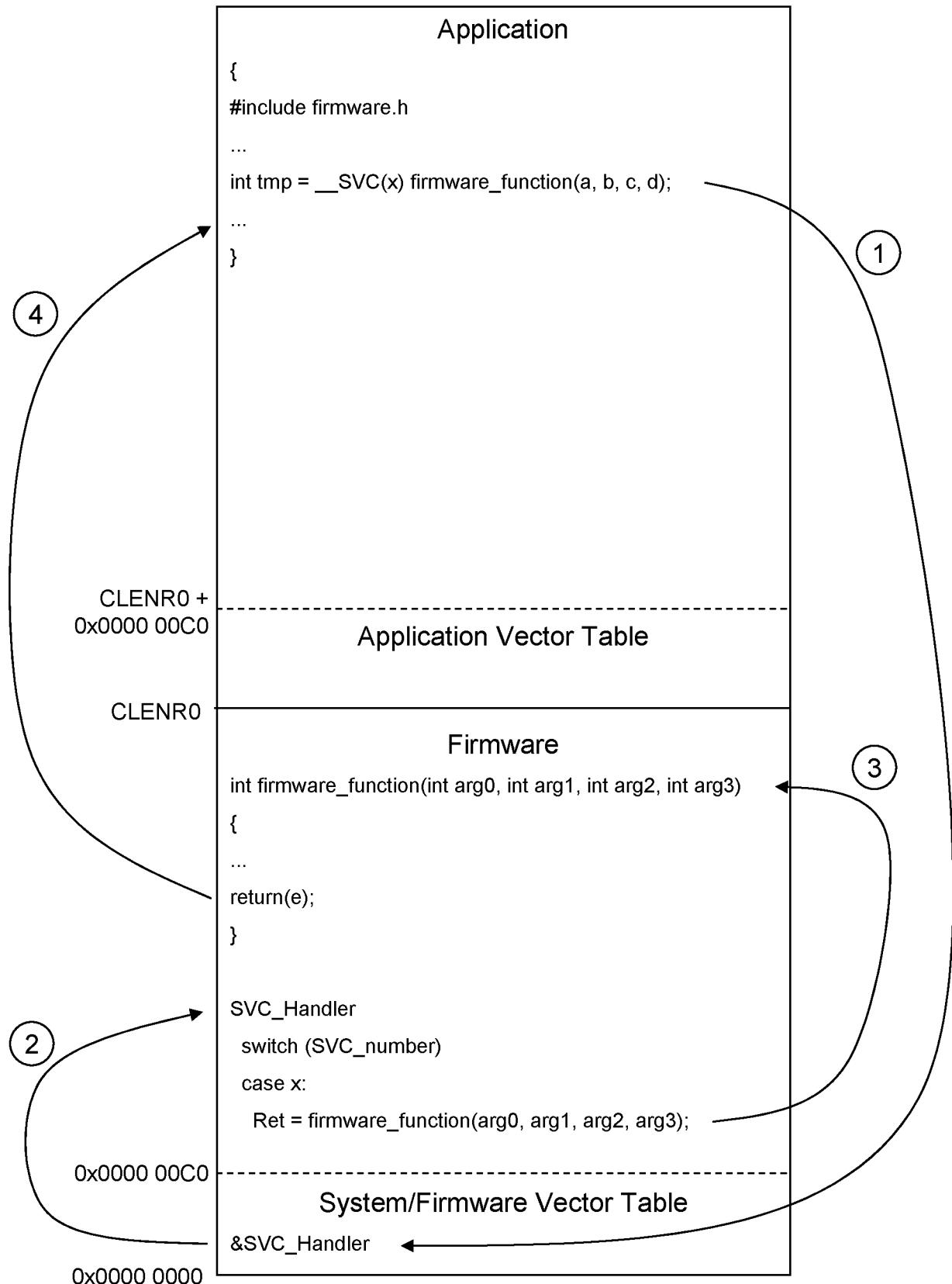


Figure 6

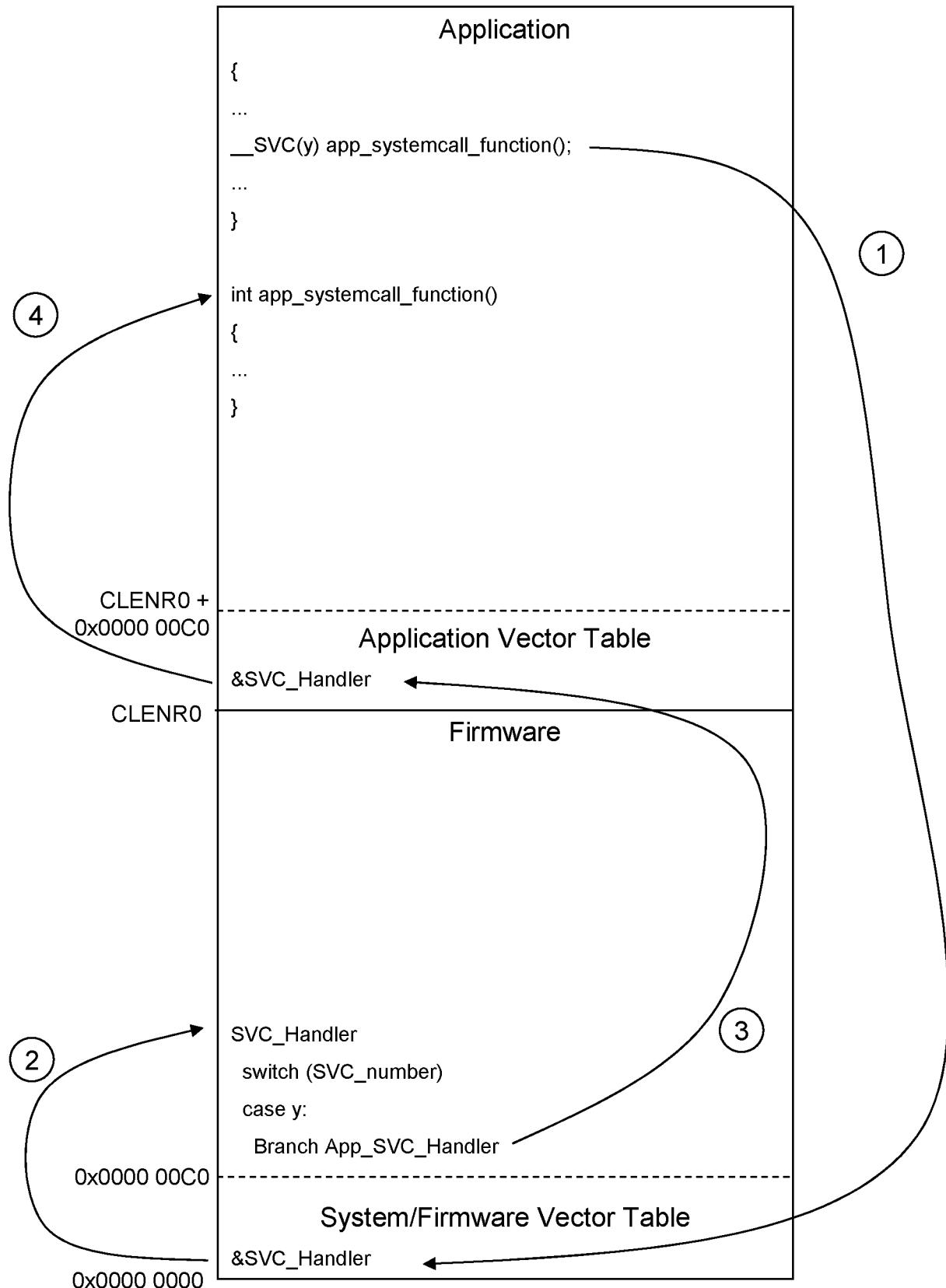


Figure 7

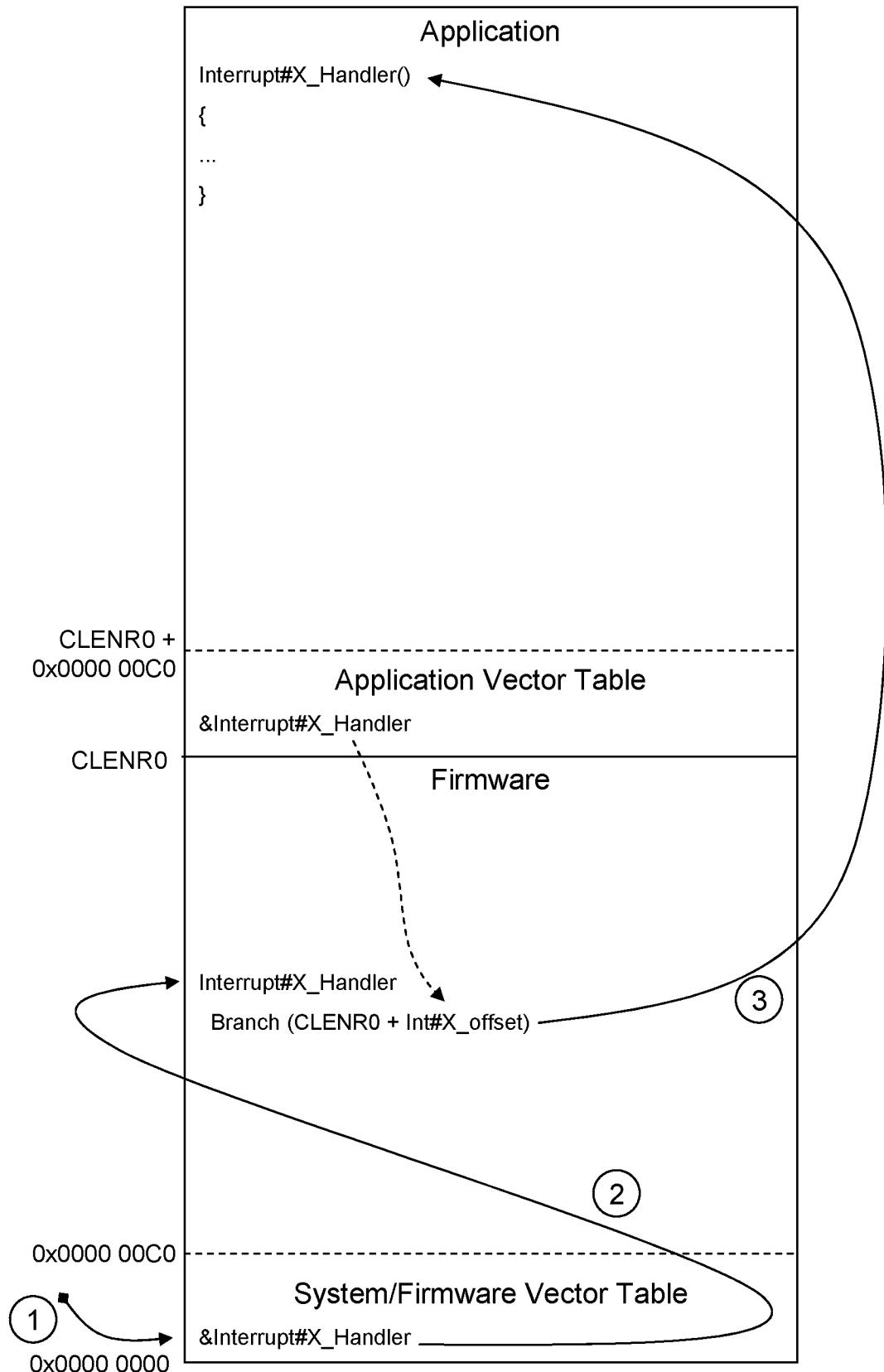


Figure 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2013/051692

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06F9/445
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2009/318078 A1 (GIRARD ERWAN [FR] ET AL) 24 December 2009 (2009-12-24) paragraph [0023] - paragraph [0054] paragraph [0065] - paragraph [0130] -----	1-29
Y	ARM: "Application Note 179 Cortex-M3 Embedded Software Development", , March 2007 (2007-03), XP002713220, Retrieved from the Internet: URL: http://infocenter.arm.com/help/topic/com.arm.doc.dai0179b/AppsNote179.pdf [retrieved on 2013-09-18] the whole document ----- -/-	1-29

Further documents are listed in the continuation of Box C.

See patent family annex.

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- "E" earlier application or patent but published on or after the international filing date
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- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"&" document member of the same patent family

Date of the actual completion of the international search

Date of mailing of the international search report

19 September 2013

02/10/2013

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INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2013/051692

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category ^{**}	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No

PCT/GB2013/051692

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