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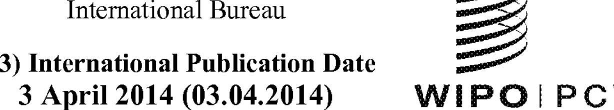

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(54) Title: PRINTED CIRCUIT BOARD

(57) Abstract:

Description

Title of Invention: PRINTED CIRCUIT BOARD

Technical Field

[1] The present invention relates to a printed circuit board, and more specifically, to a printed circuit board which can improve quality by minimizing a bulge or a dell on a surface of the printed circuit board.

Background Art

[2] As a part of a next generation multi-functional small package technology, the development of an electronic device-embedded printed circuit board has been recently noticed.

[3] In view of high functionalization as well as multi-functionality and miniaturization, the electronic device-embedded board is useful. The reason is because it provides a means capable of improving a reliability problem which may be generated during the electrical connection of an electronic device using wire bonding or a solder ball used in a flip chip or a ball grid array.

[4] In a conventional method of embedding the electronic device such as an IC, a structure in which the electronic device is embedded in only one side of a core substrate or one side of a build-up layer is adopted. The structure is an asymmetrical structure which is vulnerable to a warpage phenomenon under a thermal stress environment. This has a limitation to embedding an electronic device having a thickness less than a predetermined thickness because the warpage phenomenon is generated from the board in a direction, in which the electronic device is located, under the thermal stress environment. Furthermore, laminating materials used in the printed circuit board have a limitation that they cannot be manufactured to be less than a predetermined thickness due to an electrical insulating property. In this case, a critical thickness for preventing the warpage phenomenon is essentially limited due to material characteristics.

[5] Meanwhile, to solve the problem as described above, there is provided a printed circuit board and a manufacturing method thereof which can reduce the generation of a warpage phenomenon by geometrically forming an electronic device-equipped printed circuit board in an asymmetrical structure even through a thin device is embedded in the thin printed circuit board.

[6] FIG. 1 is a view showing an electronic device-embedded printed circuit board according to a conventional art.

[7] Referring to FIG. 1, an electronic device-embedded printed circuit board according to a conventional art includes: a core substrate 10; a via hole 12; an electronic device 20;

a first insulating layer 30; a second insulating layer 32; and a circuit pattern 34.

[8] The printed circuit board illustrated in FIG. 1 is designed and produced around the electronic device 20 in a symmetrical structure in which the extent of warpage of the board can be minimized.

[9] The symmetrical structure functions to reduce dangerousness such as an increase in a warpage phenomenon as the thicknesses of a printed circuit board and a device 20 equipped therein become thin.

[10] The printed circuit board according to the conventional art is configured such that an inner layer circuit pattern is formed on an upper surface and a lower surface of the core substrate 10, respectively, and thus the first insulating layer 30 and the second insulating layer 31 are formed in an upper part and a lower part of the core substrate 10 on which the inner layer circuit pattern is formed.

[11] FIG. 2 is a view showing a bulge and a dell phenomenon generated from the printed circuit board according to the conventional art.

[12] However, when the electronic device is adhered to the core substrate in which the inner layer circuit is formed, and the first insulating layer is then laminated on the core substrate, a void between the inner layer circuit and the electronic device becomes a factor which obstructs the flow of resin, thereby generating a difference in thickness of the first insulating layer. Accordingly, as illustrated in (a) of FIG. 2, a bulge phenomenon is generated from the printed circuit board in which the electronic device is arranged, or as illustrated in (b), a dell phenomenon is generated.

[13] That is, in the case of the general printed circuit board, a main cause why the warpage phenomenon is entirely generated from the substrate is due to a difference in coefficient of thermal expansion (CTE) between the core and the insulating layer (Prepreg) material.

[14] Also, since a core, an insulating layer (Prepreg), and an active element material and a cavity for mounting the active element are present in the electronic device-embedded printed circuit board (PCB), a difference in coefficient of thermal expansion and other differences with respect to young's modulus, contraction, and expansion are additionally largely generated, thereby causing the non-uniform generation of a bulge or a dell.

Disclosure of Invention

Technical Problem

[15] An aspect of the present invention provides a printed circuit board and a method of manufacturing the same, which can improve quality of the printed circuit board by solving bulge and dell problems caused by a difference in thickness of an insulating material and a difference in coefficient of thermal expansion (CTE) of an electronic

device.

[16] Also, an another aspect of the present invention provides a printed circuit board and a method of manufacturing the same, which can improve a mass production yield at the same time as minimizing a warpage phenomenon generated from the printed circuit board, in which an electronic device is arranged, by managing a thickness of a second insulating material corresponding to a thickness of a first insulating material.

[17] The technical problems to be solved in suggested exemplary embodiments are not limited to those mentioned above. Other technical problems, which are not mentioned, may be clearly understood by those having ordinary skill in the art to which the suggested exemplary embodiments pertain based on the description described below.

Solution to Problem

[18] According to an aspect of the present invention, there is provided a printed circuit board, including: a core substrate in which a cavity is formed; an electronic device mounted to the cavity; a first insulating layer which covers one surface of the core substrate and one surface of the electronic device; and a second insulating layer which covers another surface of the core substrate and another surface of the electronic device, wherein the first insulating layer has a same thickness at the core substrate and the electronic device.

Advantageous Effects of Invention

[19] According to one exemplary embodiment of the present invention, as a first insulating material is laminated using a separate cushion pad, the problem such as the lack of uniformity in flow of the resin caused by a space formed between a via hole of the core substrate and the electronic device can be solved, thereby enabling a deviation in thickness to be minimized.

[20] Also, according to another exemplary embodiment of the present invention, the bulge and dell problems generated from the printed circuit board in which the electronic device is arranged can be solved by minimizing the lack of uniformity in flow of the resin and a deviation in thickness, thereby enabling quality of the printed circuit board to be improved.

[21] According to still another exemplary embodiment of the present invention, when the second insulating material is laminated, an insulating material having a 10% or more larger thickness compared to a thickness of a first insulating material is used, so that the warpage phenomenon generated from the printed circuit board in which the electronic device is arranged can be minimized by managing a thickness of the second insulating material corresponding to the first insulating material, thereby enabling a mass production yield to increase.

Brief Description of Drawings

[22] The accompanying drawings are included to provide a further understanding of the present invention, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the present invention and, together with the description, serve to explain principles of the present invention. In the drawings:

[23] FIG. 1 is a view showing a electronic device-embedded printed circuit board according to a conventional art;

[24] FIG. 2 is a view showing a bulge and a dell phenomenon generated from the printed circuit board according to the conventional art;

[25] FIG. 3 is a view showing a printed circuit board and a method of manufacturing the same according to an exemplary embodiment of the present invention;

[26] FIG. 4 through FIG. 22 are views for explaining, in the order of processes, the method of manufacturing the printed circuit board according to exemplary embodiments;

[27] FIG. 23 is a view for explain a thickness of the printed circuit board of the conventional art; and

[28] FIG. 24 is a view for explain a thickness of the printed circuit board of the present invention.

Mode for the Invention

[29] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings in such a manner that the present could be easily implemented by those having ordinary skill in the art to which the present invent pertains. The present invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present invention to those skilled in the art. The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments.

[30] It will be further understood that the terms "comprises" and "includes" and/or "comprising," and "including" when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[31] To clearly explain the present invention, the parts which have no relation with the explanation are omitted, and to clearly express various layers and areas, their thicknesses are enlarged. Also, like numbers may refer to like elements throughout the description of the figures.

[32] When it is mentioned that a part such as a layer, a film, an area, a plate and the like is "above" other part, this includes a case in which the part is just above the other part as well as a case in which still another part is present in their middle. On the contrary, when it is mentioned that a part is just above other part, this means that there is no still another part in their middle.

[33] FIG. 3 is a view showing a printed circuit board and a method of manufacturing the same according to an exemplary embodiment of the present invention.

[34] Referring to FIG. 3, a printed circuit board includes: a core substrate 110; an electronic device 120 which is inserted into a via hole formed in the core substrate 110; a first insulating layer 130 which is formed on the core substrate 110 to cover an upper part of the electronic device 120; a second insulating layer 140 which is formed below the core substrate 110 to cover a lower part of the electronic device 120; a first circuit pattern 136 formed on a surface of the first insulating layer 130; a second circuit pattern 144 formed on a surface of the second insulating layer 140; a third insulating layer 160 which is formed on the first insulating layer 130 to cover the surface of the first insulating layer 130; a fourth insulating layer 170 which is formed below the second insulating layer 140 to cover the surface of the second insulating layer 140; a third circuit pattern 164 formed on a surface of the third insulating layer 160; a fourth circuit pattern 174 formed on a surface of the fourth insulating layer 170; and a protective layer 190 which covers the surface of the third insulating layer 160 and the surface of the fourth insulating layer 170, and in which the third circuit pattern 164 and a part of the fourth circuit pattern 174 are exposed.

[35] Hereinafter, an upper part of the core substrate 110 is defined as an upper direction of the electronic device 120 on the drawings, and a lower part of the core substrate 110 is defined as a lower direction of the electronic device 120.

[36] The core substrate 110 may be a thermosetting polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or a glass fiber-impregnated substrate. In a case where the core substrate includes a polymer resin, an epoxy-based insulating resin may be included therein. However, unlike this, a polyimide-based resin may be included therein.

[37] Preferably, the core substrate 110 may be formed of an epoxy-based insulating resin in which glass fabric is impregnated.

[38] A cavity 112 which passes through an upper surface and a lower surface is formed in the core substrate 110.

[39] At this time, according to the present invention, the core substrate 110 is composed of a dummy core substrate in which a circuit pattern is not formed on an upper surface thereof. Like this, when the core substrate 110 is formed of the dummy core substrate, a thickness of the first insulating layer formed in an upper part of the core substrate

110 may be more uniformly formed.

[40] The cavity 112 may be formed by any one processing method of machining, laser and chemical processes.

[41] When the cavity 112 is formed by the machining process, methods such as a milling process, a drill process, routing process and the like may be used. When the cavity 112 is formed by the laser process, an UV or CO_2 laser method may be used. Also, when the cavity 112 is formed by the chemical process, the core substrate may be opened using chemicals including aminosilane, ketones and the like.

[42] Meanwhile, the laser process is a cutting method of partially melting and evaporating a material by concentrating optical energy on a surface of the material to obtain a desired shape. When the laser process is used, even complex formation using a computer program may be easily processed, a composite material which is difficult to cut it using other methods, may be also processed

[43] Also, when the laser process is used, a cut diameter may be at least 0.005 mm, and it is advantageous that the range in processable thickness is large.

[44] An YAG (Yttrium Aluminum Garnet) laser, a CO_2 laser or an UV laser may be used as the laser process drill. The YAG laser is a laser which may process both the copper foil layer and the insulating layer, and the CO_2 laser is a laser which may process only the insulating layer.

[45] The electronic device 120 is inserted into the cavity 112.

[46] The electronic device 120 may be composed of a passive element or an active element. For example, the electronic device 120 may be a resistor, an inductor or a capacitor. A terminal 122 for receiving currents or voltages supplied from the outside is formed at both ends of the electronic device 120.

[47] The first insulating layer 130 is formed on the core substrate 110, and the second insulating layer 140 is formed below the core substrate 110.

[48] The first insulating layer 130 and the second insulating layer 140 may be a thermosetting or thermo plastic polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or glass-fiber impregnated substrate. When a polymer resin is included therein, an epoxy-based insulating resin such as FR-4, BT (Bismaleimide Triazine), ABF (Ajinomoto Build up Film) and the like may be included. Unlike this, a polymide-based resin may be included therein. However, the present invention is not specifically limited to this.

[49] Meanwhile, the first insulating layer 130 and the second insulating layer 140 may be formed in the same thickness. Here, the substantially same thickness includes the case in which a difference in thickness between the first insulating layer 130 and the second insulating layer 140 is more than 0 ㎛ but is less than 10 ㎛, as well as the case in which the first insulating layer 130 and the second insulating layer 140 have the same

thickness. More specifically, even though the thickness of the second insulating layer 140 is larger than that the first insulating layer 130, when a different in thickness is less than 10 ㎛, the thicknesses of the first insulating layer 130 and the second insulating layer 140 are deemed to be substantially identical to each other.

[50] At this time, the inner layer-circuit pattern is not formed on the surface of the core substrate 110. If the circuit pattern is directly formed on the core substrate 110, this causes various problems during a laminating process of the first insulating layer or the second insulating layer, so a surface of the printed circuit board becomes non-uniform.

[51] Thus, in the exemplary embodiment, the dummy core substrate, in which the circuit pattern is not formed, is used as the core substrate 110,and the first insulating layer 130 and the second insulating layer 140 are formed on and below the core substrate 110, respectively.

[52] Owing to this, the first insulating layer 130 is in contact with the entire upper surface of the core substrate 110, and the second insulating layer 140 is in contact with the entire lower surface of the core substrate 110.

[53] As aforementioned, when the first insulating layer 130 is laminated, a thickness of the first insulating layer 130 formed in an area of the core substrate 110 in which the electronic device is mounted and a thickness of the first insulating layer 130 formed on the core substrate 110 are equal to each other. At this time, the core substrate 110 is composed of the dummy core substrate so that the thicknesses of the first insulating layer 130 are more uniformly formed. Thus, a difference between a maximum thickness and a minimum thickness of the first insulating layer 130 ranges from 0 ㎛ to 10 ㎛.

[54] That is, in the conventional art, since the circuit pattern is formed on the core substrate, a difference in thickness was more than 10 ㎛ depending on areas of the insulating layer formed in an upper part of the core substrate. However, in the present invention, since the thicknesses of the first insulating layer 130 are uniformly formed, a difference between a maximum thickness and a minimum thickness of the insulating layer ranges from 0 ㎛ to 10 ㎛. Thus, bulge and dell problems generated from the surface of the printed circuit board can be solved.

[55] The first circuit pattern 136 is formed on the first insulating layer 130, and the second circuit pattern 144 is formed below the second insulating layer 140.

[56] The first circuit pattern 136 may have a plurality of layered structures and may be formed on the first insulating layer 130 using a metal layer which forms the first circuit pattern 136.

[57] The first circuit pattern 136 may be formed of an alloy including at least one of Al, Cu, Ag, Pt, Ni and Pd.

[58] The first circuit pattern 136 may is formed by an additive process, a subtractive

process, an MSAP (Modified Semi Additive Process) and a SAP (Semi Additive Process) which are general manufacturing processes of the printed circuit board. The detailed explanation thereon is omitted.

[59] As such, the second circuit pattern 144 may have a plurality of layered structures and may be formed on the second insulating layer 140 using a metal layer which forms the second circuit pattern 144.

[60] At this time, the first circuit pattern 136 or the second circuit pattern 144 may be composed of a CCL (Copper Clad Laminate) circuit pattern.

[61] The third insulating layer 160 is formed on the first insulating layer 130, and the fourth insulating layer 170 is formed below the second insulating layer 140.

[62] The third insulating layer 160 and the fourth insulating layer 170 may be a thermosetting polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or a glass fiber-impregnated substrate. In a case where a polymer resin is included therein, an epoxy-based insulating resin such as FR-4, BT (Bismaleimide Triazine), ABF (Ajinomoto Build up Film) may be included. However, unlike this, a polyimide-based resin may be included. However, the present invention is not limited to this

[63] Also, the third circuit pattern 164 is formed on the third insulating layer 160, and the fourth circuit pattern 174 is formed below the fourth insulating layer 170.

[64] The third circuit pattern 164 and the fourth circuit pattern 174 may be formed using an additive process, a subtractive process, an MSAP (Modified Semi Additive Process) and a SAP (Semi Additive Process) which are general manufacturing processes of the printed circuit board. The detailed explanation thereon is omitted.

[65] Meanwhile, at least one conductive via 156, 158, 186, 188 is formed on the core substrate 100, the first insulating layer 130, the second insulating layer 140, the third insulating layer 160 and the fourth insulating layer 170. The conductive via 156, 158, 186, 188 may be formed in such a manner that a via hole, which opens at least one of the core substrate 100, the first insulating layer 130, the second insulating layer 140, the third insulating layer 160 and the fourth insulating layer 170, is formed using the laser process, and an inner part of the via hole formed thereby is filled with a metal paste.

[66] The conductive via 156, 158, 186, 188 is formed to conduct electricity in at least one or more areas of the first and second circuit patterns have conductive.

[67] At this time, a metal material which forms the conductive via 156, 158, 186, 188 may be one material selected from the group consisting of Cu, Ag, Sn, Au, Ni and Pd. The filling of the metal material may be performed using any one of a non-electrolyte or electrolyte plating process, a screen printing process, a sputtering process, an evaporation process, an ink jetting process and a dispensing process, or a combination

thereof.

[68] Meanwhile, the terminal of the electronic device 120 is disposed to a side of the second insulating layer 140, and the conductive via 156 passes through the second insulating layer 140 so as to be connected to the terminal of the electronic device 120.

[69] The protective layer 190 is formed on surfaces of the third insulating layer 160 and the fourth insulating layer 170.

[70] The protective layer 190 may be a solder resist.

[71] As aforementioned, in the printed circuit board of the present invention, since the inner layer-circuit pattern is not formed on the surface of the core substrate 110, lamination quality of the first insulating layer 130 to be laminated can be improved.

[72] Also, according to the exemplary embodiment of the present invention, as the lack of uniformity in flow of the resin and a deviation in thickness are minimized, the bulge and dell problems generated from the printed circuit board in which the electronic device is arranged can be solved, thereby enabling quality of the printed circuit board to be improved

[73] Also, in the exemplary embodiment of the present invention, when the second insulating layer is laminated, an insulating material having a larger thickness up to more than 10% compared to a thickness of a first insulating material is applied thereto. Thus, a warpage phenomenon generated from the printed circuit board in which the electronic device is arranged can be minimized by managing the thickness of the second insulating layer corresponding to that of the first insulating layer, thereby increasing a mass production yield.

[74] Hereinafter, the explanation on the method of manufacturing the printed circuit board as illustrated in FIG. 3 will be described.

[75] FIG. 4 through FIG. 22 are views for explaining, in the order of processes, the method of manufacturing the printed circuit board according to the exemplary embodiment.

[76] First, as illustrated in FIG. 4, the core substrate 110 is prepared.

[77] The core substrate 110 may be a thermosetting polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or a glass fiber-impregnated substrate. In a case where the core substrate includes a polymer resin, an epoxy-based insulating resin may be included. However, unlike this, a polyimide-based resin may be included.

[78] At this time, the upper surface and the lower surface of the core substrate 110 are exposed to the outside. That is, in general, the metal layer is formed on at least one surface of the core substrate 110, and the inner layer-circuit pattern will be formed later using the metal layer.

[79] However, in the exemplary embodiment, the core substrate 110, which has a

thickness same as or thinner than that of the electronic device 120 to be inserted later, and in which the inner layer-circuit pattern (or a metal layer) is not formed on both surfaces thereof, is prepared.

[80] Then, as illustrated in FIG. 5, the cavity 112 is formed in at least one area of the core substrate 110.

[81] The cavity 112 may be formed by any one processing method of a machining process, a laser process and a chemical process.

[82] When the cavity 112 is formed by the machining process, methods such as a milling process, a drill process, routing process and the like may be used. When the cavity 112 is formed by the laser process, an UV or CO_2 laser method may be used. Also, when the cavity 112 is formed by the chemical process, the core substrate may be opened using chemicals including aminosilane, ketones and the like.

[83] Meanwhile, the laser process is a cutting method of partially melting and evaporating a material by concentrating optical energy on a surface of the material to obtain a desired shape. When the laser process is used, even complex formation using a computer program may be easily processed, a composite material which is difficult to cut it using other methods, may be also processed

[84] Also, when the laser process is used, a cut diameter may be at least 0.005 mm, and it is advantageous that the range in processable thickness is large.

[85] An YAG (Yttrium Aluminum Garnet) laser, a CO_2 laser or an UV laser may be used as the laser process drill. The YAG laser is a laser which may process both the copper foil layer and the insulating layer, and the CO_2 laser is a laser which may process only the insulating layer.

[86] At this time, the cavity 112 is processed to have a larger size as much as about 100μm to 200μm than that of the electronic device to be inserted later.

[87] Then, as illustrated in FIG. 6, an adhesive film 114 is adhered to the bottom of the core substrate 110 in which the cavity 112 is formed.

[88] The adhesive film 114 may be formed of a same material as a general tape. Also, a carrier, which is usually used in a manufacturing process of the printed circuit board, may be used.

[89] Next, as illustrated in FIG. 7, the electronic device 120 is inserted into the cavity 112.

[90] At this time, the electronic device 120 may be fixed into the cavity 112 while being supported by an adhesive film 114 adhered to the bottom of the core substrate 110.

[91] The electronic device 120 may include any one of a passive element and an active element. For example, the electronic device 120 may be a resistor, an inductor or a capacitor.

[92] The terminal 122 for receiving currents or voltages supplied from the outside is formed on at least one surface of the electronic device 120.

[93] Next, as illustrated in FIG. 8, a thickness of the first insulating material is calculated depending on a capacity of the electronic device 120 inserted into the cavity 112, thereby performing lay-up.

[94] The first insulating material forms the first insulating layer 130, and a first metal layer 132 is formed on one surface of the first insulating layer 130.

[95] The first insulating material may be a thermosetting or thermo plastic polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or glass-fiber impregnated substrate. When a polymer resin is included therein, an epoxy-based insulating resin such as FR-4, BT (Bismaleimide Triazine), ABF (Ajinomoto Build up Film) and the like may be included. Unlike this, a polyimide-based resin may be included. However, the present invention is not specifically limited to this.

[96] Hereinafter, as illustrated in FIG. 9, the cushion pad 134 is adhered onto the first metal layer 132, the first insulating 130 and the first metal layer 132 are formed on the core substrate 110 using the cushion pad 132 so that the upper part of the electronic device 120 inserted into the cavity 112 of the core substrate is embedded.

[97] At this time, the cushion pad 134 is formed on the first metal layer 132, and the first insulating layer 130 is formed on the core substrate 110 by uniformly controlling pressure using the cushion pad 34 and controlling flow of the resin.

[98] In general, in the conventional art, in order to form the first insulating layer 130, the flow of the resin was controlled using only the first insulating layer 130 and the first metal layer 132. However, because the aforesaid first metal layer 132 has low elastic coefficient, each pressure of a flat portion and a via hole portion of the substrate having a step pulley such as the cavity 112 may be generated to be different from each other. Accordingly, in the present invention, the first insulating layer 130 is formed by adhering the cushion pad 134 having high elastic coefficient onto the first metal layer, so the pressure of the flat portion in which the cavity 112 is not formed and the pressure of the part in which the cavity is formed may be uniformly maintained, thereby enabling a deviation in thickness to be reduced.

[99] At this time, the cushion pad 134 may use a product having a thickness of 350㎛. The more the thickness of the cushion pad 134 increases, the higher the uniformity of the pressure generates. Thus, it is preferable for the cushion pad to use a Si-based cushion sheet having a 350㎛ or more thickness.

[100] Meanwhile, when the core substrate 110 is composed of the dummy core substrate, the thicknesses of the first insulating layer 130 are more uniformly formed, so a difference between a maximum thickness and a minimum thickness of the first insulating layer 130 ranges from 0 ㎛ to 10 ㎛.

[101] That is, in the conventional art, because the circuit pattern is formed on the core substrate, a difference in thickness was more than 10 ㎛ depending on areas of the in-

sulating layer formed in the upper part of the core substrate. However, in the present invention, the thicknesses of the first insulating layer 130 are uniformly formed so that the difference between a maximum thickness and a minimum thickness of the first insulating layer 130 may range from 0 ㎛ to 10 ㎛. Thus, the bulge and dell problems generated from the surface of the printed circuit board can be solved.

[102] Next, as illustrated in FIG. 10, the cushion pad 132 formed on the first metal layer 132 and the adhesive film 114 adhered to the bottom of the core substrate 110 are removed by performing plasma treatment.

[103] Next, as illustrated in FIG. 11, the second insulating layer 140 and the second metal layer are laid-up in a lower part of the core substrate 110.

[104] The second metal layer 142 is formed on one surface of the second insulating layer 140.

[105] At this time, it is preferable that the second insulating layer 140 is formed to be more than 10% thicker than the first insulating layer 130.

[106] Explaining it more specifically, since the cavity for embedding the electronic device 120 is present in a lamination space of the first insulating layer 130, the flow of the resin is prevented. Thus, the thickness of the first insulating layer 130 is formed to be thick so that the resin can be prevented from flowing out to the outside of the printed circuit board.

[107] On the contrary, the thickness of the second insulating layer 140is thin compared to that of the first insulating layer because a large amount of resin flows out to the outside.

[108] Therefore, to form the thicknesses of the first insulating layer 130 and the second insulating layer 140 to be equal to each other, the process should be performed in a state of forming the second insulating layer 140 to be more than 10% thicker than the first insulating layer 130.

[109] Then, as illustrated in FIG. 12, the second insulating layer 140 is laminated below the core substrate 110 by applying pressure to the second metal layer 142, so the thicknesses of the second insulating layer and the first insulating layer 130 become equal to each other.

[110] The second insulating material may be a thermosetting or thermo plastic polymer substrate, a ceramic substrate, an organic-inorganic composite material substrate or glass-fiber impregnated substrate. When a polymer resin is included therein, an epoxy-based insulating resin such as FR-4, BT (Bismaleimide Triazine), ABF (Ajinomoto Build up Film) and the like may be included. Unlike this, a polyimide-based resin may be included. However, the present invention is not specifically limited to this.

[111] Next, as shown in FIG. 13, a first via hole 152, to which the terminal 122 of the electronic device 120 embedded in the core substrate 110 is exposed, is formed by

opening the second insulating layer 140 and the second metal layer 142.

[112] Also, a second via hole 154, which opens the core substrate 110, the first insulating layer 130, the first metal layer 132, and the second insulating layer 140 and the second metal layer 142, is formed.

[113] The first via hole 152 and the second via hole 154 may be formed by any one processing method of a machining process, a laser process and a chemical process.

[114] In a case where the first via hole 152 and the second via hole 154 are formed by the machining process, methods such as a milling process, a drilling process and a routing process and the like may be used. In a case where they are formed by the laser process, an UV or CO_2 laser method may be used. In a case where they are formed by the chemical process, chemicals including aminosilane, ketones and the like may be used.

[115] Next, as shown in FIG. 14, the first conductive via 156 and the second conductive via 158 are formed by filling the first via hole 152 and the second via hole 154 with a metal material.

[116] At this time, the first conductive via 156 may be formed to be filled with the entire of the via first hole 152. On the other hand, the second conductive via 158 may be selectively formed in only an inner wall of the second via hole 154.

[117] The metal material may be one material selected from the group consisting of Cu, Ag, Sn, Au, Ni and Pd. The filling of the metal material may be performed using any one of a non-electrolyte or electrolyte plating process, a screen printing process, a sputtering process, an evaporation process, an ink jetting process and a dispensing process, or a combination thereof.

[118] Next, as illustrated in FIG. 15, the first circuit pattern 136 is formed by patterning the first metal layer, and the second circuit pattern 144 is formed by patterning the second metal layer.

[119] The first circuit pattern 136 and the second circuit pattern 144 may be formed using an additive process, a subtractive process, a modified semi additive process (MSAP) or a semi additive process (SAP).

[120] Next, as shown in FIG. 16, the third insulating layer 160 and the third metal layer 162 are laid-up in an upper part of the first insulating layer 130, and the fourth insulating layer 170 and the fourth metal layer 172 are laid up in a lower part of the second insulating layer 140.

[121] Next, as illustrated in FIG. 17, the third insulating layer 160 in which the first circuit pattern 136 is embedded and the third metal layer 162, are formed on the first insulating layer 130, and the fourth insulating layer 170 in which the second circuit pattern 144 is embedded and the fourth metal layer 172 are formed below the second insulating layer 140.

[122] Next, as shown in FIG. 18, the third via hole 182, in which the first circuit pattern is

exposed, is formed by processing the third insulating layer 160 and the third metal layer 162.

[123] Also, a fourth via hole 184 to which the second circuit pattern 144 is exposed is formed by processing the fourth insulating layer 170 and the fourth metal layer 172.

[124] The third and fourth via holes 182, 184 may be formed using an excimer laser which emits a laser beam having the wavelength of an ultraviolet region. As the excimer laser, a KrF excimer laser (i.e. a krypton fluoride laser having a center wavelength of 248nm), or an ArF excimer laser (i.e. an argon fluoride laser having a center wavelength of 193nm) may be applied.

[125] Next, as shown in FIG. 19, the third conductive via 186 and a fourth conductive via 188 are formed by filling the third via hole 182 and the fourth via hole 184 with a metal material.

[126] At this time, the metal material may be any one material selected from the group consisting of Cu, Ag, Sn, Au, Ni and Pd. The filling of the metal material may be performed using any one process of a non-electrolytic or electrolytic plating process, a screen printing process, a sputtering process, an evaporation process, an ink jetting process and a dispensing process, or a combination thereof.

[127] Next, as shown in FIG. 20, the third circuit pattern 164 and the fourth circuit pattern 174 are formed by patterning the third metal layer 162 and the fourth metal layer.

[128] The third circuit pattern 164 and the fourth circuit pattern 174 may be formed using an additive process, a subtractive process, a modified semi additive process (MSAP) or a semi additive process (SAP).

[129] Next, as shown in FIG. 21, the protect layer 190 is formed on the third insulating layer 160 and the fourth insulating layer 170 so as to cover a surface of the third insulating layer 160, the third circuit pattern 164, a surface of the fourth insulating layer 170 and the fourth circuit pattern 174.

[130] The protective layer 190 may be formed of a solder resist.

[131] Next, as illustrated in FIG. 22, the surfaces of the third circuit pattern 164 and the fourth circuit pattern 174, which should be exposed, are exposed by opening the protective layer 190.

[132] According to still another exemplary embodiment, since the first insulating material is laminated using the separate cushion pad, the problem such as the lack of uniformity in flow of the resin caused by a space formed between the via hole of the core substrate and the electronic device can be solved, thereby enabling a deviation in thickness to be minimized.

[133] Also, according to still another exemplary embodiment, the bulge and dell problems generated from the printed circuit board in which the electronic device is arranged can be solved by minimizing the lack of uniformity in flow of the resin and a deviation in

thickness, thereby enabling quality of the printed circuit board to be improved.

[134] FIG. 23 is a view for explain a thickness of the printed circuit board of the conventional art. FIG. 24 is a view for explain a thickness of the printed circuit board of the present invention.

[135] Table 1

[Table 1]

Division	Explanation	Designed Thickness	Measured Thickness	Level of Bulge and Dell
A	Core substrate	0.2 T	0.24 T	3 mm
B	Distance between electronic device and core substrate	50 ㎛	50 ㎛	
C	Thickness of first insulating material	55 ㎛	45 ㎛	
C'	Thickness of first insulating material	55 ㎛	65 ㎛	
D	Thickness of first insulating material	60 ㎛	55 ㎛	

[136] Referring to FIG. 23, in the printed circuit board according to the conventional art, when the plurality of electronic devices 210, 220 is inserted into the inner part of the core substrate, even though a thickness (C) of a first area and a thickness (C') of a second area of the first insulating layer formed on the first electronic device 210 are designed as 55㎛ to be identical to each other, a really measured thickness of the first area of the first insulating material formed on the first electronic device 210 was 45 ㎛, and a measured thickness of the second area of the first insulating material formed on the first electronic device 210 was 65 ㎛. Thus, depending on the position of the first insulating layer, a difference in thickness reaches 20 ㎛.

[137] As aforementioned, in the conventional art, a deviation in really measured thickness of the first insulating layer ranges from 45 ㎛ to 65 ㎛. Consequently, the phenomenon of a bulge or dell of 3 mm is generated from a region of the printed circuit board in which the electronic devices 210, 220 are mounted, around the region.

[138] Table 2

[Table 2]

Division	Explanation	Designed Thickness	Measured Thickness	Level of Bulge and Dell
A	Core substrate	0.2 T	0.24 T	1 mm
B	Distance between electronic device and core substrate	50 ㎛	50 ㎛	
C	Thickness of first insulating material	55 ㎛	50 ㎛	
C'	Thickness of first insulating material	55 ㎛	60 ㎛	
D	Thickness of first insulating material	60 ㎛	55 ㎛	

[139] However, according to the present invention, as illustrated in FIG. 24, when the thickness (C) of the first area and the thickness (C') of the second area of the first insulating layer formed on the first electronic device 210 are designed as 55 ㎛ to be identical to each other as shown in Table 2,because the core substrate is the dummy core substrate in which the circuit pattern is not formed on the upper surface thereof, as shown in Table 2, a really measured thickness of the first area of the first insulating material formed on the first electronic device 210 was 55 ㎛, and a measured thickness of the second area of the first insulating material formed on the first electronic device 210 was 65 ㎛. Thus, depending on the position of the first insulating layer, a difference in thickness is only 10 ㎛.

[140] Like this, according to the present invention, because the difference in really measured thickness is only about 10㎛, a surface difference caused by a bulge or dell generated from the region of the printed circuit board in which the electronic devices 210, 220 are mounted, and around the region is only 1 mm.

[141] As previously described, in the detailed description of the invention, having described the detailed exemplary embodiments of the invention, it should be apparent that modifications and variations can be made by persons skilled without deviating from the spirit or scope of the invention. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims and their equivalents.

[142]

Claims

[Claim 1] A printed circuit board, comprising:
a core substrate in which a cavity is formed;
an electronic device mounted to the cavity;
a first insulating layer which covers one surface of the core substrate and one surface of the electronic device; and
a second insulating layer which covers another surface of the core substrate and another surface of the electronic device,
wherein the first insulating layer is configured such that a thickness of the core substrate is identical to that of the electronic device.

[Claim 2] The printed circuit board of claim 1, wherein the core substrate is a dummy core substrate in which a circuit pattern is not formed on an upper surface thereof.

[Claim 3] The printed circuit board of claim 1, wherein the first insulating layer is configured such that a difference between the thicknesses of the core substrate and the electronic device is more than 0 ㎛ but is less than 10 ㎛.

[Claim 4] The printed circuit board of claim 1, wherein the core substrate is configured such that an entire upper surface is in contact directly with the first insulating layer, and an entire lower surface is in contact directly with the second insulating layer.

[Claim 5] The printed circuit board of claim 1, wherein a difference in a thickness of the first insulating layer corresponding to an upper part of an area in which the plurality of electronic devices is mounted is more than 0 ㎛ but is less than 10 ㎛.

[Claim 6] The printed circuit board of claim 1, wherein a thickness of the second insulating layer is identical with that of the first insulating layer.

[Claim 7] The printed circuit board of claim 1, wherein the core substrate is any one of a ceramic substrate, an organic-inorganic composite material substrate and a glass-fiber impregnated substrate.

[Claim 8] The printed circuit board of claim 1, wherein the core substrate is a thermosetting polymer substrate composed of an epoxy-based insulating resin or a polyimide-based resin.

[Claim 9] The printed circuit board of claim 8, wherein the epoxy-based insulating resin is formed by impregnating glass fabric or silicon fabric in epoxy resin.

[Claim 10] The printed circuit board of claim 1, wherein a terminal of the

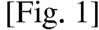
electronic device is disposed to a side of the second insulating layer.

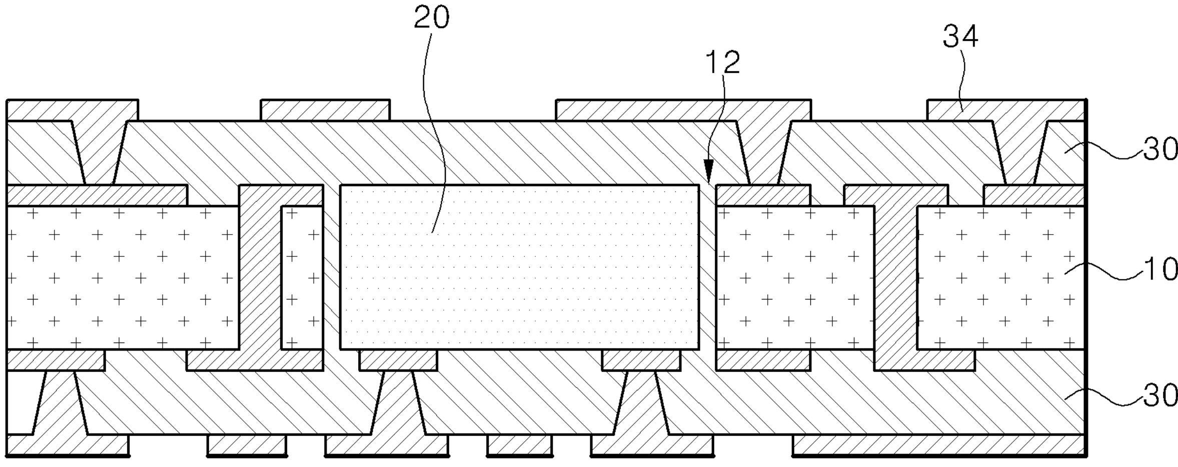
[Claim 11] The printed circuit board of claim 1, further comprising a conductive via which is configured to pass through the second insulating layer so as to be connected to the terminal of the electronic device.

[Claim 12] The printed circuit board of claim 1, further comprising at least one circuit pattern which is formed on surfaces of the first insulating layer and the second insulating layer.

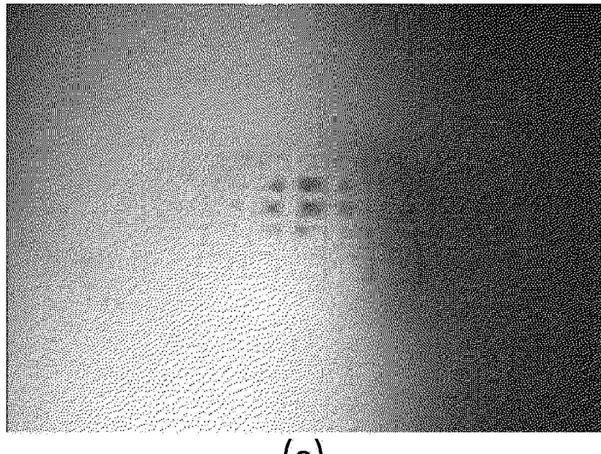
[Claim 13] The printed circuit board of claim 12, wherein the circuit pattern is composed of a CCL (Copper Clad Laminate) circuit pattern.

[Claim 14] The printed circuit board of claim 1, wherein the electronic device is a positive element or an active element.


[Fig. 1]



[Fig. 2]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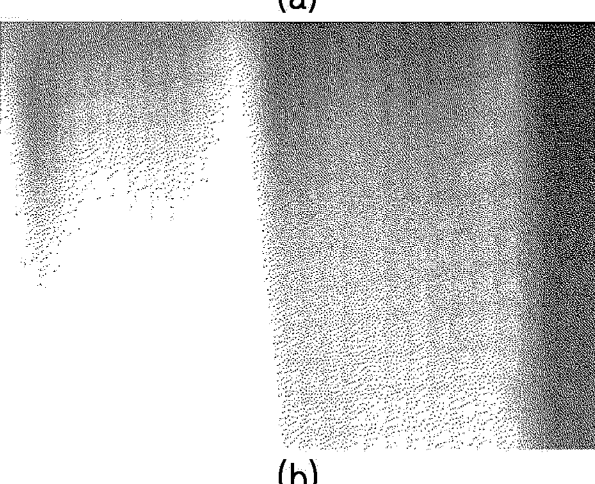
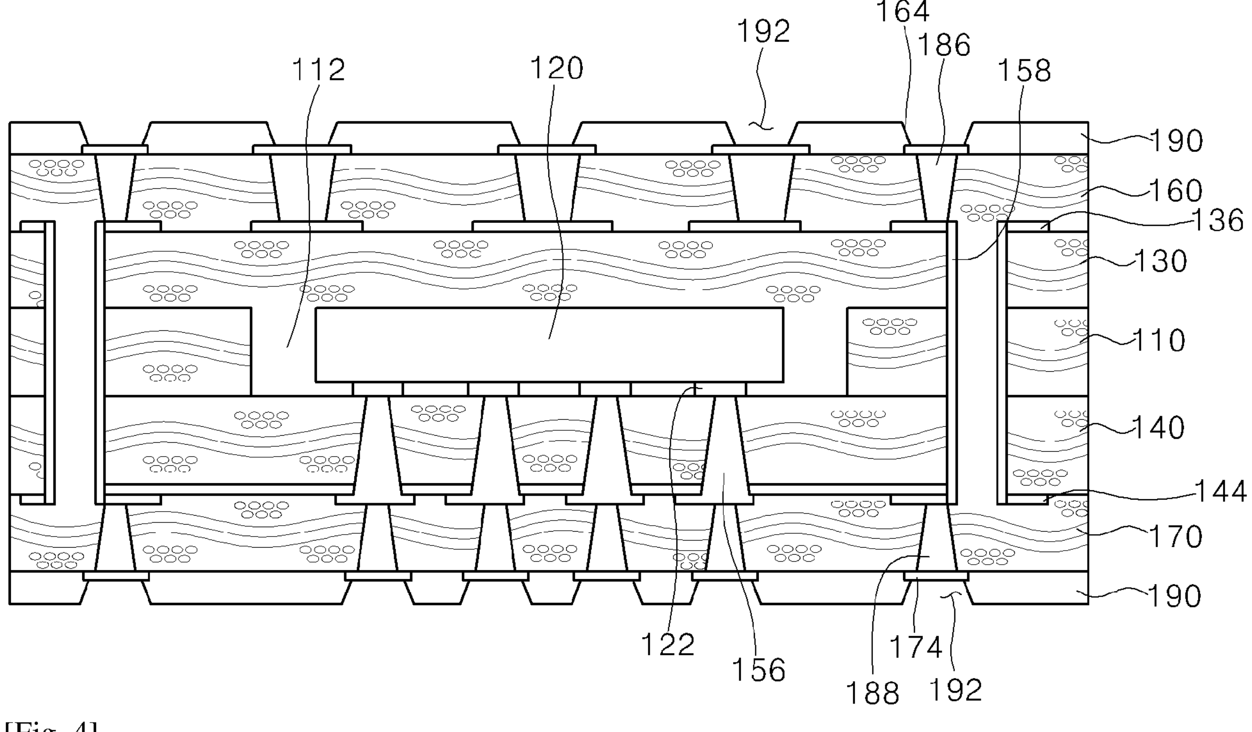
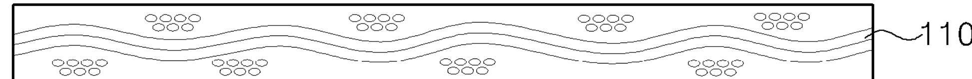

(b)

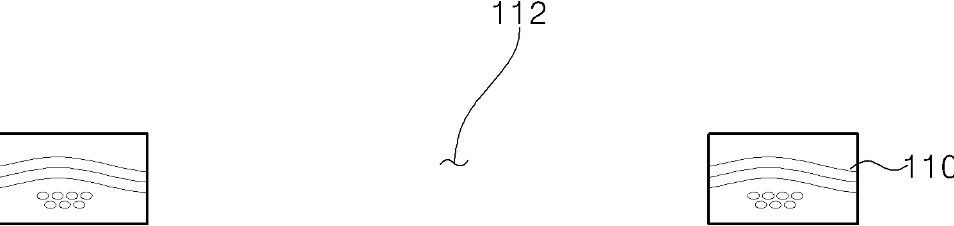
[Fig. 3]



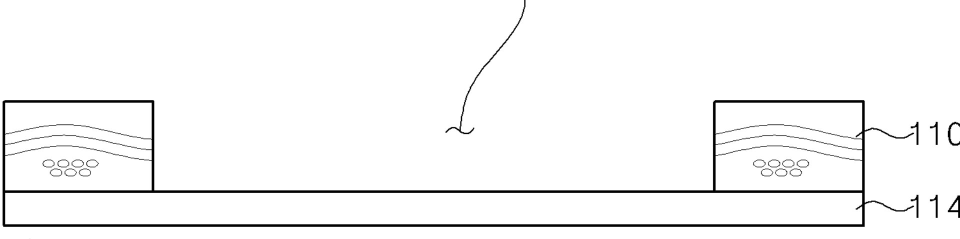
[Fig. 4]



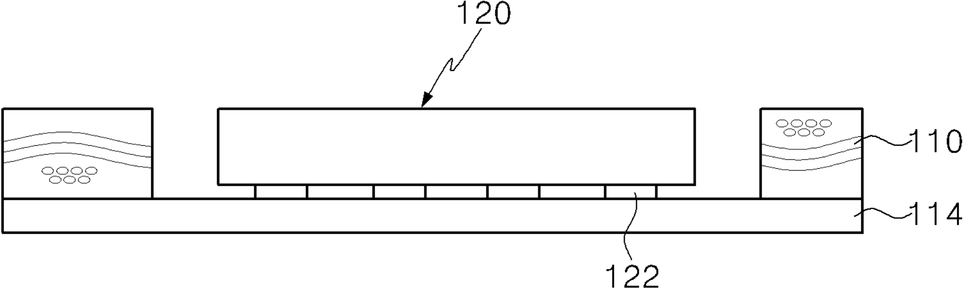
[Fig. 5]



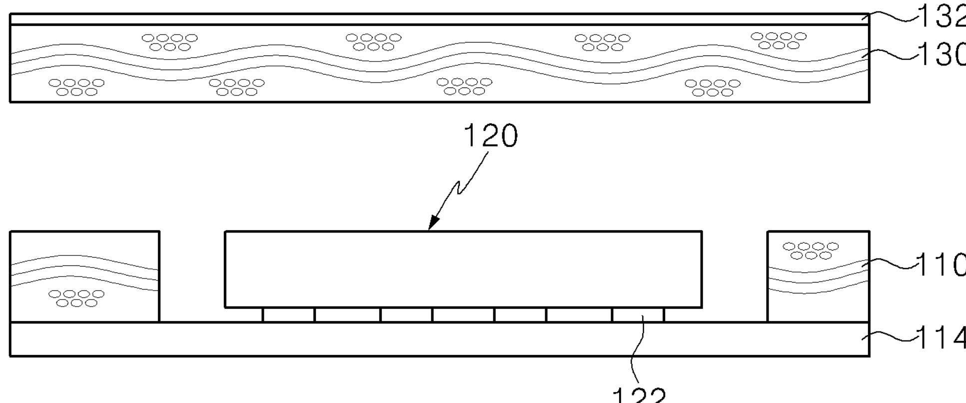
[Fig. 6]



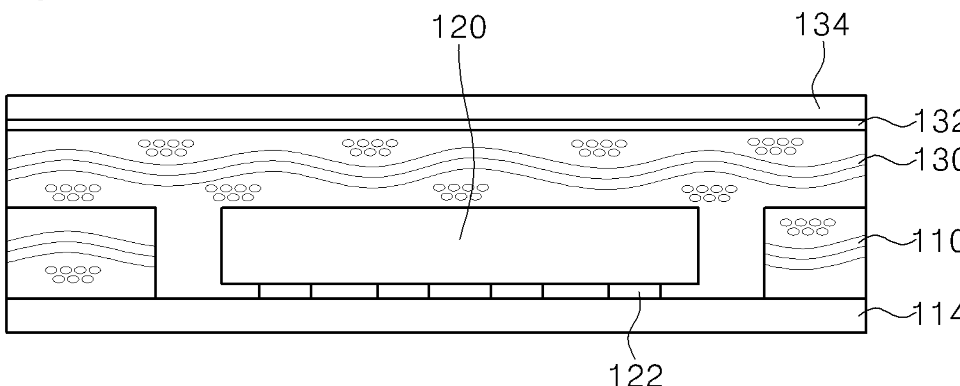
[Fig. 7]



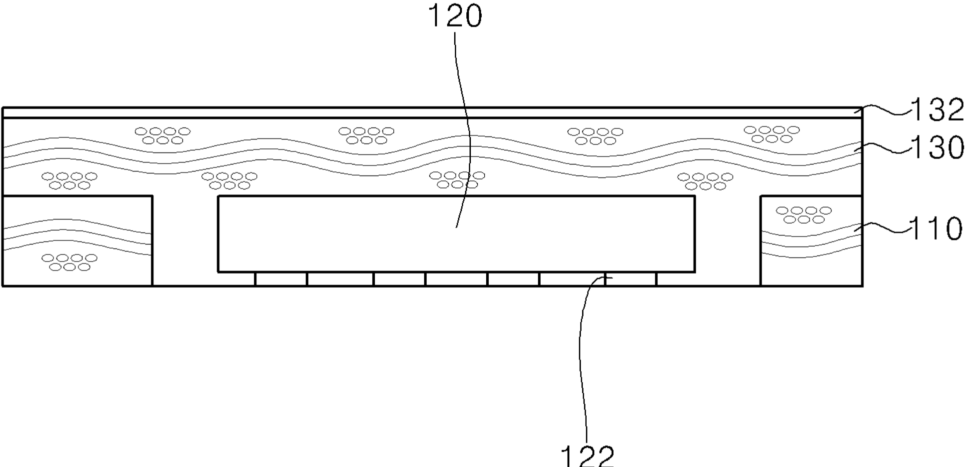
[Fig. 8]



[Fig. 9]



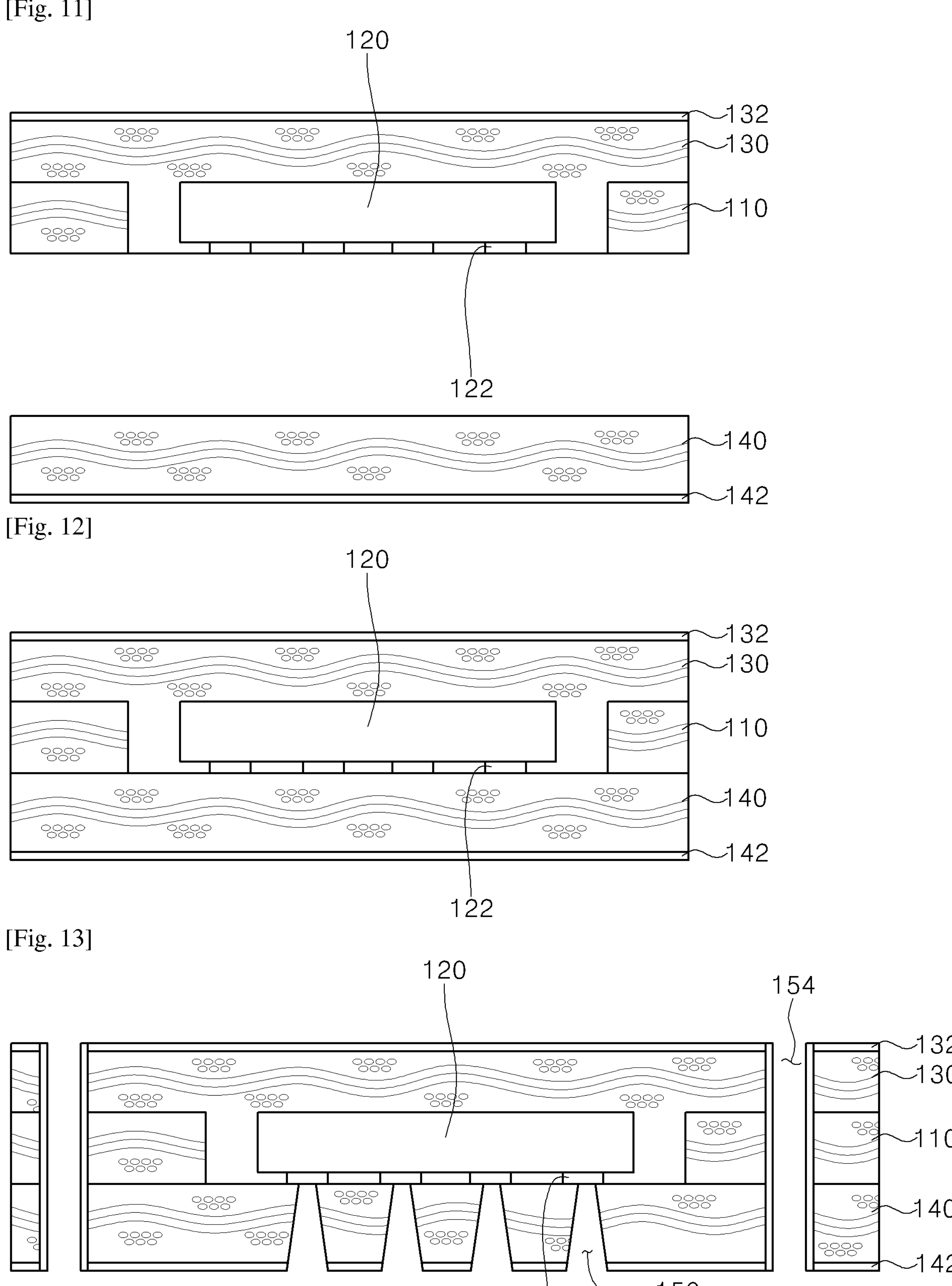
[Fig. 10]



[Fig. 11]

[Fig. 12]

[Fig. 13]



[Fig. 14]

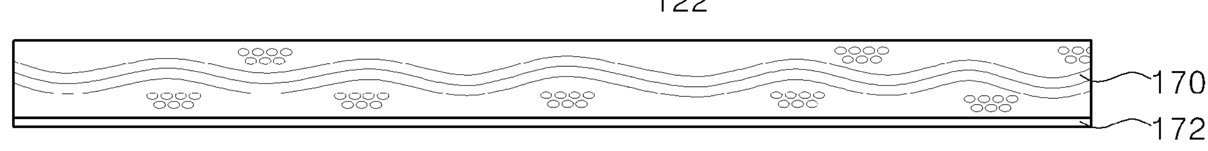
120
158
132
130
110
140
142
156
122

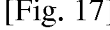
[Fig. 15]

120
158
136
130
110
140
144
156
122

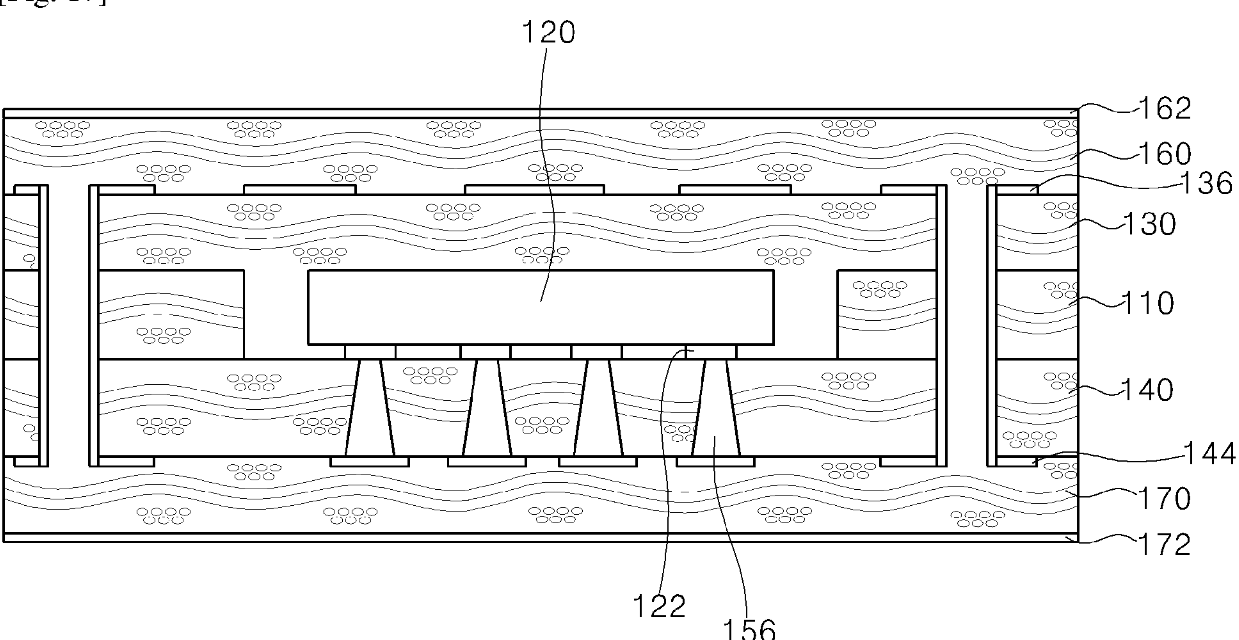
[Fig. 16]

162
160
120
158
136
130
110
140
144
156
122

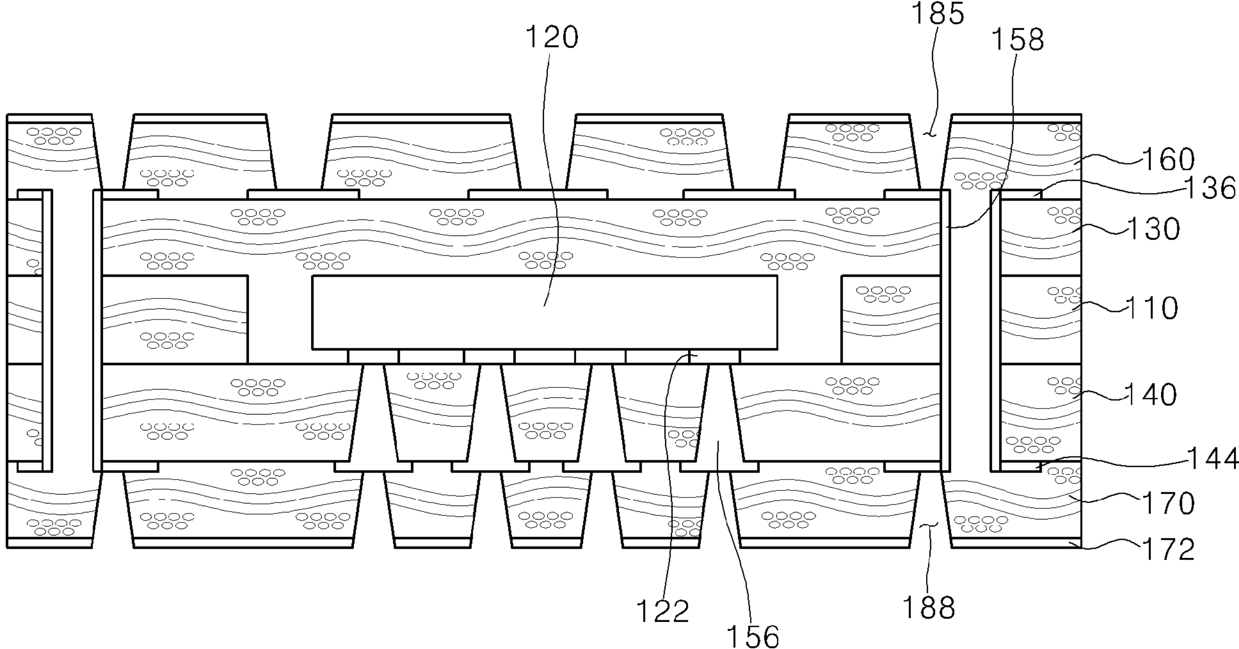


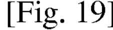


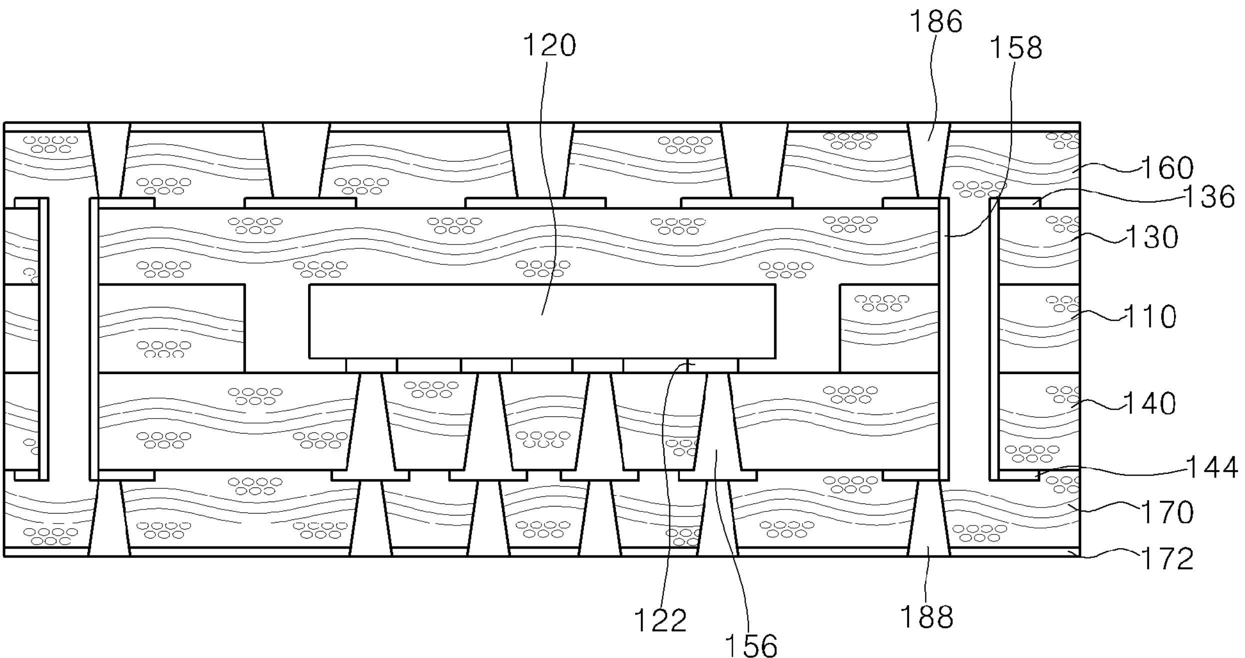
[Fig. 17]



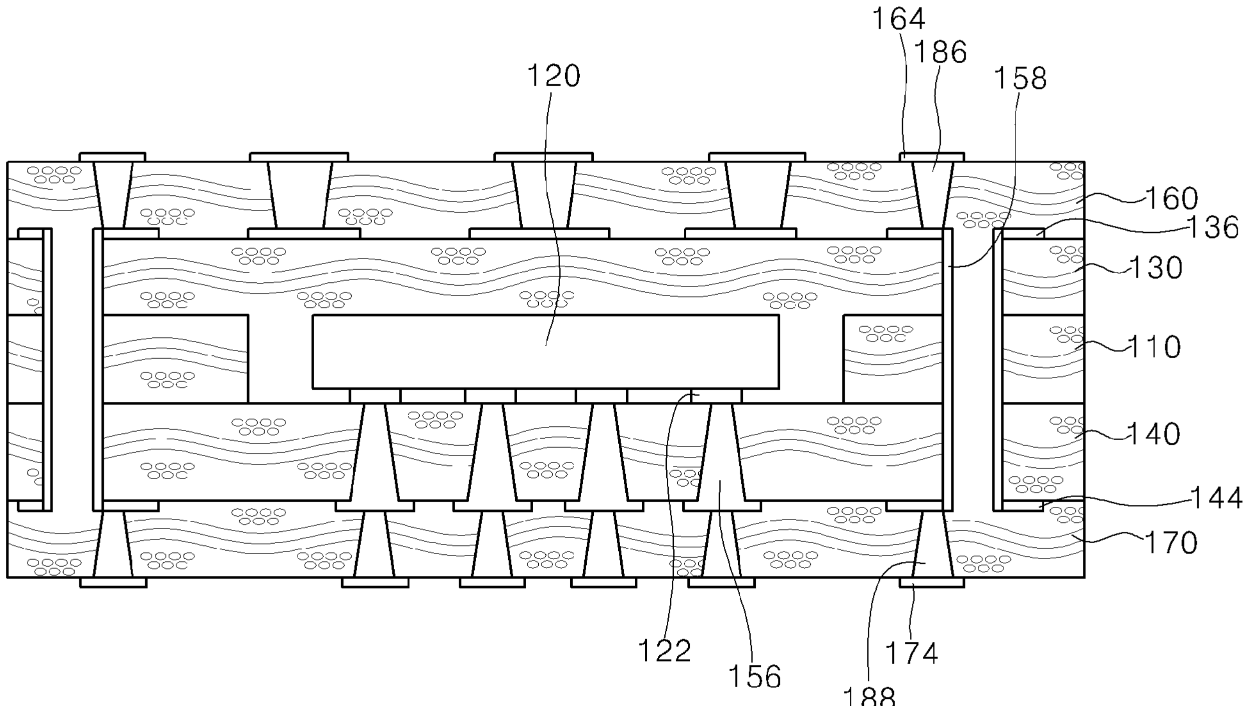
[Fig. 18]

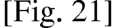



[Fig. 19]

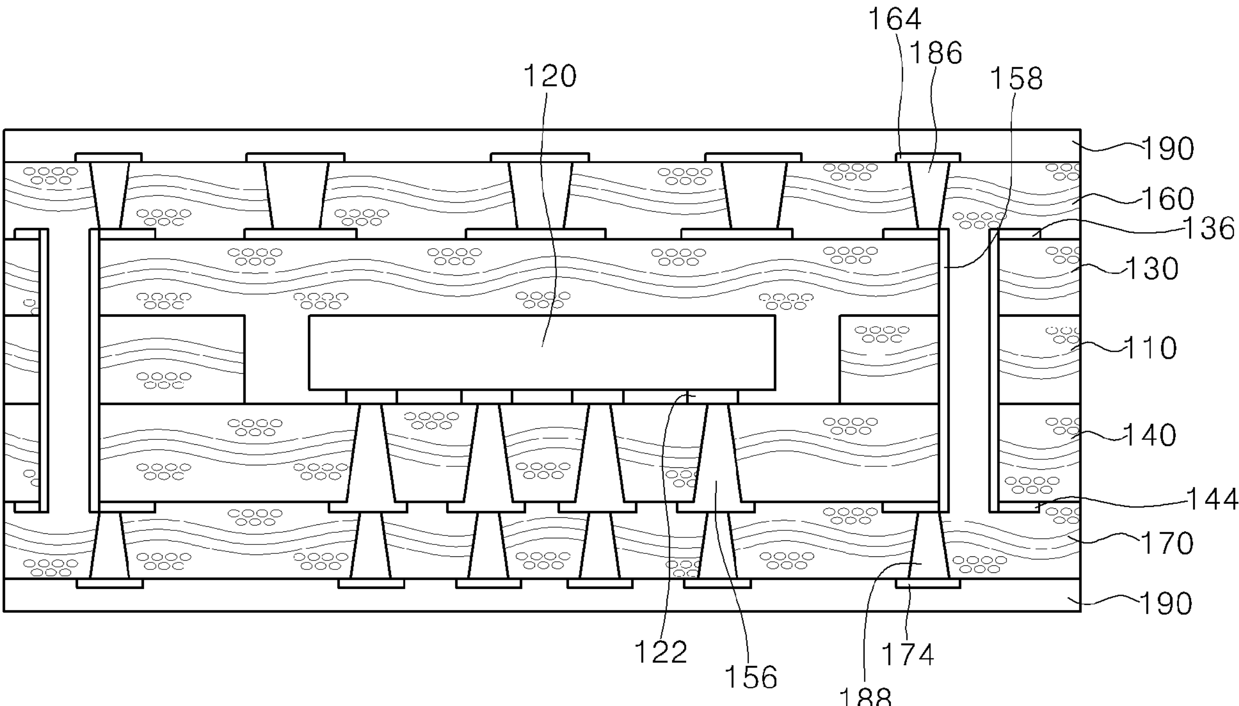


[Fig. 20]

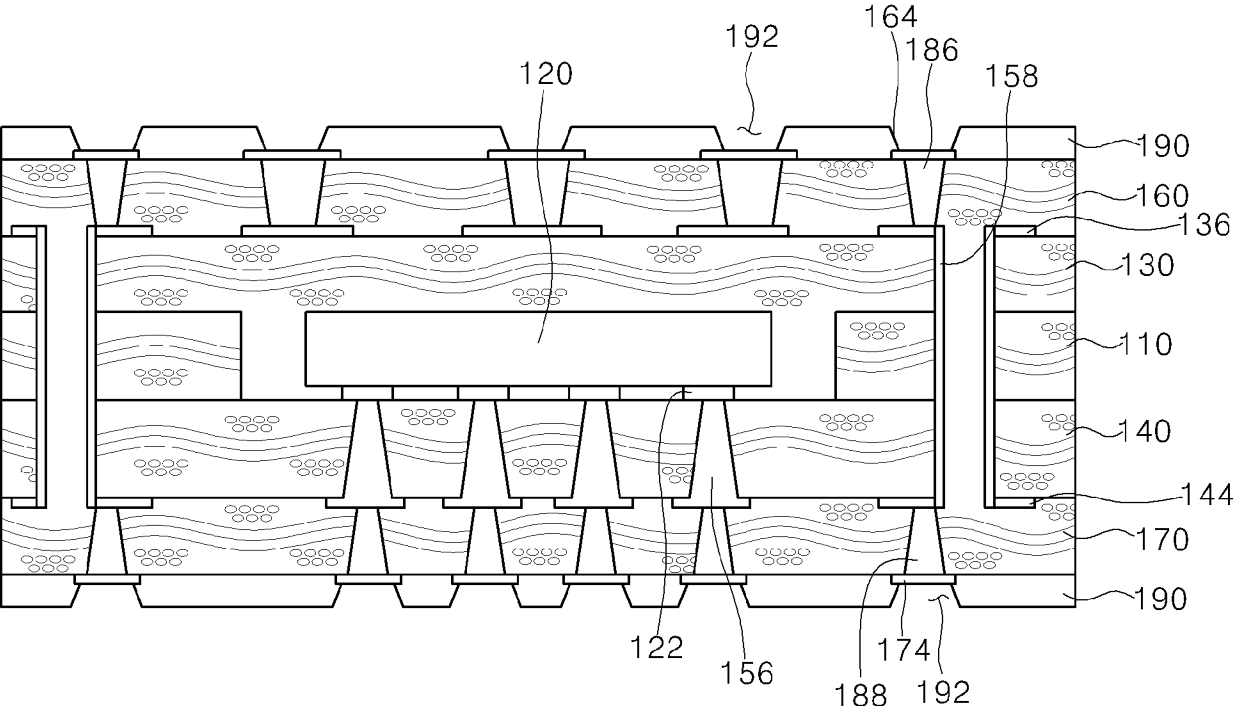




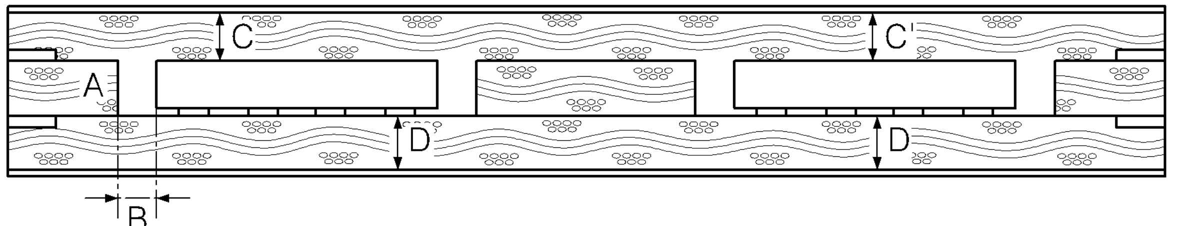
[Fig. 21]



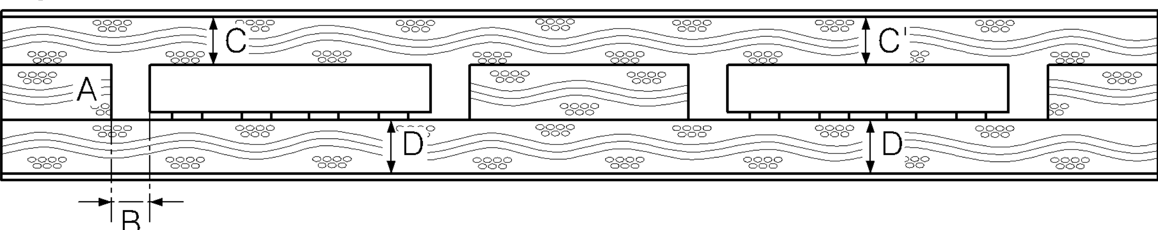
[Fig. 22]



[Fig. 23]



[Fig. 24]



PATENT COOPERATION TREATY

PCT

DECLARATION OF NON-ESTABLISHMENT OF INTERNATIONAL SEARCH REPORT
(PCT Article 17(2)(a), Rules 13*ter*.1(c) and (d) and 39)

Applicant's or agent's file reference OP-12613-PCT	**IMPORTANT DECLARATION**	Date of mailing (*day/month/year*) 27 August 2013 (27.08.2013)
International application No. **PCT/KR2013/004110**	International filing date (*day/month/year*) **09 May 2013 (09.05.2013)**	(Earlist) Priority date (*day/month/year*) 28 September 2012 (28.09.2012)
International Patent Classification (IPC) or both national classification and IPC ***H05K 3/46(2006.01)i, H05K 1/18(2006.01)i***		
Applicant **LG INNOTEK CO., LTD.**		

This International Searching Authority hereby declares, according to Article 17(2)(a), that **no international search report will be established** on the international application for the reasons indicated below.

1. ☐ The subject matter of the international application relates to:
   - a. ☐ scientific theories.
   - b. ☐ mathematical theories.
   - c. ☐ plant varieties.
   - d. ☐ animal varieties.
   - e. ☐ essentially biological processes for the production of plants and animals, other than microbiological processes and the products of such processes.
   - f. ☐ schemes, rules or methods of doing business.
   - g. ☐ schemes, rules or methods of performing purely mental acts.
   - h. ☐ schemes, rules or methods of playing games.
   - i. ☐ methods for treatment of the human body by surgery or therapy.
   - j. ☐ methods for treatment of the animal body by surgery or therapy.
   - k. ☐ diagnostic methods practised on the human or animal body.
   - l. ☐ mere presentation of information.
   - m. ☐ computer programs for which this International Searching Authority is not equipped to search prior art.
2. ☒ The failure of the following parts of the international application to comply with prescribed requirements prevents a meaningful search from being carried out:

   ☐ the description ☒ the claims ☐ the drawings
3. ☐ A meaningful search could not be carried out without the sequence listing; the applicant did not, within the prescribed time limit:
   - ☐ furnish a sequence listing on paper complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ furnish a sequence listing in electronic form complying with the standard provided for in Annex C of the Administrative Instructions, and such listing was not available to the International Searching Authority in a form and manner acceptable to it.
   - ☐ pay the required late furnishing fee for the furnishing of a sequence listing in response to an invitation under Rule 13ter.1(a) or (b)
4. Further coments:

Name and mailing address of ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. +82-42-472-7140	Authorized officer KIM Sang Keol Telephone No. +82-42-481-5742