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(54) **Title**: VARIATION RESISTANT METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

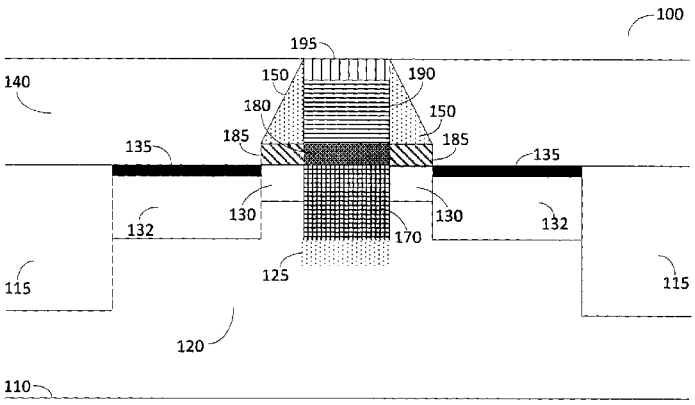

FIGURE 1

(57) **Abstract**: Variation resistant metal-oxide-semiconductor field effect transistors (MOSFET) are manufactured using a high-K, metal-gate 'channel-last' process. Between spacers formed over a well area having separate drain and source areas, a cavity is formed. Thereafter an ion implant step through the cavity results in a localized increase in well-doping directly beneath the cavity. The implant is activated by a microsecond annealing which causes minimum dopant diffusion. Within the cavity a recess into the well area is formed in which an active region is formed using an un-doped or lightly doped epitaxial layer. A high-K dielectric stack is formed over the lightly doped epitaxial layer, over which a metal gate is formed within the cavity boundaries. In one embodiment of the invention a cap of poly- silicon or amorphous silicon is added on top of the metal gate.

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VARIATION RESISTANT METAL-OXIDE-SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to the manufacturing of metal-oxide-semiconductor field effect transistors (MOSFETs), and more particularly to MOSFETs manufactured for reproducibility of threshold voltages among otherwise identical transistors.

2. Prior Art

Random variation in threshold voltage (σV_T) of metal-oxide semiconductor (MOS) field effect transistors (MOSFETs) with high-K (high dielectric constant) metal gate stack is caused by some dominant factors: (i) random dopant fluctuations (RDF) in the well and in the pocket implant regions underneath the gate, which, among other things, cause variations in depletion layer thickness; (ii) line edge roughness (LER) which causes random variation in the length of the gate electrode resulting from random variations in profile of the etched gate; and, (iii) metal gate granularity (MGG) which causes random variations in the local work function due to the grain structure of the gate material. There is a fourth source of variation, the random variations in the effective channel length, referred to as random extension fluctuations (RXF), arising from statistical variations in the position of the junction that separates the channel from either the source or the drain extensions. However, as MOSFETs become smaller, the effects of RDF, LER, and RXF increase and become major factors in determining σV_T. The first effect, RDF, has recently gained intense attention. The randomness in the position of the drain extension RXF has two principal sources: a) variations in the final position of implanted ions due to scattering; and, b) variations in the activation and positions of the source/drain extension ions as influenced by the activation and subsequent heat treatments.

It is well-known in the art that as MOSFETs move to finer and finer dimensions, variability of the threshold voltage σV_T seriously undermines the reproducibility of threshold voltages among otherwise identical transistors. This effect is inevitable, and it is

particularly severe in its impact on complimentary MOS (CMOS) static random access memories (SRAM), which use millions of near-minimum sized transistors. Development of ultra-thin silicon on insulator (SOI) structures, e.g., fully depleted SOI (FDSOI), and of three-dimensional transistors (FinFET and Tri-Gate), are largely motivated by a need to reduce the threshold spreads σV_T caused by RDF. This trend moves away from the more traditional bulk MOS manufacturing, adversely impacting costs and availability. A cross section 400 of a standard bulk MOSFET, formed in a gate-last process, is shown in Fig. 4. On a bulk 410 of one conductivity type, drain and source areas 420 of an opposite conductivity type are formed. A SiO_2 isolation layer 430 is formed over the entire MOSFET transistor, with openings for connections 470 to respective drain and source terminals. In the gate-last process of the MOSFET, the gate is formed by having spacers 440 formed above the SiO_2 layer. The SiO_2 is removed and typically replaced by a high-K dielectric stack 450 on top of which a metal gate 460 is formed. In certain embodiments the spacers are formed by repeating the deposition-and-etch process.

One method of addressing the RDF problem was described by Asenov et al. in the paper "Suppression of Random Dopant-Induced Threshold Voltage Fluctuations in Sub-0.1-μm MOSFETs with Epitaxial and δ-Doped Channels," IEEE Transactions on Electron Devices, Vol. 46, No. 8, August 1999, Pages 1718 -1724. This approach is consistent with bulk transistors, and does not have the same cost penalties associated with FinFETs and FDSOI. This scheme has three key components: a) placing a thin, approximately 10 nanometer (nm), minimally doped epitaxial layer immediately beneath the gate oxide; b) placing a thinner layer with a very high concentration of either acceptors for an NMOS device or donors for a PMOS device at the boundary of the thin epitaxial layer that is remote from the gate dielectric interface; and, c) incorporating a moderately heavily doped well layer beneath the un-doped epitaxial layer and the highly doped, thinner layer. Similar structures have been demonstrated by Fujita et al. as described in their paper "Advanced Channel Engineering Achieving Aggressive Reduction of V_T Variation for Ultra-Low-Power Applications", Electron Devices Meeting (IEDM), 2011 IEEE International, pp.32.3.1-32.3.4, 5-7 Dec. 2011. A cross section 500 of such an epitaxial transistor is shown in Fig. 5. The epitaxial layer 510 is deposited on the whole silicon wafer after the channel doping implantation through a sacrificial gate oxide and before the formation of the sacrificial polysilicon gate and the source drain regions 525. In some instances, such as

Hokazono, A., et al., in "25-nm Gate Length nMOSFET With Steep Channel Profiles Utilizing Carbon-Doped Silicon Layers (A P-Type Dopant Confinement Layer)", Electron Devices, IEEE Transactions on Electron Device, vol.58, no.5, pp.1302-1310, May 2011, carbon is introduced before the epitaxy to arrest the back diffusion of doping into the low-doped epitaxial region during the source/drain implantation activation. However this is an exceedingly difficult task, and experiment has shown that the profiles are degraded due to subsequent processing steps resulting in doping penetration into the low-doped epitaxial layer.

Recent changes to gate architectures from poly-silicon over silicon dioxide or oxynitride, to metal over high-K gate dielectric stack have changed the processing sequence. (A high-K or high dielectric constant as used herein and in the claims to follow means a dielectric constant that is higher than the dielectric constant of silicon dioxide (K = 3.9); an effective dielectric constant K exceeding 6 would be a preferred high K.) This is particularly true for the "gate last" process flow. In this process, while there is seemingly a complete transistor, with oxide and/or nitride sidewall spacers on each side of a poly gate, the gate is actually a sacrificial structure. That gate structure and the underlying protective oxide are etched away, exposing the silicon surface. Then a sequence of steps is employed: a) deposition of a high-K gate dielectric, typically by atomic layer deposition; b) deposition of a metal gate having a controlled work function to set the threshold voltage; and, c) deposition of a robust gate material, typically doped amorphous silicon. In many cases the sequence above is augmented by chemical-mechanical polishing steps to assure the localization of the various layers. However, this structure does not overcome the deficiencies resulting from RDF, LER or RXF. The morphology of the metal in the gate last process does reduce the variations identified as MGG, compared to a gate first process.

It would therefore be advantageous to find a solution compatible with bulk MOS manufacturing that would overcome deficiencies resulting from RDF, RXF and LER while generally maintaining the cost advantages and relative simplicity of standard bulk MOS manufacturing. It would be further advantageous if reductions of RDF, RXF, and LER are achieved simultaneously.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter that is regarded as the invention is particularly pointed out and distinctly claimed in the claims at the conclusion of the specification. The foregoing and other objects, features, and advantages of the invention will be apparent from the following detailed description taken in conjunction with the accompanying drawings.

Figure 1 is a schematic cross-section of a MOSFET manufactured in accordance with the principles of the invention.

Figure 2A is schematic cross-section showing a substrate with shallow trench isolation and a properly implanted core well according to an embodiment of the invention.

Figure 2B is a schematic cross-section showing a poly gate and drain/source implants according to an embodiment of the invention.

Figure 2C is a schematic cross-section showing a poly gate spacers and heavy drain/source implants according to an embodiment of the invention.

Figure 2D is a schematic cross-section showing poly gate and drain/source silicidation according to an embodiment of the invention.

Figure 2E is a schematic cross-section showing deposition of a first interlayer dielectric according to an embodiment of the invention.

Figure 2F is a schematic cross-section showing exposed poly gate after chemical/mechanical polish (CMP) according to an embodiment of the invention.

Figure 2G is a schematic cross-section showing a cavity formed by sacrificing the poly gate and an implant area implanted into the well thereunder according to an embodiment of the invention.

Figure 2H is a schematic cross section showing a channel recess formed into the buried layer of the well according to an embodiment of this invention.

Figure 2I is a schematic cross-section showing the highly-doped buried layer in the well and a lightly-doped channel epitaxial layer formed within the channel recess according to an embodiment of the invention.

Figure 2J is a schematic cross-section showing a high-K dielectric layer, a metal gate layer and an optional polysilicon cap formed within the cavity according to an embodiment of the invention.

Figure 2K is a schematic cross-section MOSFET transistor having a gate formed according to an embodiment of the invention.

Figure 3A is a diagram showing a conventional doping profile for short channel transistors.

Figure 3B is a diagram showing a doping profile realized in a channel-last process scheme according to an embodiment of the invention.

Figure 3C is a diagram showing ion implanted doping profiles for use in a channel-last process scheme according to an embodiment of the invention.

Figure 4 is a schematic cross section of a standard bulk MOSFET (prior art).

Figure 5 is a schematic cross section of an epitaxial channel MOSFET (prior art).

Figure 6 is a schematic cross section of a channel-last MOSFET further comprising a highly doped, implanted region according to an embodiment of this invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Variation resistant metal-oxide-semiconductor field effect transistors (MOSFET) are manufactured using a high-K, metal-gate 'channel-last' process. Between spacers formed over a well area having separate drain and source areas, a cavity is formed. Thereafter an ion implant step through the cavity results in localized increase in well-doping directly beneath the cavity. The implant is activated by a microsecond annealing which causes minimum dopant diffusion. Within the cavity a recess into the well area is formed in which an active region is formed using un-doped or lightly doped epitaxial layer. A high-K

dielectric stack is formed over the lightly doped epitaxial layer, over which a metal gate is formed within the cavity boundaries. In one embodiment of the invention a cap of poly-silicon or amorphous silicon is added on top of the metal gate.

According to the principles of the invention, incorporation into the manufacturing process a step of a very lightly doped, low temperature (such as 750°C or lower, preferably not exceeding 650 °C) epitaxial layer within a cavity formed for the purpose of creation a channel of a MOSFET that results in a "channel-last" process, reduces the diffusion of dopants from the heavily doped region beneath the low-doped epitaxial layer into the low-doped epitaxial layer. The low-doped epitaxial layer reduces the variations in the MOSFETs' threshold voltage arising from random doping fluctuations (RDF). The etching though the opening of the sacrificial poly silicon gate reduces the random channel length fluctuations that arise from variations in the lateral position of the edge of the drain and source extension implants, i. e., random extension fluctuations (RXF). The addition of a layer of increased doping beneath the low doped epitaxial layer reduces the short channel effects and the threshold voltage fluctuations related to line edge roughness (LER). It also offers a method of adjusting the threshold voltage to a desired value. In the descriptive paragraphs below, the heavily doped region will in fact be formed by ion implantation.

Reference is now made to Fig. 1 that depicts an exemplary and non-limiting schematic cross section of a MOSFET 100 manufactured in accordance with the principles of the invention. A well 120 is manufactured in a substrate 110, for example a silicon wafer, the well made of silicon or silicon-germanium, and typically doped to 10^{18} to 10^{19} ions per cm^3. The well may be a P-well or an N-well depending on the desired transistor type, N-channel or P-channel respectively. A silicon-oxide (SiO_2) or nitrided silicon dioxide layer 185 provides isolation in surface areas as required for proper operation of the MOSFET 100. Within the well area there are formed source and drain areas that are a combination of a low-doping area 130 and a high-doping area 132, each such source and drain area being separated from the other by a sacrificial polysilicon gate 195, though with some diffusion to extend each region slightly under the sacrificial polysilicon gate 195. Each highly doped area 132 has a silicide area 135, used to electrically connect to the source and drain of the formed MOSFET and to reduce the access resistance. Spacers 150, formed in a conventional manner over the low-doped source or drain area 130, are used to define the

gate region of the MOSFET, in a process that resembles a 'gate-last' process and as described herein below in greater detail. A shallow trench 115 separates adjacent transistors.

Within the cavity confined by the spacers 150, a recess is formed into the well 120 and a new active region is formed therein, and then completed consistent with the 'gate-last' manufacturing approach is formed therein. The final transistor structure is formed from several layers, the structure of which is unique to the invention. The processing sequence minimizes the thermal exposure of the very steep diffusion gradients implicit in this structure, ensures the low doping concentration in the epitaxial layer, and increases reproducibility of threshold voltages among otherwise identical transistors. In this embodiment, the active channel is comprised of a first highly doped buried layer 125 formed into the well essentially from the bottom of the cavity and into the well 120, and an epitaxial layer 170 that is either un-doped or lightly doped. The epitaxial layer 170 may be also referred to herein as the channel epitaxial layer 170. The highly doped buried layer 125 is doped to concentrations between $5x10^{18}$ ions/cm^3 to 10^{20} ions/cm^3. The lightly doped epitaxial layer has a doping density typically in the range of zero to 10^{17} ions/cm^3. The thickness of the buried layer 125 is typically between 1 nm and 100 nm, preferably 1 nano meter to 15 nanometers, while the channel epitaxial layer 170 has a thickness of 5 nm to 15 nm. Over the channel epitaxial layer 170 a high-K dielectric stack 180 is formed having a typical effective oxide thickness ranging between 0.5 nm and 3 nm. On top of the high-K dielectric stack 180 a metal gate 190 is formed having a typical thickness of 80 to 200 nm. In one embodiment of the invention a polysilicon cap 195 is added as a layer on top of the metal gate 190. A dielectric layer 140 is further used as part of this structure. It should be therefore understood that the invention covers, without limitation, both a full MOSFET structure 100 as described hereinabove as well as a channel region of a MOSFET that is comprised of the layers 125, 170, 180 and 190 and optionally layer 195. Incorporation of the buried layer 125 and particularly channel epitaxial layer 170 in addition with the 'gate-last' structure minimizes the thermal exposure of the very steep diffusion gradients implicit to this structure and hence increases reproducibility of threshold voltages among otherwise identical transistors. It should therefore be understood that the incorporation of layers 125 and 170 results in a "channel-last" MOSFET architecture that provides the benefits discussed herein over the prior art "gate-last" MOSFET architecture.

Figs. 2A through 2K demonstrate schematically the exemplary and non-limiting processing steps taken in order to achieve the 'channel-last' MOSFET with a channel comprising the two layers one formed by implantation into the well in the channel area and the other formed in a channel recess (also referred to herein as a recess) formed in the well. Fig. 2A shows a cross-section 200A where a substrate 110 is prepared by creating shallow trench isolation 115 and implanting an appropriate well 120 for a desired transistor. A SiO_2 or a nitrided SiO_2 layer 185 is formed over the entire surface, or in other embodiments on portions thereof, for at least electrical isolation purposes. Such a layer 185 could be of a typical thickness of 3.5 nanometers that may range between 2 nanometers and 8 nanometers, but not limited thereto. In Fig. 2B, cross-section 200B, the formation of a sacrificial poly gate 195 is shown, using appropriate manufacturing masks, for example by deposition and directional etching. Drain and source extension areas 130 are also formed as well as any other pocket implants (not shown) if and when necessary and/or applicable.

In Fig. 2C the cross-section 200C shows the spacers 150 that are created by deposition of nitride or a combination of nitride and oxide. Then anisotropic etching with vertical or tapered impact takes place. This selectively erodes the deposited sidewall material so the regions paralleling the wafer surface are removed, but vertical or tapered sections remain. In certain embodiments, the spacer is formed by repeating the deposition-and-etch process. After first deposition-and-etch step, the shallow drain/source extensions are formed by ion implantation, plasma immersion doping or a suitable process. Then, another deposition and etch step is carried out to space the drain/source from the channel. After the formation of the spacers 150, the heavily doped source and drain areas 132 can be implanted, typically using the spacers 150 as masks. In some cases (not shown), additional silicon or silicon/germanium may be deposited to elevate the top of the source and drain regions above the original silicon surface and to insert compressive strain in the p-channel MOSFET. Silicon/Germanium (Si:Ge) or Silicon/Carbon (Si:C) stressors, in some cases with a Σ shape, can also be embedded by partial etching of the source and drain regions and epitaxial regrowth of the stressors. In Fig. 2D the cross-section 200D shows the clearing of certain areas of the SiO_2 layer 185 to expose for example the drain and source areas 132. It should be noted that the anisotropic etch that forms the spacers 150 may also clear the protective oxide 185. Then a siliciding material is deposited to form a silicide layer 135 in the drain, source and poly areas. Silicidation material may include, but is not limited to

nickel, platinum or palladium, which reacts with the intended areas to form a conductive silicide on the gate 195 and the source and the drain areas 132. Fig. 2E shows a cross-section 200E where a first interlayer dielectric 140 is deposited where in Fig. 2F the cross-section 200F shows the result after chemical/mechanical polishing (CMP) of the first interlayer dielectric 140 up to the silicidation layer 135 of the poly gate 195. It should be noted that the silicide layer 135 on the poly gate 195 may or may not be lost by this step. In that regard, it should be noted that all values and ranges provided herein are exemplary only, and should not be considered as limiting the scope of the invention.

At this point of the process the gates that are to be manufactured using a 'channel-last' process are formed. This is achieved by first coating the area with a protective photoresist 810, and patterning the photoresist as shown in cross-section 200G of Fig. 2G. After patterning, the photoresist protects other devices that are not to be etched. Next, a self-aligned etching process is selected for its selectivity for the sacrificial gate material and its propensity not to etch the spacers 150 and other oxides in any significant manner (Fig. 2G). Then, a cavity 820 is formed in the area confined between the spacers 150 and which is not protected by the protective photoresist layer 810. Any remaining poly gate 195 is etched off as well all the way to the SiO_2 layer 185 that is within the cavity 820. Thereafter an implantation step takes place the peak of which is typically targeted to match the depth of the planned channel recess, typically ranging in depth of between, for example, 3 nanometers and 15 nanometers. The enhanced well doping is in the range of $5X10^{18}$ ions/cm^3 to 10^{20} ions/cm^3 and forms buried layer 125 that has a locally increased well doping, i.e., the implant has the same character, donors or acceptors, as that of the well. An activation annealing then takes place, the annealing conditions being constrained by the thermal tolerance of the silicide layers 135. A person of ordinary skill in the art would readily appreciate that Fig. 2G illustrates the use of protective dielectric 185 as a screen oxide for the ion implantation that forms the buried layer 125 of enhanced well doping; the use of a screen oxide being a common industry practice. However, in another embodiment of the invention the process design may be changed to remove the dielectric layer 185 prior to the implant. Such change of sequence should not be viewed as limiting upon the scope of the invention. It should be noted that the implant activation anneal must be completed before growing the un-doped or lightly doped channel epitaxial layer 170 discussed herein below with respect of Fig. 2I.

Fig. 2H shows a cross-section 200H depicting a channel recess 910 that is formed from within the cavity 820 into the highly implanted buried layer 125 of the well 120. This may be done by a processing step where the protective photoresist layer 810 is maintained. A self-aligned, selective etch process may be used to create a 5 to 25 nm recess into the silicon. A person of ordinary skill in the art would readily appreciate that an alternative process sequence might delay the implant that forms the buried layer 125 of enhanced well doping until after the recess 910 has been etched. Such change of sequence should not be viewed as limiting upon the scope of the invention. It should be noted that the implant activation anneal must be completed before growing the un-doped or lightly doped channel epitaxial layer 170 discussed herein below with respect of Fig. 2I. Generally the buried layer and the channel epitaxial layer will be of the same conductivity type as the well.

Fig. 2I depicts a cross section 200I of a lightly doped or un-doped channel epitaxial layer 170 grown over the locally enhanced well buried layer 125. This channel epitaxial layer 170 may be formed of silicon, but in certain instances it may be advantageous to grow the low-doped layer using some combination of silicon and germanium, or an alternate semiconducting material that is compatible with the underlying substrate. The thickness of the channel epitaxial layer 170 is controlled such that the top surface of channel epitaxial layer 170 is preferably, but not exclusively, in line with the silicon surface under the layer 185, although the surface of channel layer 170 may be slightly recessed with respect to the lower level of spacer 185. As shown in Figure 2I, the lower surface of layer 185 coincides with the upper level of channel epitaxial layer 170. The doping density of the enhanced doping buried layer 125 is chosen in combination with the un-doped channel epitaxial layer 170 thickness, the High-K gate stack thickness and the metal gate work function subsequently created to define the final, desired threshold voltage. The formation of channel layer 170 may be performed using atomic layer deposition, low temperature epitaxy or molecular beam epitaxy. Hence, the variation in σV_T, for a transistor manufactured at a 32 nm or finer process that would otherwise be in the range of 50-100 mV is reduced to the range of 20-40 mV when the invention is implemented for the same dimension process. As a result, a basically standard bulk MOS manufacturing process may be employed with the invention disclosed herein and without the need to resort to complex solutions suggested by prior art technologies.

A person of ordinary skill in the art would appreciate that the self-aligned etching step that forms recess 910, shown in Figure 2H, sacrifices any source extension ions or drain extension ions that may have diffused into the channel region. The positions of those ions reflect variations that arise from scattering events during ion implantation and/or from high temperature activation processes (900°C or higher). The formation of recess 910 eliminates those variations. The use of any one of several low-temperature processes to reconstitute the channel minimizes the movement of the source extension and drain extension ions, substantially eliminating their contribution to RXF. The etching of the overlap portion of the extensions improves the electrostatic integrity, improves the on current and reduces the overlap capacitances.

Representative doping profiles are illustrated in Figs. 3A through 3C, where the Z = 0 point is at the interface between the high-K dielectric stack 180 and the channel epitaxial layer 170. The region from Z = 0 to Z = 10 nm represents the nominal thickness of the channel epitaxial layer 170, for reference, taken at the midpoint between the source and drain regions. Fig. 3A shows a channel doping profile that is representative of normal transistor construction. In standard processes, there are multiple implants forming the wells and channel regions of the transistors. The Figure 3A profile is representative of the middle of the channel, with the combined effect of well implants, threshold voltage implants and pocket implants. The total well depth is typically 200 nm to 400 nm, but the Figures 3 all show the 75 nm lying closest to the gate. This region is normally highly doped with a shallow "threshold voltage" implant and pocket implants.

Fig. 3B shows the well profile of a simple channel last structure, in which highly doped region nearest the gate has been etched away and replaced with a very low-doped, perhaps un-doped epitaxial layer, illustrated here with a depth of 10 nanometers. Figure 3C shows a trio of representative doping profiles appropriate to the center of the channel where the well enhancing ions have been implanted and activated. The lowest profile, identified as 1E19 is the same as Fig. 3B, showing the normal well implant profiles. The curves 2E19 and 5E19 show enhanced well implants, implementing the formation of buried layer 125.

Following the steps of forming buried layer 125 and channel epitaxial layer 170, and as shown in Fig. 2J, cross-section 200J, a high-K dielectric stack 180 is formed in the cavity 820 over the second channel epitaxial layer 170. This stack may be expected to have an

effective dielectric constant K in excess of 6. The high-K dielectric stack 180 consists of a thin layer of SiO_2, typically 1 nm or less, capped by a layer of high K dielectric, usually incorporating an oxide or oxynitride of hafnium. All layers after the highly doped buried layer 125 should be formed using a low-temperature (not exceeding 900°C, preferably not exceeding 750°C, and more preferably not exceeding 650°C) deposition methods. If the present invention is used in an integrated circuit also containing transistors formed by other fabrication techniques, all layers after the highly doped buried layer 125, if used, should be formed after all high temperature operations for the entire integrated circuit have be performed. Thereafter the desired gate metal is deposited forming layer 190, where the gate metal is chosen primarily for its work function as well as for manufacturing considerations. Optionally, a manufacturing process may require a poly-silicon, or amorphous silicon, cap for protection. Fig. 2K shows cross-section 200K that depicts the structure after the removal of the excess high-K dielectric layer 180, metal layer 190 and poly layer 195, using for example CMP. Hereinafter processing may continue by, for example, adding a second dielectric layer (not shown) and thereafter continuing with additional processing steps including, but not limited to, forming metallization connectivity layers. For N and P type MOS transistors different types of metal gate are needed to incorporate work functions appropriate for the desired NMOS and PMOS threshold voltages.

Fig. 6 shows a schematic cross section 600 of a channel-last MOSFET according to another embodiment of the invention. Accordingly, the channel region is removed by selective etching between the spacers created by the spacers 440, as explained in further detail hereinabove. A layer 610 is a highly doped, resulting in a localized enhancement of the well implants, carried out either before or after the channel recess is formed and as further explained hereinabove. The region 610 doping must be activated prior to the selective epitaxial growth which creates a low-doped channel region 620. Subsequently the channel is sealed with a high-K dielectric insulator stack 450 and the gate material 460.

Hence it should be understood by those of ordinary skill in the art that an embodiment of the "channel-last" process comprises of the building of the MOSFET's channel in a recess of a cavity etched into the well area between a drain area and a source area of the MOSFET and over a locally enhanced doping area of the well. The channel may comprise of an un-doped or lightly doped epitaxial layer that is grown in the channel recess. Once the channel is created according to the principles of the invention the process is

completed similarly to the "gate-last" like processes. It should be further understood that while the process for a "channel-last" solution was described in a manner, where the implant for creation of an enhanced doping in the channel area is performed prior to the creation of the channel recess, other embodiments are possible, including without limitations the creation of the channel recess prior to performing the local enhancement of the doing of the well at the bottom of the channel recess. All such variations to the "channel-last" process should not be considered as departing from the scope of this invention and are hereby included therein.

The invention disclosed herein describes a general well which may be an N-well or a P-well, and hence suitable for a channel of a PMOS or NMOS transistor respectively. Further, the electrostatic characteristics of partially depleted SOI (silicon-on-insulator) transistors are sufficiently similar to bulk semiconductors that all the techniques described in this invention are equally applicable to partially depleted SOI devices. A person of ordinary skill-in-the-art would readily understand that the invention can be adapted for use in a plurality of ways, including integrated circuits where all transistors or a portion thereof are manufactured using the techniques disclosed hereinabove. Furthermore, although the invention is described herein with reference to the preferred embodiment, one skilled-in-the-art will readily appreciate that other applications may be substituted for those set forth herein without departing from the spirit and scope of the present invention. Accordingly, the invention should only be limited by the Claims included below.

CLAIMS

What is claimed is:

1. A method for manufacturing a metal-oxide-semiconductor field effect transistor (MOSFET) comprising:

forming a well region of a first conductivity type in a substrate;

forming a silicon oxide layer over at least a portion of the well region;

forming a poly gate in a first region of the well over the silicon oxide;

forming source and drain regions, the source region being formed in a second portion of the well region that is adjacent the first region, the drain region being formed in a third portion of the well region that is adjacent the first region and separate from the second region;

forming spacers on the silicon oxide at the sides of the poly gate;

clearing at least a portion of the silicon oxide layer;

forming a conductive layer over the poly gate and at least a part of the drain and the source regions;

forming a first interlayer dielectric over at least the first region, the second region and the third region;

polishing the interlayer dielectric to expose a top surface of the poly gate or the conductive layer over the poly gate;

sacrificing the poly gate and any remaining conductive layer over the poly gate to form a cavity between the spacers;

forming a buried layer and a recess therein by performing one of: a) clearing the part of the silicon oxide within the cavity, etching selectively the recess into the well within the cavity, and ion implanting a region at the bottom of the recess having a first doping level to form the buried layer, b) ion implanting into the well a region at the bottom of the cavity having a first doping level to form the buried layer, clearing the part of the silicon oxide within the cavity, and etching selectively a recess within the cavity into the buried layer, or, c) clearing the part of the silicon oxide within the cavity, ion implanting into the well a region at the bottom of the cavity having a first doping level to form the buried layer, and etching selectively a recess into the well within the buried layer;

forming a channel epitaxial layer in the recess, the channel epitaxial layer having a second doping level that is less than the first doping level;

forming a high-K dielectric stack over the channel epitaxial layer; and

forming a metal gate layer over the high-K dielectric layer.

2. The method of claim 1 further comprising:

activating the ion implantation region before forming the channel epitaxial layer.

3. The method of claim 2 wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes of less than 900°C.

4. The method of claim 2 wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes not exceeding 650°C.

5. The method of claim 4 wherein the MOSFET is part of an integrated circuit and wherein the integrated circuit is not subjected to a temperature exceeding 650°C after the channel epitaxial layer is formed.

6. The method of claim 1, wherein clearing the part of the silicon oxide within the cavity comprises removal of 2 nanometers to 8 nanometers of gate oxide.

7. The method of claim 1, wherein forming a conductive layer comprises:

depositing a siliciding material.

8. The method of claim 7, wherein the siliciding material is selected from at least one of: nickel, platinum, palladium.

9. The method of claim 1, wherein polishing the interlayer dielectric further comprises:

removing of the conductive layer of over the poly gate.

10. The method of claim 1, wherein polishing is performed using chemical mechanical polishing (CMP).

11. The method of claim 1, wherein etching selectively comprises removal of between 5 nanometers to 20 nanometers of the well material within the cavity.

12. The method of claim 1, wherein forming a channel epitaxial layer comprises using one of: atomic layer deposition, low-temperature epitaxy, molecular beam epitaxy.

13. The method of claim 1, wherein the channel epitaxial layer thickness is between 1 nanometer and 25 nanometers.

14. The method of claim 1, wherein the high-K dielectric stack is one of: a mixed oxide of Hafnium, a Hafnium oxynitride on a transitional silicon dioxide layer.

15. The method of claim 1, wherein effective oxide thickness of the high-K dielectric layer is between 0.5 nanometers and 3 nanometers.

16. The method of claim 1, wherein thickness of the metal gate layer is between 80 nanometers to 200 nanometers.

17. The method of claim 1, wherein the buried layer beneath the channel epitaxial layer has a thickness of between 1 nanometer and 15 nanometers.

18. The method of claim 1, wherein the buried layer remaining at the end of the method has an ion doping level between $5x10^{18}$ and 10^{21} ions per square centimeter.

19. The method of claim 1, wherein the channel epitaxial layer has a doping density between zero and 10^{17} doping ions per cubic centimeter.

20. The method of claim 1, further comprising:

forming a cap over the metal layer in the cavity.

21. The method of claim 20, wherein the cap is made of one of: poly-silicon, amorphous silicon.

22. A method of manufacture for a metal-oxide semiconductor field effect transistor (MOSFET), the method comprising:

forming a poly gate over a well and using the poly gate as a mask for forming source and drain regions;

forming spacers on the sides of the poly gate;

sacrificing the poly gate to form a cavity between the spacers;

etching selectively a recess into the well within the cavity;

implanting in the recess a buried layer having a first doping level and a first layer thickness; and

forming in the recess a channel epitaxial layer over the buried layer and having a second doping level and a second layer thickness, the buried layer having a higher dopant level than the channel epitaxial layer, the channel epitaxial layer touching the source and drain regions.

23. The method of claim 22, further comprising:

forming a high-K dielectric stack in the cavity over the channel epitaxial layer; and

forming a metal gate layer over the high-K dielectric stack in the cavity.

24. The method of claim 23, wherein thickness of the high-K dielectric layer is between 0.5 nanometers and 3 nanometers.

25. The method of claim 23, wherein thickness of the metal gate layer is between 40 nanometers and 200 nanometers.

26. The method of claim 22, wherein etching selectively comprises removal of between 5 nanometers and 20 nanometers of the well material within the cavity.

27. The method of claim 22, wherein forming channel layer comprises using one of: atomic layer deposition, low-temperature epitaxy, molecular beam epitaxy.

28. The method of claim 22, wherein the buried layer thickness is between 1 nanometer and 15 nanometers.

29. The method of claim 22, wherein the buried layer has a doping level between $5x10^{18}$ and 10^{20} doping ions per cubic centimeter.

30. The method of claim 22, wherein the channel epitaxial layer has an ion doping density between zero and 10^{17} doping ions per cubic centimeter.

31. The method of claim 22, wherein the channel epitaxial layer thickness is between 1 nanometer and 25 nanometers.

32. The method of claim 22, wherein the high-K dielectric is one of: a mixed oxide of Hafnium, a Hafnium oxynitride on a transitional silicon dioxide layer.

33. The method of claim 22, further comprising:
forming a cap over the metal layer in the cavity.

34. The method of claim 33, wherein the cap is made of one of: poly-silicon, amorphous silicon.

35. The method of claim 22, wherein the implantation is activated before forming the channel epitaxial layer.

36. The method of claim 22, wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes not exceeding 900°C.

37. The method of claim 22, wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes not exceeding 650°C.

38. The method of claim 37, wherein the MOSFET is part of an integrated circuit and wherein the integrated circuit is not subjected to a temperature exceeding 900°C after the channel epitaxial layer is formed.

39. The method of claim 22, wherein the ion implantation is done before etching selectively a recess into the well within the cavity, then the etching selectively the recess into the well is limited in depth to leave the buried layer of the ion implanted well.

40. The method of claim 22, wherein the ion implantation is done after etching selectively a recess into the well within the cavity.

41. A method of manufacture for a metal-oxide semiconductor field effect transistor (MOSFET), the method comprising:

forming a poly gate over a well and using the poly gate as a mask for forming source and drain regions;

forming spacers on the sides of the poly gate;

sacrificing the poly gate to form a cavity between the spacers;

implanting in the cavity a buried layer having a first doping level and a first layer thickness;

etching selectively a recess into the well within the cavity; and

forming in the recess a channel epitaxial layer over the buried layer and having a second doping level and a second layer thickness, the buried layer having a higher dopant level than the channel epitaxial layer, the channel epitaxial layer touching the source and drain regions.

42. The method of claim 41, further comprising:

forming a high-K dielectric stack in the cavity over the channel epitaxial layer; and

forming a metal gate layer over the high-K dielectric stack in the cavity.

43. The method of claim 42, wherein thickness of the high-K dielectric layer is between 0.5 nanometers and 3 nanometers.

44. The method of claim 42, wherein thickness of the metal gate layer is between 40 nanometers and 200 nanometers.

45. The method of claim 41, wherein etching selectively comprises removal of between 5 nanometers and 20 nanometers of the well material within the cavity.

46. The method of claim 41, wherein forming channel layer comprises using one of: atomic layer deposition, low-temperature epitaxy, molecular beam epitaxy.

47. The method of claim 41, wherein the buried layer thickness is 0.3 nanometers and 15 nanometers.

48. The method of claim 41, wherein the buried layer has a doping level between $5x10^{18}$ and 10^{20} doping ions per cubic centimeter.

49. The method of claim 41, wherein the channel epitaxial layer has an ion doping density between zero and 10^{17} doping ions per cubic centimeter.

50. The method of claim 41, wherein the channel epitaxial layer thickness is between 1 nanometer and 25 nanometers.

51. The method of claim 41, wherein the high-K dielectric is one of: a mixed oxide of Hafnium, a Hafnium oxynitride on a transitional silicon dioxide layer.

52. The method of claim 41, further comprising:
forming a cap over the metal layer in the cavity.

53. The method of claim 52, wherein the cap is made of one of: poly-silicon, amorphous silicon.

54. The method of claim 41, wherein the implantation is activated before forming the channel epitaxial layer.

55. The method of claim 41, wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes not exceeding 900°C.

56. The method of claim 41, wherein the channel epitaxial layer, the high-K dielectric stack and the metal gate layer are all formed using processes not exceeding 650°C.

57. The method of claim 41, wherein the MOSFET is part of an integrated circuit and wherein the integrated circuit is not subjected to a temperature exceeding 900°C after the channel epitaxial layer is formed.

58. The method of claim 41, wherein the ion implantation is done before etching selectively a recess into the well within the cavity, then the etching selectively the recess into the well is limited in depth to leave the buried layer of the ion implanted well.

59. The method of claim 41, wherein the ion implantation is done after etching selectively a recess into the well within the cavity.

60. A metal-oxide-semiconductor field effect transistor (MOSFET) comprising:

a well formed over a substrate;

a drain region;

a source region separate from the drain region, the source and drain regions being formed in the top of the well;

a recess formed in the well and extending through an edge of each of the source and drain regions;

a buried layer formed below the recess into the well;

a channel epitaxial layer formed in the recess and touching the source and drain regions the channel epitaxial layer;

a high-K dielectric stack formed over the channel epitaxial layer; and

a metal gate layer formed over the high-K dielectric stack.

61. The MOSFET of claim 60, wherein the edge of each of the source and drain regions are respective source extension region and drain extension region of the source and the drain of the MOSFET.

62. The MOSFET of claim 60, wherein the buried layer has a doping level between $5x10^{18}$ and 10^{20} doping ions per cubic centimeter.

63. The MOSFET of claim 60, wherein the channel epitaxial layer has an ion doping density between zero and 10^{17} doping ions per cubic centimeter.

64. The MOSFET of claim 60, wherein the high-K dielectric is one of: a mixed oxide of Hafnium, a Hafnium oxynitride on a transitional silicon dioxide layer.

65. The MOSFET of claim 60, further comprising:

a cap over the metal layer.

66. The MOSFET of claim 65, wherein the cap is made of one of: poly-silicon, amorphous silicon.

67. The MOSFET of claim 60, wherein thickness of the high-K dielectric layer is between 0.5 nanometers and 3 nanometers.

68. The MOSFET of claim 60, wherein thickness of the metal gate layer is between 40 nanometers and 200 nanometers.

69. The MOSFET of claim 60, wherein the buried layer thickness is between 1 nanometer and 15 nanometers.

70. The MOSFET of claim 60, wherein the channel epitaxial layer thickness is between 1 nanometer and 25 nanometers.

71. A method of manufacture for a metal-oxide semiconductor field effect transistor (MOSFET), the method comprising:

forming a poly gate over a well and using the poly gate as a mask for forming source and drain regions;

forming spacers on the sides of the poly gate;

sacrificing the poly gate to form a cavity between the spacers;

etching selectively a recess into the well within the cavity;

implanting a buried layer at the bottom of the recess

forming in the recess a channel epitaxial layer over the buried layer;

forming a dielectric layer over the epitaxial layer; and

forming a gate layer over the dielectric layer.

72. The method of claim 71, wherein the buried layer has a higher doping level than a doping level of the channel epitaxial layer.

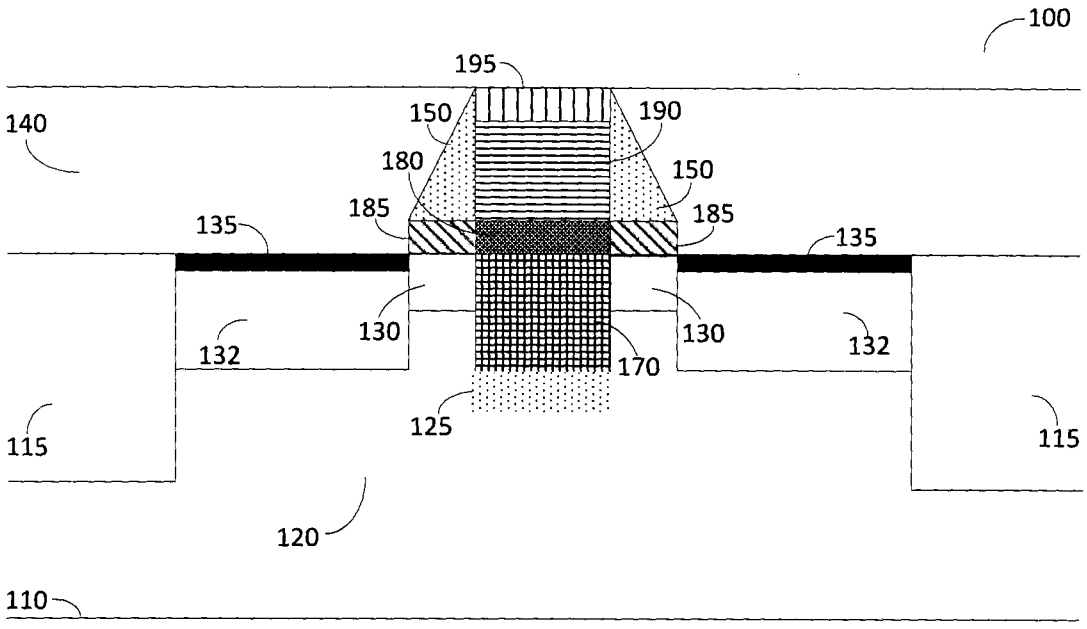

FIGURE 1

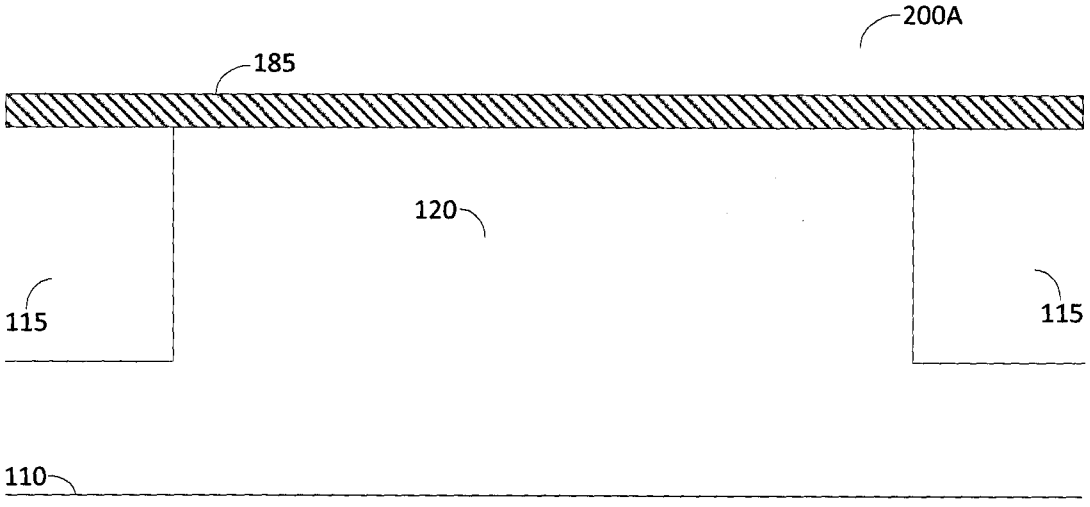

FIGURE 2A

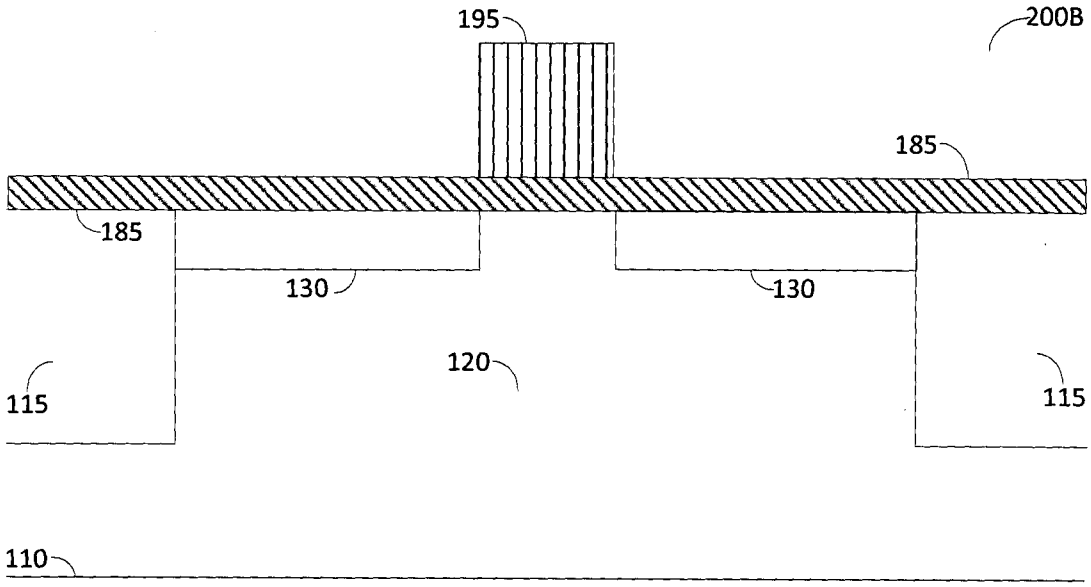

FIGURE 2B

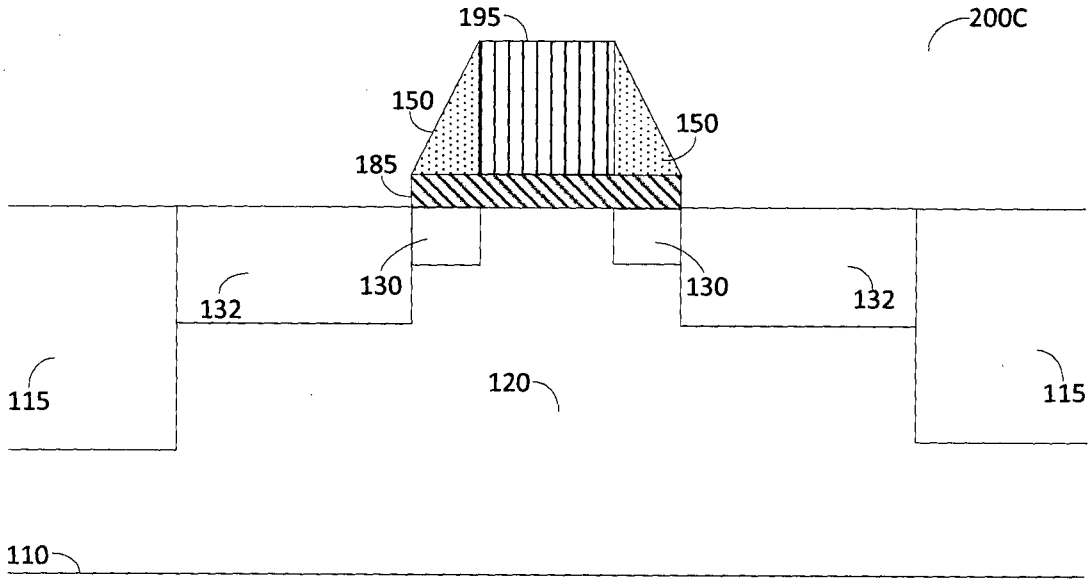

FIGURE 2C

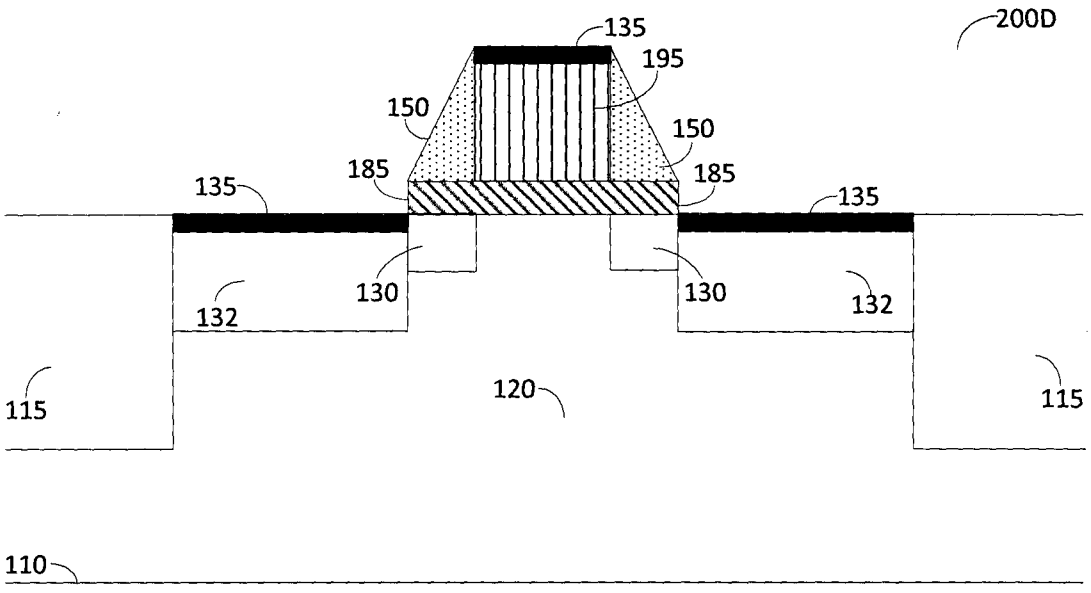

FIGURE 2D

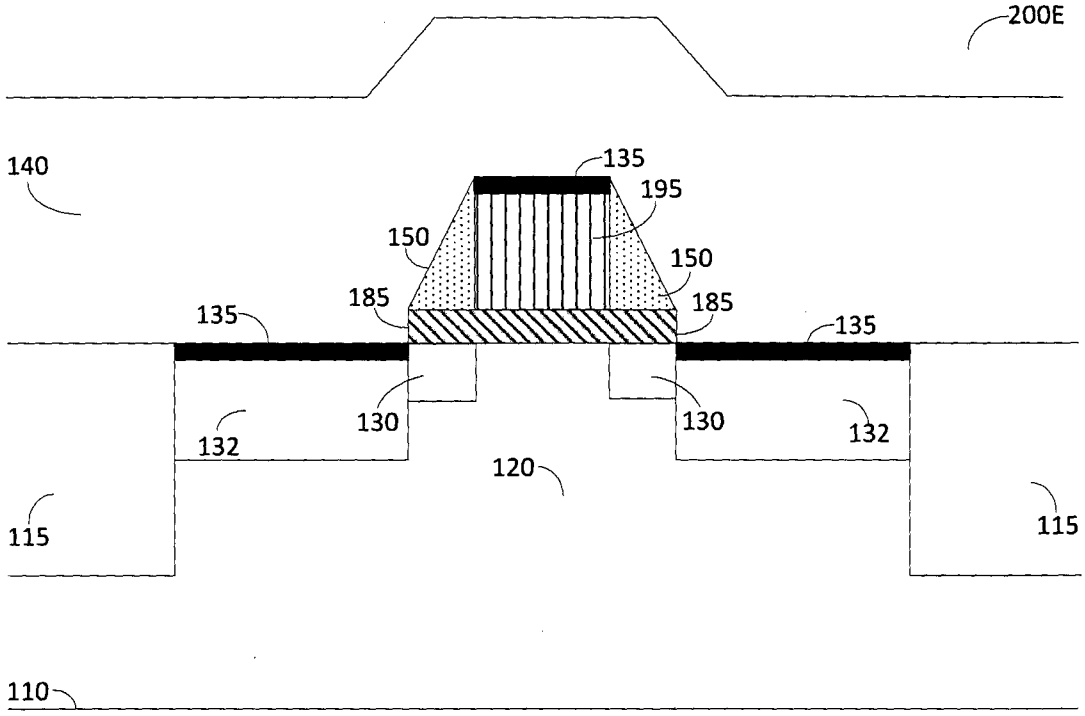

FIGURE 2E

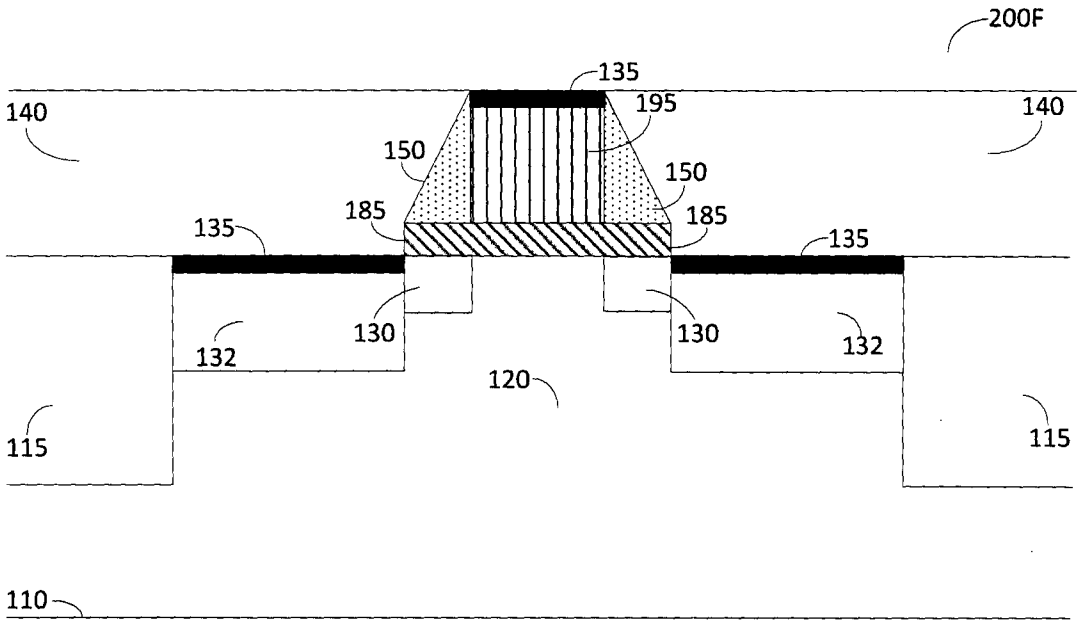

FIGURE 2F

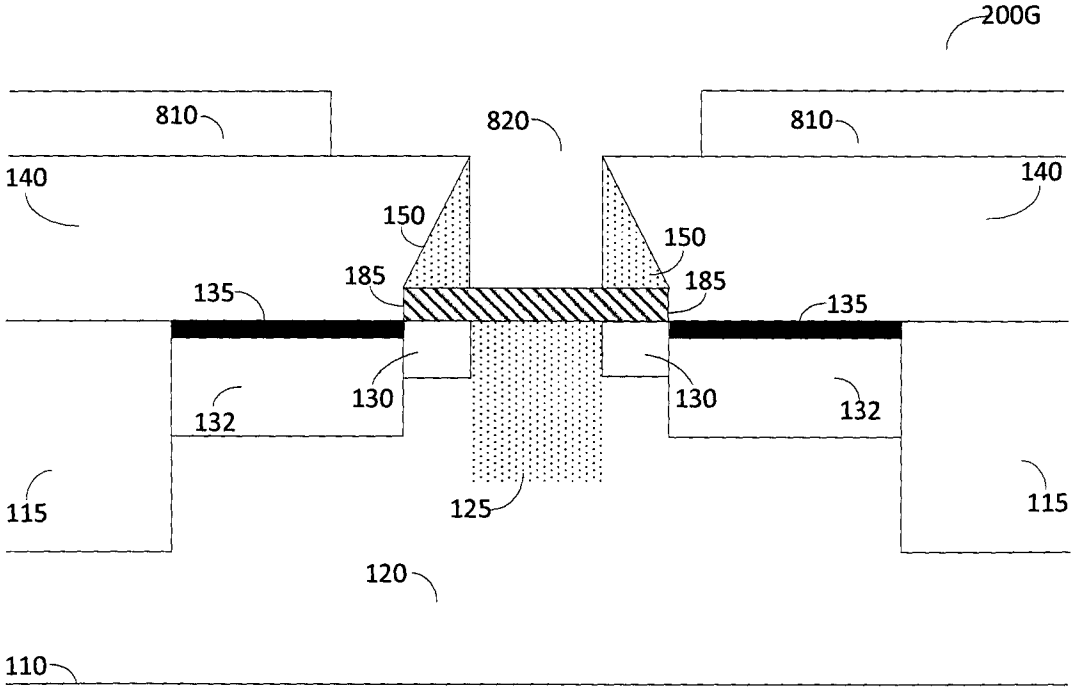

FIGURE 2G

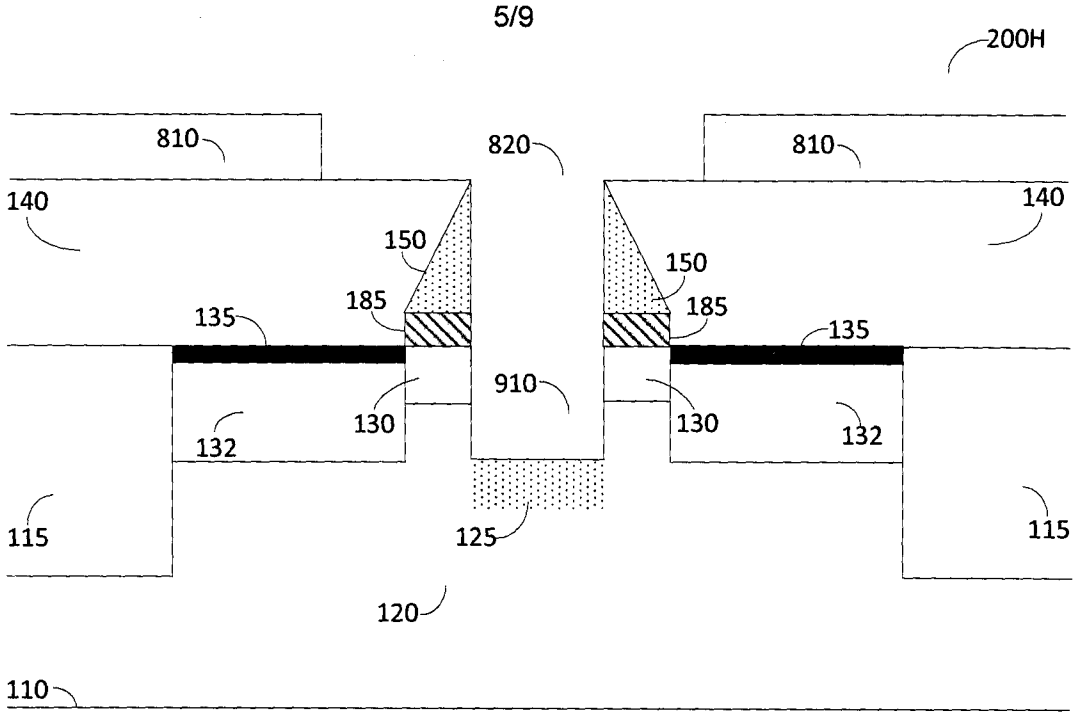

FIGURE 2H

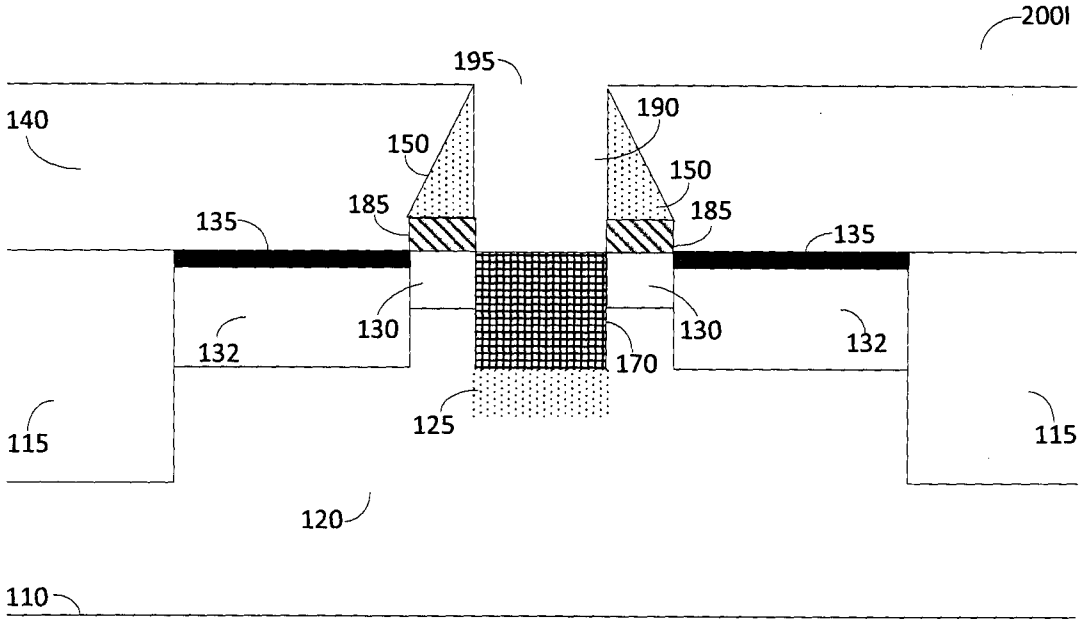

FIGURE 2I

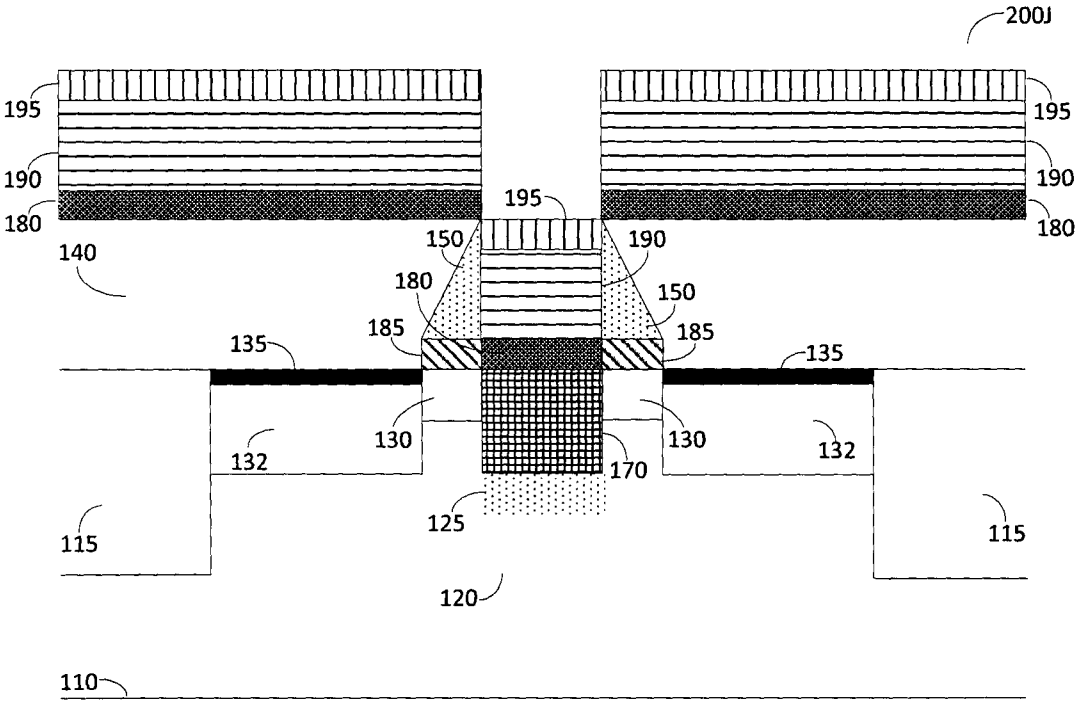

FIGURE 2J

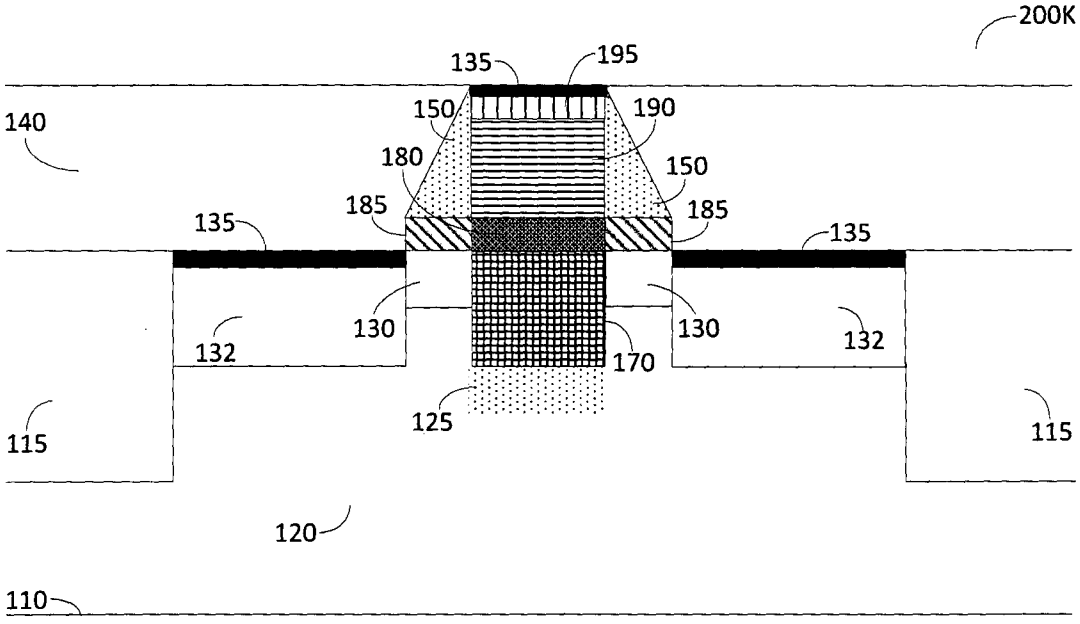

FIGURE 2K

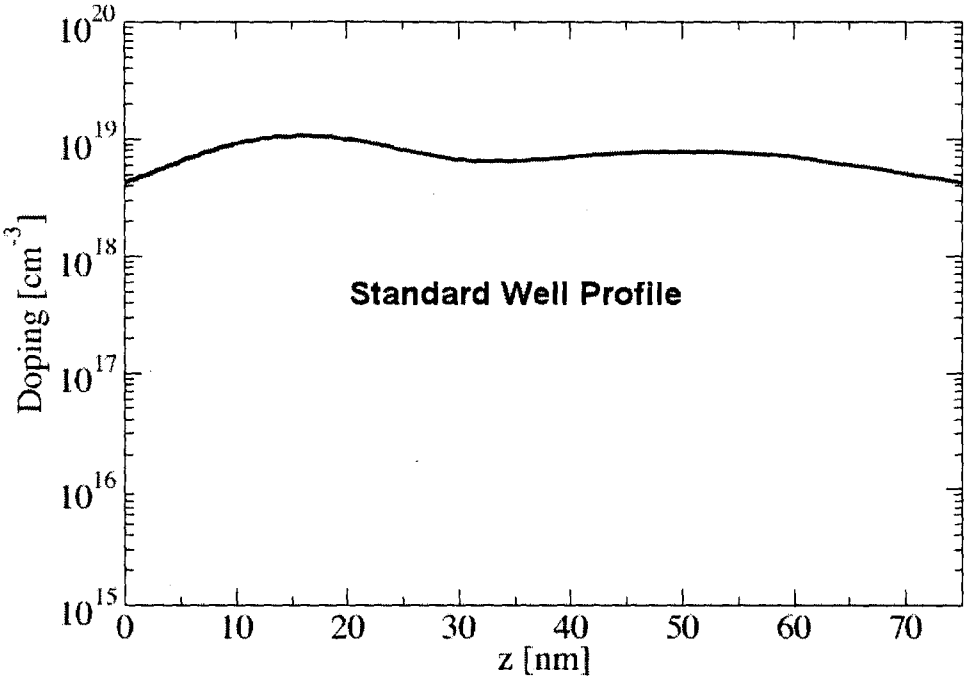

FIGURE 3A

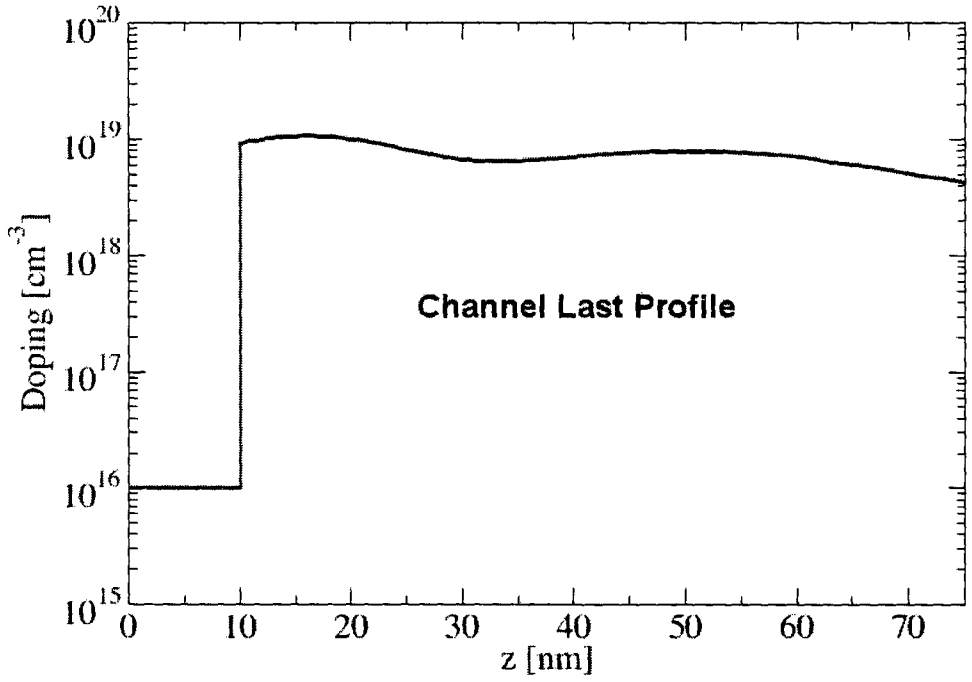

FIGURE 3B

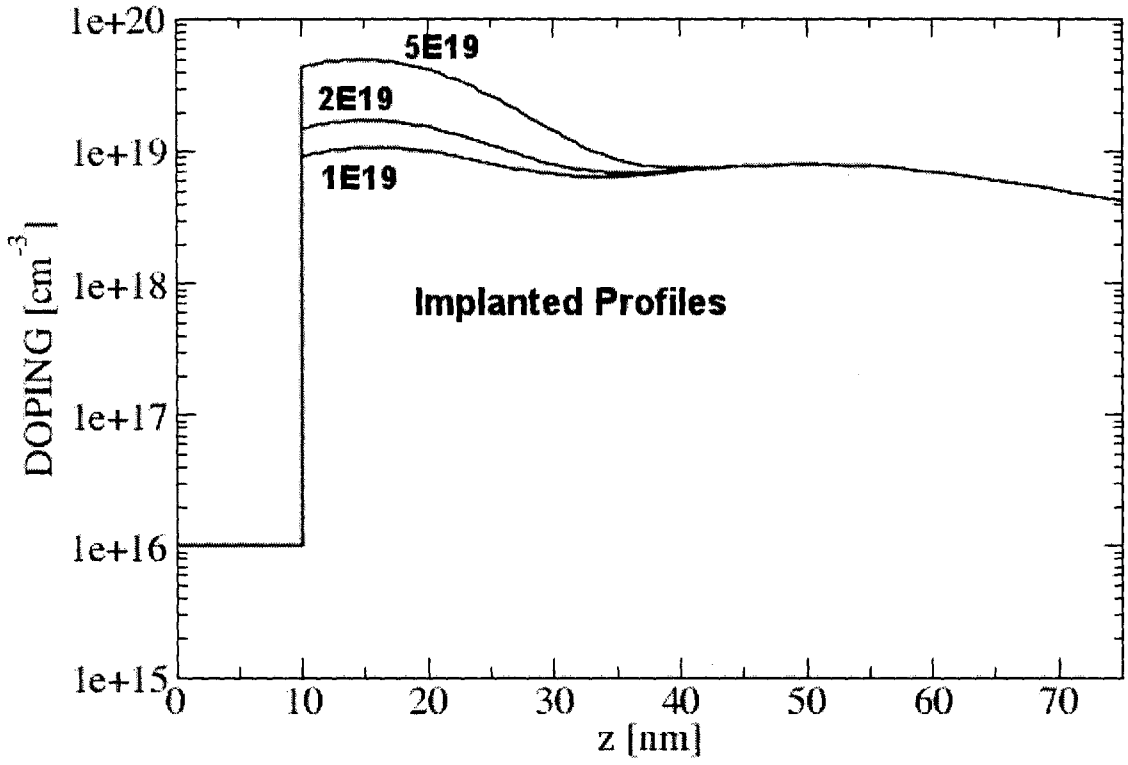
1e+20
1e+19
1e+18
1e+17
1e+16
1e+15
DOPING [cm^{-3}]
5E19
2E19
1E19
Implanted Profiles
0
10
20
30
40
50
60
70
z [nm]

FIGURE 3C

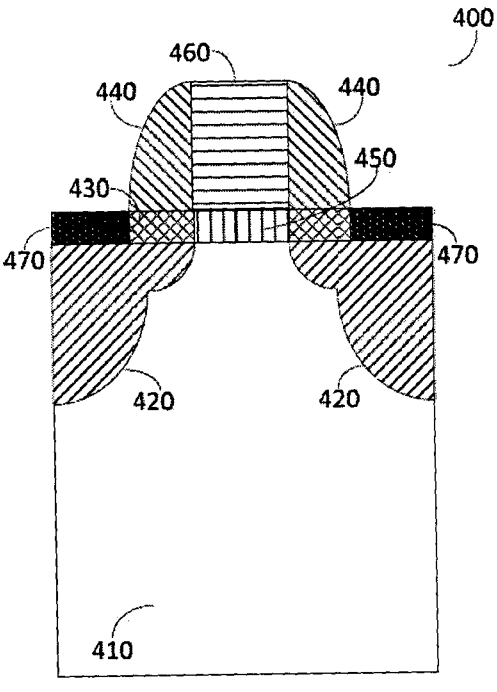

FIGURE 4 (PRIOR ART)

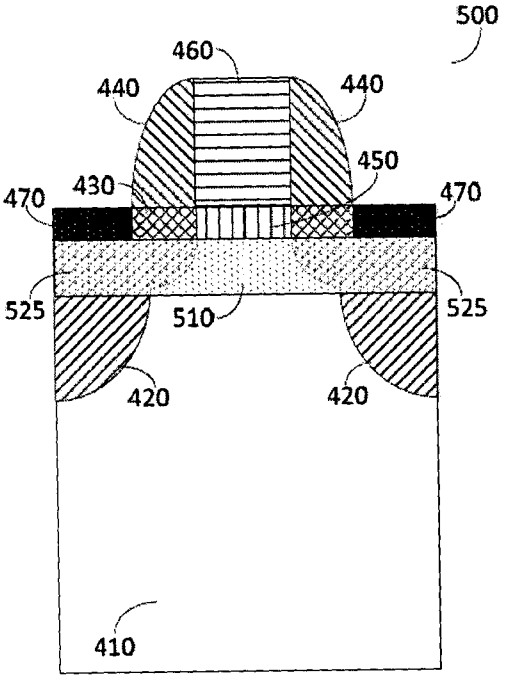

FIGURE 5 (PRIOR ART)

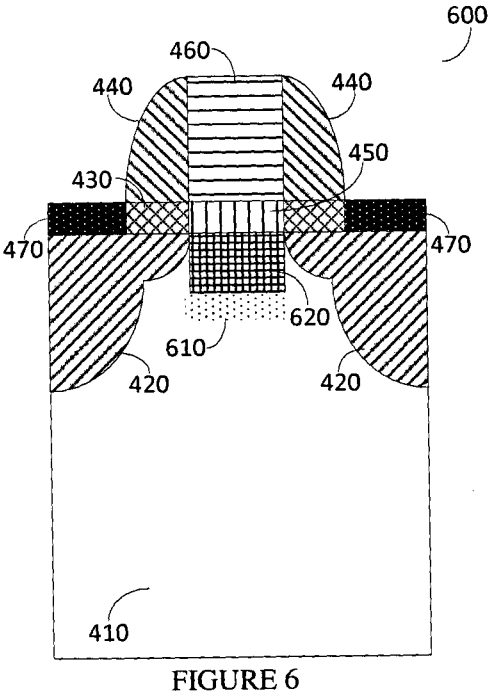

FIGURE 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2012/001069

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/10 H01L29/78 H01L29/51 H01L29/66
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/001930 A1 (LEE JUNG HO [KR]) 3 January 2002 (2002-01-03) paragraphs [0021] - [0034]; figures 2A-2F	1-40, 60-72
X	US 2002/037619 A1 (SUGIHARA KOHEI [JP] ET AL) 28 March 2002 (2002-03-28) paragraphs [0099] - [0135]; figures 1-15	1-21, 41-70
A	US 2001/009292 A1 (NISHINOHARA KAZUMI [JP] ET AL) 26 July 2001 (2001-07-26) figure 28D 28E	1
A	US 6 630 710 B1 (AUGUSTO CARLOS [US]) 7 October 2003 (2003-10-07) figures 10-20	1,7

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 October 2012	09/11/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Götz, Andreas

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2012/001069

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 6630710 B1	07-10-2003
		WO 0019510 A2	06-04-2000