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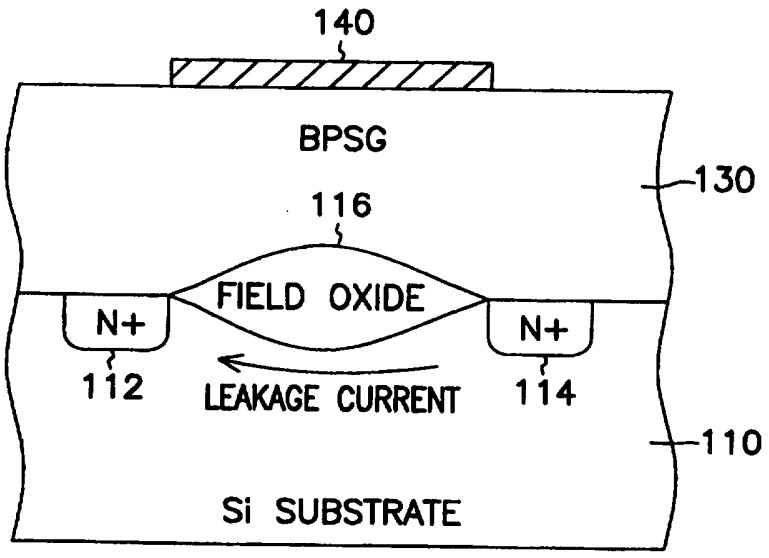
(54) Title: REDUCING FIXED CHARGE IN SEMICONDUCTOR DEVICE LAYERS



(57) Abstract

The fixed charge in a borophosphosilicate glass insulating film deposited on a semiconductor device is reduced by reacting an organic precursor such as TEOS with O_3. When done at temperatures higher than approximately 480 degrees C, the carbon level in the resulting film appears to be reduced, resulting in a higher threshold voltage for field transistor devices.

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REDUCING FIXED CHARGE IN SEMICONDUCTOR DEVICE LAYERS

Field of the Invention

The present invention relates to methods and apparatus for manufacturing semiconductor devices, and in particular to reducing the fixed charge in insulative layers on such devices.

Background of the Invention

Field effect transistors (FETs) are formed on silicon, or similar semiconductor substrates. A field effect transistor is usually formed with active areas such as two heavily doped, spaced apart regions of silicon, which are called a source and a drain. A gate structure is formed between the source and the drain, and operates to control the amount of electrical current which flows between them. When appropriate voltage is applied to the gate, an electrically conductive channel is formed under the gate, allowing current flow between the source and the drain. Active areas of adjacent transistors may be isolated from each other by the formation of a field oxide layer which acts as an insulator.

Part of the process of forming transistors involves the application of various layers of material. One such layer is utilized as an insulating layer between the gate and metal interconnects. Silane based layers have been used in the past, but do not fill tight spaces very well. Tetraethyloxysilicate (TEOS) based borophosphosilicate glass (BPSG) film layers using TEOS is a silicon containing source gas which has also been used. Doping TEOS with boron and phosphorus through the addition of triethylborane (TEB) and triethylphosphate (TEPO) respectively, increases the film's ability to reflow and fill in tight spaces. Such BPSG layers, however, have been plagued with unacceptable fixed electrical charge, thus being unsuitable for use in semiconductor devices. This is characteristic of both plasma and non-plasma TEOS based BPSG deposition. However, due to the material's superior abilities to reflow at low temperatures and getter mobile species, it is highly desirable to adapt this material for use in

semiconductor devices, particularly those employing certain silicide technologies which require lower temperatures to avoid agglomeration, such as those using titanium silicide.

Such layers are used as insulators between conductive layers. Excess fixed charge has an undesirable effect on adjacent layers. Excessive fixed charge for example can cause the silicon surface to invert under the field oxide, resulting in an undesirable channel for current to flow between two active areas that are isolated by the field oxide. This channel has a charge opposite to that of the substrate, which is also depleted of charge carriers in the region surrounding the inversion region. Thus, the excessive fixed charge creates or quickens the formation of the channel through which current flows, at undesired times. Excessive fixed charge also causes threshold voltage degradation in field transistors, causing premature and excessive leakage, in both n-type and p-type channel devices. The threshold voltage is the minimum voltage that must be applied for a current to flow in the channel between active regions. In semiconductor field transistor devices, it is paramount that the threshold voltage be maintained above a certain level to reduce leakage current between active regions.

There is a need to bring this fixed charge down to levels that do not induce a channel to form between active regions of field transistors formed in semiconductor substrates. There is also a need to provide an insulative layer having good reflow capabilities at low temperatures and which exhibit a low fixed charge.

Summary of the Invention

An insulative film layer such as borophosphosilicate glass (BPSG) is deposited on a semiconductor device by reacting Tetraethyloxysilicate (TEOS) with ozone (O_3). O_3 is formed in a corona discharge tube by flowing O_2 such that the O_3 concentration in O_2 is between approximately 2-20% by weight. Triethylphosphate (TEPO) and triethylborane (TEB) are organometallics used to dope the film with phosphorous and boron respectively. The BPSG is deposited at pressures of approximately 10 Torr to 760 Torr or atmospheric pressure. The

temperature of the BPSG layer is higher than approximately 480 degrees C. This provides a low fixed charge film of BPSG which reflows well at low temperatures. The low fixed charge raises the threshold voltage which in turn helps prevent inducement of undesired channels between unassociated active areas in devices formed in the substrate.

Brief Description of the Drawings

Figure 1 is a cross section of a semiconductor device formed in accordance with the present invention.

Figure 2 is a graph of the concentration of carbon versus depth for depositions performed at multiple temperatures.

Figure 3 is a graph of the threshold voltage of a device having insulating layer depositions performed at multiple temperatures.

Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

Numbering in the Figures is usually done with the hundreds and thousands digits corresponding to the figure number, with the exception that the same components may appear in multiple figures. Signals and connections may be referred to by the same number or label, and the actual meaning should be clear from the context of use.

In Figure 1, a semiconductor device comprising a silicon substrate or other suitable semiconductor material indicated generally at 110 has many active areas such as active areas 112 and 114 of adjacent transistors formed

therein separated by a field oxide indicated at 116. The field oxide 116 provides isolation between adjacent unassociated active areas of transistors. An insulative glass layer 130 such as an oxide film or borophosphosilicate glass (BPSG) is deposited over the active areas to a depth of approximately 25,000 Angstroms using an organic precursor. Metal conductors represented at 140 are then formed on top of the oxide layer 130. In a further embodiment, a second oxide layer is then formed as in inter metal dielectric, and further conductors and oxide layers are formed on top of that to form multiple levels of conductors.

In one embodiment, the glass 130 is formed to a depth of between 2K angstroms and 30K angstroms in a standard chemical vapor deposition (CVD) reactor such as the Applied Materials P5000 single wafer cold well CVD reactor by reacting tetraethyloxysilicate (TEOS) with ozone (O_3). O_3 is formed in a corona discharge tube by flowing O_2 at a rate of approximately 2000-8000 cubic centimeters per minute such that the O_3 concentration in O_2 is approximately 13% by weight. In further embodiments, the concentration ranges from approximate 2-20% by weight. TEOS is then pumped by liquid injectors into a flash evaporator at the rate of approximately 200-800 milligrams per minute and combined with a helium carrier gas which is provided at a rate of between approximately 2000-10,000 cubic centimeters per minute. This mixture is then combined with the oxygen mixture and introduced into the reactor through a common shower head to form the oxide layer on the substrate which is preferably heated to a temperature of at least approximately 480 degrees Celsius.

Triethylphosphate (TEPO) and Triethylborane (TEB) are organometallics used to dope the film with phosphorous and boron respectively. They are also controllably injected into the flash evaporator at rates of between 20-90 milligrams per minute and 40-300 milligrams per minute respectively to form varying percentages of doping. To form a silicon dioxide layer, neither TEPO nor TEB are added. Both are added to form a BPSG insulative oxide layer. TEPO is used alone to provide a phosphorous doped silicon dioxide layer and TEB is used alone to provide a boron doped silicon dioxide layer. The percentage of boron is varied between approximately 0.5-6%, and the percentage

of phosphorous is varied between approximately 0.5-8%. Boron doping tends to lower the temperature required for reflow of the oxide layer. Phosphorous is used as a mobile ion getterer, and in combination with boron, assists in lowering the reflow temperature. Boron and phosphorous doping may also be obtained through the use of other well known organometallics.

The glass layer 130 is deposited at a pressure of approximately 200 Torr. In further embodiments, the pressure varies between approximately 10 Torr to 760 Torr or atmospheric pressure. The temperature at which the deposition of the glass layer takes place in one embodiment is approximately 510 degrees C or higher. The heating of the substrate is provided in a known manner such as by lamp, resistive coils in the substrate chuck or infrared sources.

Following deposition of the glass layer, the substrate 110 is then transferred to a furnace for a high temperature reflow in the case of BPSG or densifying in the case of oxide. In one embodiment, a batch furnace reflow is performed at approximately 907 degrees C for 30 minutes in a nitrogen (N_2) environment at approximately atmospheric pressure. Alternatively, the wafer is reflowed by a rapid thermal process (RTP) reflow at approximately 1000 degrees C for 20 seconds, again in an N_2 environment at approximately atmospheric pressure. The exact times and temperatures for these reflows will vary significantly depending on the percentage concentrations of boron and phosphorous in the glass layer 130.

The above steps result in the introduction of carbon into the glass layer from the use of the organometallic dopants. The carbon level at the interface between the oxide film and active area silicon interface appears to be directly correlated to the amount of fixed charge in the film. By increasing the film deposition temperature higher than approximately 480 degrees C, the carbon level in the film appears to be scavenged by the O_3, leading to a lower fixed charge.

Figure 2 is a graph of the carbon level concentrations in atoms per cubic centimeter at various depths in Angstroms of each oxide layer deposited using the present invention. Oxide layers were formed at various identified

oxide deposition temperatures. The oxide layers were also reflowed for 30 minutes at 907 degrees C. The measurements were taken at various depths using standard secondary ion mass spectroscopy (SIMS).

The reflow of the layer causes the carbon to migrate toward the interface between the silicon and the oxide layer at about 26,000 Angstrom. The data presented in the graph of actual typical experimental results, shows the carbon has migrated to depths near the interface. The total concentration of carbon is seen to be significantly reduced when the film is deposited in the presence of O_3 at temperatures of approximately 480 degrees C and above. When deposited at 510 degrees C, the concentration of carbon is fewer than about 10^{18} to 10^{17} atoms per cubic centimeter at its highest concentration and the fixed charge density is less than approximately $5x10^{10}$ per square centimeter.

By reducing the carbon level in the film, a low fixed charge film of oxide is provided. In essence, a higher metal field threshold voltage is obtained for n-channel devices as indicated in Figure 3. Figure 3 is a graph of threshold voltage for 24,000 angstrom thick BPSG fields applied in an O_3 environment in a deposition chamber at the same temperatures as in Figure 2. In addition, both a batch furnace reflow for 30 minutes at 907 degrees C and a rapid thermal process (RTP) reflow for 20 seconds at 1000 degree C were performed in N_2 prior to the threshold voltages being measured. As indicated, the threshold voltage increased dramatically when the film was applied in the presence of O_3 at temperatures above approximately 510 degrees C. Improvement was also noted at temperatures above approximately 480 degrees C. It should be noted that the first three layers in Figure 3 were formed with 3% boron (B_2O_3) and 6% phosphorous (P_2O_5). At 530 degrees C, the percentages of boron and phosphorous were both 5%. An inorganic control group silane (SiH_4) is also shown.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the

invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method of forming a thin film of glass having a low fixed charge on a semiconductor device in a deposition chamber comprising the steps of:

positioning a semiconductor device in the deposition chamber;

providing O_3 within the chamber;

heating the chamber to greater than approximately 480 degrees C; and

depositing silicon dioxide using an organometallic precursor onto the semiconductor device at such temperature.

2. The method of claim 1 wherein O_2 is also provided within the chamber, and the concentration of O_3 in O_2 is between approximately 2 and 20% by weight.

3. The method of claim 2 wherein the concentration of O_3 in O_2 is approximately 13%.

4. The method of claim 2 wherein the step of providing O_3 in the chamber comprises the step of flowing O_2 in a corona discharge tube.

5. The method of claim 3 wherein the step of depositing silicon dioxide comprises the step of reacting tetraethyloxysilicate with the ozone.

6. The method of claim 5 and further comprising the step of reflowing the thin film at high temperature.

7. The method of claim 1 wherein the organometallic precursor is used to dope the thin film with at least one of phosphorous and boron.

8. The method of claim 7 wherein the organometallic precursor comprises at least one of triethylborane and triethylphosphate.

9. The method of claim 1 and further comprising the step of controlling the pressure within the chamber during the depositing step to be within the range of approximately 10 Torr to 760 Torr.

10. The method of claim 1 wherein the resulting thin film comprises fewer than 10^{18} carbon atoms per cubic centimeter.

11. A device formed in a semiconductor substrate having a borophosphosilicate glass thin film formed thereon using organometallic precursors, the film comprising fewer than 10^{18} carbon atoms per cubic centimeter and having a fixed charge density less than approximately $5x10^{10}$ per square centimeter.

12. The device of claim 11 wherein the film comprises fewer than 10^{18} carbon atoms per cubic centimeter following a high temperature reflow and has a fixed charge density less than approximately $5x10^{10}$ per square centimeter.

13. The device of claim 11 wherein the thin film comprises between 0.5% to 6% boron by weight and between approximately 0.5% to 8% phosphorous by weight.

14. The device of claim 11 wherein the thin film is approximately 26,000 angstroms thick or less.

15. The device of claim 11 and further comprising active areas formed in the substrate beneath the thin film.

16. A method for reduction of fixed charge in an insulating film utilized in semiconductor devices, comprising the steps of:

a) reacting material source gases, including at least one organic precursor for deposition;

b) depositing said material on said semiconductor device in an atmosphere containing O_3 at a temperature greater than approximately 480 degrees C.

17. The method of claim 16 wherein said insulating film material is borophosphosilicate glass.

18. The method of claim 17 wherein said source gas is tetraethyloxysilicate.

19. The method of claim 18 wherein said source gas is tetraethyloxysilicate, mixed with triethylphosphate and triethylborane.

20. The method of claim 16 wherein the O_3 is formed by flowing O_2 in a corona discharge tube.

21. The method of claim 20 wherein the O_2 is flowed at a rate of between approximately 2000 to 8000 cubic centimeters per minute.

22. The method of claim 21 wherein said the concentration of O_3 in O_2 provided by the corona discharge tube is approximately 2-20% by weight.

23. The method of claim 22 wherein the concentration of O_3 in O_2 is approximately 13%.

24. The method of claim 17 wherein said deposition takes place at pressures of approximately 10 to 760 Torr.

25. A method for reduction of fixed charge in a tetraethyloxysilicate-based borophosphosilicate glass insulating film utilized in semiconductor devices, comprising the steps of:

a) reacting material source gases including at least one organic precursor for deposition;

b) depositing said material on said semiconductor device at a temperature of approximately 480 degrees Celsius or greater in an atmosphere containing O_2 and O_3.

26. The method of claim 25 wherein tetraethyloxysilicate, triethylborane and O_3 are the gases reacted.

27. The method of claim 25 wherein tetraethyloxysilicate, triethylphosphate and O_3 are the gases reacted.

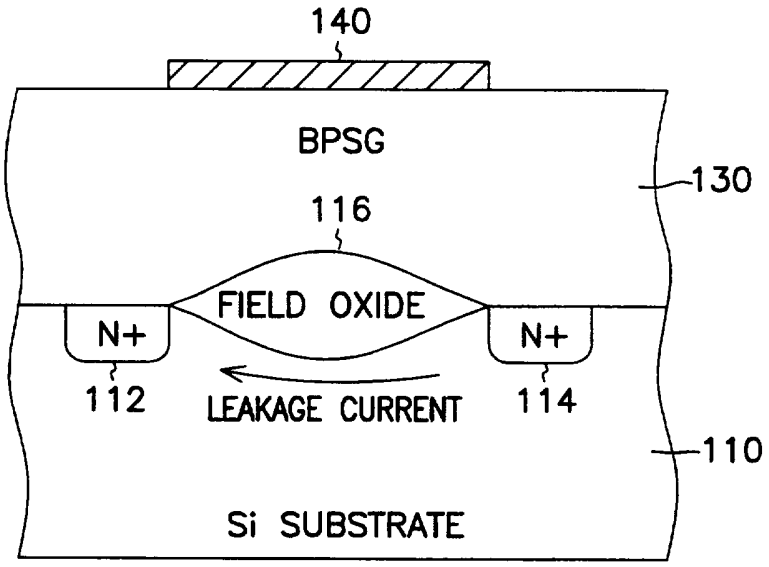
28. A method of forming a thin film of borophosphosilicate glass on a semiconductor device in a deposition chamber comprising the steps of:

positioning a semiconductor device in the deposition chamber;

providing O_3 within the chamber;

heating the chamber to greater than 480 degrees C; and

depositing borophosphosilicate glass onto the semiconductor device at such temperature using an organic precursor.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N+
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LEAKAGE CURRENT
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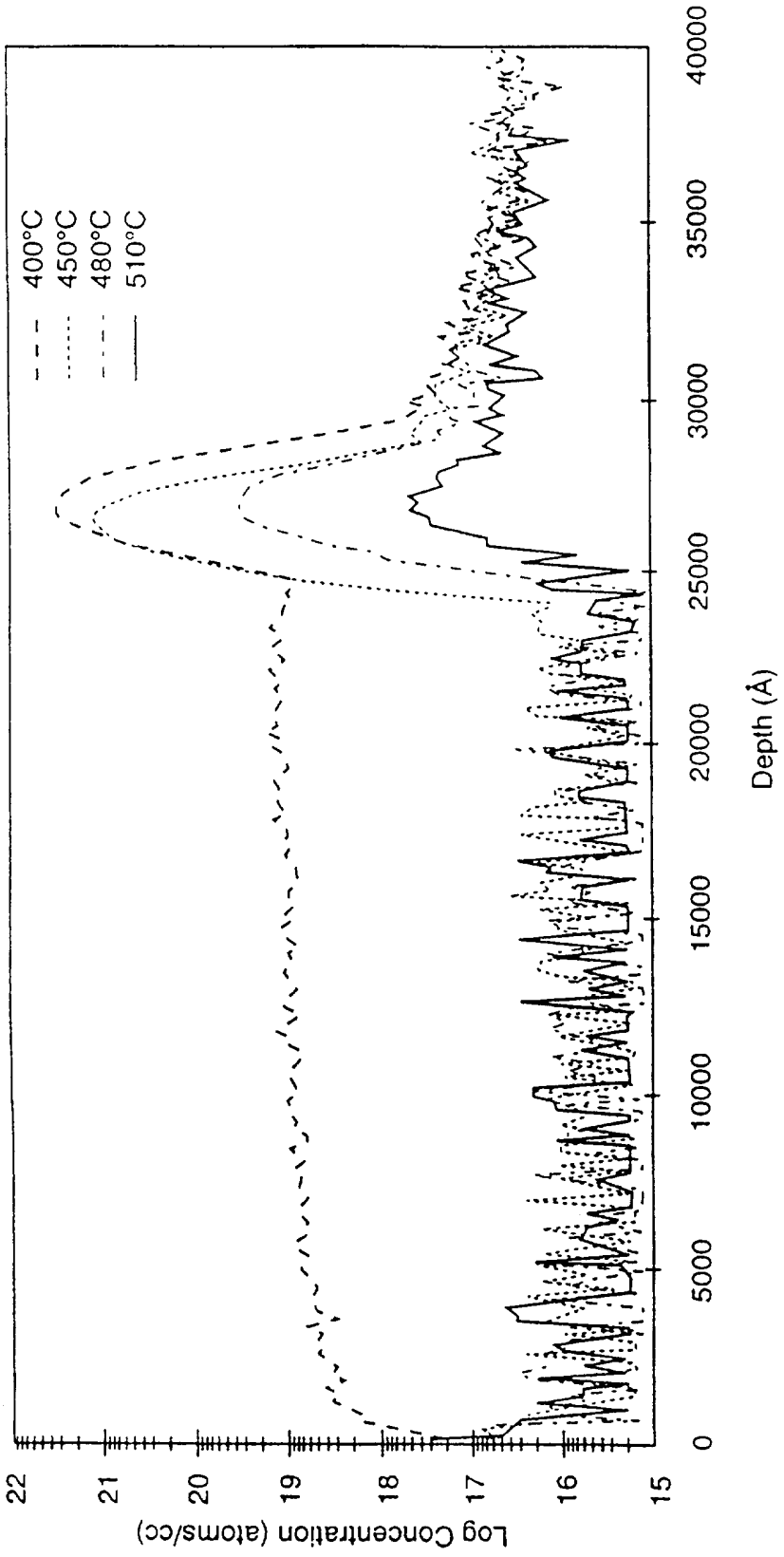
110
Si SUBSTRATE

FIG. 1

FIG. 2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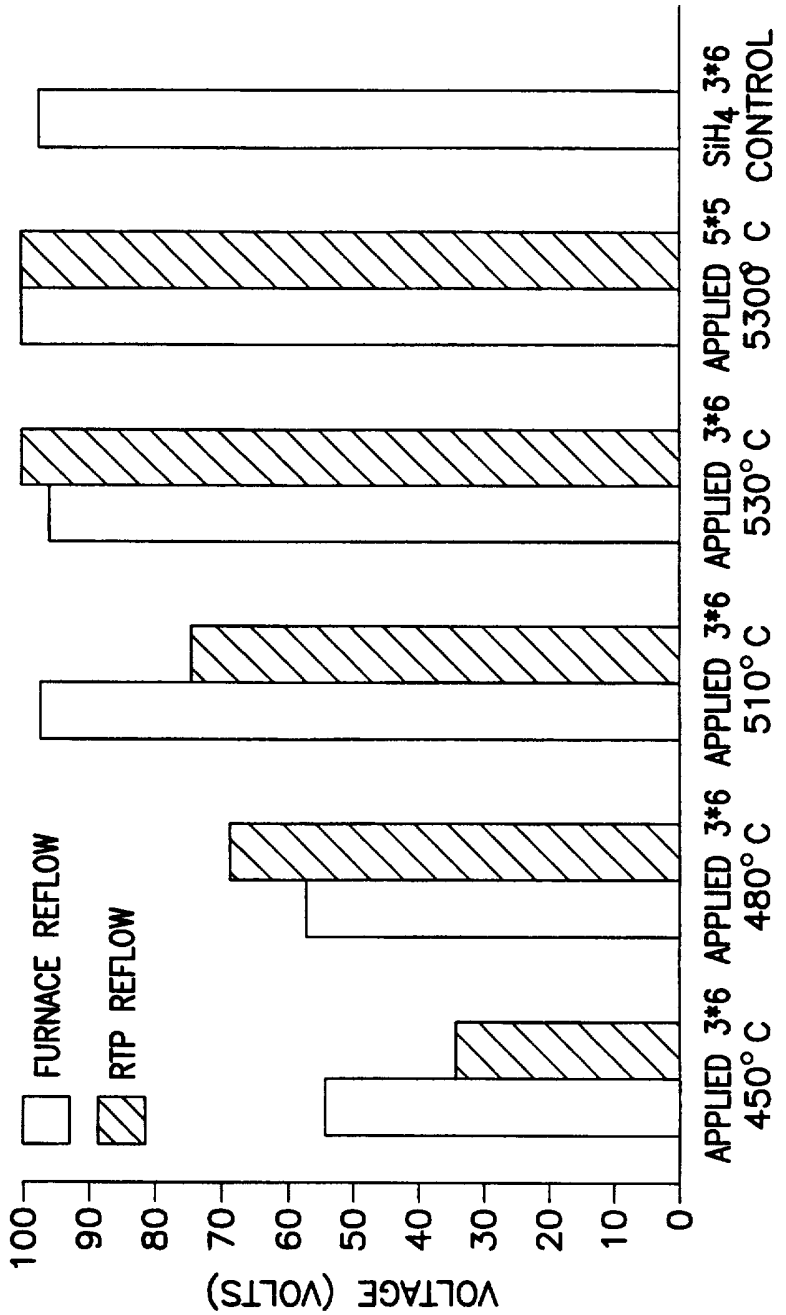
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RTP REFLOW
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80
70
60
50
40
30
20
10
0
APPLIED 3*6 450° C
APPLIED 3*6 480° C
APPLIED 3*6 510° C
APPLIED 3*6 530° C
APPLIED 5*5 5300° C
SiH4 3*6 CONTROL

FIG. 3

INTERNATIONAL SEARCH REPORT

Inter nal Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,5 354 715 (WANG DAVID N-K ET AL) 11 October 1994 see column 23, line 15 - column 25, line 15; claims 1-16 ---	1,2,7,9, 16,18, 25,28
X	EP,A,0 272 140 (APPLIED MATERIALS INC) 22 June 1988 see column 28, line 38 - column 29, line 23 --- -/--	1,2,7,9, 16,18, 25,28

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
10 September 1996	30. 09. 96

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Inter nal Application No
PCT/US 96/10196

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 138, no. 10, 1 October 1991, pages 3019-3024, XP000248007 FUJINO K ET AL: "DOPED SILICON OXIDE DEPOSITION BY ATMOSPHERIC PRESSURE AND LOW TEMPERATURE CHEMICAL VAPOR DEPOSITION USING TETRAETHOXYSILANE AND OZONE" see page 3019 - page 3024 ---	1-3,7-9, 13-19, 24-28
A	SOLID STATE TECHNOLOGY, vol. 37, no. 3, 1 March 1994, page 31/32, 34, 36, 38, 40 XP000440989 WALLACE FRY H ET AL: "APPLICATIONS OF APCVD TEOS/O3 THIN FILMS IN ULSI IC FABRICATION" see page 83 - page 88 ---	1-3,7-9, 13-19, 24-28
A	SOLID STATE TECHNOLOGY, vol. 36, no. 6, 1 June 1993, pages 83-86, 88, XP000383890 KAZUO MAEDA ET AL: "CVD TEOS/O3: DEVELOPMENT HISTORY AND APPLICATIONS" see page 32, paragraph 6 - page 40, paragraph 1 -----	1-3,7-9, 13-19, 24-28

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inte nal Application No
PCT/US 96/10196

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A-5354715	11-10-94	US-A- 5362526	08-11-94
		US-A- 5000113	19-03-91
		DE-D- 3789142	31-03-94
		DE-T- 3789142	26-05-94
		EP-A- 0272140	22-06-88
		ES-T- 2049729	01-05-94
		JP-A- 6013368	21-01-94
		JP-A- 6013367	21-01-94
		JP-A- 8055843	27-02-96
		JP-A- 8070035	12-03-96
		JP-B- 6012771	16-02-94
		JP-A- 63246829	13-10-88
		US-A- 4872947	10-10-89
		US-A- 4892753	09-01-90
		US-A- 4960488	02-10-90
		US-A- 5158644	27-10-92
EP-A-0272140	22-06-88	US-A- 5000113	19-03-91
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		JP-A- 8070035	12-03-96
		JP-B- 6012771	16-02-94
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		US-A- 4872947	10-10-89
		US-A- 4892753	09-01-90
		US-A- 4960488	02-10-90
		US-A- 5362526	08-11-94
		US-A- 5158644	27-10-92
		US-A- 5354715	11-10-94