IRREGULARLY STRUCTURED, LOW DENSTY PARITY CHECK CODES

Abstract: An error correction codeword. In one embodiment, an irregularly structured LDPC code ensemble possessing strong overall error performance and attractive storage requirements for a large set of codeword lengths. Embodiments of the invention can offer communication systems with better performance and lower terminal costs due to possible reductions in mandatory non-volatile memory over conventional systems.
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.
IRREGULARLY STRUCTURED, LOW DENSITY PARITY CHECK CODES

FIELD OF THE INVENTION

[0001] The present invention relates generally to correction codes in communication systems. More particularly, the present invention relates to the use of correction codes for reliably conveying information through channels having random events.

BACKGROUND OF THE INVENTION

[0002] Modern communication systems use Forward Error Correction (FEC) codes in an attempt to convey information more reliably through channels with random events. One such FEC error control system uses low density parity check (LDPC) codes. LDPC codes can have error correcting capabilities that rival the performance of "Turbo-Codes" and can be applicable over a wide range of statistical channels. In fact, some random irregular LDPC constructions based upon edge ensemble designs have error correcting capabilities measured in Bit Error Rate (BER) that are within 0.05 dB of the rate-distorted Shannon limit. Unfortunately, these LDPC code constructions often require long codeword constructions (on the order of $10^6$ to $10^7$ bits) in order to achieve these error rates. Despite good BER performance, these random code constructions often have poor Block Error Rate (BLER) performances. Therefore, these random constructions typically do not lend themselves well to packet-based communication systems.

[0003] Another disadvantage of random constructions based on edge distribution ensembles is that, for each codeword length, a separate random construction is needed. Thus, communication systems employing variable block sizes (e.g. TCP/IP systems) require multiple code definitions. Such multiple code definitions can consume a significant amount of non-volatile memory for large combinations of codeword lengths and code rates.
[0004] As an alternative to random LDPC constructions, structured LDPC constructions typically rely on a general algorithmic approach to constructing LDPC matrices which often requires much less non-volatile memory than random constructions. One such structured approach is based upon array codes. This approach can exhibit improved error performance (both BER and BLER performance) and a relatively low error floor for relatively high code rates (higher than 0.85).

However, for code rates below 0.85, these code constructions have relatively poor performance with respect to irregular random constructions designed for lower code rates. One reason for this poor performance can be that their constructions are typically based on code ensembles that have poor asymptotic performances despite being an irregular construction.

[0005] One challenge therefore is to design irregular structured LDPC codes that have good overall error performance for a wide range of code rates with attractive storage requirements. Such resulting LDPC codes would provide a better performing communication system with lower cost terminals. These factors can make such FEC attractive for applications over a wide range of products, including but not limited to, wireless LAN systems, next generation cellular systems, and ultra wide band systems.

SUMMARY OF THE INVENTION

[0006] Embodiments of the present invention provides for an irregularly structured LDPC code ensemble that has strong overall error performance and attractive storage requirements for a large set of codeword lengths. Embodiments of the invention offer communication systems with better performance and lower terminal costs due to the reduction in mandatory non-volatile memory over conventional systems.

[0007] In contrast to conventional approaches, embodiments of the invention provide a structured approach to construction, offering reduced storage requirements and a simple construction. When used with seed matrices with good asymptotic performances and good girth properties, the irregularly structured LDPC codes used in embodiments of the present invention offer an improved overall level of error performance. Embodiments of the invention also offer a parity-check matrix that is
lower in density than conventional array codes because there are fewer non-zero sub-
matrices (i.e. there are more sub-matrices consisting of the all zeros matrix).

[0008] These and other objects, advantages and features of the invention, together
with the organization and manner of operation thereof, will become apparent from the
following detailed description when taken in conjunction with the accompanying
drawings, wherein like elements have like numerals throughout the several drawings
described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 is an overview diagram of a system within which embodiments of
the invention may be implemented;
[0010] Figure 2 is a perspective view of a mobile telephone that can be used in the
implementation of one embodiment the present invention;
[0011] Figure 3 is a schematic representation of the telephone circuitry of the
mobile telephone of Figure 2;
[0012] Figure 4 is a flow chart showing the implementation of one embodiment of
the present invention;
[0013] Figure 5 is an example of a code rate 1/2 irregular parity-check matrix
according to one embodiment of the present invention;
[0014] Figure 6 is an example of a code rate 2/3 irregular parity-check matrix
according to one embodiment of the present invention; and
[0015] Figure 7 is an example of a code rate 3/4 irregular parity-check matrix
according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Various exemplary embodiments of the invention are described below with
reference to the drawing figures. One embodiment of the invention can be described
in the general context of method steps, which may be implemented in one
embodiment by a program product including computer-executable instructions, such
as program code, executed by computers in networked environments. Embodiments
of the invention may be implemented in either hardware or software, and can be placed both within a transmitter and/or a receiver.

[0017] Figure 1 shows a system 10 illustrating one embodiment of the invention, comprising multiple communication devices that can communicate through a network. The system 10 may comprise any combination of wired or wireless networks including, but not limited to, a mobile telephone network, a wireless Local Area Network (LAN), a Bluetooth personal area network, an Ethernet LAN, a token ring LAN, a wide area network, the Internet, etc. The system 10 may include both wired and wireless communication devices.

[0018] For exemplification, the system 10 shown in Figure 1 can include a mobile telephone network 11 and the Internet 28. Connectivity to the Internet 28 may include, but is not limited to, long range wireless connections, short range wireless connections, and various wired connections including, but not limited to, telephone lines, cable lines, power lines, and the like.

[0019] Exemplary communication devices of the system 10 may include, but are not limited to, a mobile telephone 12, a combination PDA and mobile telephone 14, a PDA 16, an integrated messaging device (IMD) 18, a desktop computer 20, and a notebook computer 22. The communication devices may be stationary or mobile as when carried by an individual who is moving. The communication devices may also be located in a mode of transportation including, but not limited to, an automobile, a truck, a taxi, a bus, a boat, an airplane, a bicycle, a motorcycle, etc. Some or all of the communication devices may send and receive calls and messages and communicate with service providers through a wireless connection 25 to a base station 24. The base station 24 may be connected to a network server 26 that allows communication between the mobile telephone network 11 and the Internet 28. The system 10 may include additional communication devices and communication devices of different types. A communication device may communicate using various media including, but not limited to, radio, infrared, laser, cable connection, and the like. One such portable electronic device incorporating a wide variety of features is shown in Figure 4. This particular embodiment may serves as both a video gaming device and a portable telephone.
[0020] The communication devices may communicate using various transmission technologies including, but not limited to, Code Division Multiple Access (CDMA), Global System for Mobile Communications (GSM), Universal Mobile Telecommunications System (UMTS), Time Division Multiple Access (TDMA), Frequency Division Multiple Access (FDMA), Transmission Control Protocol/Internet Protocol (TCP/IP), Short Messaging Service (SMS), Multimedia Messaging Service (MMS), e-mail, Instant Messaging Service (IMS), Bluetooth, IEEE 802.11, etc.

[0021] Figures 2 and 3 show one representative mobile telephone 12 within which one embodiment of the present invention may be implemented. It should be understood, however, that the present invention is not intended to be limited to one particular type of mobile telephone 12 or other electronic device. The mobile telephone 12 of Figures 2 and 3 comprises a housing 30, a display 32 in the form of a liquid crystal display, a keypad 34, a microphone 36, an ear-piece 38, a battery 40, an infrared port 42, an antenna 44, a smart card 46 in the form of a universal integrated circuit card (UICC) according to one embodiment of the invention, a card reader 48, radio interface circuitry 52, codec circuitry 54, a controller 56 and a memory 58.

[0022] Generally, program modules can include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types. Computer-executable instructions, associated data structures, and program modules represent examples of program code for executing steps of the methods disclosed herein. The particular sequence of such executable instructions or associated data structures represents examples of corresponding acts for implementing the functions described in such steps.

[0023] Software and web implementations of the present invention could be accomplished with standard programming techniques with rule-based logic and other logic to accomplish the various database searching steps, correlation steps, comparison steps and decision steps. It should also be noted that the words "component" and "module" as used herein, and in the claims, are intended to encompass implementations using one or more lines of software code, and/or hardware implementations, and/or equipment for receiving manual inputs.
By taking into account the density evolution of messages passed in belief propagation decoding, random constructions of irregular LDPC codes can be developed that approach Shannon limits for an assortment of channels (e.g. Additive White Gaussian Noise (AWGN), Binary Erasure Channel (BEC), Binary Symmetric Channel (BSC)). These are typically described as ensembles with variable and check edge polynomials $\lambda(x) = \sum_{i=2}^{d_v} \lambda_i x^{i-1}$ and $\rho(x) = \sum_{j=2}^{d_c} \rho_j x^{j-1}$, respectively, where $\lambda_i$ and $\rho_j$ are the fraction of total edges connected to variable and check nodes of degree $i = 2, 3, \ldots, d_v$ and $j = 2, 3, \ldots, d_c$ respectively. These random constructions sometimes require the relatively long codeword lengths to approach the capacity limit and do not always provide the strong BLER performance required by packet-based communication systems. In actual communication terminals, these random constructions can require storage of the entire parity-check matrix, and for systems employing variable packet-length, the storage of multiple random constructions is both necessary and costly.

Alternatively, structured approaches to LDPC code designs that allow for reduced storage requirements and simple code description may be used. One such example is the LDPC code construction based upon array constructions. For code rates 0.85 and above, these code constructions can have acceptable performance with good error floors and BLERs. However, with respect to random constructions, these constructions sometimes suffer at lower code rates because they have edge distributions that result in relatively poor asymptotic performance and thus poor performance in general.

It is desirable thus, to provide irregularly structured LDPC codes that have good overall error performance for a wide range of code rates with attractive storage requirements that make communication terminals cost effective. The result of such LDPC codes can do a better performing communication system with lower cost terminals. These factors can make such a FEC attractive for applications over a wide range of products including but not limited to wireless LAN, next generation cellular systems, and ultra wide band systems.
As discussed herein, an irregular "seed" parity-check matrix can be used as the "seed" for irregular structured LDPC code some embodiments according to the present invention. One embodiment involves the construction of an irregular "seed" low-density parity check-matrix $H_{\text{seed}}$ of dimension $(N_{\text{seed}} - K_{\text{seed}}) \times N_{\text{seed}}$ derived from an edge distribution, $\lambda_{\text{seed}}(x)$ and $\rho_{\text{seed}}(x)$, with good asymptotic performance and good girth properties. In one embodiment, good asymptotic performance may be characterized by a good threshold value using belief propagation decoding and good girth may be characterized by having very few if no variable nodes with a girth of 4. This can be accomplished manually or via a software program once given the code ensemble and/or node degrees.

Although there are no limits on the maximum values of $K_{\text{seed}}$ and $N_{\text{seed}}$, which represent the number of information bits and the resulting codeword length, respectively in one embodiment, for the code defined by $H_{\text{seed}}$, these values can be relatively small in comparison to the target message-word and codeword length. This can allow for more potential integer multiples of $N_{\text{seed}}$ within the target range of codeword lengths, reduced storage requirements, and simplified code descriptions. In one embodiment of the invention, the smallest possible value for $H_{\text{seed}}$ can be used with edge distributions defined by $\lambda_{\text{seed}}(x)$ and $\rho_{\text{seed}}(x)$, while still maintaining good girth properties.

One function of the seed matrix can be to identify the location and type of sub-matrices in the expanded LDPC parity-check matrix $H$ constructed from $H_{\text{seed}}$ and a given set of permutation matrices. The permutation matrices in $H_{\text{seed}}$ can determine the location of sub-matrices in the expanded matrix $H$ that contain a permutation matrix of dimension $(N_{\text{spread}} \times N_{\text{spread}})$ from the given set. One selection within the given set of permutation matrices is defined below. As an example only, the given set of permutation matrices used herein can be finite and consist of the set

$$\{P_{\text{spread}}^0, P_{\text{spread}}^1, P_{\text{spread}}^2, \ldots, P_{\text{spread}}^{P-1}\}$$
where \( p \) is a positive integer (a prime number in a preferred embodiment of the invention), \( P_{\text{spread}}^0 = I \) is the identity matrix, \( P_{\text{spread}}^1 \) is a full-rank permutation matrix, \( P_{\text{spread}}^2 = P_{\text{spread}}^1 P_{\text{spread}}^1 \), etc. up to \( P_{\text{spread}}^{p-1} \). One example embodiment of \( P_{\text{spread}}^1 \) is a single circular shift permutation matrix

\[
P_{\text{spread}}^1 = \begin{bmatrix}
0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1 \\
1 & 0 & 0 & 0 & 0
\end{bmatrix}
\]

for \( N_{\text{spread}} = 5 \).

[0030] Another example embodiment of \( P_{\text{spread}}^1 \) is an alternate single circular shift permutation matrix

\[
P_{\text{spread}}^1 = \begin{bmatrix}
0 & 0 & 0 & 0 & 1 \\
1 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0
\end{bmatrix}
\]

for \( N_{\text{spread}} = 5 \).

[0031] For notational sake, \( P_{\text{spread}}^\infty \) denotes the all zeros matrix \( 0 \) of dimension \( (N_{\text{spread}} \times N_{\text{spread}}) \) (i.e. \( P_{\text{spread}}^\infty = 0 \) where every element is a zero), and the zeros in \( H_{\text{seed}} \) indicate the location of the sub-matrix \( P_{\text{spread}}^\infty = 0 \) in the expanded matrix \( H \).

Thus, the expanded LDPC matrix \( H \) can be of dimension \( (N_{\text{spread}} \times N_{\text{spread}}) \) with sub-matrices consisting of permutation matrices of dimension \( (N_{\text{spread}} \times N_{\text{spread}}) \) raised to an exponential power from the set of \( \{0,1,\ldots,p-1,\infty\} \).

[0032] Furthermore, the expanded LDPC code can have the same edge distribution as \( H_{\text{seed}} \) and hence can achieve the desired asymptotic performance described by \( \lambda_{\text{seed}}(x) \) and \( \rho_{\text{seed}}(x) \), provided both \( H_{\text{seed}} \) and the expanded matrix \( H \) have satisfactory girth properties.

[0033] The following description concerns one embodiment of the invention that constructs a structured array exponent matrix that may be described as
\[ E_{\text{ARRAY}} = \begin{bmatrix} E_{1,1} & E_{1,2} & \cdots & E_{1,p} \\ E_{2,1} & E_{2,2} & \cdots & E_{2,p} \\ \vdots & \vdots & & \vdots \\ E_{p,1} & E_{p,2} & \cdots & E_{p,p} \end{bmatrix}, \text{ where } E_{i,j} = (i-1)(j-1) \mod p \]

using modulo arithmetic (but not limited to) of a number \( p \). In one embodiment of the invention, \( p \) can be a prime number, but this is not necessary for the principles of the present invention. \( p \) can be at least the column dimension of the irregular “seed” parity check matrix and the column dimension of the spreading permutation matrix. In one embodiment, \( N_{\text{SEED}} \leq p \) and \( N_{\text{SPREAD}} \leq p \). However, other values are also possible.

[0034] Other embodiments of the present invention can use transformed versions of \( E_{\text{ARRAY}} \). In particular, one such transformation involves the shifting of rows to construct an upper triangular matrix while replacing vacated element locations with \( \infty \), i.e.

\[ E_{\text{SHIFT}} = \begin{bmatrix} E_{1,1} & E_{1,2} & E_{1,3} & \cdots & E_{1,p} \\ \infty & E_{2,1} & E_{2,2} & \cdots & E_{2,p-1} \\ \infty & \infty & E_{3,1} & \cdots & E_{3,p-2} \\ \vdots & \vdots & \vdots & & \vdots \\ \infty & \infty & \infty & \cdots & E_{p,1} \end{bmatrix} \]

[0035] Another embodiment of the present invention transforms \( E_{\text{ARRAY}} \) by the truncation of columns and/or rows to select a sub-matrix of \( E_{\text{ARRAY}} \) for implementation with a specified \( H_{\text{SEED}} \). Still another embodiment of the invention uses the combination of both shifting and truncation. For example, given

\( N_{\text{SEED}} + 1 \leq p \) and \( N_{\text{SPREAD}} \leq p \) (with \( p \) being a prime number in a particular embodiment of the invention)

\[ E_{\text{TRUNCATE1}} = \begin{bmatrix} E_{1,2} & E_{1,3} & E_{1,4} & \cdots & E_{1,(N_{\text{SEED}}-K_{\text{SEED}})} & \cdots & E_{1,(N_{\text{SEED}}+1)} \\ E_{2,1} & E_{2,2} & E_{2,3} & \cdots & E_{2,(N_{\text{SEED}}-K_{\text{SEED}}-1)} & \cdots & E_{2,(N_{\text{SEED}}+1)} \\ \infty & E_{3,1} & E_{3,2} & \cdots & E_{3,(N_{\text{SEED}}-K_{\text{SEED}}-2)} & \cdots & E_{3,(N_{\text{SEED}}+1)} \\ \vdots & \vdots & \vdots & & \vdots & \vdots & \vdots \\ \infty & \infty & \infty & \cdots & E_{(N_{\text{SEED}}-K_{\text{SEED}})+1} & \cdots & E_{(N_{\text{SEED}}-K_{\text{SEED}})+(K_{\text{SEED}}+2)} \end{bmatrix} \]
For $N_{\text{seed}} + 2 \leq p$ and $N_{\text{spread}} \leq p$ (with $p$ being a prime number in a particular embodiment of the invention)

$$E_{\text{TRUNCATE2}} = \left[ \begin{array}{ccccccc} E_{2,2} & E_{2,3} & E_{2,4} & \cdots & E_{2,(N_{\text{seed}} - K_{\text{seed}})} & \cdots & E_{2,(N_{\text{seed}} + 1)} \\
E_{3,1} & E_{3,2} & E_{3,3} & \cdots & E_{3,(N_{\text{seed}} - K_{\text{seed}} - 1)} & \cdots & E_{3,N_{\text{seed}}} \\
\infty & E_{4,1} & E_{4,2} & \cdots & E_{4,(N_{\text{seed}} - K_{\text{seed}} - 2)} & \cdots & E_{4,(N_{\text{seed}} - 1)} \\
\vdots & \vdots & \vdots & \ddots & \vdots & \ddots & \vdots \\
\infty & \infty & \infty & \cdots & E_{(N_{\text{seed}} - K_{\text{seed}} + 1),1} & \cdots & E_{(N_{\text{seed}} - K_{\text{seed}} + 1),(K_{\text{seed}} + 2)} \end{array} \right]$$

Many shift and truncate embodiments can be used with the present invention, as well as column and row permutation transformations performed either prior to or after other individual transformations in a nested fashion. More generally, the transformation of the $E_{\text{ARRAY}}$ matrix can be described using the functional notation $T(E_{\text{ARRAY}})$ that represents a transformed exponent matrix of dimension $((N_{\text{seed}} - K_{\text{seed}}) \times N_{\text{seed}})$. Yet another embodiment of this family of transformations may include an identity transformation. For example, in another embodiment of the invention, $T(E_{\text{ARRAY}}) = E_{\text{ARRAY}}$.

In one embodiment of the present invention $H_{\text{seed}}$ and $T(E_{\text{ARRAY}})$ can be used to construct the final exponent matrix in order to expand the seed matrix into $H$. The final exponent matrix may be defined as

$$F_{\text{FINAL}} = \left[ \begin{array}{ccccccc} F_{1,1} & F_{1,2} & \cdots & F_{1,N_{\text{seed}}} \\
F_{2,1} & F_{2,2} & \cdots & F_{2,N_{\text{seed}}} \\
\vdots & \vdots & \ddots & \vdots \\
F_{(N_{\text{seed}} - K_{\text{seed}}),1} & F_{(N_{\text{seed}} - K_{\text{seed}}),2} & \cdots & F_{(N_{\text{seed}} - K_{\text{seed}}),N_{\text{seed}}} \end{array} \right]$$

of dimension $((N_{\text{seed}} - K_{\text{seed}}) \times N_{\text{seed}})$ by replacing each one in $H_{\text{seed}}$ with the corresponding matrix element (i.e. the same row and column) in the transformed structured array exponent matrix $T(E_{\text{ARRAY}})$ and each zero in $H_{\text{seed}}$ with $\infty$. Thus, the elements of $F_{\text{FINAL}}$ can belong to the set $\{0,1,\ldots,p-1,\infty\}$ if modulo arithmetic is used in the construction of $E_{\text{ARRAY}}$.

The following is a discussion of one embodiment of the expansion of $H_{\text{seed}}$ using $F_{\text{FINAL}}$ to construct a final LDPC parity-check matrix $H$ that describes the
LDPC code. The matrix $H_{\text{SEED}}$ of dimension $((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})$ can be spread or expanded using the elements of the permutation matrix set

$$\{P_{\text{SPREAD}}^0, P_{\text{SPREAD}}^1, P_{\text{SPREAD}}^2, \ldots, P_{\text{SPREAD}}^{p-1}\}$$

with elements of dimension $\left(N_{\text{SPREAD}} \times N_{\text{SPREAD}}\right)$, where $P_{\text{SPREAD}}^0 = \mathbf{0}$ is the all zeros matrix, $P_{\text{SPREAD}}^0 = \mathbf{I}$ is the identity matrix, $P_{\text{SPREAD}}^1$ is a permutation matrix, $P_{\text{SPREAD}}^2 = P_{\text{SPREAD}}^1 P_{\text{SPREAD}}^1$, $P_{\text{SPREAD}}^3 = P_{\text{SPREAD}}^1 P_{\text{SPREAD}}^1 P_{\text{SPREAD}}^1$, etc. (but not limited to) to construct

$$H = \begin{bmatrix}
    P_{\text{SPREAD}}^1 & P_{\text{SPREAD}}^2 & \cdots & P_{\text{SPREAD}}^p \\
    P_{\text{SPREAD}}^1 & P_{\text{SPREAD}}^2 & \cdots & P_{\text{SPREAD}}^p \\
    \vdots & \vdots & \ddots & \vdots \\
    P_{\text{SPREAD}}^{N_{\text{SEED}} - K_{\text{SEED}}} & P_{\text{SPREAD}}^{N_{\text{SEED}} - K_{\text{SEED}} + 1} & \cdots & P_{\text{SPREAD}}^{N_{\text{SEED}} - K_{\text{SEED}}}
\end{bmatrix}$$

of dimension $\left(N_{\text{SPREAD}} (N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SPREAD}} N_{\text{SEED}}\right)$. Thus, this embodiment of the present invention can be used to describe an expanded LDPC code with sub-matrices of dimension $\left(N_{\text{SPREAD}} \times N_{\text{SPREAD}}\right)$ in the $(i, j)^{th}$ sub-matrix location consisting of the permutation matrix $P_{\text{SPREAD}}$ raised to the $F_{i,j}$ power (i.e. $P_{\text{SPREAD}}^{F_{i,j}}$).

[0040] The following is one particular example of the implementation of one embodiment of the present invention. In this example,

$$H_{\text{SEED}} = \begin{bmatrix}
    1 & 0 & 0 & 1 & 0 & 0 \\
    0 & 1 & 1 & 0 & 1 & 1 \\
    0 & 1 & 1 & 0 & 0 & 1 \\
    0 & 0 & 1 & 0 & 1 & 1
\end{bmatrix}, \text{ thus } N_{\text{SEED}} = 6,$$

while

$$P_{\text{SPREAD}}^1 = \begin{bmatrix}
    0 & 0 & 1 \\
    1 & 0 & 0 \\
    0 & 1 & 0
\end{bmatrix}, \text{ thus } N_{\text{SPREAD}} = 3.$$ 

[0041] Therefore, $p = 11$ is the smallest prime number that satisfies the example conditions $N_{\text{SEED}} + 2 \leq p$ and $N_{\text{SPREAD}} \leq p$. The interim and final exponent matrices as defined above can be:
\[ E_{\text{TRUNCATE}} = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 & 6 \\ 0 & 2 & 4 & 6 & 8 & 10 \\ \infty & 0 & 3 & 6 & 9 & 1 \\ \infty & \infty & 0 & 4 & 8 & 1 \end{bmatrix} \quad \text{and} \quad F = \begin{bmatrix} 1 & \infty & 4 & \infty & \infty \\ 0 & 2 & \infty & 6 & 8 & \infty \\ \infty & 0 & 3 & \infty & \infty & 1 \\ \infty & \infty & 0 & \infty & 8 & 1 \end{bmatrix}, \]

and the corresponding expanded LDPC matrix can be:

\[ H = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \]

[0042] One embodiment of a method for constructing irregularly structured LDPC codes according to the present invention is depicted in Figure 4. At step 100, an irregular "seed" parity check matrix \( H_{\text{SEED}} \) of dimension \((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}}\) can be constructed, being derived from an edge ensemble, \( \lambda_{\text{SEED}}(x) \) and \( \rho_{\text{SEED}}(x) \), with good asymptotic performance. In one embodiment, good asymptotic performance can be characterized by good threshold value using belief propagation decoding and good girth properties such as by having very few if no variable nodes with girth of 4. At step 110, a structured array exponent matrix can be constructed, as shown below:

\[ E_{\text{ARRAY}} = \begin{bmatrix} E_{1,1} & E_{1,2} & \cdots & E_{1,p} \\ E_{2,1} & E_{2,2} & \cdots & E_{2,p} \\ \vdots & \vdots & \ddots & \vdots \\ E_{p,1} & E_{p,2} & \cdots & E_{p,p} \end{bmatrix} \quad \text{where} \quad E_{i,j} = (i-1)(j-1) \mod p \]

[0043] This matrix can be constructed using modulo arithmetic of a number \( p \) that can be at least the column dimension of the irregular "seed" parity check matrix and
the column dimension of the spreading permutation matrix. In other words, $N_{\text{SEED}} \leq p$ and $N_{\text{SPREAD}} \leq p$.

[0044] At step 120, the structured array exponent matrix can be transformed using a transform $T(E_{\text{ARRAY}})$ that may perform shifts, truncations, permutations, etc. operations to construct an exponent matrix of dimension $((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})$ from $E_{\text{ARRAY}}$. At step 130, a final exponential matrix can be constructed,

$$F_{\text{FINAL}} = \begin{bmatrix}
F_{1,1} & F_{1,2} & \cdots & F_{1,N_{\text{SEED}}} \\
F_{2,1} & F_{2,2} & \cdots & F_{2,N_{\text{SEED}}} \\
\vdots & \vdots & \ddots & \vdots \\
F_{(N_{\text{SEED}} - K_{\text{SEED}}),1} & F_{(N_{\text{SEED}} - K_{\text{SEED}}),2} & \cdots & F_{(N_{\text{SEED}} - K_{\text{SEED}}),N_{\text{SEED}}}
\end{bmatrix}$$

of dimension $((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})$ by replacing each one in $H_{\text{SEED}}$ with the corresponding element in the transformed structured array exponent matrix $T(E_{\text{ARRAY}})$ and each zero in $H_{\text{SEED}}$ with $\infty$. Thus, the elements of $F_{\text{FINAL}}$ belong to the set $\{0, 1, \ldots, p-1, \infty\}$.

[0045] At step 140, the expanded parity check matrix can be constructed,

$$H = \begin{bmatrix}
P_{1,1}^{E_{\text{SPREAD}}} & P_{1,2}^{E_{\text{SPREAD}}} & \cdots & P_{1,N_{\text{SEED}}}^{E_{\text{SPREAD}}} \\
P_{2,1}^{E_{\text{SPREAD}}} & P_{2,2}^{E_{\text{SPREAD}}} & \cdots & P_{2,N_{\text{SEED}}}^{E_{\text{SPREAD}}} \\
\vdots & \vdots & \ddots & \vdots \\
P_{(N_{\text{SPREAD}} - K_{\text{SEED}}),1}^{E_{\text{SPREAD}}} & P_{(N_{\text{SPREAD}} - K_{\text{SEED}}),2}^{E_{\text{SPREAD}}} & \cdots & P_{(N_{\text{SPREAD}} - K_{\text{SEED}}),N_{\text{SEED}}}^{E_{\text{SPREAD}}}
\end{bmatrix}$$

of dimension $(N_{\text{SPREAD}} (N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SPREAD}} N_{\text{SEED}})$ that describes the expanded LDPC code with sub-matrices of dimension $(N_{\text{SPREAD}} \times N_{\text{SPREAD}})$ in the $(i,j)^{th}$ sub-matrix location consisting of the permutation matrix $P_{\text{SPREAD}}$ raised to the $F_{i,j}$ power, i.e. $P_{i,j}^{E_{\text{SPREAD}}}$, where $F_{i,j}$ is the matrix element in the $(i,j)^{th}$ location of $F_{\text{FINAL}}$.

[0046] Figure 5 is an example of one embodiment of a rate 1/2 irregular parity-check matrix. Figure 6 is an example of one embodiment of a rate 2/3 irregular parity-check matrix. Figure 7 is an example of one embodiment of a rate 3/4 irregular parity-check matrix.
[0047] The foregoing description of embodiments of the present invention have been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the present invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the present invention. The embodiments were chosen and described in order to explain the principles of the present invention and its practical application to enable one skilled in the art to utilize the present invention in various embodiments and with various modifications as are suited to the particular use contemplated.
WHAT IS CLAIMED IS:

1. A method of generating an error correction codeword, the method comprising:
   constructing an irregular seed parity check matrix derived from an edge ensemble, the seed parity check matrix having a column dimension and a row dimension;
   constructing a structured array exponent matrix using modulo arithmetic of a number equal to or greater than the seed parity check matrix column dimension;
   constructing a final exponential matrix by replacing each one in the seed parity check matrix with the corresponding element from the structured array exponent matrix and each zero in the seed parity check matrix with infinity; and expanding the final exponential matrix to form a parity check matrix corresponding to the error correction code.

2. The method of claim 1 further comprising transforming the structured array exponent matrix prior to constructing the final exponential matrix.

3. The method of claim 2, wherein transforming the structured array exponent matrix comprises performing shift, truncation, and/or permutation operations on the structured array exponent matrix.

4. The method of claim 1 further comprising constructing a set of permutation matrices, wherein the permutation matrices are used to expand the final exponential matrix.

5. The method of claim 4 wherein the set of permutation matrices comprises \( \{ P_{\text{Spread}}^0, P_{\text{Spread}}^1, P_{\text{Spread}}^2, \ldots, P_{\text{Spread}}^{p-1} \} \) and each permutation matrix in the set of permutation matrices comprises a matrix of dimension \( (N_{\text{Spread}} \times N_{\text{Spread}}) \) where \( N_{\text{Spread}} \) comprises a column dimension of each permutation matrix, \( p \) is a positive integer, \( P_{\text{Spread}}^\infty = 0 \) is the all zeros matrix,
6. The method of claim 5, wherein the error correction codeword includes a number of information bits and a length and wherein the seed parity check matrix comprises $H_{\text{SEED}}$ of dimension $((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})$, wherein $K_{\text{SEED}}$ is the number of information bits of the error correction codeword and $N_{\text{SEED}}$ is the resulting error correction codeword length.

7. The method of claim 6, wherein the structured array matrix comprises

$$E_{\text{ARRAY}} = \begin{bmatrix}
E_{1,1} & E_{1,2} & \cdots & E_{1,p} \\
E_{2,1} & E_{2,2} & \cdots & E_{2,p} \\
\vdots & \vdots & \ddots & \vdots \\
E_{p,1} & E_{p,2} & \cdots & E_{p,p}
\end{bmatrix},$$

where $E_{i,j} = (i-1)(j-1) \mod p$, where $p$ is greater than or equal to the column dimension of the seed parity check matrix and the column dimension of each permutation matrix.

8. The method of claim 7 wherein the final exponential matrix comprises

$$F_{\text{FINAL}} = \begin{bmatrix}
F_{1,1} & F_{1,2} & \cdots & F_{1,N_{\text{SEED}}} \\
F_{2,1} & F_{2,2} & \cdots & F_{2,N_{\text{SEED}}} \\
\vdots & \vdots & \ddots & \vdots \\
F_{(N_{\text{SEED}} - K_{\text{SEED}}),1} & F_{(N_{\text{SEED}} - K_{\text{SEED}}),2} & \cdots & F_{(N_{\text{SEED}} - K_{\text{SEED}}),N_{\text{SEED}}}
\end{bmatrix}$$

of dimension $((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})$ and the parity check matrix

$$H = \begin{bmatrix}
P_{1,1}^{F_{1,1}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & P_{1,2}^{F_{1,2}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & \cdots & P_{1,N_{\text{SEED}}}^{F_{1,N_{\text{SEED}}}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} \\
P_{2,1}^{F_{2,1}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & P_{2,2}^{F_{2,2}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & \cdots & P_{2,N_{\text{SEED}}}^{F_{2,N_{\text{SEED}}}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} \\
\vdots & \vdots & \ddots & \vdots \\
P_{N_{\text{SEED}}}^{F_{N_{\text{SEED}},1}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & P_{N_{\text{SEED}},2}^{F_{N_{\text{SEED}},2}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}} & \cdots & P_{N_{\text{SEED}},N_{\text{SEED}}}^{F_{N_{\text{SEED}},N_{\text{SEED}}}^{(N_{\text{SEED}} - K_{\text{SEED}}),1}}
\end{bmatrix}$$

of dimension $(N_{\text{SPREAD}}(N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SPREAD}} N_{\text{SEED}})$ describing a low density parity check code with sub-matrices of dimension $(N_{\text{SPREAD}} \times N_{\text{SPREAD}})$ in the $(i,j)_{th}$ sub-matrix location consisting of a permutation matrix $P_{\text{SPREAD}}$ raised to the $F_{i,j}$ power, where $F_{i,j}$ is the matrix element in the $(i,j)_{th}$ location of $F_{\text{FINAL}}$. 

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9. The method of claim 5, wherein \( p \) is a prime number.

10. A computer program product for generating an error correction codeword, the method comprising:
    computer code for constructing an irregular seed parity check matrix derived from an edge ensemble, the seed parity check matrix having a column dimension and a row dimension;
    computer code for constructing a structured array exponent matrix using modulo arithmetic of a number equal to or greater than the seed parity check matrix column dimension;
    computer code for constructing a final exponential matrix by replacing each one in the seed parity check matrix with the corresponding element from the structured array exponent matrix and each zero in the seed parity check matrix with infinity; and
    computer code for expanding the final exponential matrix to form a parity check matrix corresponding to the error correction code.

11. The computer code product of claim 10 further comprising computer code for transforming the structured array exponent matrix prior to constructing the final exponential matrix.

12. The computer code product of claim 11, wherein transforming the structured array exponent matrix comprises performing shift, truncation, and/or permutation operations on the structured array exponent matrix.

13. The computer code product of claim 10 further comprising computer code for constructing a set of permutation matrices, wherein the permutation matrices include a column dimension and the permutation matrices are used to expand the final exponential matrix.

14. The computer code product of claim 13, wherein the error correction codeword includes a number of information bits and a length and wherein the seed parity check matrix comprises \( H_{\text{seed}} \) of dimension \( (N_{\text{seed}} - K_{\text{seed}}) \times N_{\text{seed}} \),
wherein $K_{\text{SEED}}$ is the number of information bits of the error correction codeword and $N_{\text{SEED}}$ is the resulting error correction codeword length.

15. The computer code product of claim 14, wherein the structured array

$$
\begin{bmatrix}
E_{1,1} & E_{1,2} & \cdots & E_{1,p} \\
E_{2,1} & E_{2,2} & \cdots & E_{2,p} \\
\vdots & \vdots & \ddots & \vdots \\
E_{p,1} & E_{p,2} & \cdots & E_{p,p}
\end{bmatrix}
$$

where $E_{i,j} = (i-1)(j-1) \mod p$,

where $p$ is greater than or equal to the column dimension of the seed parity check matrix and the column dimension of the permutation matrices.

16. The computer code product of claim 15 wherein the final exponential matrix comprises

$$
\begin{bmatrix}
F_{1,1} & F_{1,2} & \cdots & F_{1,N_{\text{SEED}}} \\
F_{2,1} & F_{2,2} & \cdots & F_{2,N_{\text{SEED}}} \\
\vdots & \vdots & \ddots & \vdots \\
F_{(N_{\text{SEED}}-K_{\text{SEED}}),1} & F_{(N_{\text{SEED}}-K_{\text{SEED}}),2} & \cdots & F_{(N_{\text{SEED}}-K_{\text{SEED}}),N_{\text{SEED}}}
\end{bmatrix}
$$

of dimension $((N_{\text{SEED}}-K_{\text{SEED}}) \times N_{\text{SEED}})$ and the parity check matrix comprises

$$
\begin{bmatrix}
\mathbf{P}_{1,1}^{\text{SPREAD}} & \mathbf{P}_{1,2}^{\text{SPREAD}} & \cdots & \mathbf{P}_{1,N_{\text{SEED}}}^{\text{SPREAD}} \\
\mathbf{P}_{2,1}^{\text{SPREAD}} & \mathbf{P}_{2,2}^{\text{SPREAD}} & \cdots & \mathbf{P}_{2,N_{\text{SEED}}}^{\text{SPREAD}} \\
\vdots & \vdots & \ddots & \vdots \\
\mathbf{P}_{(N_{\text{SEED}}-K_{\text{SEED}}),1}^{\text{SPREAD}} & \mathbf{P}_{(N_{\text{SEED}}-K_{\text{SEED}}),2}^{\text{SPREAD}} & \cdots & \mathbf{P}_{(N_{\text{SEED}}-K_{\text{SEED}}),N_{\text{SEED}}}^{\text{SPREAD}}
\end{bmatrix}
$$

of dimension $(N_{\text{SPREAD}}(N_{\text{SEED}}-K_{\text{SEED}}) \times N_{\text{SEED}})$ describing a low density parity check code with sub-matrices of dimension $(N_{\text{SPREAD}} \times N_{\text{SPREAD}})$ in the $(i,j)^{th}$ sub-matrix location consisting of a permutation matrix $\mathbf{P}_{\text{SPREAD}}$ raised to the $F_{i,j}$ power, where $F_{i,j}$ is the matrix element in the $(i,j)^{th}$ location of $\mathbf{F}_{\text{FINAL}}$.

17. The computer code product of claim 15, wherein $p$ is a prime number.

18. An electronic device, comprising:

a processor; and

a memory unit operative connected to the processor and including:
computer code for generating an error correction codeword, the
computer code comprising:
   computer code for constructing an irregular seed parity check
matrix derived from an edge ensemble, the seed parity check matrix having a column
dimension and a row dimension;
   computer code for constructing a structured array exponent
matrix using modulo arithmetic of a number equal to or greater than the seed parity
check matrix column dimension;
   computer code for constructing a final exponential matrix by
replacing each one in the seed parity check matrix with the corresponding element
from the structured array exponent matrix and each zero in the seed parity check
matrix with infinity; and
   computer code for expanding the final exponential matrix to
form a parity check matrix corresponding to the error correction code.

19. The device of claim 18 further comprising computer code for
transforming the structured array exponent matrix prior to constructing the final
exponential matrix.

20. The device of claim 19, wherein transforming the structured array
exponent matrix comprises performing shift, truncation, and/or permutation
operations on the structured array exponent matrix.

21. The device of claim 18 further comprising computer code for
constructing a set of permutation matrices, wherein the permutation matrices include a
column dimension and the permutation matrices are used to expand the final
exponential matrix.

22. The device of claim 21, wherein the error correction codeword
includes a number of information bits and a length and wherein the seed parity check
matrix comprises $H_{\text{SEED}}$ of dimension $(N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}}$, wherein $K_{\text{SEED}}$ is
the number of information bits of the error correction codeword and $N_{\text{SEED}}$ is the
resulting error correction codeword length.
The device of claim 22, wherein the structured array matrix comprises
\[
\begin{bmatrix}
E_{1,1} & E_{1,2} & \cdots & E_{1,p} \\
E_{2,1} & E_{2,2} & \cdots & E_{2,p} \\
\vdots & \vdots & \ddots & \vdots \\
E_{p,1} & E_{p,2} & \cdots & E_{p,p}
\end{bmatrix},
\]
where \( E_{i,j} = (i-1)(j-1) \mod p \), where \( p \) is greater than or equal to the column dimension of the seed parity check matrix and the column dimension of the permutation matrices.

The device of claim 23 wherein the final exponential matrix comprises
\[
\begin{bmatrix}
F_{1,1} & F_{1,2} & \cdots & F_{1,N_{\text{SEED}}} \\
F_{2,1} & F_{2,2} & \cdots & F_{2,N_{\text{SEED}}} \\
\vdots & \vdots & \ddots & \vdots \\
F_{(N_{\text{SEED}}-k_{\text{SEED}}),1} & F_{(N_{\text{SEED}}-k_{\text{SEED}}),2} & \cdots & F_{(N_{\text{SEED}}-k_{\text{SEED}}),N_{\text{SEED}}}
\end{bmatrix}
\]
of dimension \(((N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SEED}})\) and the parity check matrix
\[
\begin{bmatrix}
P_{k_{\text{SEED}}}^{F_{1,1}} & P_{k_{\text{SEED}}}^{F_{1,2}} & \cdots & P_{k_{\text{SEED}}}^{F_{1,N_{\text{SEED}}}} \\
P_{k_{\text{SEED}}}^{F_{2,1}} & P_{k_{\text{SEED}}}^{F_{2,2}} & \cdots & P_{k_{\text{SEED}}}^{F_{2,N_{\text{SEED}}}} \\
\vdots & \vdots & \ddots & \vdots \\
P_{k_{\text{SEED}}}^{F_{(N_{\text{SEED}}-k_{\text{SEED}}),1}} & P_{k_{\text{SEED}}}^{F_{(N_{\text{SEED}}-k_{\text{SEED}}),2}} & \cdots & P_{k_{\text{SEED}}}^{F_{(N_{\text{SEED}}-k_{\text{SEED}}),N_{\text{SEED}}}}
\end{bmatrix}
\]
of dimension \((N_{\text{SPREAD}} (N_{\text{SEED}} - K_{\text{SEED}}) \times N_{\text{SPREAD}} N_{\text{SEED}})\) describing a low density parity check code with sub-matrices of dimension \((N_{\text{SPREAD}} \times N_{\text{SPREAD}})\) in the \((i,j)^{th}\) sub-matrix location consisting of a permutation matrix \(P_{\text{SPREAD}}\) raised to the \(F_{i,j}\) power, where \(F_{i,j}\) is the matrix element in the \((i,j)^{th}\) location of \(F_{\text{FINAL}}\).

The device of claim 34, wherein \(p\) is a prime number.
FIG. 7

\[ H_{\text{seed}, 56} = \begin{bmatrix}
10000000000001001000000100111100000000100100110111010
1100000000000001100111000000010000000001011011111
011000000000010010000001000001000001000001111101111
00110000000000010000000110000010000001111111111
0001100000000001100101010100100100100100101010110101
000110000000000100000010000001000100010100010101111110
00001100000000001000001000000100010011110111101
000001110000000000001000001100000111010101111001
000000110000000000000101001000000000100000010000101111111
000001100000000010000010000000100011101100000011
000000011000000100001010100100101000010100001100101111101
000000000000000110000001100000000001111011000001111110
0000000000000001000000100100000000010000000100001100101101101
00000000000001100000000100000000000111000000000011111111110
00000000000000011010000001000000000000011110101111111101
\end{bmatrix} \]
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER

IPC: see extra sheet
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: HO3M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE, DK, FI, NO classes as above

Electronic data base consulted during the international search (name of data base and, where practiseable, search terms used)

EPO-INTERNAL, WPI DATA, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
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</table>

Further documents are listed in the continuation of Box C.

See patent family annex.

Date of the actual completion of the international search
23 November 2005

Date of mailing of the international search report
30-11-2005

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<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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| A        | HAO ZHONG ET AL  
Design of VLSI implementation-oriented LDPC codes  
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IEEE 58 th  
Publication Date 6-9 Oct 2003  
Volume 1, pages 670-673  
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| A        | DHOLAKIA, A. ET AL  
Rate-compatible low-density parity-check codes for digital subscriber lines  
Communications,, 2004 IEEE International Conference on  
Publication Date: 20-24 June 2004  
Volumn 1, pages 415-419  
ISBN: 0-7803-8533-0  
See chapter II Rate compatibility of LDPC codes and chapter III Rate compatible array LDPC codes | 1-25 |
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| A        | SRIDHARAN, A. ET AL  
A construction for low density parity check convolutional codes based on quasi-cyclic block codes  
Publication Date: 2002, pages 481-  
Accession Number: 7651938  
See whole document | 1-25 |
<table>
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<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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Irregular Structured LDPC Codes  
IEEE 802.16 Broadband Wireless Access Working Group  
Date submitted 2004-08-17  
<http://ieee802.org/16>  
See whole document | 1-25 |