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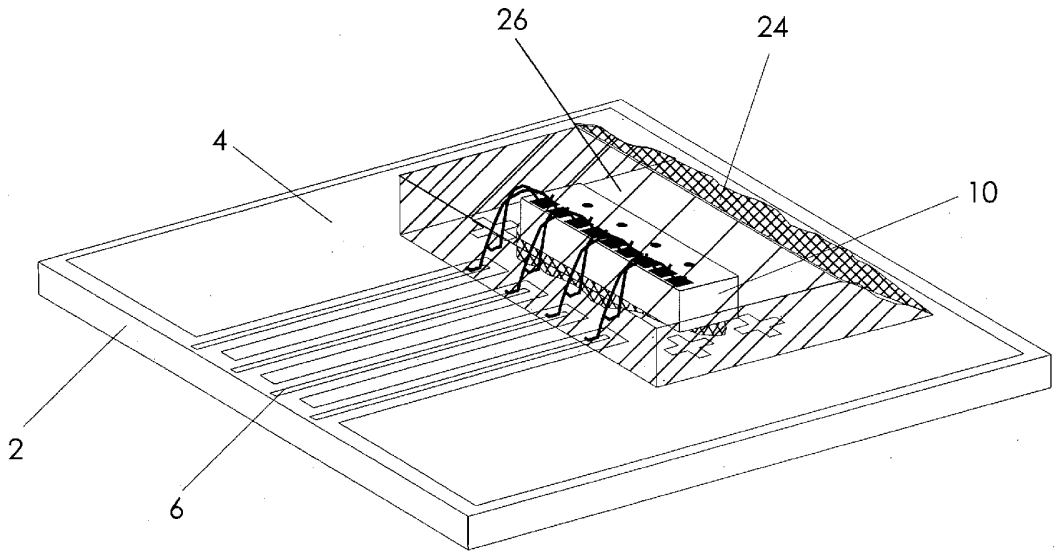
(54) Title: ENCAPSULATED OPTICAL PACKAGE



(57) Abstract: A method for providing an encapsulated optoelectronic chip is provided. The optoelectronic chip is secured on a substrate. A translucent coating substance is then applied on said optoelectronic chip and the translucent coating substance is then polished away to enable an optical coupling.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

ENCAPSULATED OPTICAL PACKAGE

TECHNICAL FIELD

[0001] This invention relates to the field of optical packages. More precisely, this invention pertains to the field of packaging and coupling an optoelectronic chip, namely the encapsulation of optoelectronic devices and the provision for creating an optically flat and transparent window above the active region(s) of the optoelectronic device.

BACKGROUND OF THE INVENTION

[0002] Optoelectronic systems are increasing in their application to electronic equipment. High performance computers and computer network components increasingly involve conversion of computer data signals to photonic signals for transmission from one device to another, while such photonic signals require conversion to electronic data signals for use in the recipient electronic device.

[0003] Coupling optoelectronic components to waveguides remains an awkward aspect of manufacturing optoelectronic systems. Optoelectronic components are manufactured as small as possible, and therefore coupling requires precision alignment of components to waveguides. At the same time, waveguides such as optical fibers are very fragile and require secure encapsulation for mechanical stability and endurance. It is also difficult to achieve such requirements while keeping the resulting volume of a coupling as small as possible, a parameter that can be very important, if not essential, in many applications.

[0004] The encapsulation of microelectronic chips is very well known in the art and is commonly used to protect microchips in all varieties of chip packages. The method commonly used is to use a plastic resin and drop a glob of the resin over the wirebonded microchip within its package. US Patent 4,819,041 granted April 4, 1989 and US Patent 5,313,365 granted May 17, 1994 both are good examples of methods used to encapsulate microchips within specific packages. These methods use types of plastic resins to fill a cavity where the microchip has been placed with (typically) opaque resin and without any

consideration for the surface profile of the resin. Other examples in the prior art describe transparent epoxies such as US Patent 6,075,911 granted June 13, 2000 and US Patent 6,269,209 granted July 31, 2001 are examples of transparent epoxy or silicon are used with optoelectronic device and optical fibers. These patents describe how the two elements are aligned and then subsequent to the alignment how the epoxy or silicon is injected between the optoelectronic device and the optical fiber to increase coupling and provide protection.

[0005] There are several prior-art references that are still patent pending that describe encapsulation of optoelectronics. US patent application Pub. No. US 2002/0001869 dated January 3, 2002 describes an encapsulation technique that uses a sacrificial layer over the encapsulated optoelectronic and includes methods for placing lenses over the open window, but does not describe a polishing method to reduce the thickness of the encapsulation, nor is alignment an issue. US patent application Pub. No. US 2002/0020803 dated February 21, 2002 describes a method of encapsulating an entire photodetector and support electronics in an over-molded type transparent resin that includes an embedded lens that allows for light to pass through the resin to the optoelectronic device. This prior-art also does not allow for 2-D alignment and does not include polishing to create the window. Finally, US patent application Pub. No. US 2002/0181899 dated December 5, 2002 discusses a method for imprinting a flat, but angled surface, on a transparent epoxy resin that encapsulated an optoelectronic device. The alignment method requires dowel pin alignment and is not amenable to polishing or 2-D alignment.

SUMMARY OF THE INVENTION

[0006] It is an object of the invention to provide a method for providing an encapsulated optoelectronic device.

[0007] According to a general aspect of the present invention, there is provided an assembly that can be treated the same way as other packaged microchips (for example: the placement of packaged chips on printed circuit boards) by encapsulating the optoelectronic device to form a complete package. However,

the main reason for the requirement of a flat, transparent window over the optoelectronic device package is to provide the possibility for coupling other optical devices (such as optical fibers) to the optoelectronic device. The flat, transparent window facilitates the alignment procedure used between the optoelectronic device package and a second assembly (fiber optic ferrule, lens array, laser, etc.). The second assembly can be placed on the flat surface and aligned to the optoelectronic with a maximum of 3-degrees of movement required (2-lateral and 1-rotational). This methodology is known as stackable (or 2-D) optics, and greatly simplifies the alignment procedure. A specific example of this alignment strategy involves a vertical cavity surface emitting laser (VCSEL) array chip with an array of linear parallel optical fibers. Once the VCSEL array chip has been encapsulated in a transparent resin, it has a window (or flat, transparent surface) created above the array of Lasers on the VCSEL chip. The surface is essentially co-planar with the surface of the VCSEL chip. The distance between the surface of the VCSEL chip and the flat, transparent surface is kept to a minimum, without exposing the VCSEL chip, so that a maximum amount of coupling into optical fibers is possible.

[0008] This arrangement offers several other beneficial aspects as well. The encapsulated optoelectronic device is hermetically sealed so that no moisture or contaminants can develop over the device. It is also more resilient to vibration, especially if wirebonding is used to connect to the optoelectronic device. The transparent resin can also reduce the divergence of the light emitted from the optoelectronic device (assuming a high index of refraction epoxy is used for the desired wavelength of light) and thereby allow for a longer physical distance for the same optical distance that the light can travel.

[0009] According to another aspect of the invention, there is provided a method for manufacturing an encapsulated optoelectronic package comprising an optoelectronic chip, comprising providing a substrate, securing an optoelectronic chip on the substrate, providing a translucent coating substance over the optoelectronic chip, and polishing the translucent coating substance to create planar surface over at least the optoelectronic chip, substantially parallel

to the substrate, wherein the planar surface over the optoelectronic chip provides an optical coupling window.

[0010] According to yet another aspect, the invention allows multiple parts to be manufactured at the same time. This involves providing an array of patterned substrates on a larger substrate, securing multiple optoelectronic chips to the substrates, electrically connecting all chips to their respective traces on their respective patterned substrates, providing a translucent coating substance over all of the optoelectronic chips and surrounding area, using a rigid squeegee to screen-print a precise amount of the translucent coating substance with a flattened surface over the chips, then masking certain regions and curing the translucent coating substance over other regions to produce planar surfaces with an optical coupling window over each optoelectronic chip.

[0011] The invention therefore also provides a method for manufacturing an optoelectronic package comprising an optoelectronic chip, comprising: providing a substrate; securing an optoelectronic chip on said substrate; applying a translucent coating substance, over at least a portion of the optoelectronic chip to create a planar surface, over at least said optoelectronic chip, substantially parallel to said substrate; and allowing said coating substance to harden; wherein said planar surface provides an optical coupling window for said optoelectronic chip.

[0012] According to still another aspect of the invention, there is provided an optoelectronic package comprising: a substrate; an optoelectronic chip mounted on said substrate; a translucent coating substance forming a planar surface, over at least a portion of said optoelectronic chip, substantially parallel to said substrate; and wherein said planar surface provides an optical coupling window for said optoelectronic chip.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Further features and advantages of the present invention will become apparent from the following detailed description, taken in combination with the appended drawings, in which:

[0014] Figs. 1a,b are a 3D perspective view and a top view of a substrate; the substrate comprises conductive trace lines and a location for receiving an optoelectronic chip;

[0015] Fig. 1c is a 3D perspective view of a standard Ceramic-Pin Grid Array (C-PGA) carrier with an optoelectronic device and transparent epoxy deposited in the open cavity;

[0016] Fig. 1d is a 3D perspective view of a custom carrier with the optoelectronic device on a separate block and a printed circuit board adjacent to the optoelectronic device;

[0017] Figs. 2a,b are a 3D perspective view and a top view of a substrate where an optoelectronic chip has been secured using electrically conductive epoxy;

[0018] Figs. 3a,b are a 3D perspective view and a top view of a substrate where a bump of transparent epoxy has been placed over the secured optoelectronic chip;

[0019] Fig. 4a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the bump of epoxy has been polished over said optoelectronic chip;

[0020] Fig. 5 is a diagram which shows a geometric determination of maximum polish height;

[0021] Figs. 6a,b a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where a protection plate surrounding the optoelectronic chip has been placed;

[0022] Figs. 7a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the protection plate surrounding the optoelectronic chip has been placed together with epoxy;

[0023] Figs 8a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip where the protection plate surrounding the optoelectronic chip has been placed together with polished epoxy; and

[0024] Figs. 9a,b are a 3D perspective view and a top view of a substrate with a secured optoelectronic chip with an optional removal of the protection plate.

[0025] Fig. 10a is a 3D perspective view of a optical ferrule over the packaged optoelectronic chip;

[0026] Fig. 10b is a 3D perspective view of a metallic layer coated over the optical ferrule and packaged optoelectronic chip;

[0027] Fig. 10c is a 3D perspective view of a plastic protection resin (glob-top) over the metal coated optical ferrule and packaged optoelectronic chip;

[0028] Fig. 11 is a 3D perspective view of an example 3x3 array of substrates where optoelectronic chips have been secured and wirebonded using electrically conductive epoxy and wirebonds, respectively;

[0029] Fig. 12 is a 3D perspective view of the 3x3 array of substrates with a raised border surrounding;

[0030] Fig. 13 is a 3D perspective view of the 3x3 array of substrates with an optically transparent encapsulating material deposited over the entire area;

[0031] Fig. 14 is a 3D perspective view of the screen-printing process of dragging a rigid squeegee or edge over the optically transparent encapsulating material to produce a thin, flat layer that covers the optoelectronic chips and wirebonds;

[0032] Fig. 15 is a 3D perspective view of the 3x3 array with an opaque mask placed over the optically transparent encapsulating material;

[0033] Fig. 16 is a 3D perspective view of several regions of hardened optically transparent encapsulating material; and

[0034] Fig. 17 is a 3D perspective view of the 3x3 array having been divided into 9 individual encapsulated packages.

[0035] It will be noted that throughout the appended drawings, like features are identified by like reference numerals.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0036] The encapsulated optical package provides a simple method of producing an optical quality flat window over the active region of an optoelectronic device. The optical window is created perpendicularly to the direction of light emission/detection of the optoelectronic device.

[0037] In the case of an array of surface-emitting lasers , such as vertical cavity surface emitting laser (VCSEL) array chip, the window is created over the chip and is co-planar with the chip.

[0038] The optical window allows a method of alignment that eliminates several undesirable degrees of mechanical freedom. The flat, co-planar window restricts alignment to 2 lateral movements and one rotational movement (X, Y and θ_Z). Typically, there are 6 degrees of mechanical movement (X, Y, Z, θ_X, θ_Y, θ_Z).

[0039] Electrical trace lines that extend from the encapsulated optoelectronic device to an external electrical connection, such as bond-fingers or a press-fit connector, provide the electrical access to the optoelectronic device.

[0040] In some embodiments, the optoelectronic device is first bonded onto the substrate using an electrically and thermally conductive epoxy. The exact placement of the optoelectronic chip with respect to the substrate can be done with low positional accuracy. It is one aspect of this invention that allows the subsequent alignment of optical fibers, lenses, or other optical components to the packaged optoelectronic device to be the critical alignment step for both the lateral and rotational position. Once optical fibers, lenses, or other optical components are aligned and fixed over the packaged optoelectronic device, the far-end of the optical fibers, lenses, or other optical components becomes the optical reference surface and the electrical connections on the substrate must accommodate any positional error.

[0041] This packaging method also hermetically seals the optoelectronic chip so that it is not susceptible to humidity. Also, since the chip is encapsulated, its tolerance to mechanical vibration is greatly increased.

[0042] By encapsulating using a transparent material with a high refractive index, the divergence angle of the light-emitting device is decreased, allowing for a better coupling efficiency.

[0043] **First preferred embodiment – polished transparent epoxy**

[0044] As shown in Figures 1a and 1b, the substrate (2) is the mechanical support for the assembly. It carries all of the elements and is used to electrically access the optoelectronic chip. There are many possible configurations for the chip carrier. The first is to use off-the-shelf pin grid array (PGA) chip carriers that have an inner cavity where the optoelectronic is placed and outer connection pins which are plugged into the PCB as shown in **Figure 1c**. Transparent epoxy would be placed in the inner cavity over the optoelectronic chip and then polished flat. A second version, as shown in **Figures 1a and 1b** is a more custom approach and could be based on patterning gold on an alumina substrate. A thin gold layer can typically be deposited on a flat aluminum oxide wafer or chip onto which the optoelectronic can be glued and wirebonded. As implied in the preferred embodiment, the external electrical connections to this custom-made chip carrier would allow, preferably, a second set of wirebonds from the substrate to an external PCB to take up the slack for any initial misalignment of the optoelectronic device with respect to the substrate. A third version is another custom approach that uses PCB technology and a small form connector to create the chip carrier as shown in **Figure 1d**. The PCB **(3)** consists of trace lines **(5)** and a card-edge or similar electrical connection **(7)**. The optoelectronic is placed on a metallic heat sink **(9)** over which the PCB is placed and bonded. The primary gain of this type of carrier is its adaptable geometry and its heat-sinking capabilities. The steps described below involving transparent epoxy and polishing could all be equally applied to any of these mentioned arrangements of chip packages.

[0045] In the following embodiment, the chip carrier will be based on the second version, as shown in **Figures 1a,b**, described above based on the gold patterned alumina substrate. The Encapsulated Optical Package consists of 5 elements. The elements are described as a substrate (or carrier package), transparent epoxy, electrically conductive epoxy, wirebonds, and an optoelectronic chip.

[0046] The custom-made alumina substrate is on the order of 1.5-cm x 1.5-cm x 0.2-cm in size. The top of the alumina substrate is patterned with a set of parallel gold trace lines **(6)** that start near the center of the substrate and end near one side of the substrate. The rest of the substrate, outside the trace lines is patterned with a continuous layer of gold **(4)** with alignment marks **(8)** for the placement of the optoelectronic chip. Preferably, the gold thickness and quality is amenable to wedge or ball wirebonding. The trace lines are used to transmit electrical signals from the perimeter of the substrate to the middle of the substrate where the chip will be placed as shown in **Figures 2a,b**.

[0047] The optoelectronic chip **(10)** is placed near the middle of the substrate on a portion of the gold layer, within a reasonable distance for wirebonding from the tips of the trace lines. The emitting device, such as a vertical cavity laser **(12)**, or a detecting device, such as a photodetector, is oriented so that its direction of operation is normal to the substrate for vertical coupling of the light, although side-launched optoelectronic device may also be contemplated. The exact placement of the chip is not critical, as long as the chip can be properly wirebonded to the trace lines. The chip is epoxied in place using electrically conductive epoxy **(16)** and is then wirebonded to the trace lines. Preferably, the wirebonds **(14)** are made as flat as possible so that their peaks are no more than 30-40-microns above the surface of the chip. Since the chip is higher than the trace lines, low wirebonds will be possible. For simplicity, and for when the chip has a common cathode, or anode, on its backside, the trace lines for the common, or ground, potential may be connected directly to the area below the chip as shown in **Figures 2a,b**.

[0048] A transparent epoxy is then used that will harden using time, heat, or UV-light with a sufficiently high hardness factor so that it can be polished. Preferably, the epoxy has sufficient viscosity before being set so that it does not spread out over the surface too quickly. The following epoxies were found to be well suited to this application: Dymax (model: OP-4-20632), Dexter (model: Hysol CNB753-42) and Eques (model: UV Laquer 1322 000 40045). These epoxies do not limit this application but only serve as examples of epoxies that have shown good properties in terms of wavelength, hardness, durability and moisture resistance.

[0049] The epoxy is deposited carefully over the optoelectronic chip, so not to damage the wirebonds. Preferably, the epoxy forms a somewhat convex bump **(18)** over the optoelectronic chip that completely encapsulates both the chip and the wirebonds, as shown in **Figures 3a,b**. Preferably, the epoxy does not cover the distant ends of the trace lines so that the chip can still be accessed electrically.

[0050] The whole package is then placed on a polishing machine so that the bump of epoxy faces the polishing paper. Preferably, standard lapping and polishing techniques are applied, including progressively finer grits of polishing paper, correct timing, appropriate slurry mixtures, and a method of holding the parts in a rigid manner. Preferably, the polishing is stopped before the wirebonds or optoelectronic chip are damaged and an optically flat window **(20)**, that is co-planar with the surface of the optoelectronic device and chip substrate is formed. A thin, transparent layer of epoxy will remain over the chip as shown in **Figures 4a,b**.

[0051] The maximum distance above an optoelectronic chip before optical crosstalk would occur can be calculated, as shown in **Figure 5**. For a light emitter such as a VCSEL, the epoxy index of refraction "n_e", the pitch of the light emitting devices on the optoelectronic chip "p", and the open-air full divergence angle "θ" in radians of the light source determines the maximum usable height of the epoxy above the chip:

[0052] Max. height=(p/2)*(1/tan((θ/2)/n_e)

[0053] For example, if p=250-microns, θ=28-degrees=0.4887-rad, and n_e=1.5, max. height is equal to 760.5-microns. However, distances as low as 50-microns are also desirable to couple the maximum amount of light into optical fiber.

[0054] **Alternative embodiment – polished transparent epoxy with removable protection plate**

[0055] To aid in the process of polishing the transparent epoxy and/or to aid in containing the epoxy within a more confined volume on the substrate (2) around the chip (10), an intervening step can be performed.

[0056] The chip carrier, the chip, and the wirebonds are identical to the first preferred embodiment. However, before the transparent epoxy is placed over the chip, a frame or protection plate can be introduced. The protection plate **(22)** would typically have a hole or notch such that when it was placed on the chip carrier, it would surround the optoelectronic chip and the wirebonds. As shown in **Figures 6a,b**, the protection plate could be made of various materials (glass, plastic, etc.) and would offer protection to the optoelectronic chip during the polishing procedure.

[0057] The thickness of the protection plate could be chosen to be slightly higher that the optoelectronic chip and wirebonds, and be of a material that would polish less quickly than the transparent epoxy. This would help ensure that the optoelectronic chip was not damaged. Depending on the protection plate material, and the method of depositing the epoxy, the plate could be either removed, in some manner, or left in place. Preferably, the plate is also non-conductive or at least insulated from the trace lines on the substrate, and allows access to the distant ends of the trace lines for electrical access to the optoelectronic chip.

[0058] The transparent epoxy is then injected into the open hole, or notch, over the optoelectronic chip provided by the protection plate. Enough epoxy **(24)** is

used to completely encapsulate the chip and form a rounded surface of epoxy that is higher than the protection plate as shown in **Figures 7a,b**. The epoxy is then time, heat or UV cured.

[0059] The assembly is then placed up side down on a polishing machine so that the protection plate and the epoxy face the polishing surface. The epoxy is polished until it is level with the protection plate and an optically flat window **(26)**, that is co-planar with the chip and the substrate, is formed over the optoelectronic chip. Preferably, standard lapping and polishing techniques are applied, including progressively finer grits of polishing paper, de-ionized water, correct timing, appropriate slurry mixtures, and a method of holding the parts in a rigid manner as shown in **Figures 8a,b**.

[0060] The resulting effect is shown in **Figures 9a,b**, when the protection plate is removed.

[0061] **Assembly – Complete Encapsulation Methods:**

[0062] Ultimately, the encapsulated optical package must be placed into a useful support structure that allows access to the optical input or output and the electrical input or output. This requires that the encapsulated optical package be itself packaged in a second tier package (such as a transceiver housing) that may involve further encapsulation for mechanical stability and to protecting the transparent epoxy from moisture absorption or other contaminates. A standard method for sealing transparent epoxies is proposed in US patent 6,269,209 and US patent 6,075,911, both use resin barriers over their transparent epoxies to eliminate moisture absorption.

[0063] Although these referenced US patents may serve to protect against moisture, in the above embodiments, the use of a sufficiently moisture resistant resin or epoxy is assumed. Such epoxies were outlined above.

[0064] However, further to this patent disclosure is a method that allows for moisture resistance, electromagnetic interference protection and mechanical stability over the encapsulated optical package.

[0065] As shown in **Figure 10a**, an optical ferrule **(28)** has been placed over the encapsulated optical package of **Figure 8a**.

[0066] As shown in **Figure 10b**, the area over the transparent epoxy where the 45-degree beveled optical fibers **(30)** exist has been coated with a metallic layer **(32)**, preferably by selective masking and gold evaporation techniques, so that: 1) the transparent epoxy is protected from moisture, 2) the optoelectronic is electromagnetically shielded when the shield is grounded, and 3) a metallic mirror is formed over the beveled optical fibers to aid in optical reflection into the optical fiber.

[0067] Finally, the entire assembly is coated in a protective standard thermoplastic resin **(34)** to mechanically bond the parts within a larger assembly as shown in **Figure 10c**.

[0068] **Volume Manufacturability – Third Embodiment:**

[0069] Another embodiment of the desired encapsulated package that lends itself to volume manufacturability involves screen printing the optically transparent material over an array of optoelectronic chips.

[0070] The pattern for a single package as shown in **Figure 1a** is essentially replicated several times in an array pattern on a larger substrate as shown in **Figure 11**. An optoelectronic chip **(10)** is attached and wirebonded to the area just in front of the parallel gold trace lines **(4)**.

[0071] The entire large substrate is then placed in an assembly rig **(36)** that has slightly higher borders **(38)** than the substrate and the optoelectronic chip as shown in **Figure 12**. If the substrate is 1-mm thick and the optoelectronic chip is 0.15-mm thick, then the border **(38)** should be approximately 1.25-mm thick to allow for a 0.1-mm layer over the top of the chip including the allowance for the loop height of the wedge wirebond.

[0072] Once the substrate is fixed into the assembly rig, the transparent optical material **(40)**, such as the epoxy OG142-17 from Epoxy Technology Inc., can be liberally applied over the surface of the substrate as in **Figure 13**. Some care

must be taken not to disturb the wirebonds, but this can usually be accomplished by gently pouring the epoxy around and then over the chip and wirebonds. The epoxy can be worked, or squeegeed, multiple times using a tool having a flat edge **(42)** (e.g., squeegee) until the surface has the desired flatness and is free of defects, more epoxy can be added over the area as well during the squeegee process as in **Figure 14**.

[0073] In the next step, once the epoxy has been flattened and covers all the parts uniformly, the assembly rig and substrate are covered with a mask **(44)** as in **Figure 15**. The mask is typically a rigid glass plate that has opaque areas and transparent areas. The transparent regions of the mask are then centered over regions containing the optoelectronic chips and the opaque regions of the mask are centered over the regions where the bonding fingers are present. The goal is to harden the epoxy over the optoelectronic chips to create the flat optical windows **(46)**, but leave the bonding fingers exposed to air as shown in **Figure 16**. Once the epoxy has hardened, the unexposed epoxy can be washed away using ethanol or other gentle cleaning solutions and what remains is the flat encapsulating windows above the chips.

[0074] The array can then be cut, diced, snapped or broken into its individual packages **(50)** as shown in **Figure 17**. Two preferred methods of separating these parts are 1) using a wafer dicing saw and cutting each part out of the array, and 2) using pre-cuts or scoring trenches **(48)** under the substrate so that the parts can be snapped apart.

[0075] The embodiments of the invention described above are intended to be exemplary only. The scope of the invention is therefore intended to be limited solely by the scope of the appended claims.

WE CLAIM:

1. A method for manufacturing an optoelectronic package comprising an optoelectronic chip, comprising:

providing a substrate;

securing an optoelectronic chip on said substrate;

providing a translucent coating substance over the optoelectronic chip; and

polishing the translucent coating substance to create a planar surface, over at least said optoelectronic chip, substantially parallel to said substrate;

wherein said planar surface provides an optical coupling window for said optoelectronic chip.

2. The method as claimed in claim 1, further comprising the step of providing a frame on said substrate, surrounding at least one part of the optoelectronic chip, wherein the translucent coating substance is surrounded by said frame, further wherein the coating substance has a lower hardness than said frame.

3. The method as claimed in claim 1 or 2, wherein the polishing of said substrate is performed using a precision machine.

4. The method as claimed in any one of claims 1 to 3 , further comprising the step of securing the optoelectronic chip on said substrate using an electrically conductive substance to provide one electrical connection between said chip and said substrate.

5. The method as claimed in claim 4, wherein the electrically conductive substance is electrically conductive epoxy.

6. The method as claimed in any one of claims 1 to 5, further comprising the step of connecting each input pins of the provided optoelectronic chip to a trace line on said substrate.

7. The method as claimed in claim 6, wherein said connecting said input pins to said trace lines comprises using wire bonding.

8. The method as claimed in claim 6, wherein said substrate comprises ceramic.

9. The method as claimed in claim 6, further comprising a step of connecting said trace lines near a periphery of said substrate to corresponding trace lines on a printed circuit board.

10. The method as claim in any one of claims 1 to 9, wherein the translucent coating substance comprises transparent epoxy.

11. The method as claimed in claim 1 or 2, wherein the translucent coating substance is applied in liquid form as a bead over said optoelectronic chip and is allowed to harden.

12. The method as claimed in claim 11, wherein the translucent coating substance encapsulates said optoelectronic chip, further comprising the step of buffing said planar surface.

13. The method as claimed in claim 12, wherein said optoelectronic chip is wirebonded to said substrate, and said translucent coating substance encapsulates wirebonds of said chip.

14. The method as claimed in claim 11, further comprising the step of buffing said planar surface.

15. The method as claimed in claim 12, wherein the translucent coating substance comprises moisture-resistant transparent epoxy.

16. The method as claimed in any one of claims 1 to 15, further comprising the steps of: optically and mechanically coupling on said window one of an optical ferrule, optical component and an optoelectronic component to said optoelectronic chip; coating said package with a metallic layer to provide shielding; and coating said metallic layer with a protective material.

17. The method as claimed in claim 16, wherein an optical ferrule is coupled, said ferrule having a beveled end providing a reflective surface for at least one optical fiber of said ferrule, said metallic coating ensuring a reflective property of said beveled end.

18. A method for manufacturing an optoelectronic package comprising an optoelectronic chip, comprising:

providing a substrate;

securing an optoelectronic chip on said substrate;

applying a translucent coating substance, over at least a portion of the optoelectronic chip to create a planar surface, over at least said optoelectronic chip, substantially parallel to said substrate; and

allowing said coating substance to harden;

wherein said planar surface provides an optical coupling window for said optoelectronic chip.

19. The method as in claim 18, further comprising providing borders around at least part of said optoelectronic package to retain said substance.

20. The method as in claim 18 or 19, wherein allowing said coating substance to harden comprises curing said coating substance.

21. The method as in claim 20, further comprising masking regions of said coating substance prior to said curing.

22. The method as in claim 21, further comprising removing portions of said coating substance that are uncured.

23. The method as in any one of claims 18 to 22, further comprising flattening said substance to create said planar surface.

24. The method as in claim 18, further comprising providing more than one optoelectronic chip, said optoelectronic chips forming a chip array.

25. The method as in claim 24, further comprising providing borders around at least part of said chip array to retain said substance.

26. The method as in claim 24 or 25, wherein allowing said coating substance to harden comprises curing said coating substance.

27. The method as in claim 26, further comprising masking regions of said coating substance prior to said curing.

28. The method as in claim 27, further comprising removing portions of said coating substance that are uncured.

29. The method as in any one of claims 25 to 28, further comprising flattening said substance to create said planar surface.

30. The method as in any one of claims 25 to 29, further comprising separating said optoelectronic chips.

31. The method as in any one of claims 18 to 30, wherein the translucent coating substance comprises transparent epoxy.

32. The method as in any one of claims 18 to 30, wherein the translucent coating substance comprises moisture resistant transparent epoxy

33. An optoelectronic package comprising

a substrate;

an optoelectronic chip mounted on said substrate;

a translucent coating substance forming a planar surface, over at least a portion of said optoelectronic chip, substantially parallel to said substrate; and

wherein said planar surface provides an optical coupling window for said optoelectronic chip.

34. The optoelectronic package as in claim 33, wherein said planar surface comprises at least one of a polished planar surface and a screen-printed planar surface.

35. The optoelectronic package as in any one of claims 33 to 34, wherein the translucent coating substance comprises transparent epoxy.

36. The optoelectronic package as in any one of claims 33 to 34, wherein the translucent coating substance comprises moisture resistant transparent epoxy

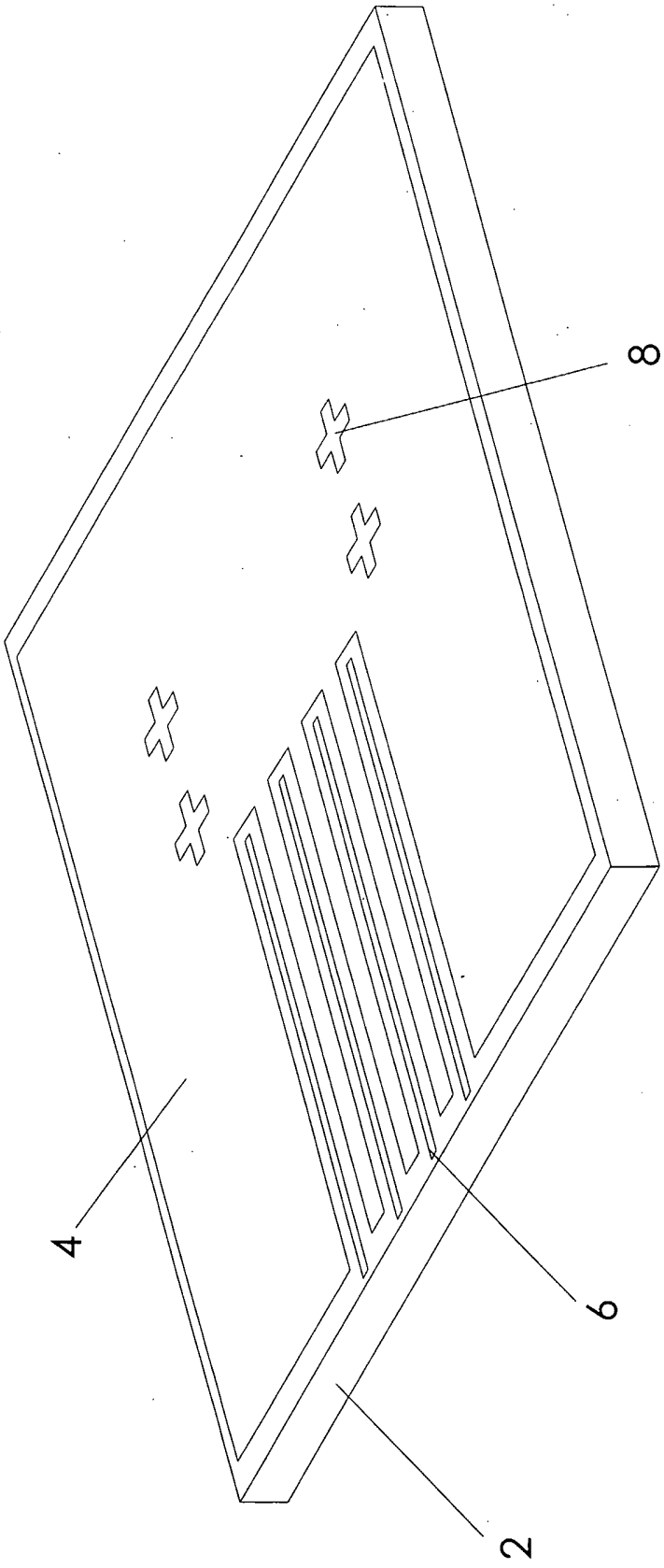

Fig. 1a

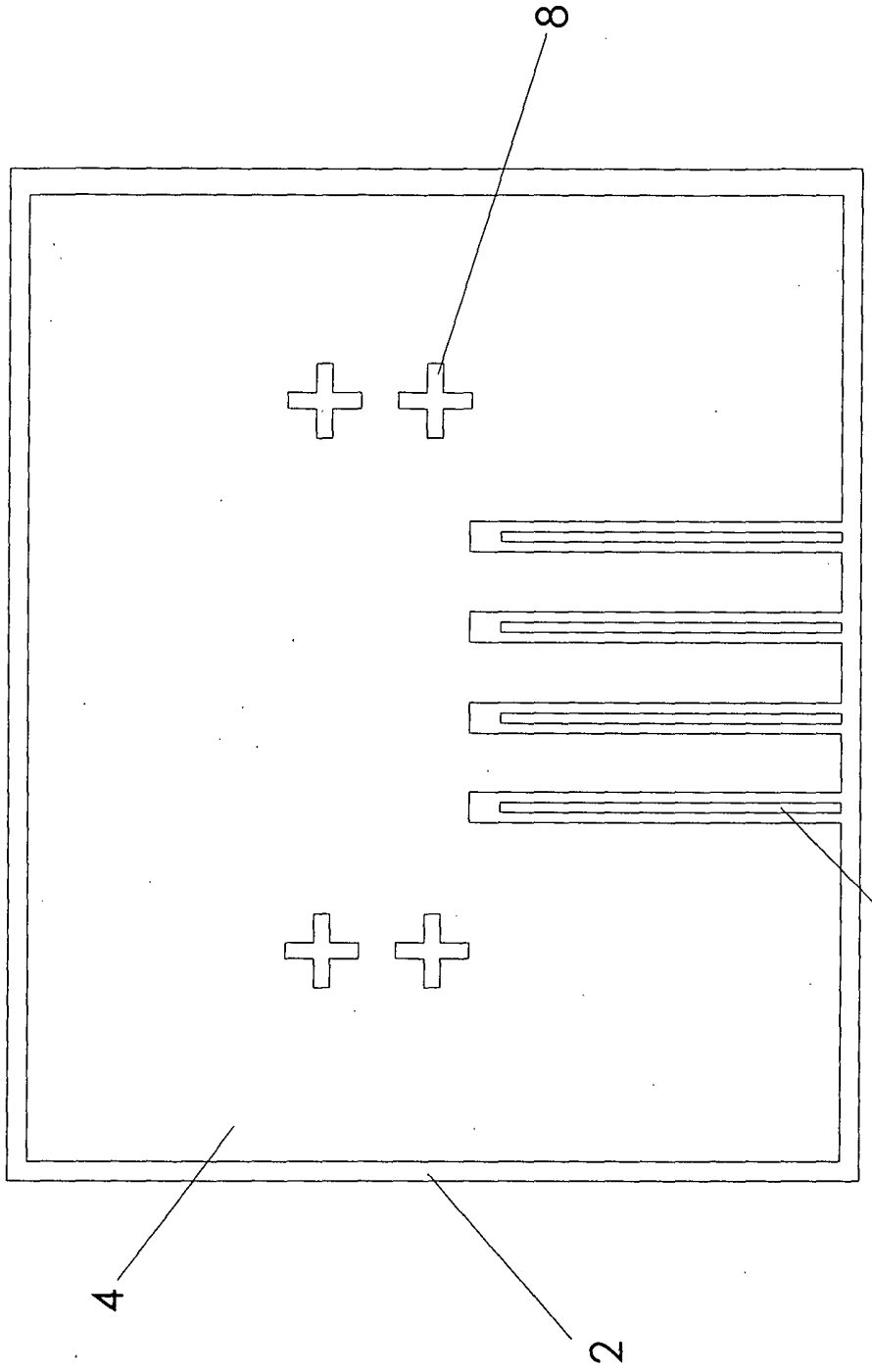

Fig.1b

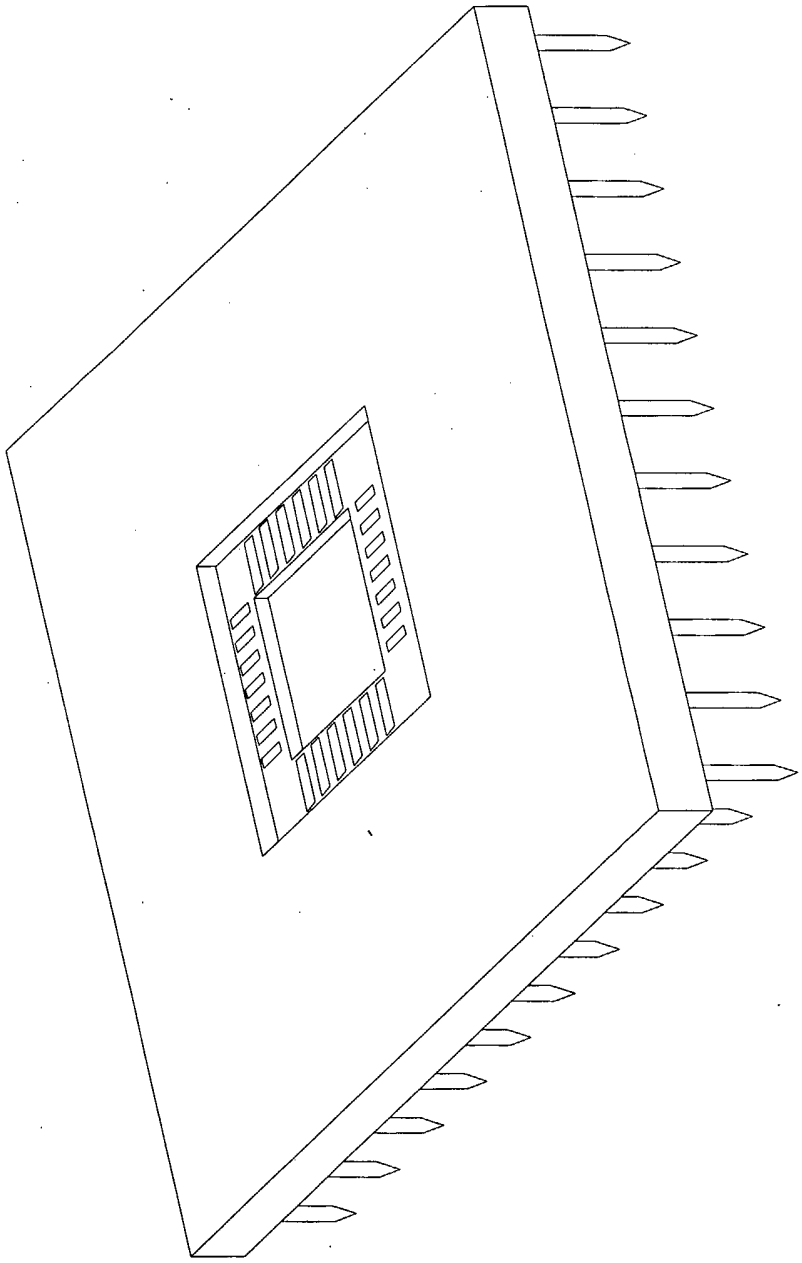

Fig. 1c

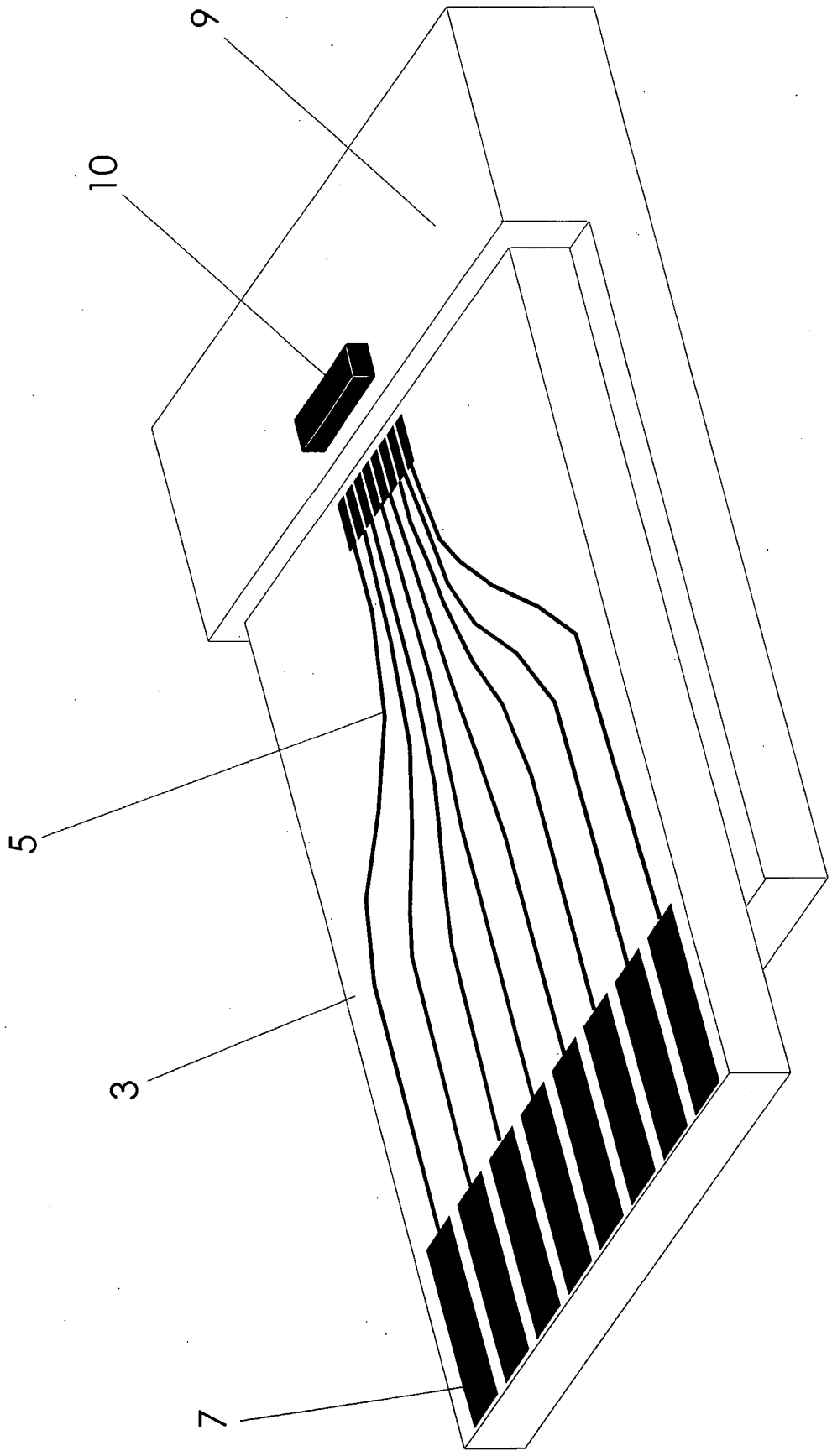

Fig. 1d

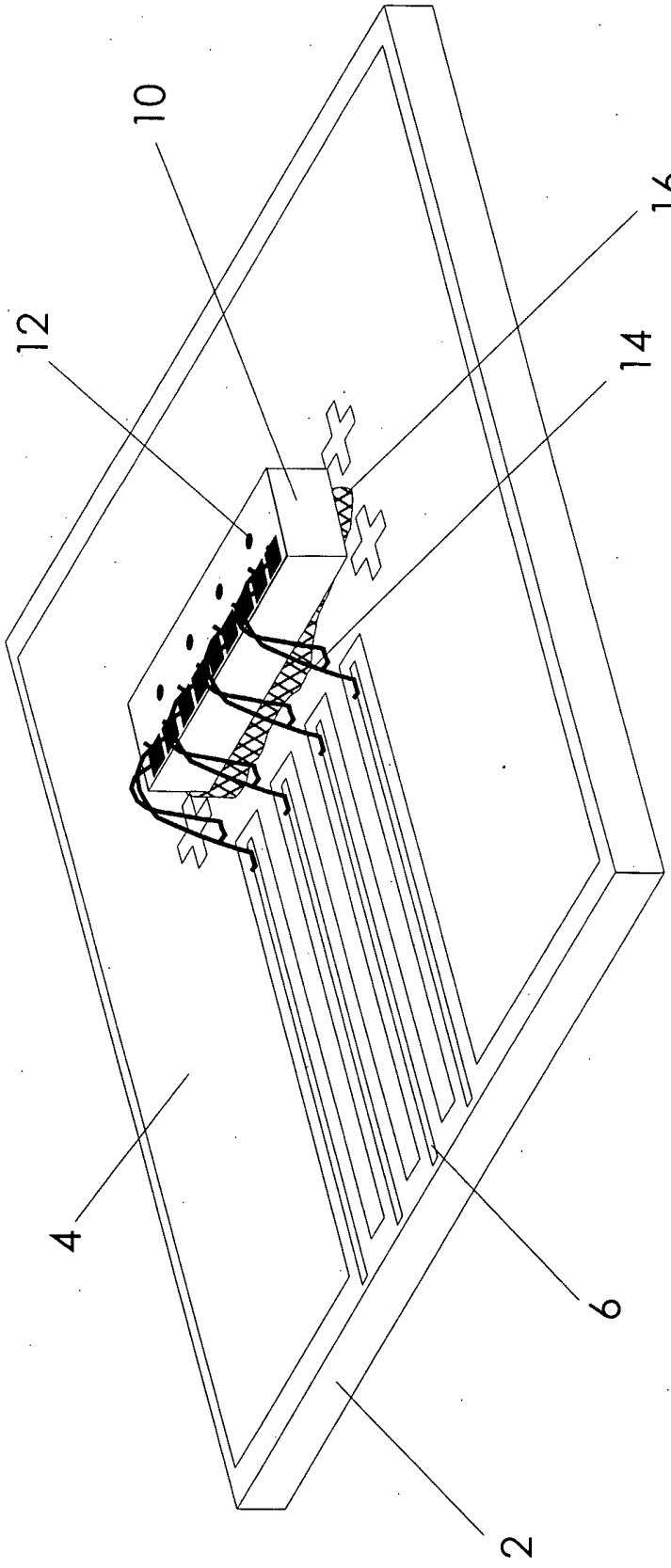

Fig.2a

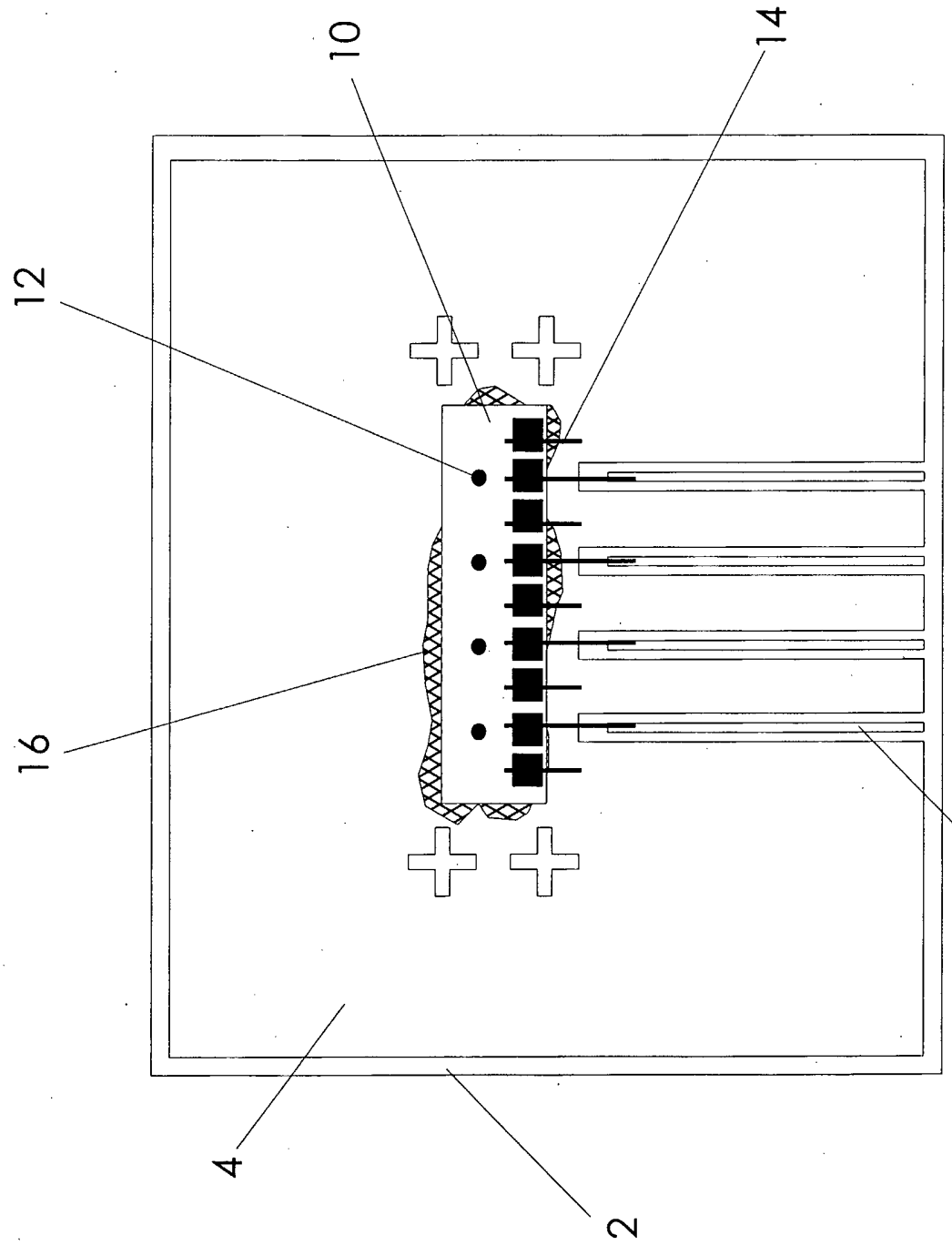

Fig. 2b

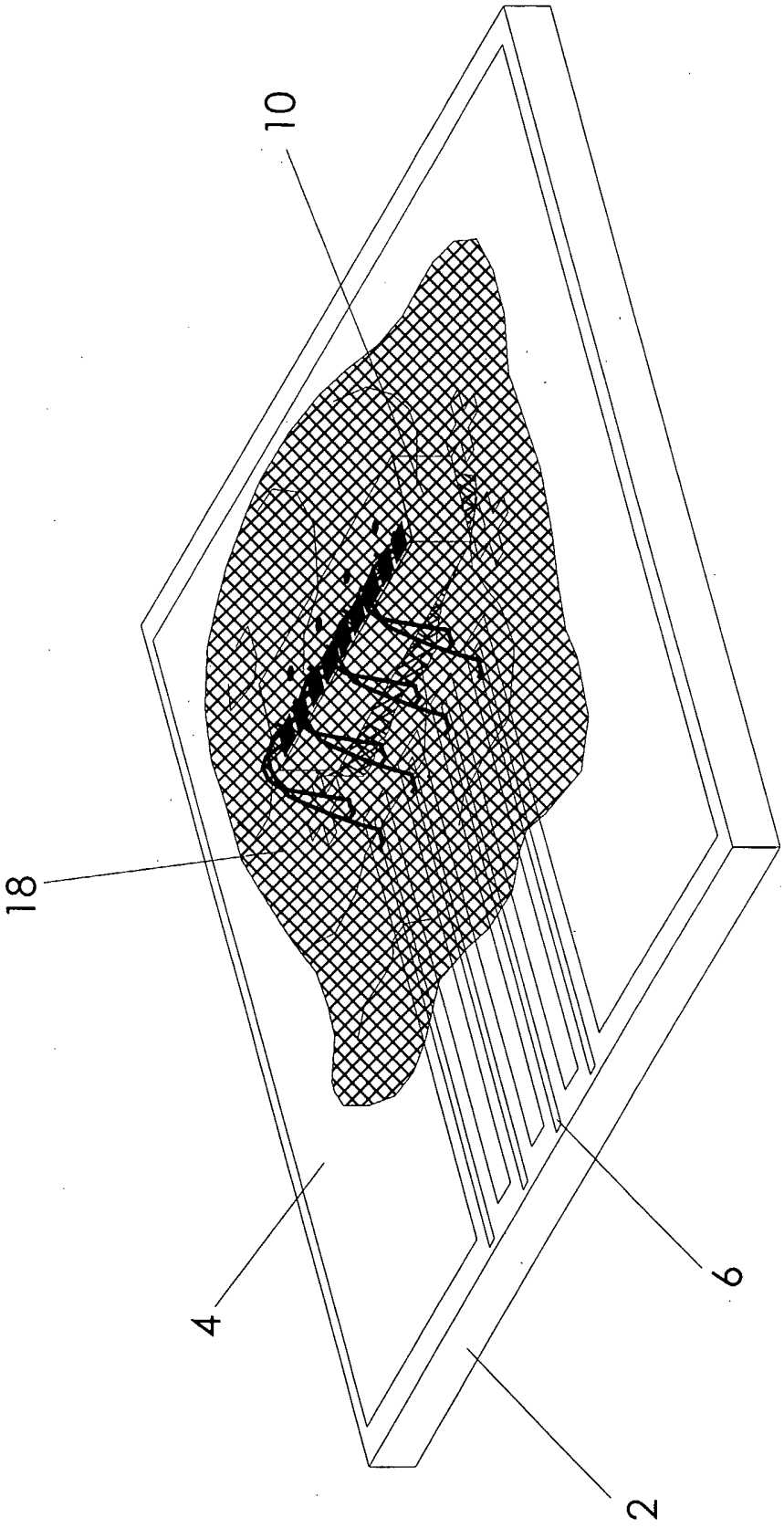

Fig. 3a

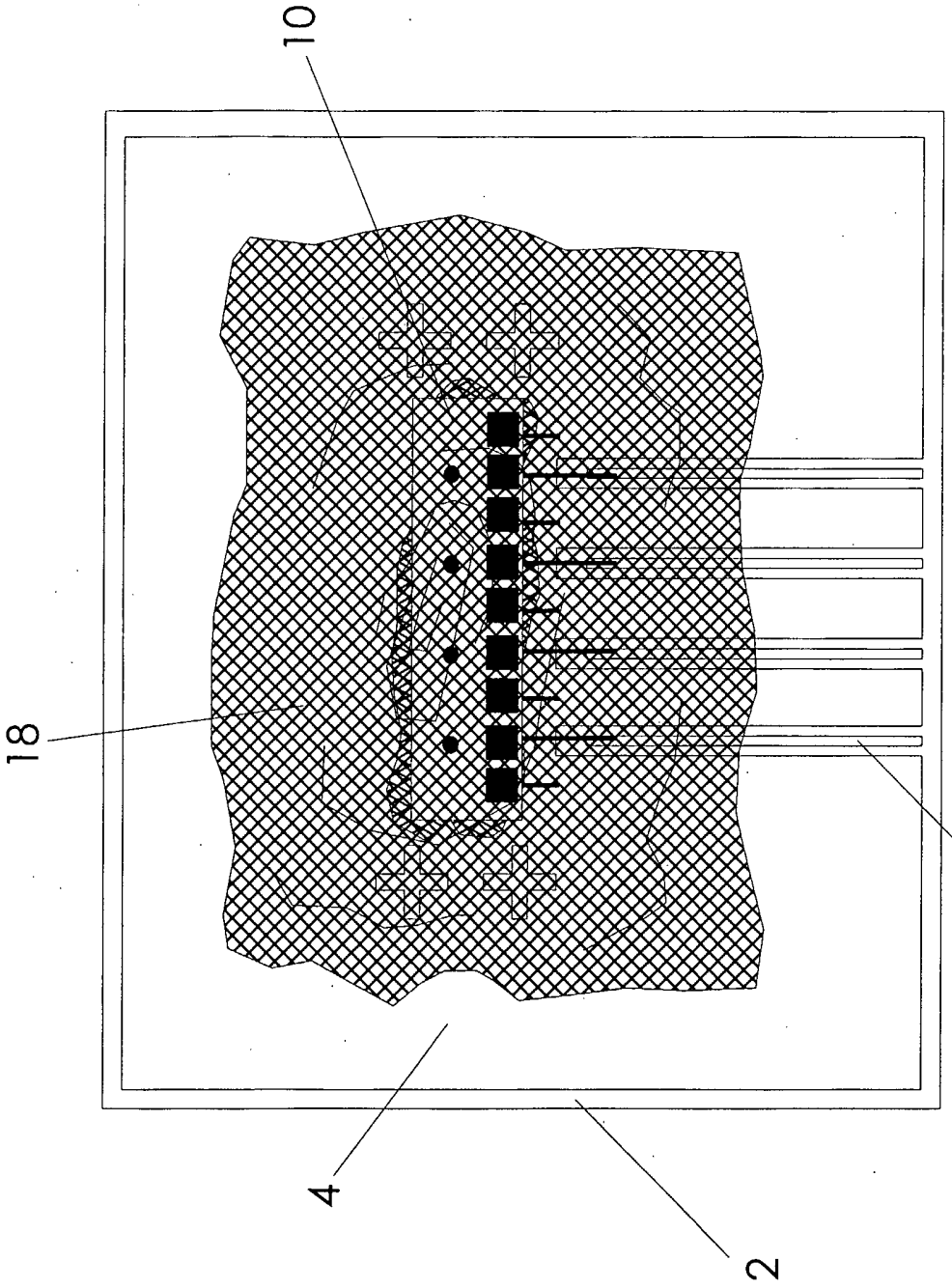

Fig. 3b

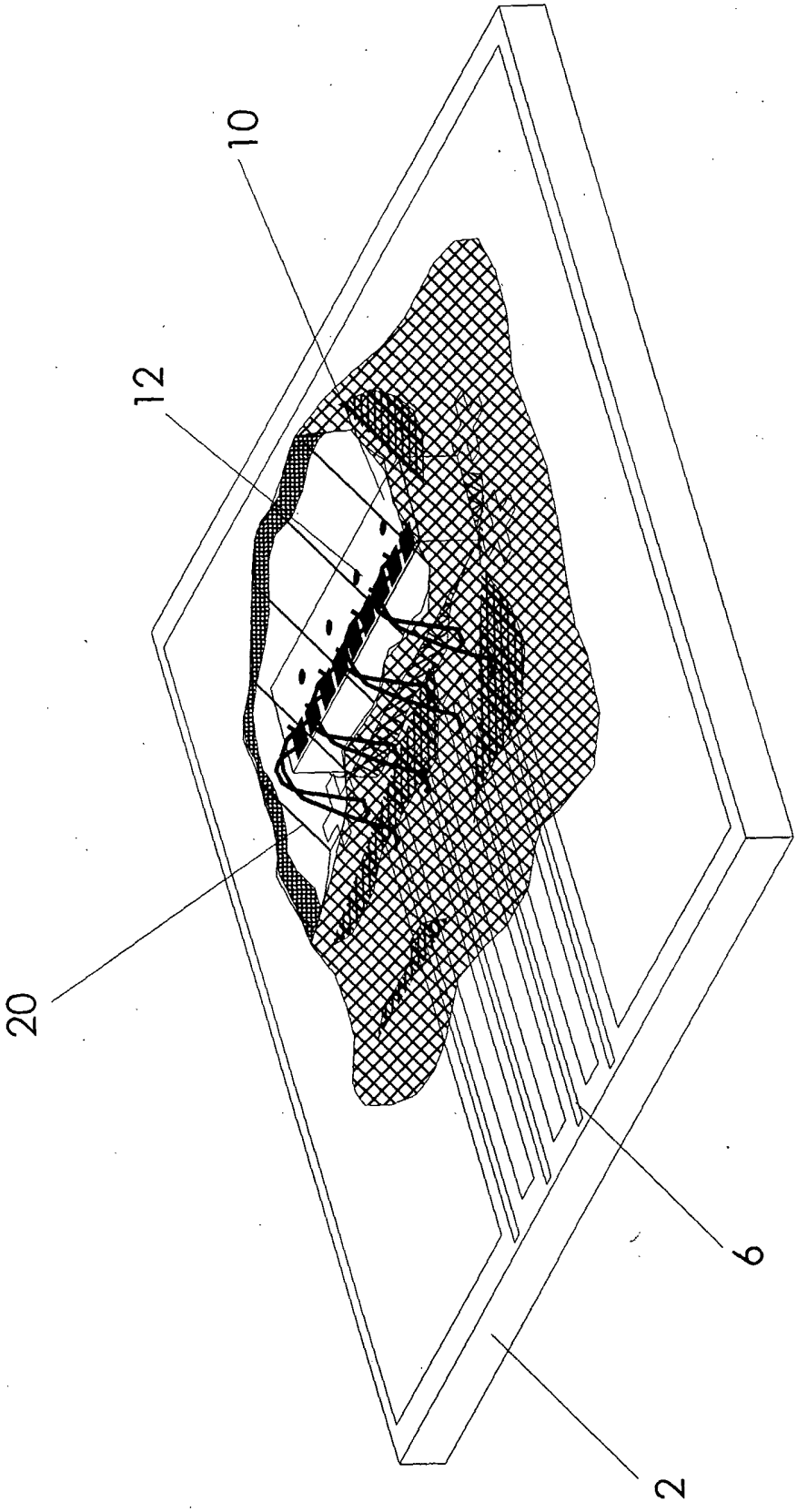

Fig.4a

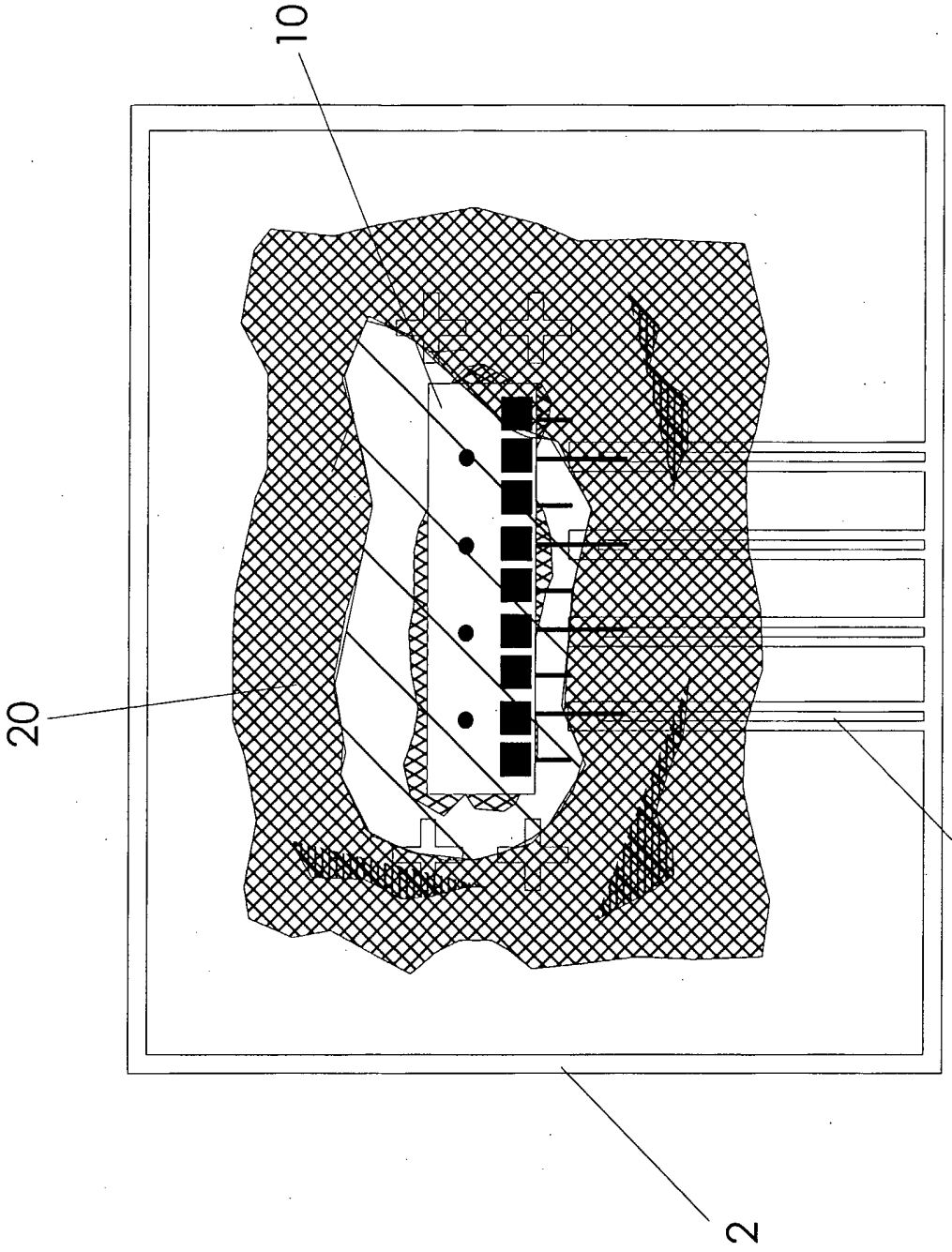

Fig. 4b

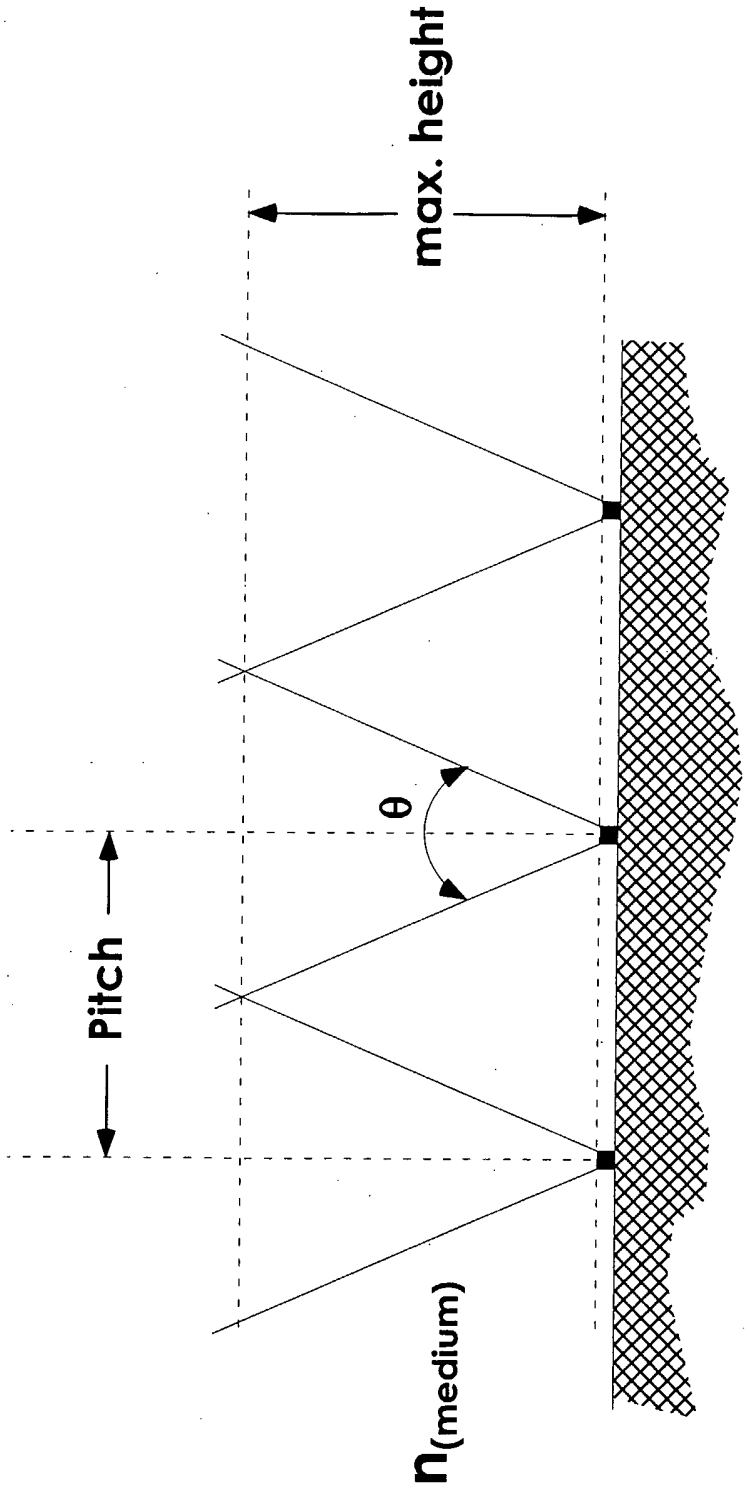

Fig. 5

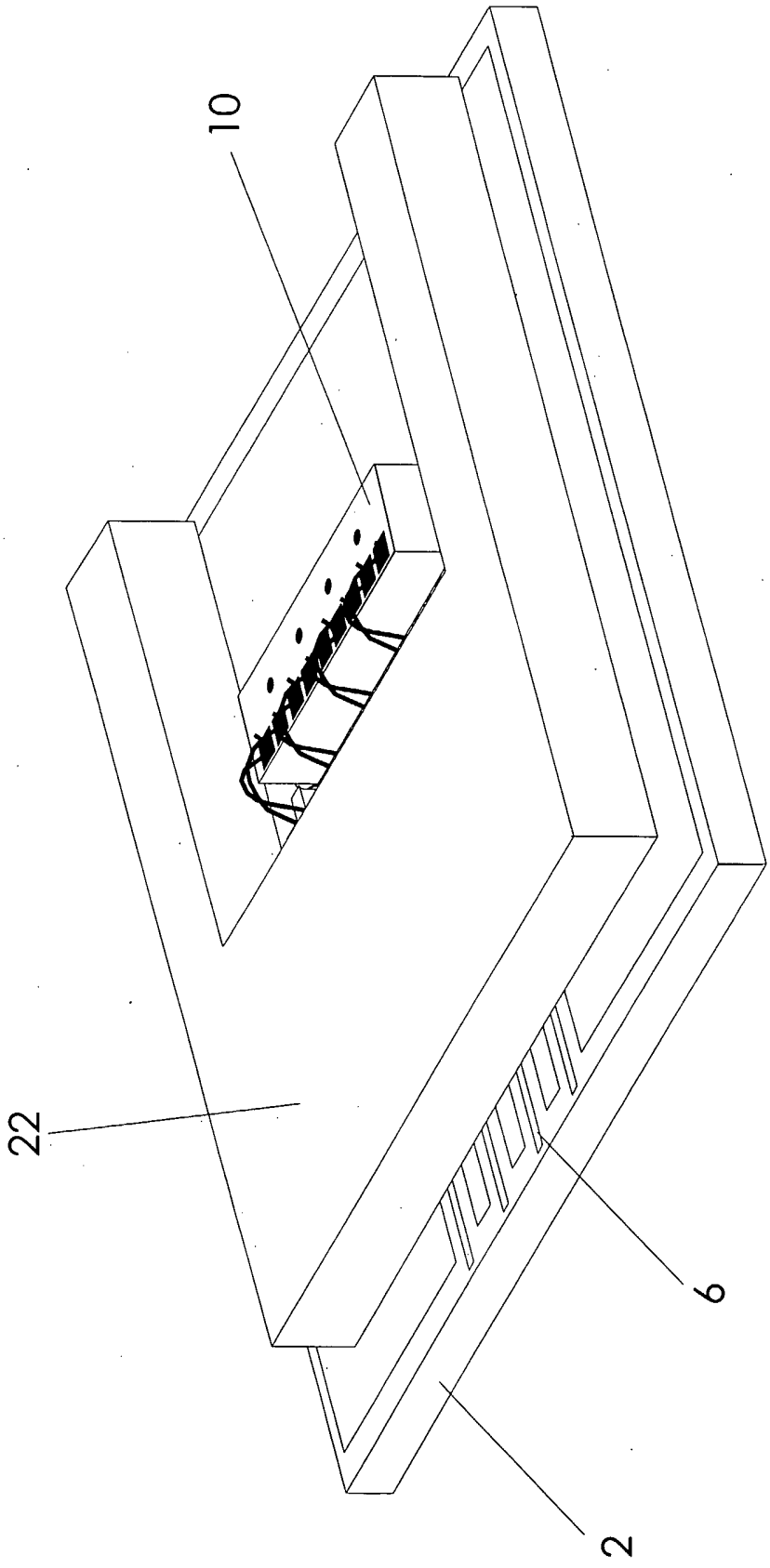

Fig. 6a

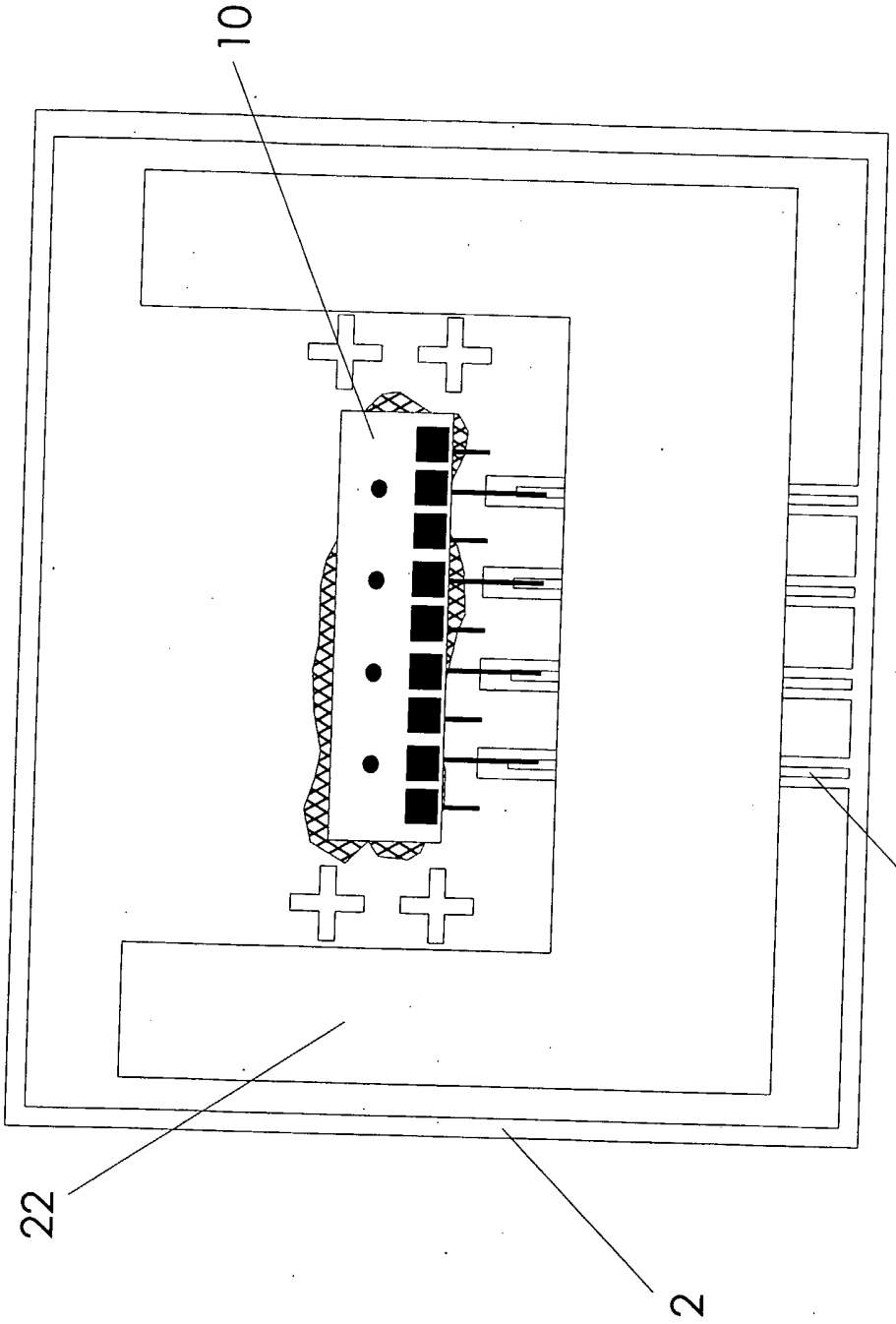

Fig. 6b

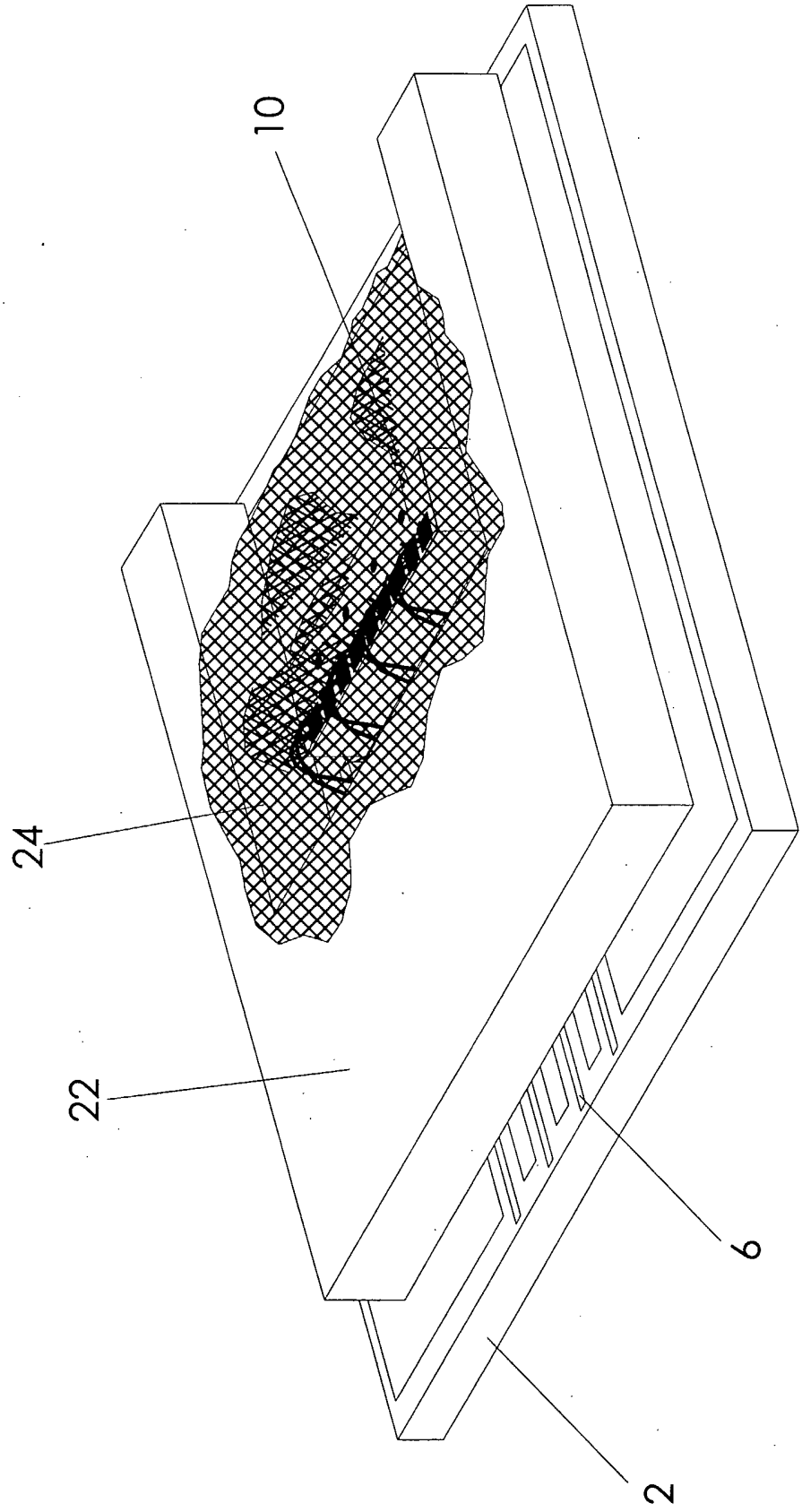

Fig. 7a

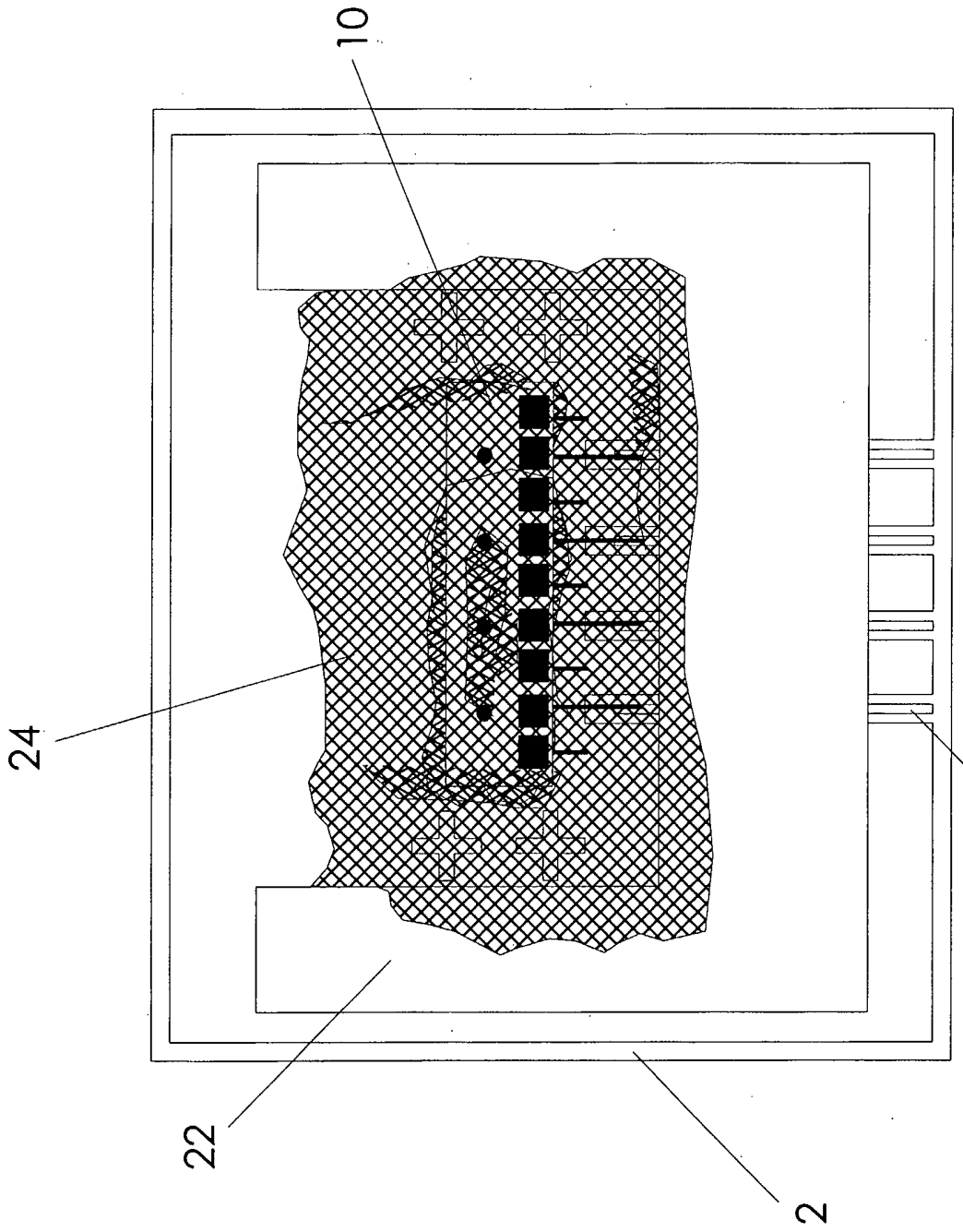

Fig. 7b

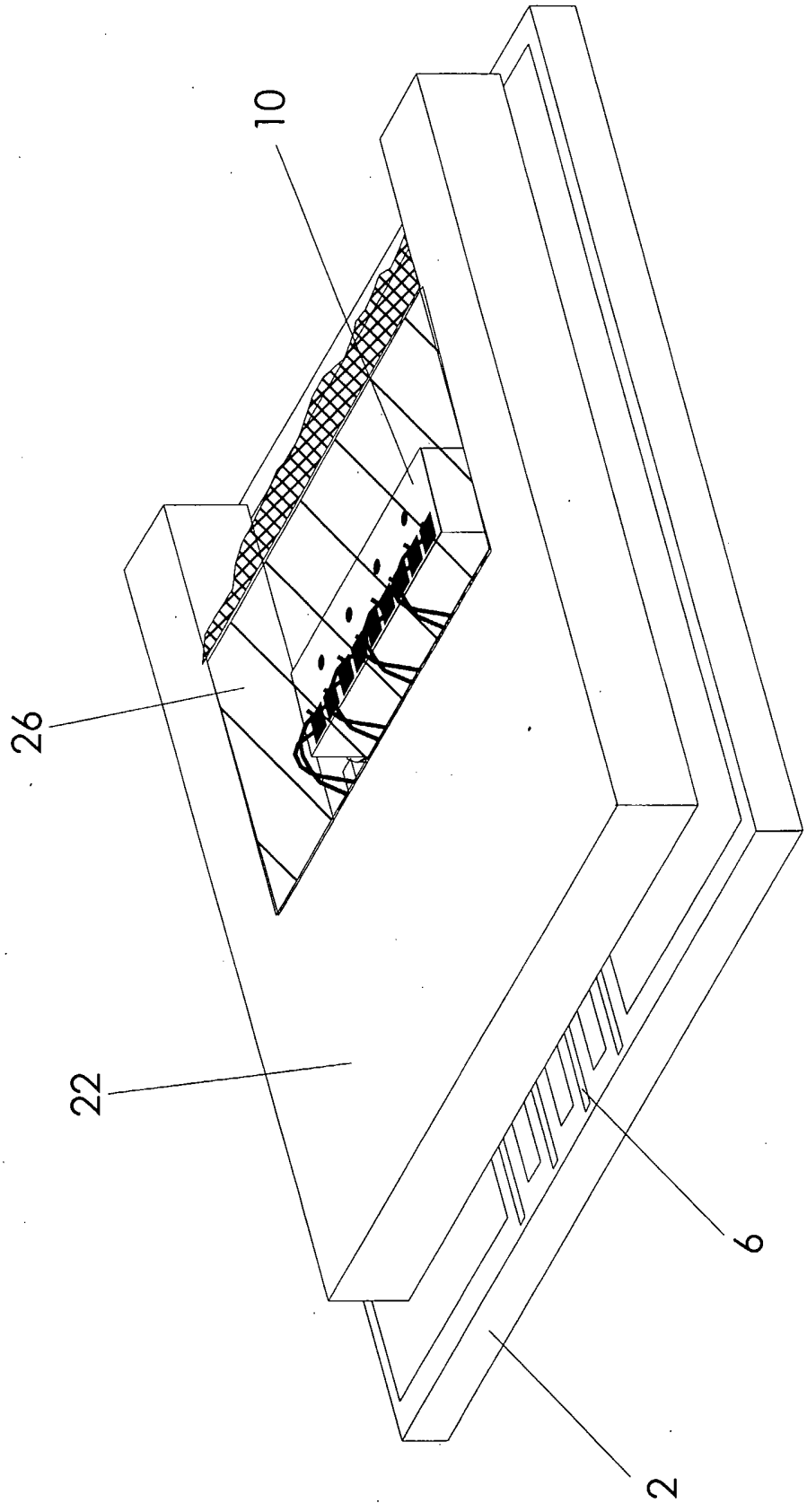

Fig. 8a

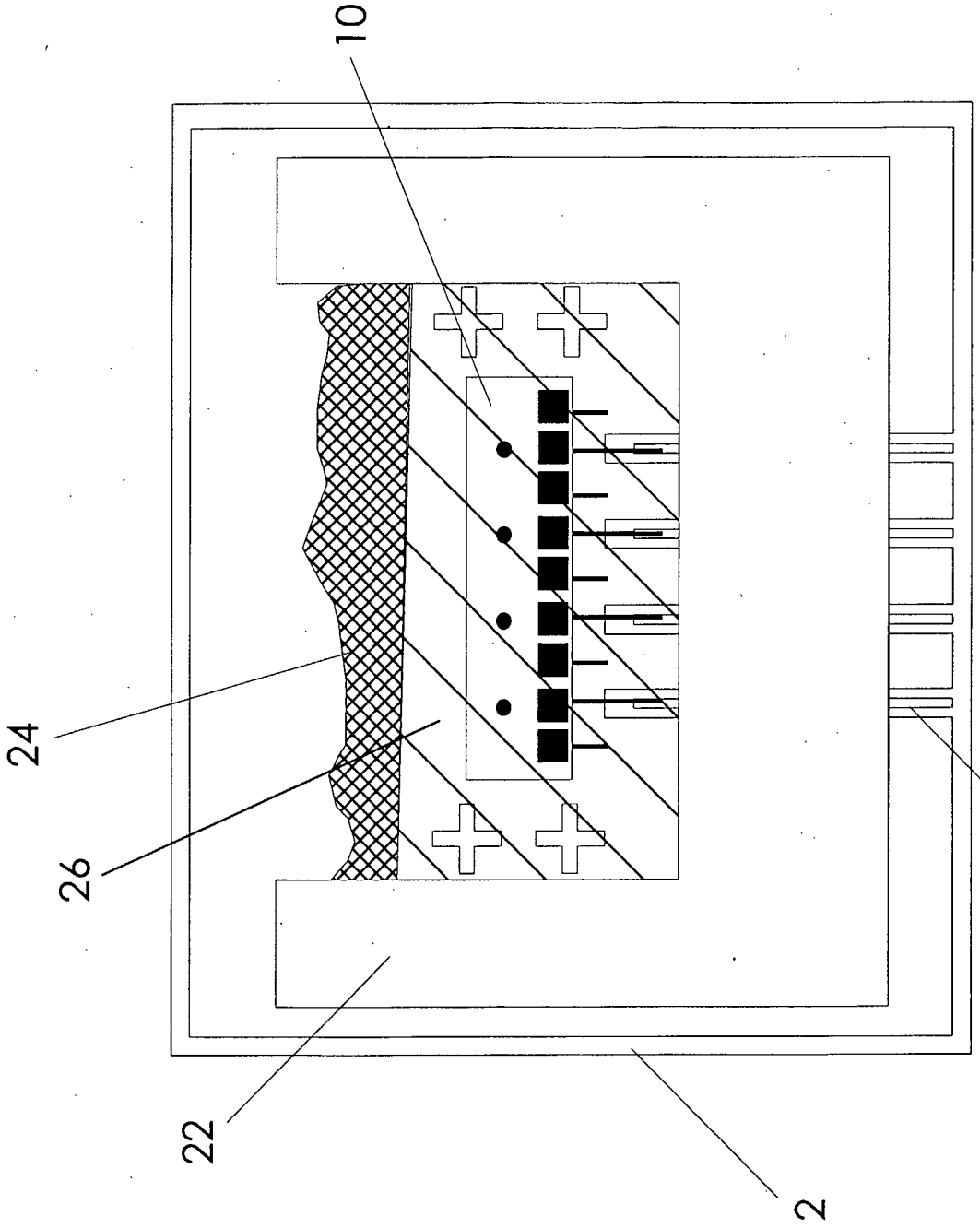

Fig. 8b

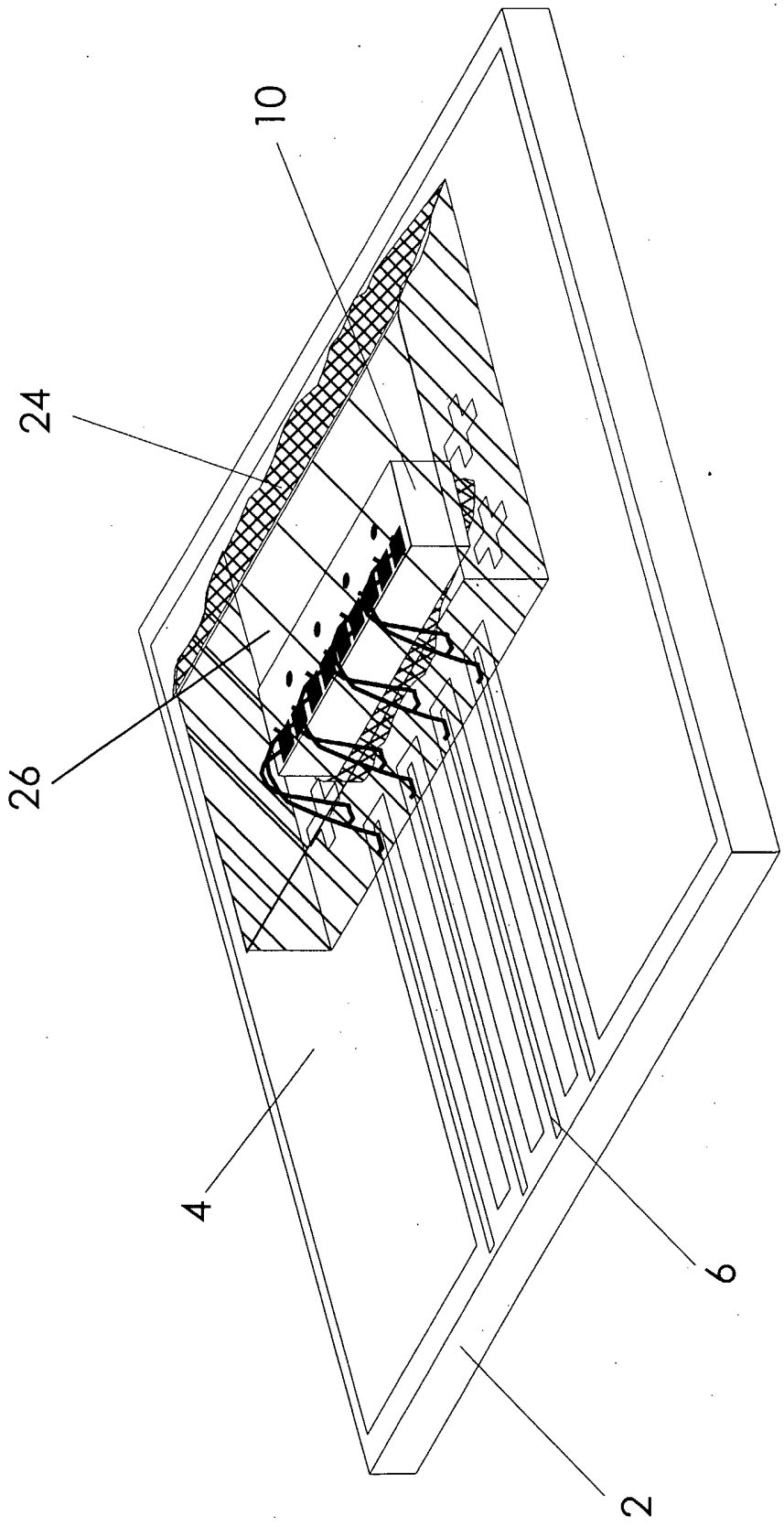

Fig. 9a

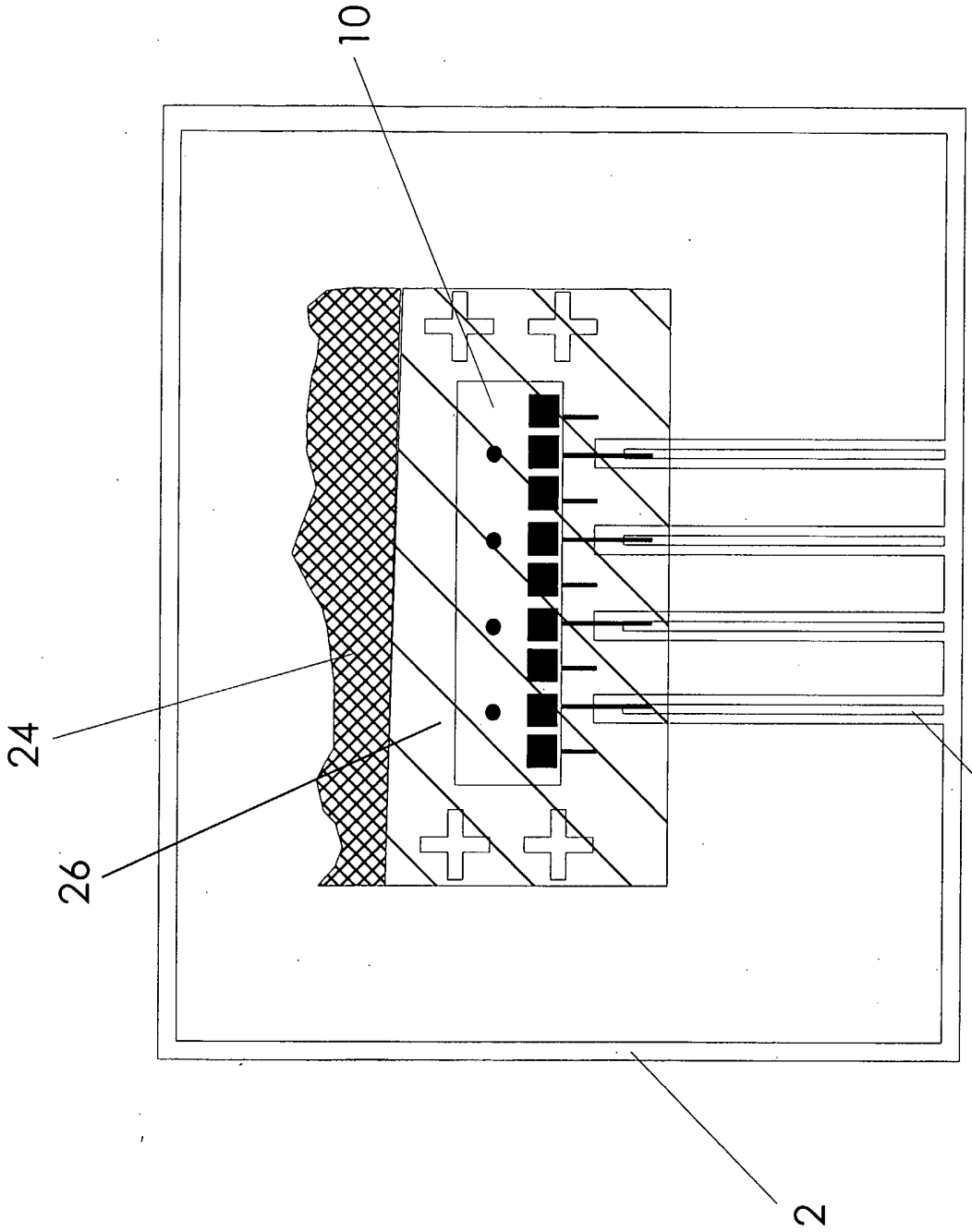

Fig. 9b

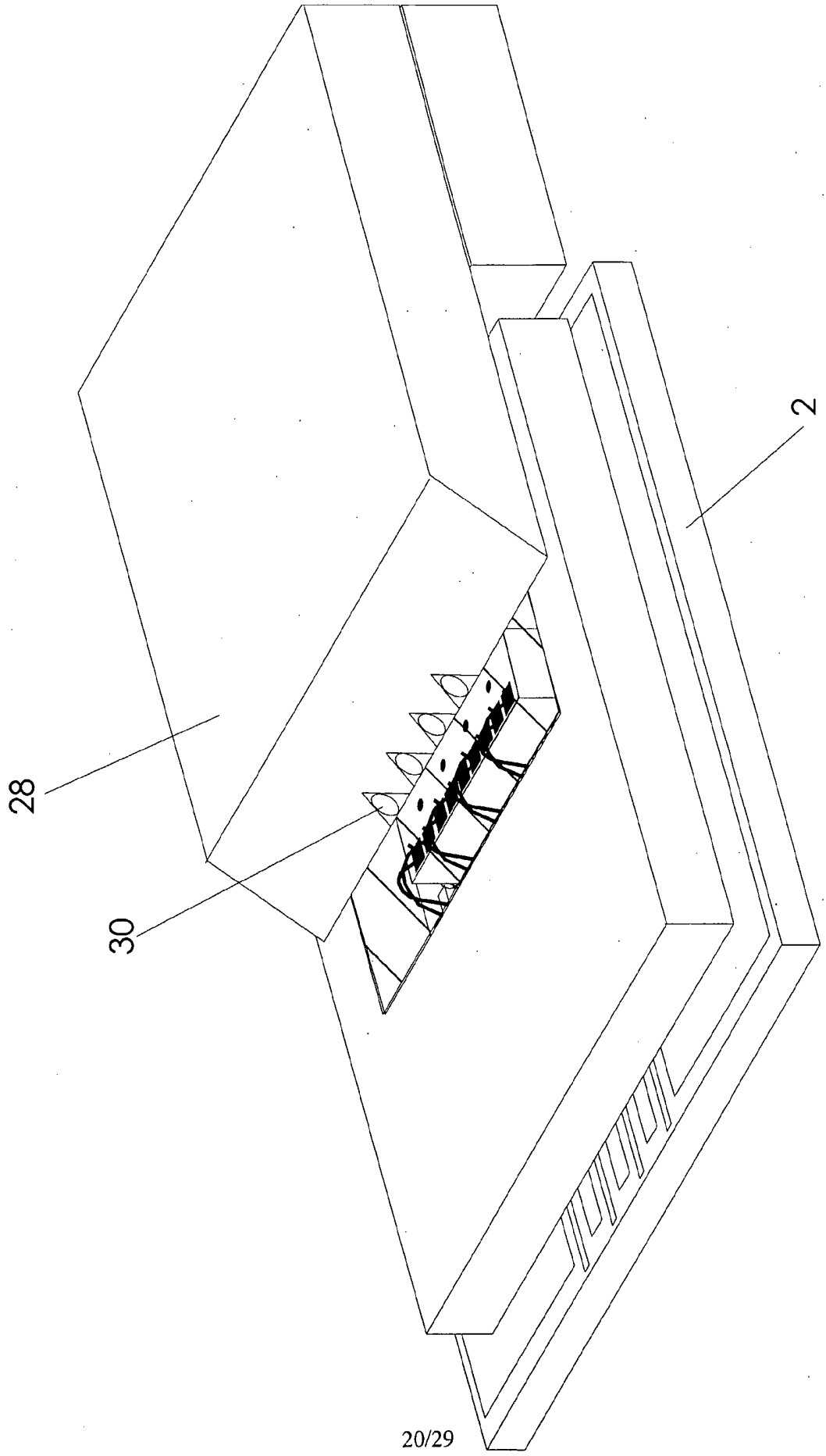

Fig. 10a

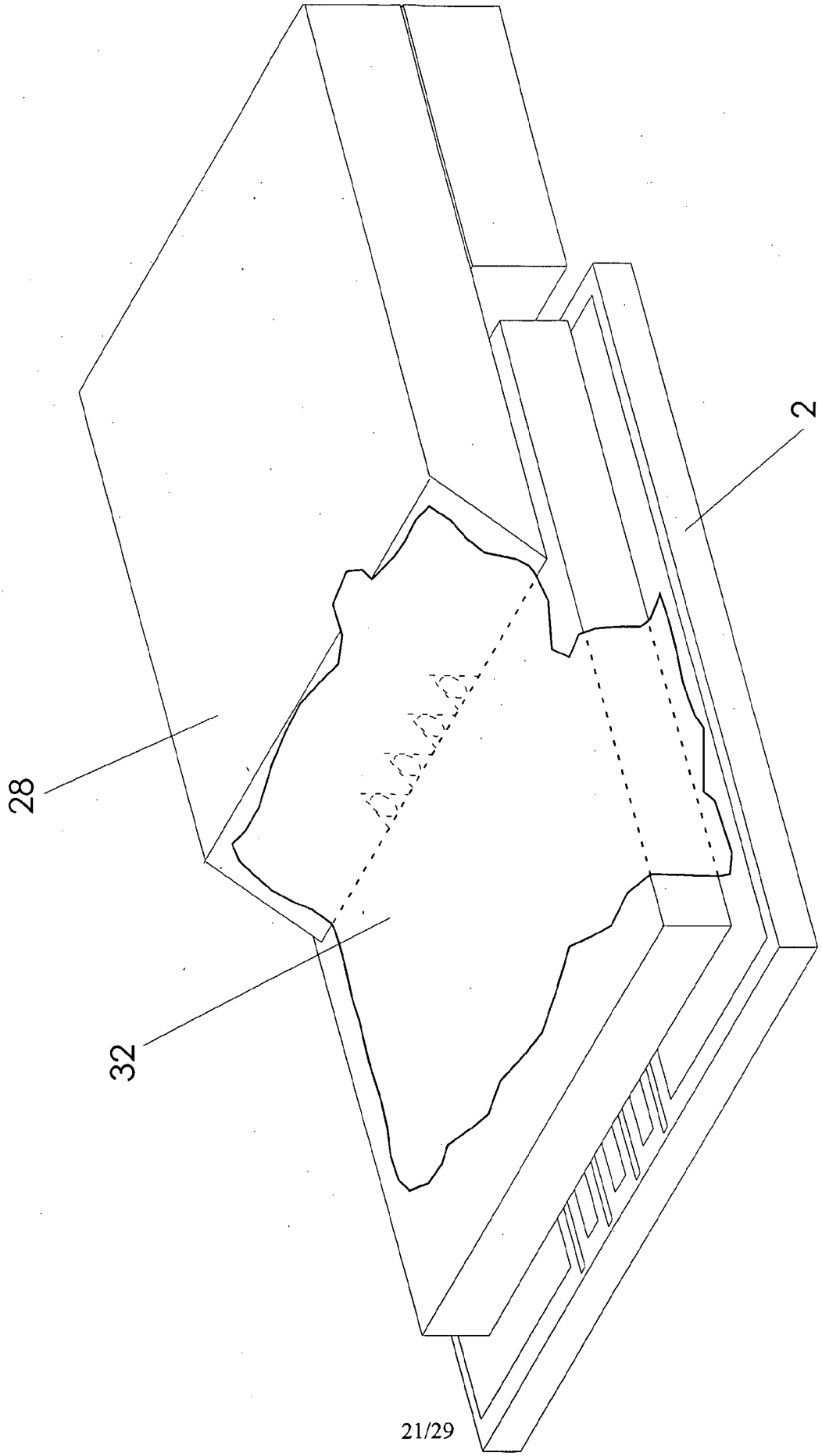

Fig. 10b

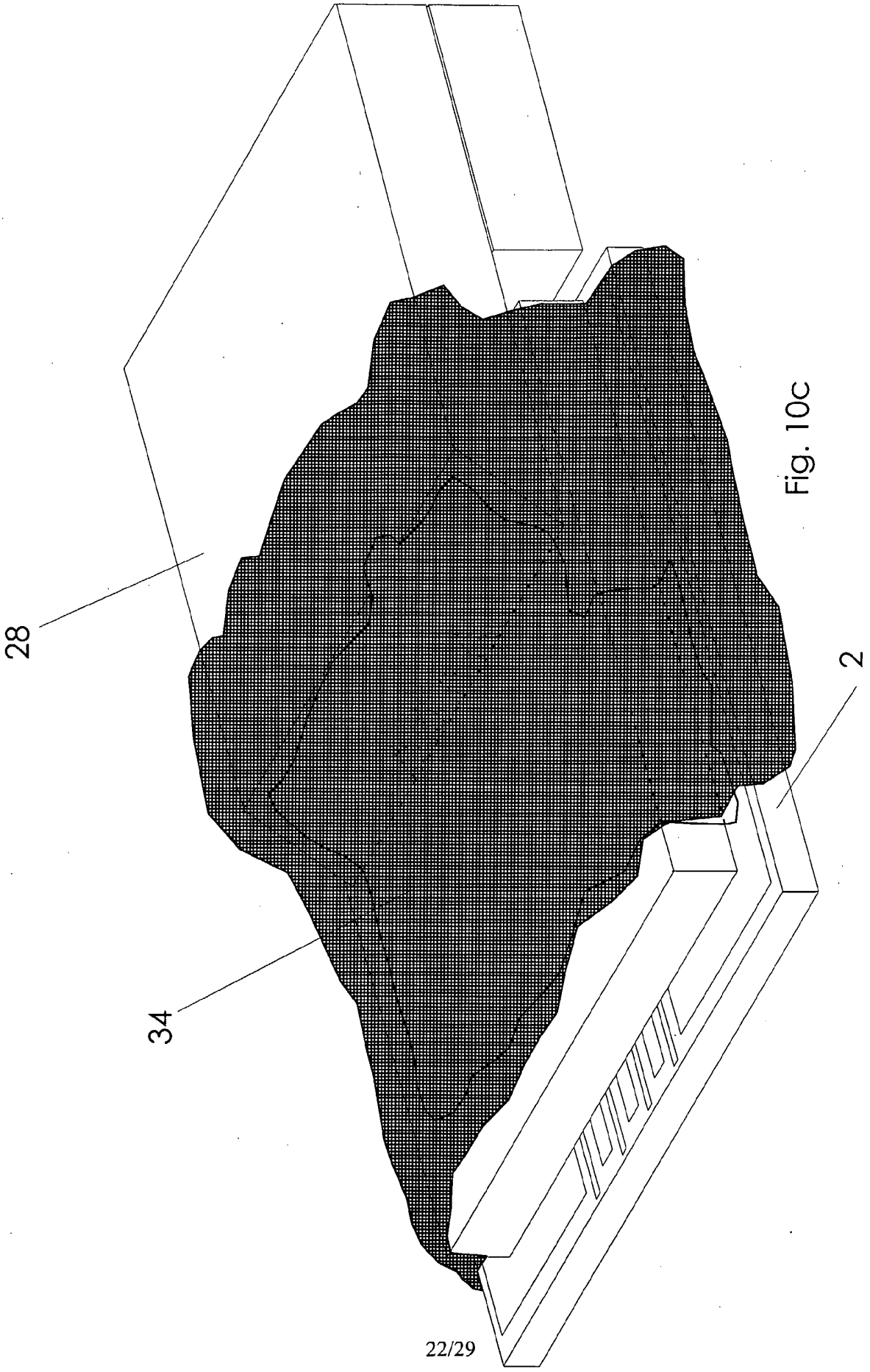

Fig. 10c

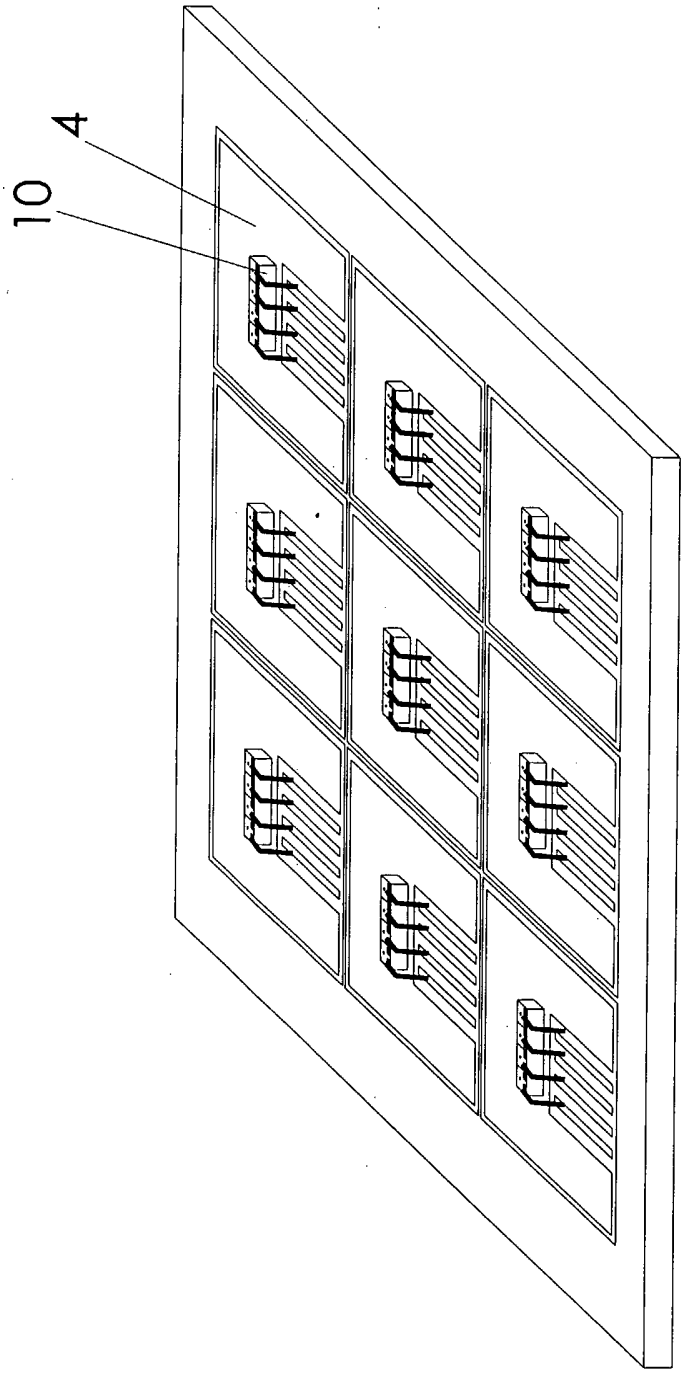

Fig. 11

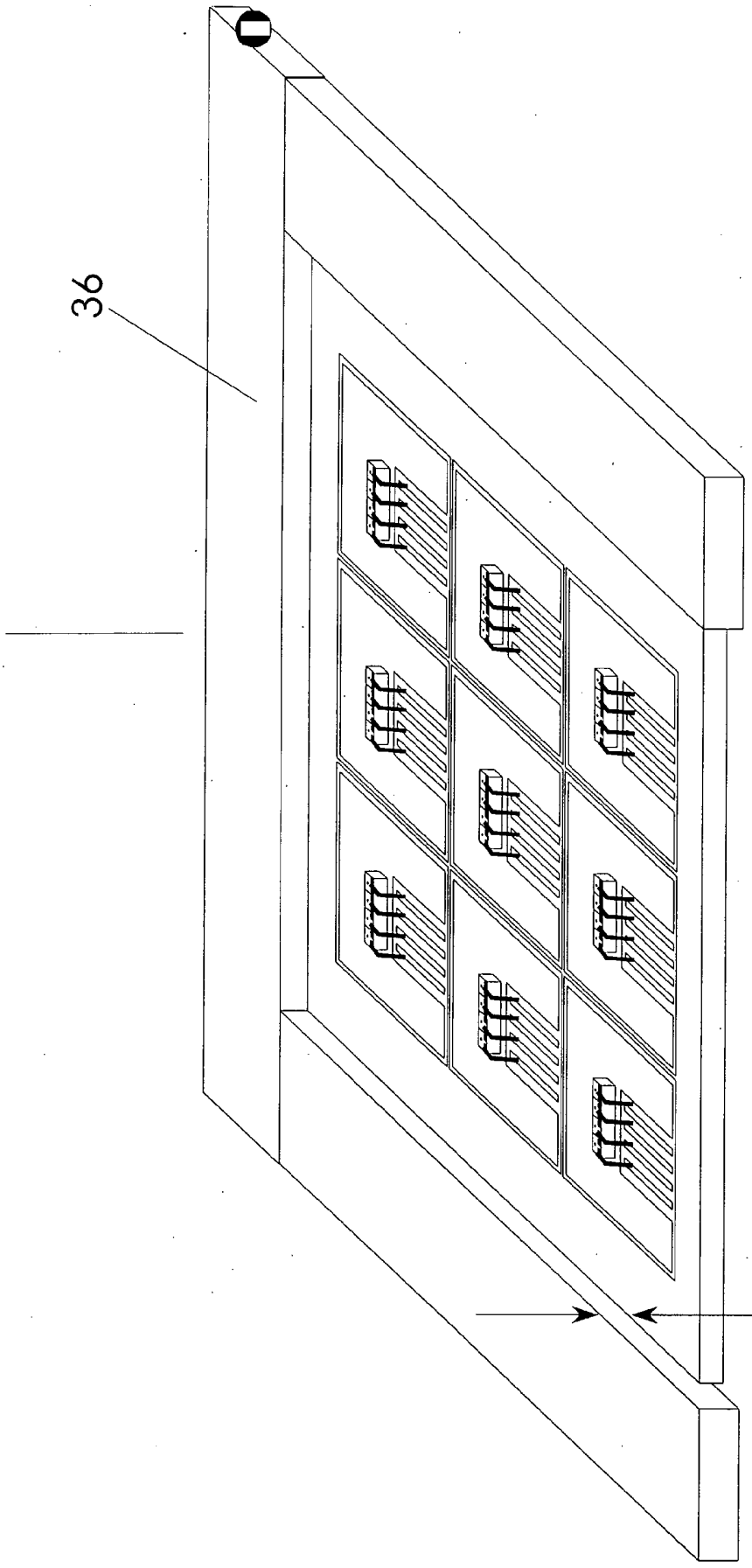

Fig. 12

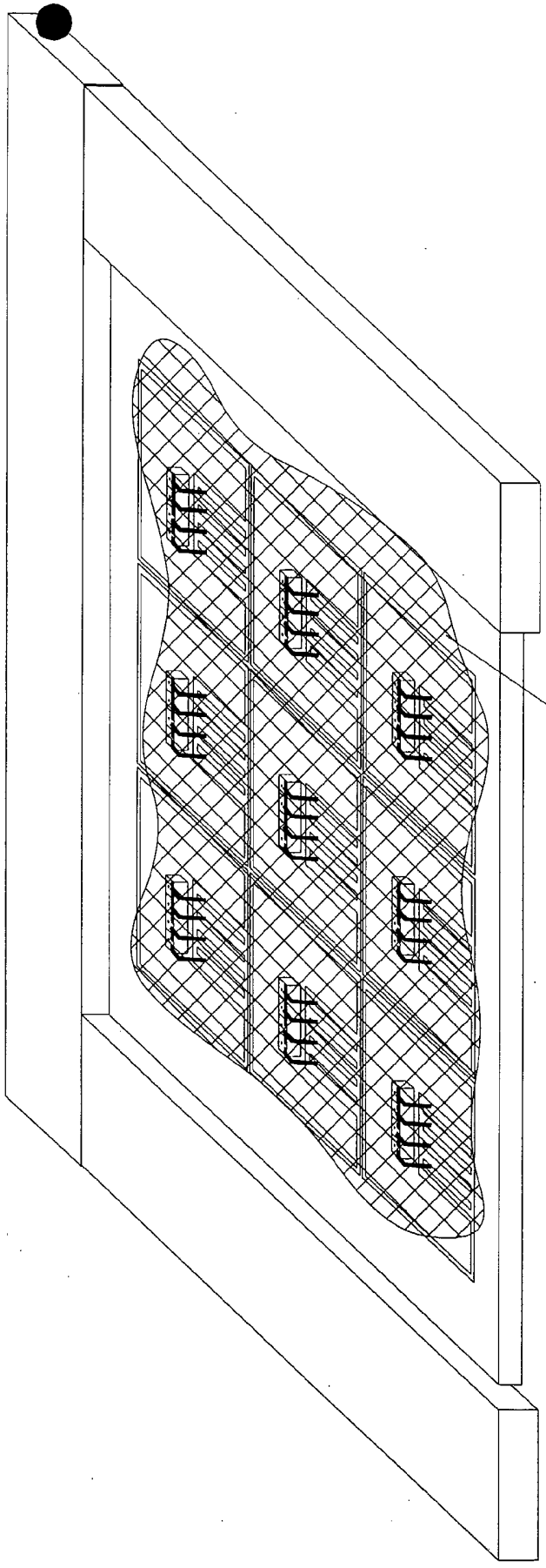

Fig. 13

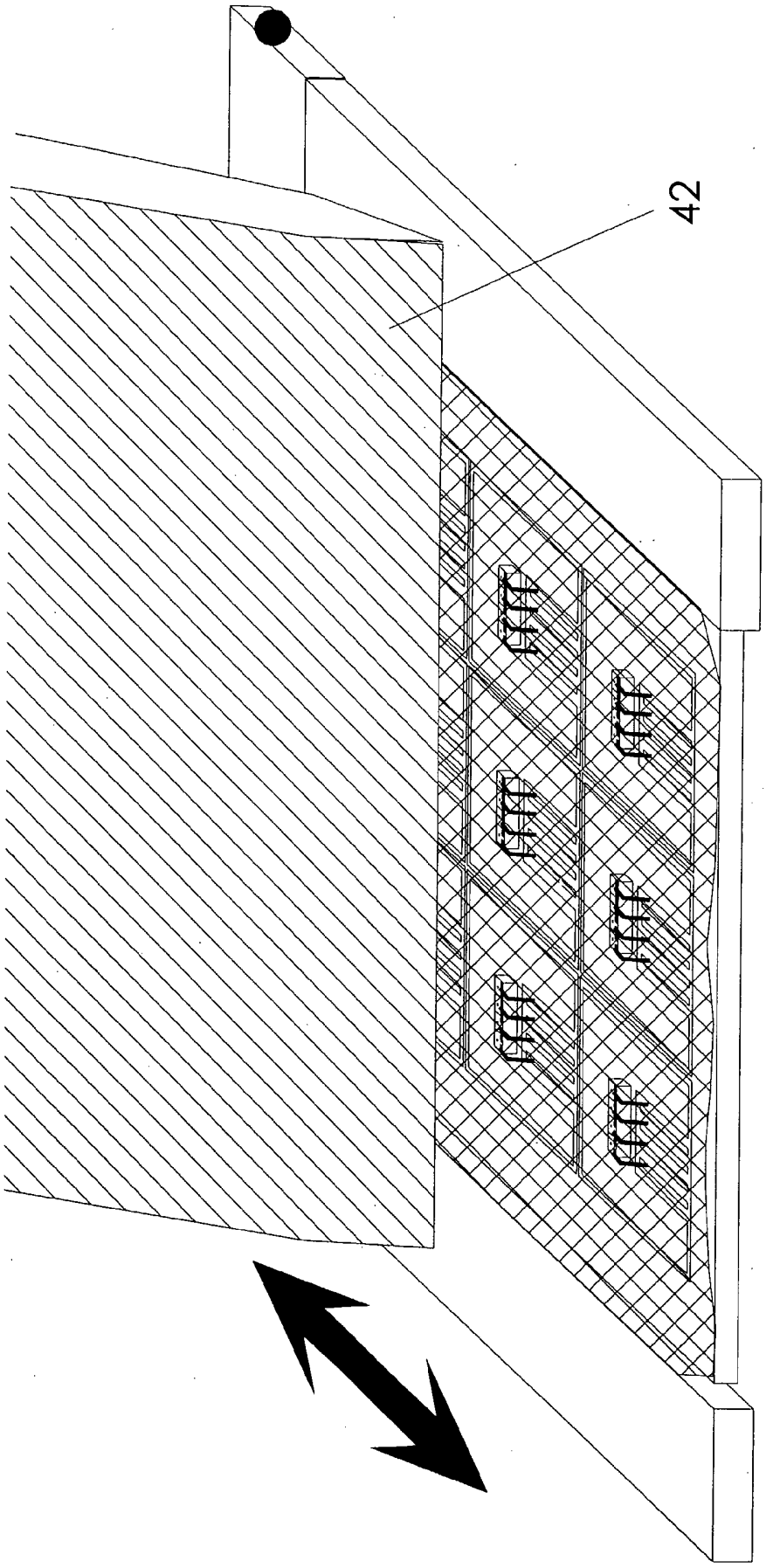

Fig. 14

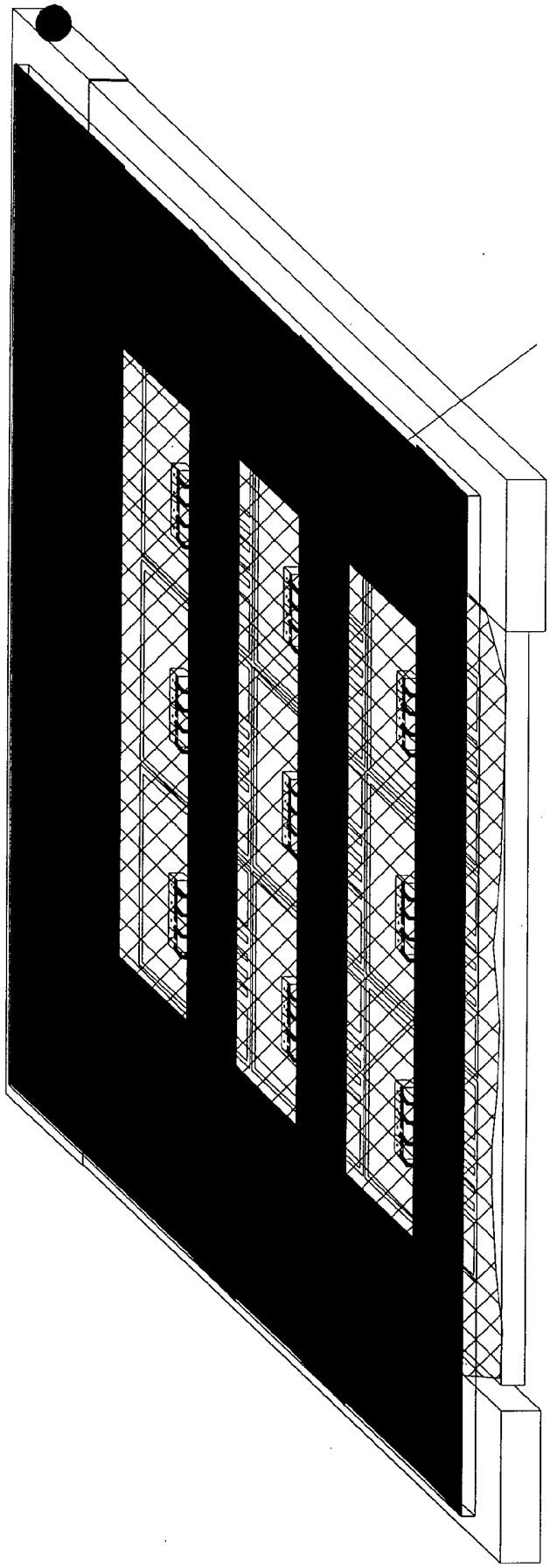

Fig. 15

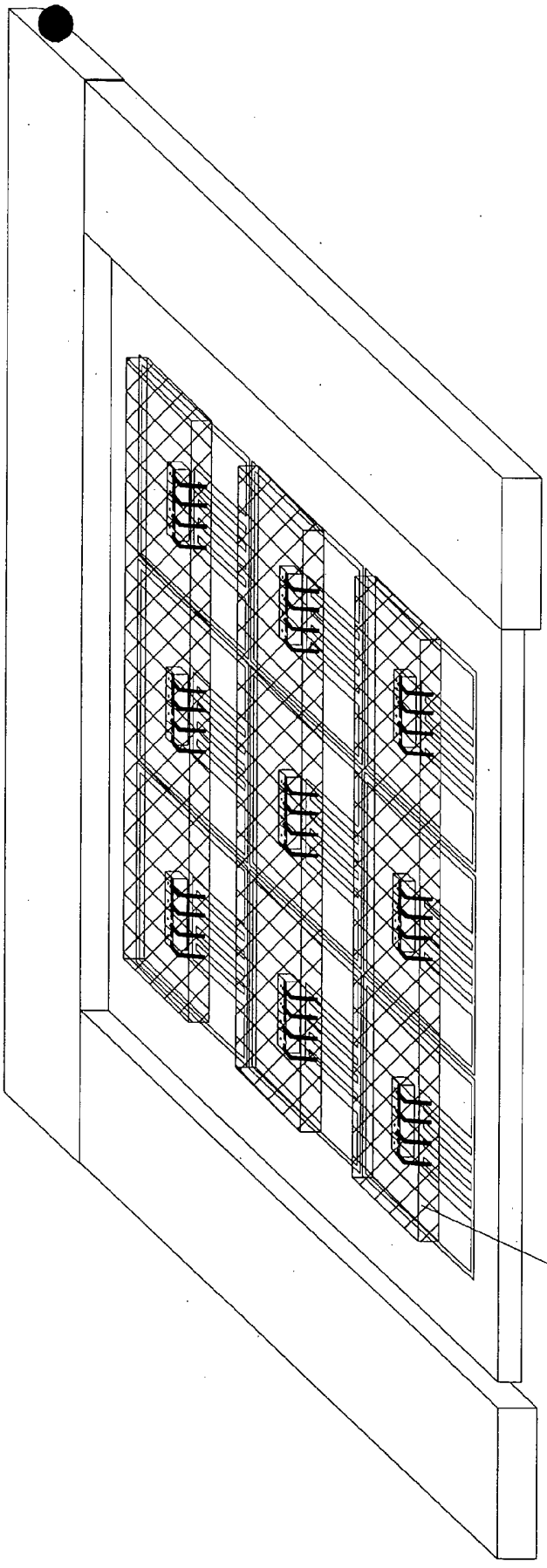

Fig.16

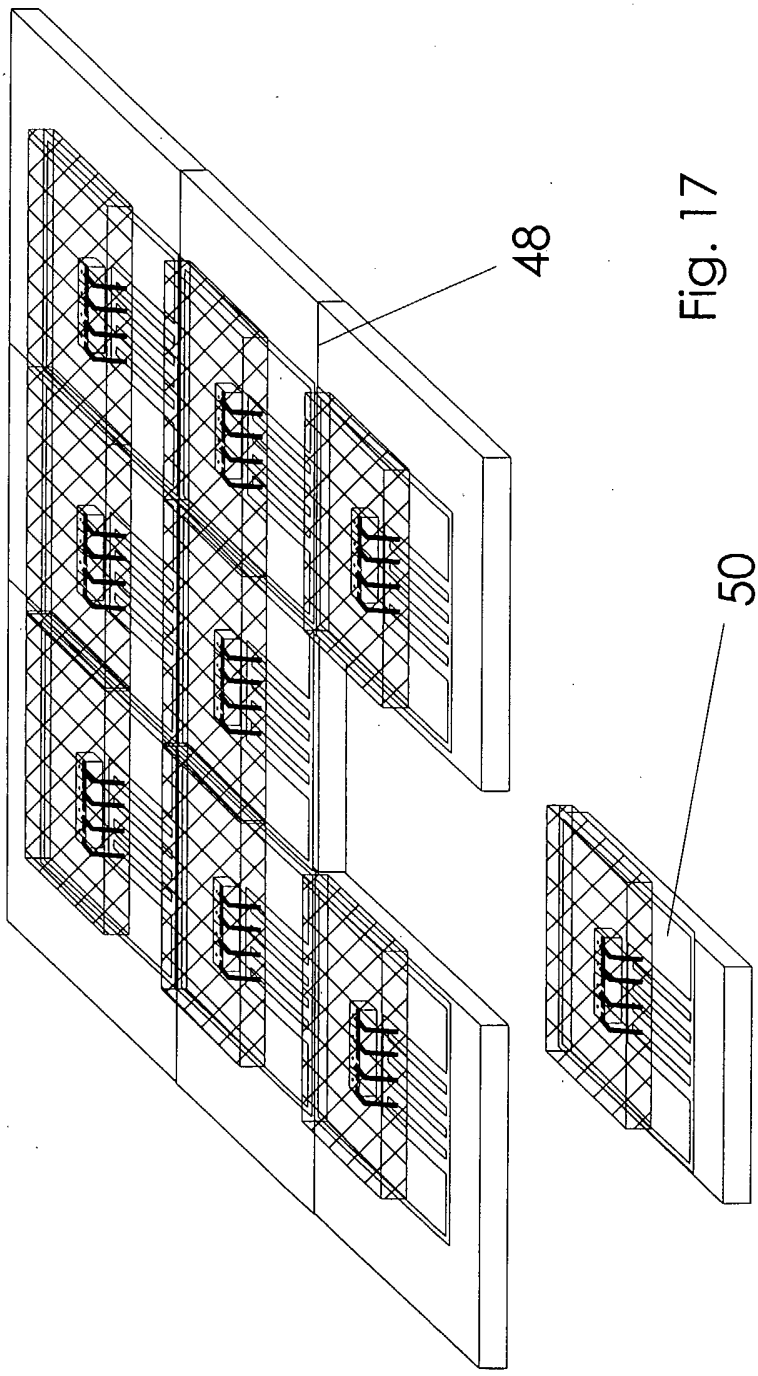

Fig. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2004/001408

A. CLASSIFICATION OF SUBJECT MATTER IPC(7): G02B-6/12 G02B-6/13, G02B-6/42

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(7,6): G02B-6/12, G02B-6/42, H01J-40, H01L-21, H01L-27, H01L-31, H01L-39, H04B-10 and H05K-7

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base(s) consulted during the international search (name of data base(s), and, where practicable, search terms used)
Delphion, Derwent, US West and Japanese Patent Database; search terms used: encapsulat*, transparent, clear, cont. on pg.

B. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 6 054 716 A (Sonobe et al.) 25 April 2000 (25-04-2000) abstract; figures 19b and 21b; col. 19, lines 42 to 53; and col. 21, lines 38 to 45.	18, 19, 20 and 33 1 to 17, 21 to 32 and 34 to 36
Y	EP 0 466 950 B1 (Nishimori et al.) 07 Oct 1998 (07-10-1998) page 4, lines 8 to 11; and page 6, lines 32 to 36 and 38 to 41.	1 to 3, 12, 14, 18, 23, 29 and 31 to 36
A	US 5 960 141 (Sasaki et al.) 28 Sept 1999 (28-09-1999) figures 9, 10, 13 and 14; col. 4, lines 23 to 39.	4, 8
A	US 2002 0 181 899 A1 (Tataglia et al.) 05 Dec 2002 (05-12-2002) abstract; figures 3B, 4, 5B, 6, 7 , 10 and 11; page 1, col. 1, lines 16 to 33,; and page 2, col. 2 lines 33 to 35. (cited in the application)	4 to 11, 13, 15, 16 (in part), 17 (in part), 20, 31, 32, 35 and 36
A	US 4 130 343 (Miller et al.) 19 Dec 1978 (19-12-1978) abstract; figure 2B; col. 2 lines 3 to 1; and col. 3, line 56 to col. 4, line 3.	17

Further documents are listed in the continuation of Box C. Patent family members are listed in annex.

* Special categories of cited documents :
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international-type search	Date of mailing of the international-type search report
08 November 2004 (08-11-2004)	12 November 2004 (12-11-2004)
Name and mailing address of the ISA/ *Commissioner of Patents* *Canadian Patent Office - PCT* *Ottawa/Gatineau K1A 0C9* Facsimile No. 1-819-953-9358	Authorized officer Daniel Weslake (819) 997-2999

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2004/001408

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 269 209 B1 (Terada et al.) 31 July 2001 (31-07-2001) abstract; figures 6A to 6D; col. 1, line 55 to col. 2, line 14; col. 2, lines 27 to 42; and col. 5, line 41 to col. 6, line 11. (cited in the application)	21, 22, 27 and 28
A	US 2002 0 001 869 A1 (Fjelstad) 03 Jan 2002 (03-01-2002) abstract; figures 3E to 3I; page 1, col. 2, line 51 to page 2, col.1, line 26. (cited in the application)	24, 25 and 30

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2004/001408

Continuation of Box. B - Fields searched - search terms used

search terms used: transmissive, translucent, epoxy, adhesive, sealant, window, port, aperture, polish*, buff*, lap*, parallel, flat, hermetic

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2004/001408

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