

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
29 January 2004 (29.01.2004)

PCT

(10) International Publication Number
WO 2004/010583 A1

(51) International Patent Classification⁷: **H03L 7/089**,
7/093

(21) International Application Number:
PCT/US2003/013108

(22) International Filing Date: 28 April 2003 (28.04.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/199,422 19 July 2002 (19.07.2002) US
10/199,421 19 July 2002 (19.07.2002) US
10/230,726 29 August 2002 (29.08.2002) US
10/230,649 29 August 2002 (29.08.2002) US
10/230,596 29 August 2002 (29.08.2002) US
10/230,862 29 August 2002 (29.08.2002) US

(71) Applicant: **SUN MICROSYSTEMS, INC.** [US/US];
4150 Network Circle, Santa Clara, CA 95054 (US).

(72) Inventors: **GAUTHIER, Claude, R.**; 20207 Northbrook Square, Cupertino, CA 95014 (US). **TRIVEDI, Pradeep, R.**; 992-6 Belmont Terrace, Sunnyvale, CA 94086 (US). **BOBBA, Sudhakar**; 410 N. Mary Avenue, Sunnyvale, CA 94085 (US). **AMICK, Brian, W.**; 4600 Seton Center Parkway, #320, Austin, TX 78759 (US). **LIU, Dean**; 1219 Crescent Terrace, Sunnyvale, CA 94086 (US).

(74) Agents: **ROSENTHAL, Alan, D.** et al.; Rosenthal & Osha L.L.P., Suite 2800, 1221 McKinney, Houston, TX 77010 (US).

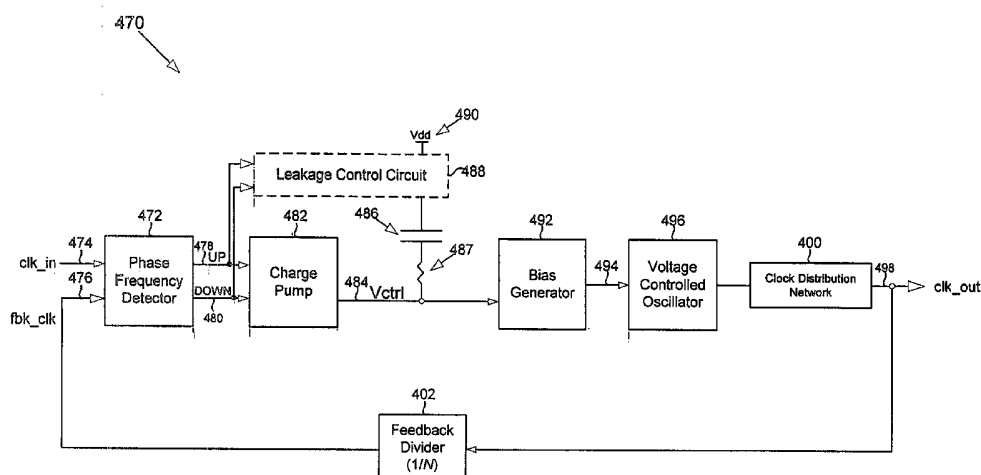
(81) Designated States (*national*): JP, KR.

(84) Designated States (*regional*): European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR).

Published:
— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: LOOP FILTER CAPACITOR LEAKAGE CURRENT CONTROL



(57) Abstract: A locked loop circuit (470) uses a control circuit (488) to adjust a leakage current through a loop filter capacitor (486) of the locked loop circuit (470). The control circuit (488) comprises a switch connected in series with the loop filter capacitor (486) which is responsive to the phase frequency detector (472).

LOOP FILTER CAPACITOR LEAKAGE CURRENT CONTROL

Background of Invention

[0001] As shown in Figure 1, a typical computer system (10) has, among other components, a microprocessor (12), one or more forms of memory (14), integrated circuits (16) having specific functionalities, and peripheral computer resources (not shown), e.g., monitor, keyboard, software programs, etc. These components communicate with one another via communication paths (19), e.g., wires, buses, etc., to accomplish the various tasks of the computer system (10).

[0002] In order to properly accomplish such tasks, the computer system (10) relies on the basis of time to coordinate its various operations. To that end, a crystal oscillator (18) generates a system clock signal (referred to and known in the art as “reference clock” and shown in Figure 1 as SYS_CLK) to various parts of the computer system (10). Modern microprocessors and other integrated circuits, however, are typically capable of operating at frequencies significantly higher than the system clock signal, and thus, it becomes important to ensure that operations involving the microprocessor (12) and the other components of the computer system (10) use a proper and accurate reference of time.

[0003] One component used within the computer system (10) to ensure a proper reference of time among the system clock signal and a microprocessor clock signal, i.e., “chip clock signal” or CHIP_CLK, is a type of clock generator known as a phase locked loop (PLL) (20). The PLL (20) is an electronic circuit that controls an oscillator such that the oscillator maintains a constant phase relative to the system clock signal. Referring to Figure 1, the PLL (20) has as its input the system clock signal, which is its reference signal, and outputs a chip clock signal (shown in Figure 1 as CHIP_CLK) to the microprocessor (12). The system clock signal and chip clock signal have a specific phase and frequency relationship controlled by the PLL (20). This relationship between

the phases and frequencies of the system clock signal and chip clock signal ensures that the various components within the microprocessor (12) use a controlled and accounted for reference of time. When this relationship is not maintained by the PLL (20), however, the operations within the computer system (10) become non-deterministic.

[0004] Figure 2 shows a block diagram of a typical PLL (200). The PLL (200) includes a PLL core (250), buffers (212, 214, 216, 218), and a feedback loop signal (221) on a feedback loop path. The buffers (212, 214) increase the drive strength of an output clock signal (215) to supply other circuits of the microprocessor (12 in Figure 1) with a chip clock signal (217). The buffers (216, 218) buffer the chip clock signal (217) to additional circuits of the microprocessor (12 in Figure 1). The time delay created by the buffers (212, 214, 216, 218) is accounted for in the feedback signal (221) that is supplied to the PLL core (250).

[0005] The PLL core (250) is designed to output the chip clock signal (217), which is a multiple of the system clock signal (201). When the PLL is in "lock," the chip clock signal (217) and system clock signal (201) maintain a specific phase relationship. To allow different multiplication ratios, the PLL core (250) may use several "divide by" circuits. A "divide by" circuit reduces the frequency of the input to the "divide by" circuit at its output by a specified factor. For example, the PLL core (250) uses a divide by A circuit (220) with the system clock signal (201), a divide by C circuit (222) with a voltage-controlled oscillator (210) output signal (213), and a divide by B circuit (224) with the feedback loop signal (221).

[0006] A phase-frequency detector (202) aligns the transition edge and frequency of a clock A signal (221) and a clock B signal (223). The phase-frequency detector (202) adjusts its output frequency in order to zero any phase and frequency difference between the clock A signal (221) and the clock B signal (223). The phase-frequency detector (202) produces signals that control charge pumps (204, 234). The phase-frequency detector (202), using control

signals up (203) and down (205), controls the charge pumps (204, 234) to increase or decrease their output. The charge pump (204) adds or removes charge from a capacitor C_1 (206) that changes the voltage potential at the input of a bias-generator (208). The capacitor (206) is connected between a power supply V_{DD} and a control voltage V_{CTRL} (207). The charge pump (234) adds or removes charge from a bias voltage V_{BP} (209) of a bias-generator (208).

[0007] The bias-generator (208) produces bias voltages V_{BP} (209) and V_{BN} (211) in response to the control voltage (207). The PLL core (250) may be self-biased by adding the charge pump (234) to the bias-generator (208) bias voltage V_{BP} (209). The addition of a second charge pump (234) allows the removal of a resistor in series with the capacitor (206). A voltage-controlled oscillator (210) produces an output signal (213) that has a frequency related to the bias voltages V_{BP} (209) and V_{BN} (211).

[0008] The “divide by” circuits (220, 222, 224) determine the frequency multiplication factor provided by the PLL core (250). The addition of “divide by” circuits (220, 222, 224) enables the PLL core (250) to multiply the system clock signal (201). Multiplying the system clock signal (201) is useful when the chip clock signal (217) must have a higher frequency than the system clock signal (201).

[0009] For example, during normal operation, the variables A and C may both be set to one in the divide by A circuit (220) and divide by C circuit (222), respectively. The variable B may be set to 10 in the divide by B circuit (224). The phase-frequency detector (202) aligns the transition edge and frequency of the clock A signal (221) and the clock B signal (223). The phase-frequency detector (202) adjusts PLL core (250) output clock signal (215) frequency in order to zero any phase and frequency difference between the clock A signal (221) and the clock B signal (223). Because the clock B signal (223) has a divide by B circuit (224) that reduces its input frequency by 10, the phase-frequency detector (202) adjusts the voltage-controlled oscillator (210) output signal (213) to a frequency 10 times greater than the clock A signal (221).

Accordingly, the chip clock signal (217) is 10 times higher in frequency than the system clock signal (201).

[0010] The power consumption of a microprocessor is of concern. Reducing the frequency of the chip clock signal (217) reduces the switching rate of other circuits in the microprocessor (12 in Figure 1). A low power mode may be entered when there is no activity in the microprocessor for an extended period of time. A slower switching rate typically reduces the power consumption of a microprocessor (12 in Figure 1).

[0011] A change in the frequency of the chip clock signal (217) is accomplished by changing the ratio in the divide by circuits (220, 222, 224). For example, during reduced power operation, the variable A may be set to 16 in the divide by A circuit (220); the variable B may be set to 5 in the divide by B circuit (224); and the variable C may be set to 32 in the divide by C circuit (222). In this example, the frequency of the chip clock signal (217) is 5/16 times the system clock signal (201). Also, the phase-frequency detector (202) updates 16 times less frequently compared to the non-reduced power example above.

[0012] Proper operation of the microprocessor (12 shown in Figure 1) depends on the PLL (200) maintaining a constant phase and frequency relationship between the system clock signal (201) and the chip clock signal (217).

[0013] As the frequencies of modern computers continue to increase, the need to rapidly transmit data between chip interfaces also increases. To accurately receive data, a clock signal is often sent to help recover the data. The clock signal determines when the data should be sampled or latched by a receiver circuit.

[0014] The clock signal may transition at the beginning of the time the data is valid. The receiver circuit, however, may require that the clock signal transition during the middle of the time the data is valid. Also, the transmission of the clock signal may degrade as it travels from its transmission point. In

both circumstances, a delay locked loop, or “DLL,” can regenerate a copy of the clock signal at a fixed phase shift with respect to the original clock signal.

[0015] Figure 3 shows a section of a typical computer system component (100). Data (114) that is K bits wide is transmitted from circuit A (112) to circuit B (134) (also referred to as the “receiver circuit”). To aid in the recovery of the transmitted data, a clock signal (116) is also transmitted with the data (114). The circuits could also have a path to transmit data from circuit B (134) to circuit A (112) along with an additional clock (not shown). The clock signal (116) may transition from one state to another at the beginning of the data transmission. Circuit B (134) requires a clock signal temporally located some time after the beginning of the valid data. Furthermore, the clock signal (116) may have degraded during transmission. The DLL has the ability to regenerate the clock signal (116) to a valid state and to create a phase shifted version of the clock signal (116) to be used by other circuits. For example, the receiver circuit (134) may use the phase shifted version of the clock signal (116) as the receiver circuit’s sampling signal. The receiver circuit’s sampling signal determines when the input to the receiver circuit should be sampled. The performance of a DLL is critical, and the DLL must maintain a proper reference of time on the CPU, or generically, an integrated circuit.

[0016] Figure 4 shows a block diagram of a typical DLL (300). Clock signal (301) is input to the DLL (300) to create a phased (i.e., delayed) output. Clock signal (301) is input to a voltage-controlled delay line (310) and to a phase detector (302). The phase detector (302) measures whether a phase difference between the clock signal (301) and an output signal, clk_out (317), of the voltage-controlled delay line (310) has the desired amount of delay. The phase detector (302) produces signals that control a charge pump (304). The phase detector (302) controls the charge pump (304) to increase or decrease its output current using up and down signals, U (303) and D (305). To ensure that the charge pump (304) maintains some nominal current output, the charge pump (304) is internally biased. The internal biasing of the charge pump (304) is

dependent on bias signals, V_{BP} (309) and V_{BN} (311), generated from a bias generator (308) (discussed below). The up and down signals (303, 305) adjust the current output of the charge pump (304) with respect to the nominal current set by the bias signals (309, 311).

[0017] The charge pump (304) adds or removes charge from a capacitor C_1 (306), which in turn, changes a voltage potential at the input of the bias-generator (308). The capacitor (306) is connected between a power supply, V_{DD} , and a control signal, V_{CTRL} (307). The bias-generator (308) produces the bias signals (309, 311) in response to the control signal (307), which, in turn, controls the delay of the voltage-controlled delay line (310) and maintains a nominal current output from the charge pump (304).

[0018] In Figure 4, the voltage-controlled delay line (310) may be implemented using current starved elements. This means that the delays are controlled by modifying the amount of current available for charging and discharging capacitances. The linearity of a voltage controlled delay line's characteristics determines the stable range of frequencies over which the DLL (300) can operate. The output signal (317) of the voltage-controlled delay line (310) represents a phase delayed copy of clock signal (301) that is then used by other circuits.

[0019] Still referring to Figure 4, the negative feedback created by the output signal (317) in the DLL (300) adjusts the delay through the voltage-controlled delay line (310). The phase detector (302) integrates the phase error that results between the clock signal (301) and the output signal (317). The voltage-controlled delay line (310) delays the output signal (317) by a fixed amount of time such that a desired delay between the clock signal (301) and the output signal (317) is maintained.

[0020] Accordingly, proper operation of the receiver circuit (134 in Figure 3) depends on the DLL (300) maintaining a constant phase delay between the clock signal (301) and the output signal (317).

Summary of Invention

[0021] According to an aspect of one or more embodiments of the present invention, an integrated circuit comprises: (1) a locked loop circuit comprising means for detecting a phase difference between a first clock signal and a second clock signal, means for generating a control signal dependent on the phase difference, a capacitor that stores a charge dependent on the control signal, and means for generating the second clock signal dependent on the control signal; and (2) a leakage current control circuit operatively connected to the capacitor, where the leakage current control circuit is arranged to adjust the stored charge.

[0022] According to an aspect of one or more embodiments of the present invention, a method for performing a locked loop circuit operation comprises: comparing a phase difference between a first clock signal and a second clock signal; generating a control signal dependent on the comparing; storing charge dependent on the control signal using a capacitor connected to the control signal; controlling a leakage current of the capacitor; and generating the second clock signal dependent on the control signal.

[0023] Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0024] Figure 1 shows a typical computer system component.

[0025] Figure 2 shows a block diagram of a prior art phase locked loop.

[0026] Figure 3 shows a typical computer system component.

[0027] Figure 4 shows a block diagram of a prior art delay locked loop.

[0028] Figure 5 shows a circuit in accordance with an embodiment of the present invention.

[0029] Figure 6 shows a portion of the circuit shown in Figure 5 in accordance

with an embodiment of the present invention.

[0030] Figure 7 shows a portion of a circuit in accordance with an embodiment of the present invention.

[0031] Figure 8 shows a schematic diagram of a phase-frequency detector.

[0032] Figure 9 shows a schematic diagram of a charge pump.

[0033] Figure 10 shows a timing diagram for the phase-frequency detector shown in Figure 8.

[0034] Figure 11 shows a block diagram of a circuit with an adjustable leakage current control circuit in accordance with an embodiment of the present invention.

[0035] Figure 12 shows a block diagram of a circuit with an adjustable leakage current control circuit in accordance with an embodiment of the present invention.

[0036] Figure 13 shows a schematic diagram of a programmable current source in accordance with an embodiment of the present invention.

[0037] Figure 14 shows a block diagram of a circuit with an adjustable leakage current control circuit in accordance with an embodiment of the present invention.

Detailed Description

[0038] As device features, such as transistor features, used to implement integrated circuit components, e.g., PLLs/DLLs, continue to get smaller, they may have higher leakage currents (i.e., higher gate tunneling currents). This is due to the fact that as transistor features are designed smaller, the thickness of the transistor's oxide layer (located between the transistor's gate and the semiconductor substrate) is reduced. As the oxide layer is reduced to a few angstroms, the transistor's gate terminal begins to leak charge to the other terminals of the transistor. In the case of a loop filter capacitor, which is

typically desired to be large from a capacitance perspective and that can be implemented with a transistor, such reduction in transistor size features and consequential increase in leakage current can adversely affect the behavior of the PLL/DLL. In some cases, particular amounts of leakage current through the loop filter capacitor can even cause the PLL/DLL to malfunction. Accordingly, there is a need for a PLL/DLL design that guards against or compensates for a loop filter capacitor's leakage current.

[0039] Figure 5 shows an exemplary locked loop circuit in accordance with an embodiment of the present invention. Those skilled in the art will understand that although the particular type of locked loop circuit in Figure 5 is a PLL (470), the principles of the present invention are similarly applicable to a DLL. In Figure 5, the PLL (470) uses a phase frequency detector (472) that detects a phase difference between an input clock signal, *clk_in* (474), and a feedback clock signal, *fbk_clk* (476). Dependent on the phase difference detected by the phase frequency detector (472), the phase frequency detector (472) outputs pulses on UP (478) and DOWN (480) signals to a charge pump (482). The charge pump (482), dependent on the pulses on the UP (478) and DOWN (480) signals, generates a voltage control signal, *Vctrl* (484).

[0040] For stability, the PLL (470) uses a loop filter, formed by a loop filter capacitor (486) and a loop filter resistor (487), that is operatively connected to the voltage control signal (484). The loop filter capacitor (486) stores/dissipates charge dependent on the voltage control signal (484). Those skilled in the art will understand that the loop filter capacitor (486) may be implemented using the gate capacitance of a metal-oxide semiconductor field-effect transistor (MOSFET). The UP (478) and DOWN (480) signals are pulsed only once per clock cycle, and therefore, the voltage control signal (484) may not be maintained due to the leakage current of the loop filter capacitor (486). To guard against increased leakage currents associated with smaller transistor features, a leakage current control circuit (488) is positioned between the loop filter capacitor (486) and a voltage potential *Vdd* (490). Those skilled

in the art will note, that in one or more other embodiments, the leakage current control circuit (488) may be connected to a voltage potential V_{ss} , or ground (as shown in Figure 7), instead of the voltage potential V_{dd} (490).

[0041] As shown in Figure 5, the leakage current control circuit (488) is operatively connected to the UP (478) and DOWN (480) signals such that the leakage current control circuit (488) (1) allows the loop filter capacitor (486) to leak when the charge pump (482) is 'on,' (the charge pump (482) is said to be 'on' when the charge pump (482) actively sources or sinks current to/from the voltage control signal (484)) and (2) restricts the leakage current of the loop filter capacitor (486) when the charge pump (482) is 'off.' Those skilled in the art will understand that whenever one or both of the UP (478) and DOWN (480) signals is pulsed, the charge pump (482) turns 'on' for the duration of the pulse(s). A more detailed description of a leakage current control circuit is given below with reference to Figures 6 and 7.

[0042] Referring to Figure 5, the voltage control signal (484) serves as an input to a bias generator (492) that produces at least one bias signal (494) to a voltage-controlled oscillator (VCO) (496). The voltage-controlled oscillator (496), dependent on the at least one bias signal (494) from the bias generator (492), generates an output clock signal, clk_out (498). The output clock signal (498), in addition to serving as an output of the PLL (470), is fed back to an input of the phase frequency detector (472) through a clock distribution network (400) and a feedback divider (402). Those skilled in the art will note that, in one or more other embodiments, the PLL (470) may be implemented without the bias generator (492) by operatively connecting the voltage-controlled oscillator (496) with the voltage control signal (484).

[0043] Figure 6 shows an implementation of the leakage current control circuit (488) shown in Figure 5 in accordance with an embodiment of the present invention. In Figure 6, the leakage current control circuit (488) includes a p-channel transistor switch (500) and NOR gate circuitry (508) responsive to the UP (478) and DOWN (480) signals (from the phase frequency detector (472) as

shown in Figure 5). More particularly, the p-channel transistor switch (500) has a first terminal (502) operatively connected to the voltage potential Vdd (490) and a second terminal (504) operatively connected to the loop filter capacitor (486). A gate terminal (506) of the p-channel transistor switch (500) is operatively connected to an output of the NOR gate circuitry (508). The NOR gate circuitry (508) outputs 'low' when one or both of the UP (478) and DOWN (480) signals are 'high' and outputs 'high' when both the UP (478) and DOWN (480) signals are 'low.' Accordingly, when one or both of the UP (478) and DOWN (480) signals are 'high,' (i.e., the charge pump ((482) in Figure 5) is 'on'), the NOR gate circuitry (508) outputs 'low' to the p-channel transistor switch (500), which, in turn, causes the p-channel transistor switch (500) to switch 'on' and allow the loop filter capacitor (486) to leak. Conversely, when both the UP (478) and DOWN (480) signals are 'low' (i.e., the charge pump ((482) in Figure 5) is 'off'), the NOR gate circuitry (508) outputs 'high' to the p-channel transistor switch (500), which, in turn, causes the p-channel transistor switch (500) to switch 'off' and restrict the leakage current of the loop filter capacitor (486).

[0044] Due to this configuration, the leakage current of the loop filter capacitor (486) is controlled because it cannot get larger than the source to drain current of the p-channel transistor switch (500). Moreover, because the charge pump ((482) in Figure 5) is 'off' the majority of the time, the cumulative reduction of the loop filter capacitor's (486) leakage current facilitates the increased integrity of the voltage control signal (484), which, in turn, leads to reliable and stable PLL operation.

[0045] Figure 7 shows a leakage current control circuit (514) in accordance with another embodiment of the present invention. In Figure 7, a PLL loop filter capacitor (510) is referenced to a voltage potential Vss, or ground (512), instead of the voltage potential Vdd ((490) in Figures 5 and 6). In this embodiment, the leakage current control circuit (514) includes a n-channel transistor switch (516) an OR gate circuitry (524) responsive to the UP (478)

and DOWN (480) signals (from the phase frequency detector (472) as shown in Figure 5). More particularly, the n-channel transistor switch (516) has a first terminal (520) operatively connected to the voltage potential ground (512) and a second terminal (518) operatively connected to the loop filter capacitor (510). A gate terminal (5220) of the n-channel transistor switch (516) is operatively connected to an output of the OR gate circuitry (524). The OR gate circuitry (524) outputs 'high' when one or both of the UP (478) and DOWN (480) signals are 'high' and outputs 'low' when both the UP (478) and DOWN (480) signals are 'low.' Accordingly, when one or both of the UP (478) and DOWN (480) signals are 'high,' (i.e., the charge pump ((482) in Figure 5) is 'on'), the OR gate circuitry (524) outputs 'high' to the n-channel transistor switch (516), which, in turn, causes the n-channel transistor switch (516) to switch 'on' and allow the loop filter capacitor (510) to leak. Conversely, when both the UP (478) and DOWN (480) signals are 'low' (i.e., the charge pump ((482) in Figure 5) is 'off'), the OR gate circuitry (524) outputs 'low' to the n-channel transistor switch (516), which, in turn, causes the n-channel transistor switch (516) to switch 'off' and restrict the leakage current of the loop filter capacitor (516).

[0046] Due to this configuration, the leakage current of the loop filter capacitor (510) is controlled because it cannot get larger than the source to drain current of the n-channel transistor switch (516). Moreover, because the charge pump ((482) in Figure 5) is 'off' the majority of the time, the cumulative reduction of the loop filter capacitor's (510) leakage current facilitates the increased integrity of the voltage control signal (484), which, in turn, leads to reliable and stable PLL operation.

[0047] Those skilled in the art will understand that, in other embodiments, the switches in the leakage current control circuit ((488) in Figure 6 and (514) in Figure 7) may be implemented using devices other than p- and n-channel transistors.

[0048] As mentioned above, those skilled in the art will understand that the

foregoing discussion with reference to Figures 5-7 is similarly applicable to a DLL.

[0049] Embodiments of the present invention also relate to an adjustment and calibration system for post-fabrication adjustment of a locked loop circuit. With reference to Figure 2, charge may leak from the capacitor (206), which, in turn, changes the stored voltage potential on the capacitor (206). Accordingly, the frequency of the voltage-controlled oscillator (210) may drift. The same is the case with a DLL as shown in Figure 4.

[0050] The adjustment system of the present invention includes combinational logic that controls a leakage current control circuit using an adjustment circuit that compensates for such a leakage current. Thus, with respect to the PLL shown in Figure 2, the leakage current of the capacitor (206) may be offset so that the capacitor (206) maintains a constant voltage potential. The same is possible with a DLL.

[0051] Figure 8 shows a block diagram of a phase-frequency detector (600). The phase-frequency detector (600) is representative of the phase-frequency detector (202) shown in Figure 2. Those skilled in the art will understand that the phase-frequency detector (600) is similar to that of the phase detector of the DLL shown in Figure 4. In Figure 8, the phase-frequency detector (600) integrates the phase error that results between the clock A signal (221) and the clock B signal (223). The clock A signal (221) clocks a flip-flop (606) and the clock B signal (223) clocks a flip-flop (608).

[0052] When clock A signal (221) transitions from a low state to a high state, flip-flop (606) transfers the high state created by the power supply V_{DD} (651) on an input of the flip-flop (606) to the up signal (203). When the clock B signal (223) transitions from a low state to a high state, flip-flop (608) transfers the high state created by the power supply V_{DD} (651) on an input of the flip-flop (608) to the down signal (205). When both the up and down signals (203, 205) are at a high state, the AND gate (603) outputs a high state on signal line

(607). The high state on signal line (607) resets both flip-flop (606) and flip-flop (608). The up and down signals (203, 205) transition to a low state when the flip-flop (606) and flip-flop (608) are reset, respectively.

[0053] Figure 9 shows a block diagram of a charge pump (700). The charge pump (700) is representative of the charge pumps (204, 234) shown in Figure 2. Those skilled in the art will understand that the charge pump (700) is similar to that of the charge pump of the DLL shown in Figure 4. In Figure 9, the charge pump (700) has two current sources (702, 708). The current source (702) is connected between the power supply V_{DD} (701) and the signal line (703). The current source (708) is connected between the power supply V_{SS} (707) and the signal line (705).

[0054] In Figure 9, the up and down signals (203, 205) from the phase-frequency detector (600) shown in Figure 8 determine whether switches (704, 706) are closed, respectively. When the up signal (203) is at a high state, the switch (704) is closed. The switch (704) is connected between signal (703) and the control voltage (207). When closed, the switch (704) allows the current generated by the current source (702) to add charge to the capacitor (e.g., 206 shown in Figure 2) using the control voltage (207).

[0055] When the down signal (205) is at a high state, the switch (706) is closed. The switch (706) is connected between signal (705) and the control voltage (207). When closed, the switch (706) allows the current generated by the current source (708) to remove charge from the capacitor (e.g., 206 shown in Figure 2) using the control voltage (207).

[0056] A short time period exists when both the up and down signals (203, 205) are at a high state. In Figure 8, when both the up and down signals (203, 205) transition to a high state, the AND gate (603) resets the flip-flops (606, 608) by generating a high state on the signal line (607). A finite time duration is needed for the AND gate (603) and the flip-flops (606, 608) to respond to this change in state. In Figure 9, both the switches (704, 706) are closed when both

the up and down signals (203, 205) signals are high. During this time, a nominal amount of charge is added to the capacitor (e.g., 206 shown in Figure 2). Some or all of the current generated by the current source (702) is transferred to the V_{SS} power supply (707) through the current source (708).

[0057] Figure 10 shows a timing diagram (800) for the phase-frequency detector (600) shown in Figure 8. The timing diagram (800) shows two clock cycles. The first clock cycle shows the clock B signal (223) lagging the clock A signal (221) (i.e., they are out of phase). The second cycle shows the clock B signal (223) properly aligned with the clock A signal (221).

[0058] In the first cycle, when the clock A signal (221) transitions from a low state to a high state, the up signal (203) transitions from a low state to a high state. When the clock B signal (223) transitions from a low state to a high state, the down signal (205) transitions from a low state to a high state. Because both the up and down signals (203, 205) are at a high state, the AND gate (603 shown in Figure 8) resets both flip-flops (606, 608 shown in Figure 8). The up and down signals (203, 205) output a low state when the flip-flops (606, 608 shown in Figure 8) are reset, respectively.

[0059] In the first cycle, the up signal (203) is at a high state for a longer duration than the down signal (205). Accordingly, the current source (702 shown in Figure 9) adds charge to the capacitor (e.g., 206 shown in Figure 2). If the down signal (205) was at a high state for a longer duration than the up signal (203), the current source (708 shown in Figure 9) would remove charge from the capacitor (206 shown in Figure 2). The change in the voltage potential maintained by the capacitor (e.g., 206 shown in Figure 2) affects the frequency of the voltage-controlled oscillator (e.g., 210 shown in Figure 2).

[0060] In Figure 10, in the second cycle, both the clock A signal (221) and the clock B signal (223) transition from a low state to a high state at the same time. In other words, the clock A signal (201) and the clock B signal (223) are in phase. Accordingly, both the up and down signals (203, 205) transition from a

low state to a high state at the same time. Also, both the flip-flops (606, 608 shown in Figure 8) are reset simultaneously. Because a finite time duration (i.e., t_{MIN}) is needed for the AND gate (603 shown in Figure 8) and the flip-flops (606, 608 shown in Figure 8) to respond to the change in state, both the up and down signals (203, 205) have a finite time duration for which they are high. A nominal amount of charge is added to the capacitor (e.g., 206 shown in Figure 2) to maintain the present voltage potential on the control voltage (207 shown in Figure 2).

[0061] In Figure 10, the times during which the charge pump (700 shown in Figure 9) may modify or maintain the charge on the capacitor (e.g., 206 shown in Figure 2) are indicated. When the clock A signal (221) and the clock B signal (223) are aligned, the time duration that the charge pump (700 shown in Figure 9) is active is relatively small (i.e., t_{MIN}) compared to the time duration the charge pump is inactive. During the time the charge pump (700 shown in Figure 9) is inactive (i.e., when both switches (704, 706) are open), the voltage potential on the capacitor (e.g., 206 shown in Figure 2) may drift due to leakage currents inherent with devices used to form the capacitor (e.g., 206 shown in Figure 2). Furthermore, the time duration that the charge pump (700 shown in Figure 9) is inactive (i.e., when both switches (704, 706) are open) is increased during power reduction modes. As in the example above, the time duration between the charge pump (700 shown in Figure 9) activity is increased 16 times in a power reduction mode compared to normal operation. The voltage potential on the capacitor (e.g., 206 in Figure 2) may drift a larger amount during the power reduction mode. A means to compensate for the drift and store the amount of compensation is needed.

[0062] Semiconductor capacitors are typically parallel plate capacitors formed by connecting the source and drain of a transistor together to create one terminal of the capacitor. The other terminal of the capacitor is formed by the gate connection of the transistor. Tunneling through the gate creates a path for leakage current. Leakage current causes the voltage potential originally stored

on the capacitor to change. In a locked loop circuit such as a PLL, the capacitor (e.g., 206 shown in Figure 2) helps maintain the amount of frequency produced by the voltage-controlled oscillator (e.g., 210 shown in Figure 2).

[0063] In Figure 2, the relatively long time durations between the charge pump (204) updating the charge stored (i.e., voltage potential stored) on the capacitor (206) may result in a drift in the expected amount of frequency of the PLL (200). Although a designer may intend for an integrated circuit to have a particular value for the leakage current of the capacitor (206), actual values for these parameters are typically unknown until the integrated circuit has been fabricated (i.e., in a post-fabrication stage).

[0064] For example, a designer may intend for the frequency drift of the PLL (200) to be within in a particular range. The leakage current of the capacitor (206) may be unintentionally affected by many factors in the fabrication process. Because the leakage current cannot be redesigned in the post-fabrication stage without considerable temporal and monetary expenditures, these fabrication factors may cause the PLL (200) to have a different frequency drift range than the range the PLL (200) was designed. Consequently, the PLL (200) may have poor performance. Accordingly, there is a need for a technique and design that facilitates increased post-fabrication control of leakage current in the capacitor (206) of the PLL (200).

[0065] Figure 11 shows an exemplary adjustable locked loop circuit in accordance with an embodiment of the present invention. Those skilled in the art will understand that although Figure 11 shows a particular locked loop circuit as being a PLL (900), the principles of the present invention are similarly applicable to a DLL. The phase-frequency detector (202), capacitor (206), bias-generator (208), and voltage-controlled oscillator (210) of the adjustable PLL (900) operate similar to those respective components described above with reference to Figure 2.

[0066] In Figure 11, a leakage current control circuit (904) is connected

between the control voltage (207) and a power supply V_{SS} . As the capacitor (206) leaks current, the voltage potential on the control voltage (207) has a tendency to drift toward the power supply V_{DD} . The leakage current control circuit (904) is arranged to pull the voltage potential on the control voltage (207) toward a power supply V_{SS} . For example, an n-channel transistor is used as the leakage current control circuit (904).

[0067] One of ordinary skill in the art will understand that in other embodiments, the capacitor (206) may be connected between the control voltage (207) and the power supply V_{SS} . In this case, the leakage current control circuit (904) is connected between the control voltage (207) and the power supply V_{DD} . A leakage current control circuit (904) in this arrangement may be a p-channel transistor.

[0068] In Figure 11, an adjustment circuit (954) is used to adjust the leakage current control circuit (904) to compensate for the leakage current of the capacitor (206). A bias voltage potential, V_{BIAS} (961), is used to control the amount of compensation applied to offset the leakage current. The bias voltage potential (961) may be adjusted to increase, decrease, turn off, or maintain the amount of leakage current compensation (i.e., leakage current offset) produced by the leakage current control circuit (904).

[0069] In Figure 11, a combinational logic circuit (952) controls the adjustment circuit (954) using multiple adjustment signals N (953). The values of the multiple adjustment signals N (953) are determined by the combinational logic circuit (952). The combinational logic circuit (952) may communicate through an interface (not shown) using M communication lines (951). Those with ordinary skill in the art will understand that the interface and M communication lines (951) may take a wide variety of forms. The communication may be defined by an industry standard.

[0070] The combinational logic circuit (952) generates the multiple adjustment signals N (953) in response to the signal values on the M communication lines

(951). The combinational logic circuit (952) may have 2^M input combinations. For example, M may equal four and N may equal six. Accordingly, sixteen combinations exist for values on the six adjustment signals N (953).

[0071] Those skilled in the art will understand that the adjustable PLL (900) may be analog, digital, or a combination of both types of circuits.

[0072] Figure 12 shows another exemplary locked loop circuit in accordance with an embodiment of the present invention. Those skilled in the art will understand that although Figure 12 shows a particular locked loop circuit as being a PLL (1000), the principles of the present invention are similarly applicable to a DLL. The phase-frequency detector (202), capacitor (206), bias-generator (208), voltage-controlled oscillator (210), leakage current control circuit (904), and adjustment circuit (954) of the adjustable PLL (1000) operate similar to those respective components described above with reference to Figure 11.

[0073] In Figure 12, a combinational logic circuit (1062) controls the adjustment circuit (954) using multiple adjustment signals N (953). The values of the multiple adjustment signals N (953) are determined by the combinational logic circuit (1062). The up and down signals (203, 205) from the phase-frequency detector (202) control the combinational logic circuit (1062).

[0074] The combinational logic circuit (1062) generates the multiple adjustment signals N (953) in response to the up and down signals (203, 205). In one or more embodiments, the combinational logic circuit (1062) may use a state machine to generate the multiple adjustment signals N (953). In other embodiments, the combinational logic circuit (1062) may be an analog circuit with an analog-to-digital converter to generate the multiple adjustment signals N (953). In other embodiments, the combinational logic circuit (1062) and adjustment circuit (954) may be combined to perform a function similar to the charge pump (204) where this additional charge pump controls the leakage current control circuit (904).

[0075] Those skilled in the art will understand that the adjustable PLL (1000) may be analog, digital, or a combination of both types of circuits.

[0076] Figure 13 shows a programmable current source (1100) in accordance with an embodiment of the present invention. The programmable current source can be representative of the adjustment circuits (954) shown in Figures 11 and 12. The programmable current source (1100) includes multiple p-channel transistors (1102, 1106, 1110) connected respectively to multiple current sources (1122, 1124, 1126) arranged in parallel with each other. The current sources (1122, 1124, 1126) connect to the power supply V_{DD} and the p-channel transistors (1102, 1106, 1110), respectively. The p-channel transistors (1102, 1106, 1110) have a common node on which the bias voltage potential V_{BIAS} (961) is supplied to the leakage current control circuit (904 shown in Figure 11 and Figure 12). The programmable current source (1100) also includes multiple n-channel transistors (1104, 1108, 1112) connected respectively to multiple current sources (1128, 1130, 1132) arranged in parallel with each other. The current sources (1128, 1130, 1132) connect to the power supply V_{SS} and the n-channel transistors (1104, 1108, 1112), respectively. The n-channel transistors (1104, 1108, 1112) connect to the bias voltage potential V_{BIAS} (961).

[0077] Each transistor has a corresponding individual control signal that turns “on” or “off” the respective p-channel transistors (1102, 1106, 1110) and respective n-channel transistors (1104, 1108, 1112). The p-channel transistors (1102, 1106, 1110) have control signals EN_P_0 (1101), EN_P_1 (1105), and EN_P_N (1109) connected to their gates, respectively. The n-channel transistors (1104, 1108, 1112) have control signals EN_N_0 (1103), EN_N_1 (1107), and EN_N_N (1111) connected to their gates, respectively. A “low” voltage potential on any of the EN_P_x control signals (1101, 1105, 1109), where “x” represents any index 0 through N, turns “on” the respective p-channel transistor (1102, 1106, 1110). A “high” voltage potential on any of the EN_N_x control signals (1103, 1107, 1111), where “x” represents any index 0 through N, turns

“on” the respective n-channel transistor (1104, 1108, 1112).

[0078] A p-channel transistor (1102, 1106, 1110) that is “on” changes the bias voltage potential (961) toward power supply V_{DD} . The change in the bias voltage potential (961) is caused by current flow provided by one or more of the current sources (1122, 1124, 1126) onto the bias voltage potential (961). An n-channel transistor (1104, 1108, 1112) that is “on” changes the bias voltage potential (961) toward power supply V_{SS} . The change in the bias voltage potential (961) is caused by current flow provided by one or more of the current sources (1128, 1130, 1132) away from the bias voltage potential V_{BIAS} (961). By selecting which p-channel transistors (1102, 1106, 1110) and/or n-channel transistors (1104, 1108, 1112) are “on,” a selected change in the bias voltage potential V_{BIAS} (661) may be achieved.

[0079] Those with ordinary skill in the art will understand that the current sources (1122, 1124, 1126, 1128, 1130, 1132) may be designed using transistors that operate in a saturated region. Furthermore, the p-channel transistors (1102, 1106, 1110) and n-channel transistors (1104, 1108, 1112) operate as switches to connect the current sources (1122, 1124, 1126, 1128, 1130, 1132) to the bias voltage potential V_{BIAS} (961).

[0080] Those with ordinary skill in the art will understand that the p-channel transistors (1102, 1106, 1110) and n-channel transistors (1104, 1108, 1112) may be turned “on” individually or as a group. Each current source (1122, 1124, 1126, 1128, 1130, 1132) may provide a fixed amount of current; although, the current provided by each current source (1122, 1124, 1126, 1128, 1130, 1132) may differ from the other current sources (1122, 1124, 1126, 1128, 1130, 1132). The current sources (1122, 1124, 1126, 1128, 1130, 1132) may be designed to provide a linear, exponential, or other function as the current sources (1122, 1124, 1126, 1128, 1130, 1132) are connected or disconnected from bias voltage potential V_{BIAS} (961).

[0081] The p-channel transistors (1102, 1106, 1110) and n-channel transistors

(1104, 1108, 1112) may be used to add or subtract a fixed amount of current from the current on the bias voltage potential V_{BIAS} (661). The p-channel transistors (1102, 1106, 1110) and n-channel transistors (1104, 1108, 1112) control the operation of the programmable current source (1100). The programmable current source includes a plurality of current sources with each current source operatively connected to a switch. The switch controls the current flow from the current source.

[0082] In Figure 11, the combinational logic circuit (952) generates a binary control word that determines which n-channel transistors (1104, 1108, 1112 shown in Figure 13) and p-channel transistors (1102, 1106, 1110 shown in Figure 13) are “on” and which are “off” in the adjustment circuit (954). Depending on the signal values of the M communication lines (951) received by the combinational logic circuit (952), multiple adjustment signals N (953) that represent EN_N_X signals (1103, 1107, 1111 in Figure 13) and EN_P_X signals (1101, 1105, 1109 in Figure 13) may turn “on” or turn “off” the p-channel transistors (1102, 1106, 1110 shown in Figure 13) and n-channel transistors (1104, 1108, 1112 shown in Figure 13) in the adjustment circuit (954). The bias voltage potential V_{BIAS} (961) of the adjustment circuit (954) adjusts the leakage current control circuit (904) to compensate for the leakage current of the capacitor (206).

[0083] In Figure 12, the combinational logic circuit (1052) generates a binary control word that determines which n-channel transistors (1104, 1108, 1112 shown in Figure 13) and p-channel transistors (1102, 1106, 1110 shown in Figure 13) are “on” and which are “off” in the adjustment circuit (954). The multiple adjustment signals N (653) that represent EN_N_X signals (1103, 1107, 1111 in Figure 13) and EN_P_X signals (1101, 1105, 1109 in Figure 13) may turn “on” or turn “off” the p-channel transistors (1102, 1106, 1110 shown in Figure 13) and n-channel transistors (1104, 1108, 1112 shown in Figure 13) in the adjustment circuit (954). The bias voltage potential V_{BIAS} (961) of the adjustment circuit (954) adjusts the leakage current control circuit (904) to

compensate for the leakage current of the capacitor (206).

[0084] The adjustable PLL (900 in Figure 11 and 700 in Figure 12), after fabrication, may demonstrate undesirable operating characteristics that may not have been apparent from simulation. In one or more embodiments, because the adjustment circuit (954 shown in Figure 11 and Figure 12) may modify the operating characteristics of the adjustable PLL (900 in Figure 11 and 700 in Figure 12), the adjustable PLL (900 in Figure 11 and 700 in Figure 12) may be adjusted.

[0085] Those skilled in the art will understand that the principles of foregoing discussion with reference to Figures 8-13 is similarly applicable to a DLL.

[0086] Figure 14 shows an exemplary locked loop circuit in accordance with another embodiment of the present invention. Those skilled in the art will understand that although Figure 14 shows a particular locked loop circuit as being a PLL (1200), the principles of the present invention are similarly applicable to a DLL. The phase-frequency detector (202), capacitor (206), bias-generator (208) and voltage-controlled oscillator (210) of the adjustable PLL (1200) operate similar to those respective components described above with reference to Figure 2.

[0087] In Figure 14, a leakage current control circuit (1204) is connected between the control signal (207) and a power supply V_{SS} . As the capacitor (206) leaks current, the voltage potential on the control signal (207) has a tendency to drift toward the power supply V_{DD} . The leakage current control circuit (1204) is arranged to pull the voltage potential on the control signal (207) toward a power supply V_{SS} . For example, in Figure 14, an n-channel transistor is used as the leakage current control circuit (1204).

[0088] One of ordinary skill in the art will understand that in other embodiments, the capacitor (206) may be connected between the control signal (207) and the power supply V_{SS} . In this case, the leakage current control circuit (1204) is connected between the control signal (207) and the power supply

V_{DD} . A leakage current control circuit (1204) in this arrangement may be a p-channel transistor.

[0089] In Figure 14, an adjustment circuit (1254) is used to adjust the leakage current control circuit (1204) to compensate for the leakage current of the capacitor (206). A bias voltage potential, V_{BIAS} (1261), is used to control the amount of compensation applied to offset the leakage current. The bias voltage potential (1261) may be adjusted to increase, decrease, turn off, or maintain the amount of leakage current compensation (i.e., leakage current offset) produced by the leakage current control circuit (1204). The adjustment circuit (1254) may be similar to the one described with respect to and shown in Figure 13.

[0090] In Figure 14, a test processor unit (1252) controls the adjustment circuit (1254) using multiple adjustment signals N (1253). The values of the multiple adjustment signals N (1253) are determined by the test processor unit (1252). The test processor unit (1252) generates the multiple adjustment signals N (1253), or binary control word, from registers that determine the settings of the adjustment circuit (1254). The test processor unit (1252) may change the contents of its registers through a host interface.

[0091] In one or more embodiments of the present invention, the test processor unit (1252) may respond to instructions. The instructions may be interpreted by the test processor unit (1252) and may result in a change to register contents stored in the test processor unit (1252). A change to register contents may result in a change to the multiple adjustment signals N (1253).

[0092] The test processor unit (1252) may communicate through a host interface using M communication lines (1251). Those of ordinary skill in the art will understand that the host interface and M communication lines (1251) may take a wide variety of forms. In one or more embodiments, the host interface may be operatively connected to a separate computer system. Further, in one or more embodiments, the host interface may be defined by an industry standard.

[0093] As mentioned above, the host interface may be used to operatively connect to a separate computer system. For example, a tester (not shown) may communicate with the test processor unit (1252). In some embodiments, the tester (not shown) may instruct the test processor unit (1252) to adjust adjustment circuit (1254) to modify the offset of a leakage current of the adjustable PLL (1200). In some embodiments, the tester (not shown) may measure an operating characteristic of the adjustable PLL (1200) or a representative operating characteristic of an integrated circuit on which the adjustable PLL (1200) resides to determine the effect of the adjustment. A variety of different adjustments may be made in order to identify the adjustment settings that produce the desired operating characteristics of the adjustable PLL (1200).

[0094] For example, the tester (not shown) may be used to adjust the adjustable PLL (1200) until the delay drift in the voltage-controlled oscillator (210) is minimized. The tester (not shown) may also be used to adjust the adjustable PLL (1200) until the operating characteristics of the adjustable PLL (1200) reaches a desired performance level. Such operating characteristics may include delay drift, maximum operating frequency, minimum operating frequency, lock time, etc.

[0095] One of ordinary skill in the art will understand that even though the adjustment circuit (1254) may be connected to the bias voltage potential (1261) of the leakage current control circuit (1204), the adjustment circuit (1254) may be turned "off." In other words, the adjustment circuit (1254) may be controlled so as not to have an effect on the adjustable PLL (1200). The test processor unit (1252) operatively controls the adjustment circuit (1254). The bias voltage potential (1261) of the adjustment circuit (1254) adjusts the leakage current control circuit (1204).

[0096] Those skilled in the art will understand that the adjustable PLL (1200) may be analog, digital, or a combination of both types of circuits.

[0097] Those skilled in the art will understand that the principles of the foregoing discussion with reference to Figure 14 is similarly applicable to a DLL.

[0098] Advantages of the present invention may include one or more of the following. In one or more embodiments, because a leakage current of a PLL/DLL loop filter capacitor may be controlled, a more stable and reliable operation of the PLL/DLL may be facilitated. Accordingly, the phase shift of the PLL/DLL may not drift or may not drift as much as a PLL/DLL design that does not use a switch to resistively isolate the loop filter capacitor.

[0099] In one or more embodiments, because a switch positioned in series with a PLL/DLL loop filter capacitor helps control a leakage current of the PLL/DLL loop filter capacitor, the chip area consumed by the PLL/DLL loop filter capacitor may be reduced because the PLL/DLL loop filter capacitor does not have to be as large to maintain the voltage potential on a voltage control signal.

[00100] The adjustable PLL/DLL, after fabrication, may demonstrate undesirable operating characteristics that may not have been apparent from simulation. In one or more embodiments, because the adjustment circuit may modify the operating characteristics of the adjustable PLL/DLL, the adjustable PLL/DLL may be adjusted.

[00101] In one or more embodiments, because the adjustable PLL/DLL may be fabricated with a means for compensating the leakage current of the capacitor, fewer design iterations and higher confidence in the adjustable PLL/DLL operating characteristics may be afforded.

[00102] In one or more embodiments, because an adjustment circuit may modify the operating characteristics of the adjustable PLL/DLL, an investigation of the adjustable PLL/DLL's response during operating conditions may be performed.

[00103] In one or more embodiments, a limited number of adjustable PLL/DLLs may need to be tested to determine a desired adjustment that may be used for

future, non-adjustable PLL/DLLs.

[00104] In one or more embodiments, a current source in programmable current source may have a fixed current supply. A fixed current source may be easier to design and maintain at a fixed current supply. The programmable current source may add, subtract, and/or redirect current from the current sources using digital control of switches.

[00105] In one or more embodiments, because the adjustment circuit may modify the operating characteristics of the adjustable PLL/DLL, an investigation of the adjustable PLL/DLL's response during operating conditions may be performed. Realistic results help determine appropriate values for circuit elements within the adjustable PLL/DLL and help alleviate costly over design.

[00106] In one or more embodiments, a tester and test processor unit may communicate so that performance characteristics may be analyzed, and/or adjustments made to the adjustable PLL/DLL.

[00107] While the invention has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.

Claims

- [c1] An integrated circuit, comprising:
- a locked loop circuit comprising:
 - means for detecting a phase difference between a first clock signal and a second clock signal,
 - means for generating a control signal dependent on the phase difference,
 - a capacitor that stores a charge dependent on the control signal,
 - and
 - means for generating the second clock signal dependent on the control signal; and
 - a leakage current control circuit operatively connected to the capacitor, wherein the leakage current control circuit is arranged to adjust the stored charge.
- [c2] The integrated circuit of claim 1, wherein the leakage current control circuit is connected between the capacitor and a voltage potential, wherein the leakage current control circuit comprises a switch responsive to the means for detecting, and wherein the switch is positioned in series with the capacitor.
- [c3] The integrated circuit as in claims 1 or 2, further comprising:
- a programmable current source connected to the leakage current control circuit, wherein the programmable current source comprises a first current source and a first switch arranged to control the leakage current control circuit; and
 - a combinational logic circuit operatively connected to the programmable current source, wherein the combinational logic circuit is arranged to selectively adjust the programmable current source.

- [c4] The integrated circuit as in claims 1, 2, or 3, further comprising:
- an adjustment circuit operatively connected to the leakage current control circuit, wherein the adjustment circuit is arranged to control the leakage current control circuit; and
 - a test processor unit operatively connected to the adjustment circuit, wherein the test processor unit is arranged to selectively adjust the adjustment circuit.
- [c5] The integrated circuit as in claims 1, 2, 3, or 4, wherein the locked loop circuit is one of a phase locked loop and a delay locked loop.
- [c6] The integrated circuit of claim 3, wherein the first current source and the first switch are arranged to control current flow between a first voltage potential and an output of the programmable current source dependent on a first control signal, and wherein the output is operatively connected to the leakage current control circuit.
- [c7] The integrated circuit of claim 6, the programmable current source further comprising:
- a second current source and a second switch arranged to control current flow between a second voltage potential and the output of the programmable current source dependent on a second control signal.
- [c8] The integrated circuit of claim 3, wherein the combinational logic circuit is arranged to adjust the programmable current source responsive to the phase difference between the first clock signal and the second clock signal.
- [c9] The integrated circuit of claim 4, wherein the adjustment circuit comprises:
- a first switch arranged to control current flow between a first voltage potential and an output of the adjustment circuit; and
 - a second switch arranged to control current flow between a second voltage potential and the output of the adjustment circuit, wherein

the output is operatively connected to the leakage current control circuit.

[c10] The integrated circuit as in claims 4 or 9, wherein the adjustment circuit comprises a first p-channel transistor and a first n-channel transistor, wherein the first p-channel transistor and the first n-channel transistor are connected in series.

[c11] The integrated circuit of claim 10, the adjustment circuit further comprising:
a second p-channel transistor connected in parallel with the first p-channel transistor; and
a second n-channel transistor connected in parallel with the first n-channel transistor, wherein the first p-channel transistor and second p-channel transistor are in series with the first n-channel transistor and second n-channel transistor.

[c12] The integrated circuit as in any of the preceding claims, the locked loop circuit further comprising:
means for outputting at least one bias signal dependent on the control signal, wherein the means for generating the second clock signal is dependent on the at least one bias signal.

[c13] A method for performing a locked loop circuit operation, comprising:
comparing a phase difference between a first clock signal and a second clock signal;
generating a control signal dependent on the comparing;
storing charge dependent on the control signal using a capacitor connected to the control signal;
controlling a leakage current of the capacitor; and
generating the second clock signal dependent on the control signal.

[c14] The method of claim 13, wherein the controlling the leakage current of the capacitor comprises using a switch positioned in series with the capacitor,

wherein the switch is responsive to the comparing.

[c15] The method as in claims 13 or 14, wherein the controlling the leakage current of the capacitor comprises:

using a leakage current control circuit responsive to a programmable current source, wherein the programmable current source comprises a first current source and a first switch arranged to control the leakage current control circuit; and

selectively adjusting the programmable current source using a combinational logic circuit operatively connected to the programmable current source.

[c16] The method as in claims 13, 14, or 15, wherein the controlling the leakage current of the capacitor comprises:

generating a binary control word using a test processor unit; and
selectively adjusting an adjustment circuit responsive to the binary control word.

[c17] The method of claim 15, further comprising:

using the first current source and the first switch to control current flow between a first voltage potential and an output of the programmable current source dependent on a first control signal, wherein the output is operatively connected to the leakage current control circuit.

[c18] The method of claim 15, wherein the selectively adjusting comprises:

using the combinational logic circuit to adjust the programmable current source to one of a fixed number of possible settings, and wherein the selectively adjusting is responsive to the comparing.

[c19] The method of claim 16, wherein the selectively adjusting the adjustment circuit comprises:

controlling a first current flow between a first voltage potential and an

output of the adjustment circuit; and
controlling a second current flow between a second voltage potential
and the output of the adjustment circuit.

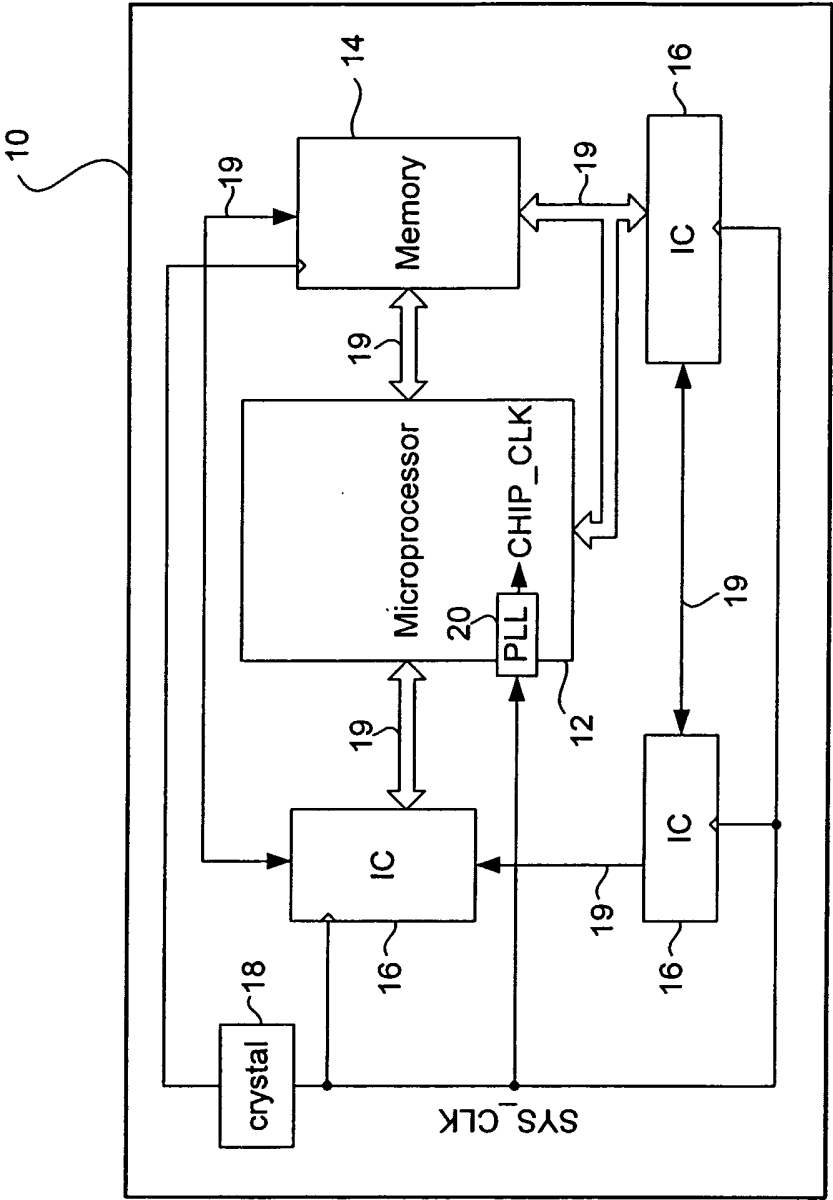


FIGURE 1
(Prior Art)

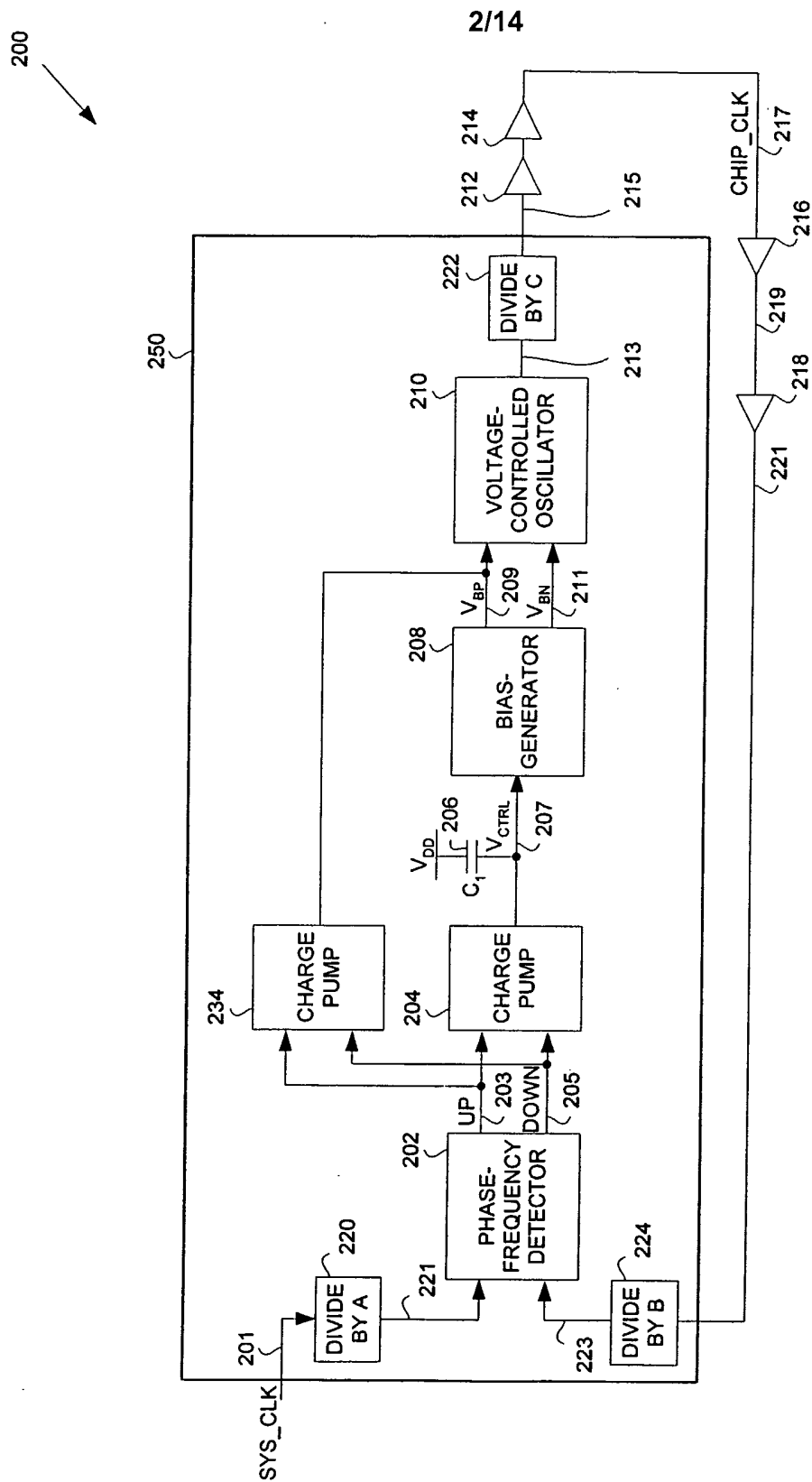


FIGURE 2
(Prior Art)

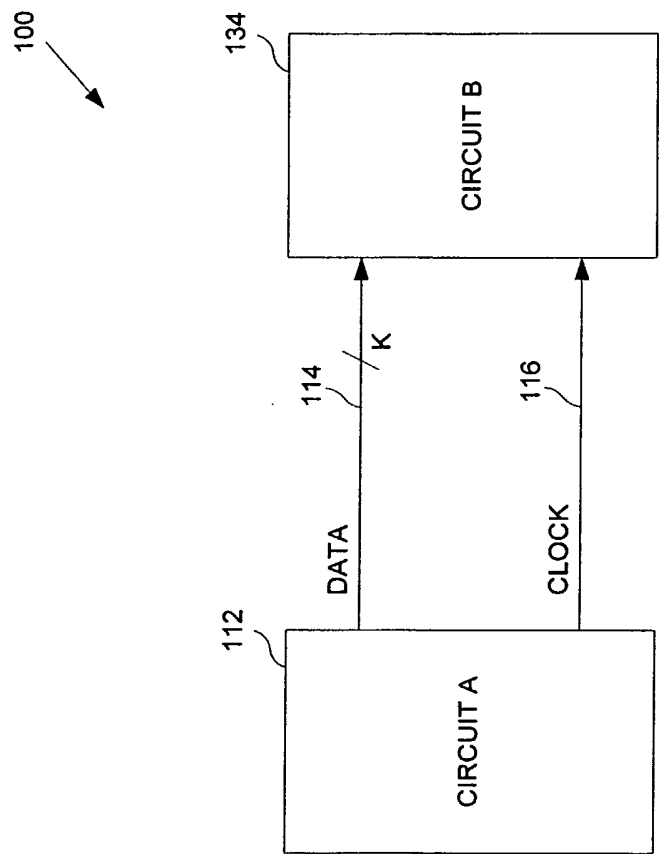


FIGURE 3
(Prior Art)

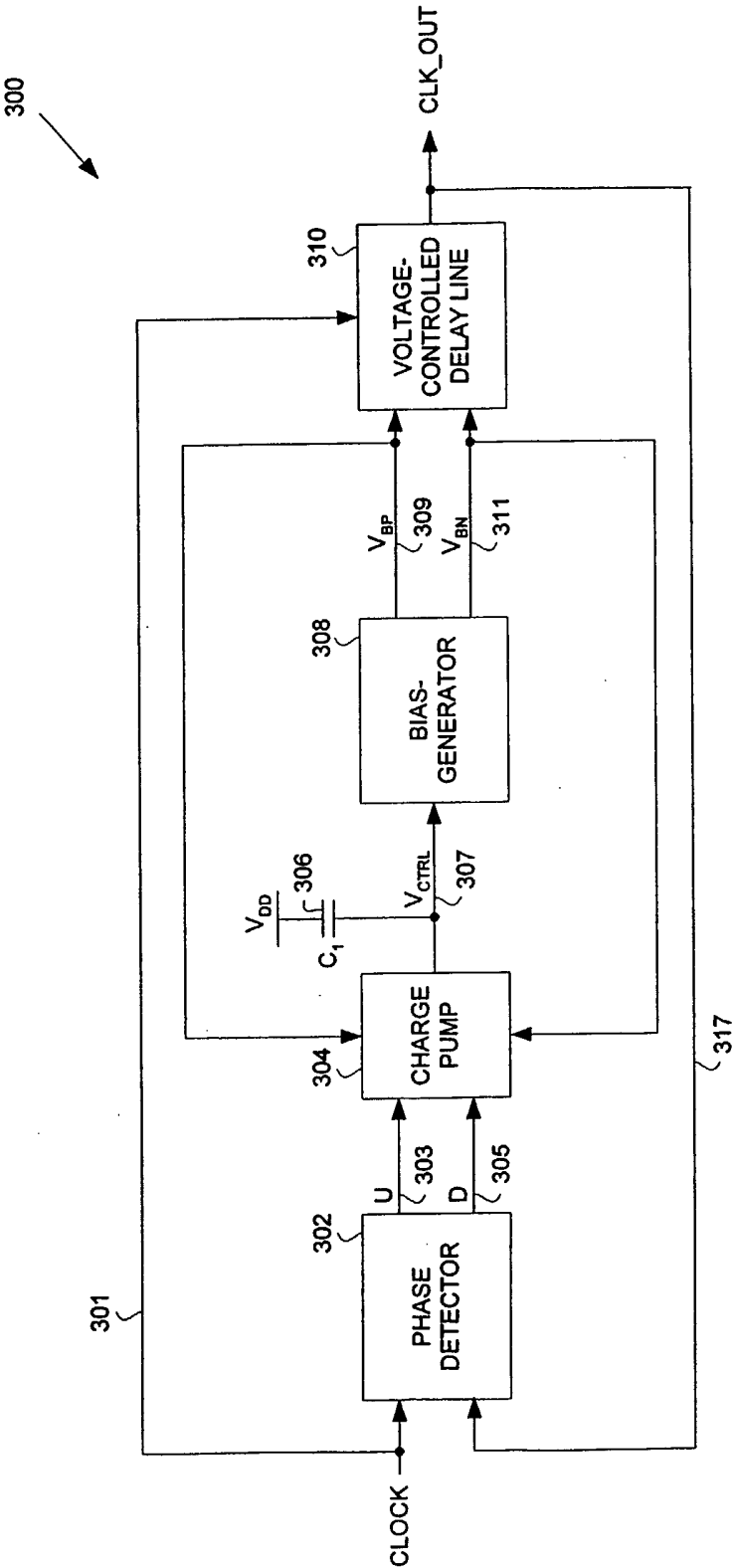


FIGURE 4
(Prior Art)

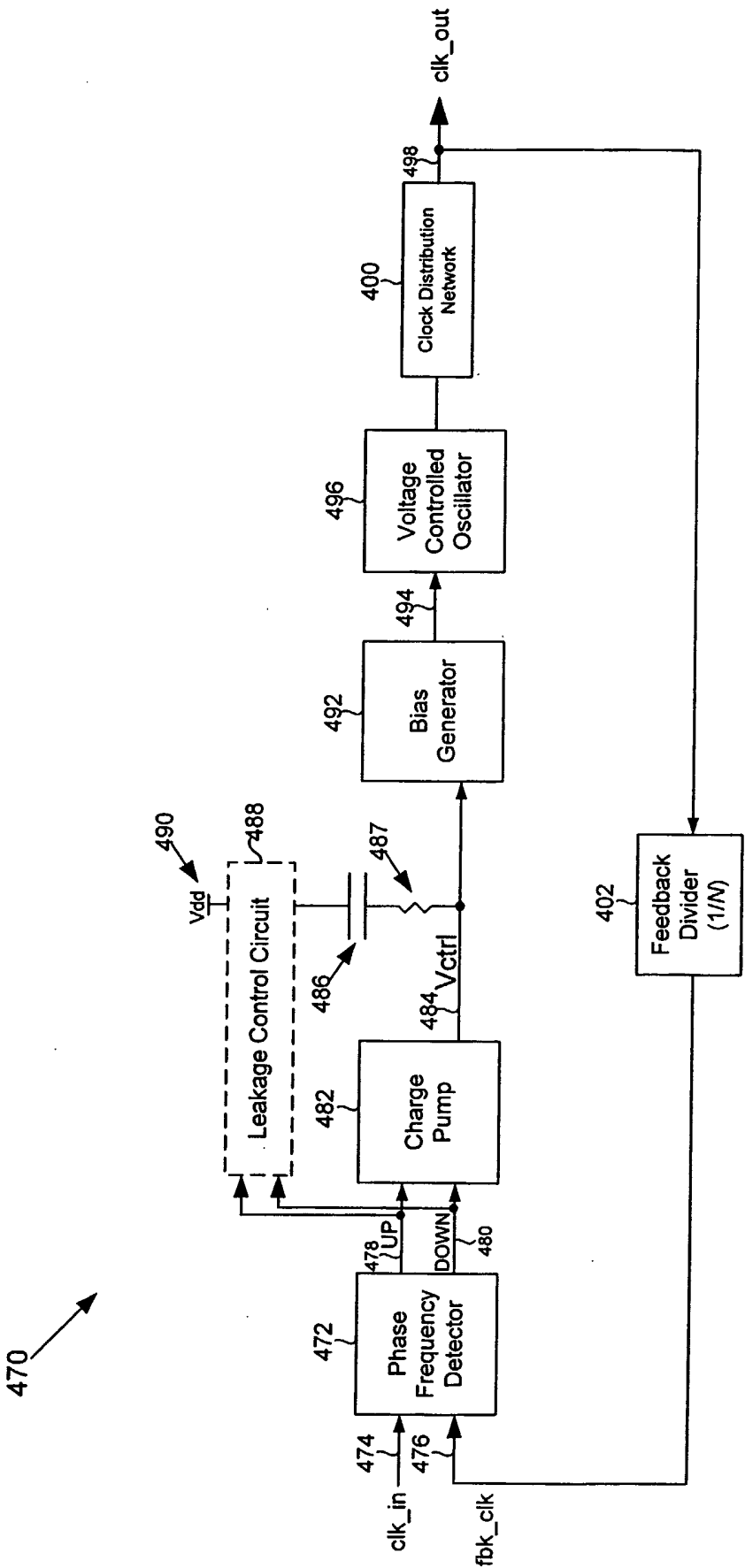


FIGURE 5

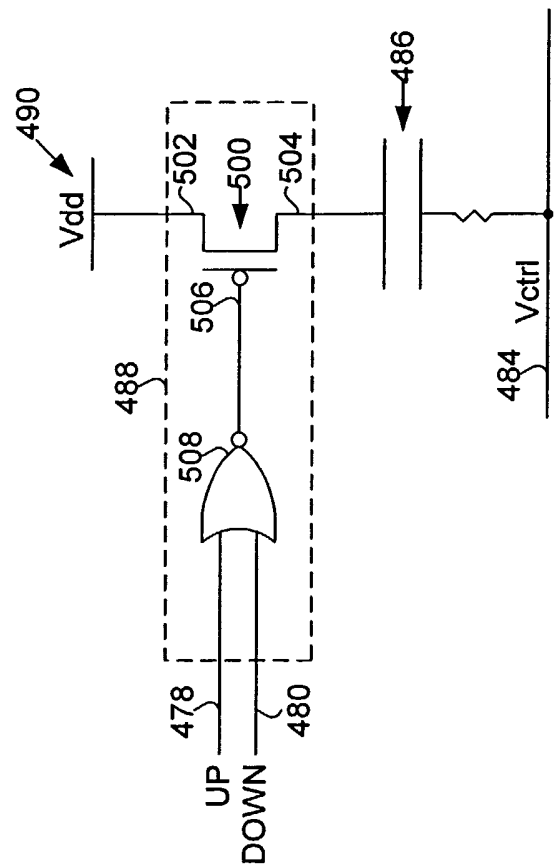


FIGURE 6

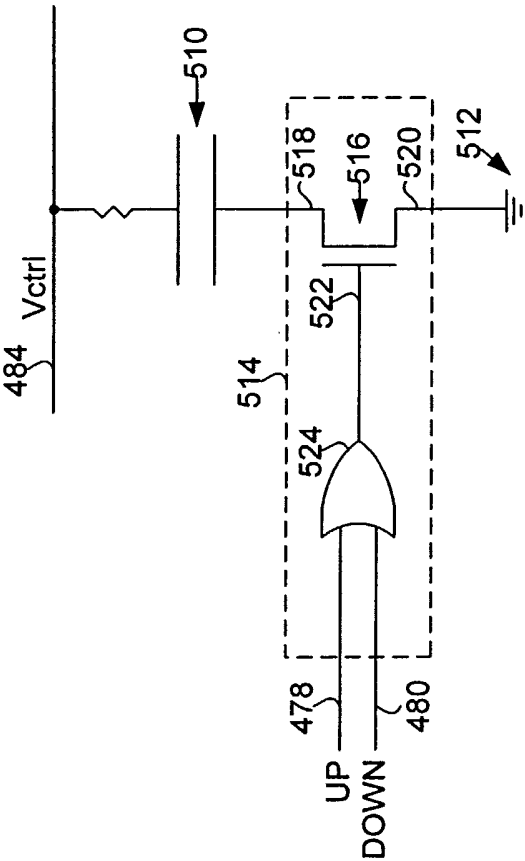


FIGURE 7

600

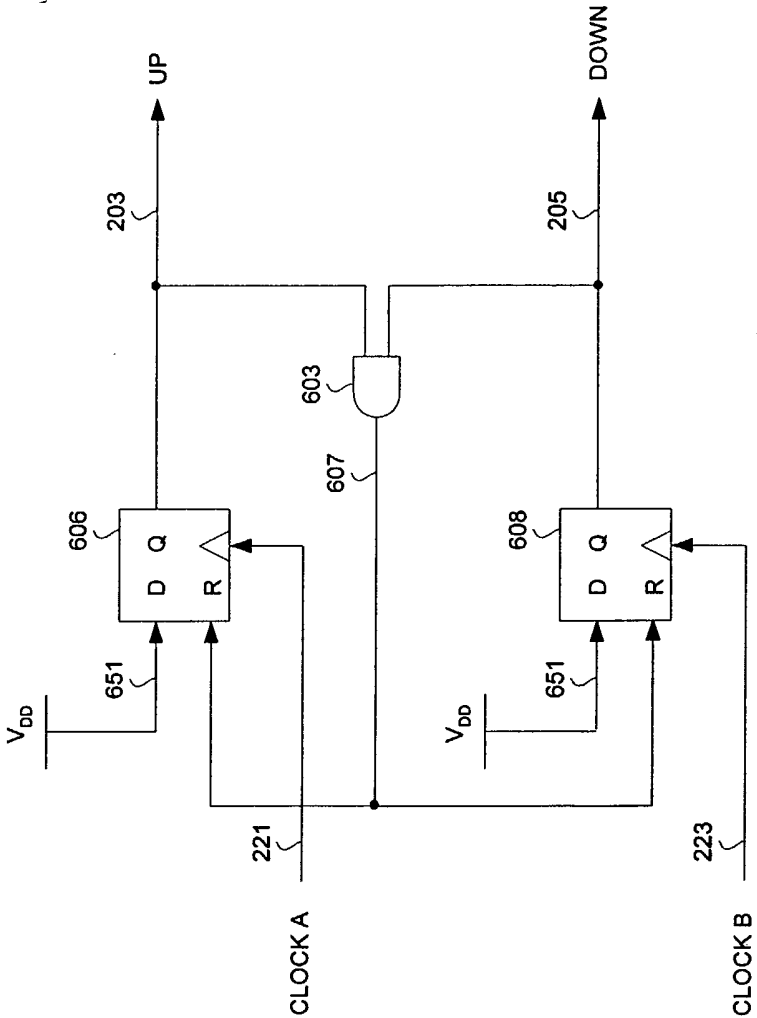


FIGURE 8

700

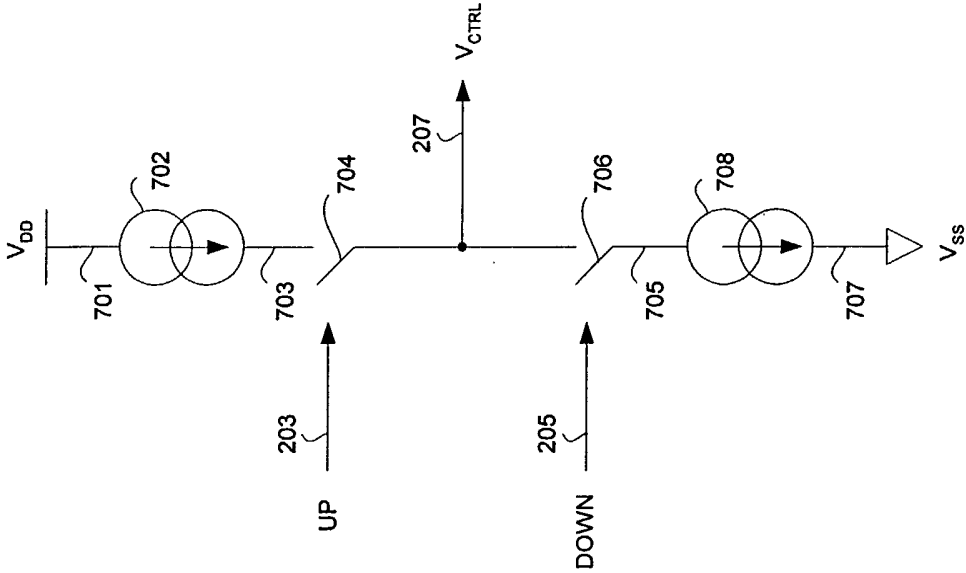


FIGURE 9

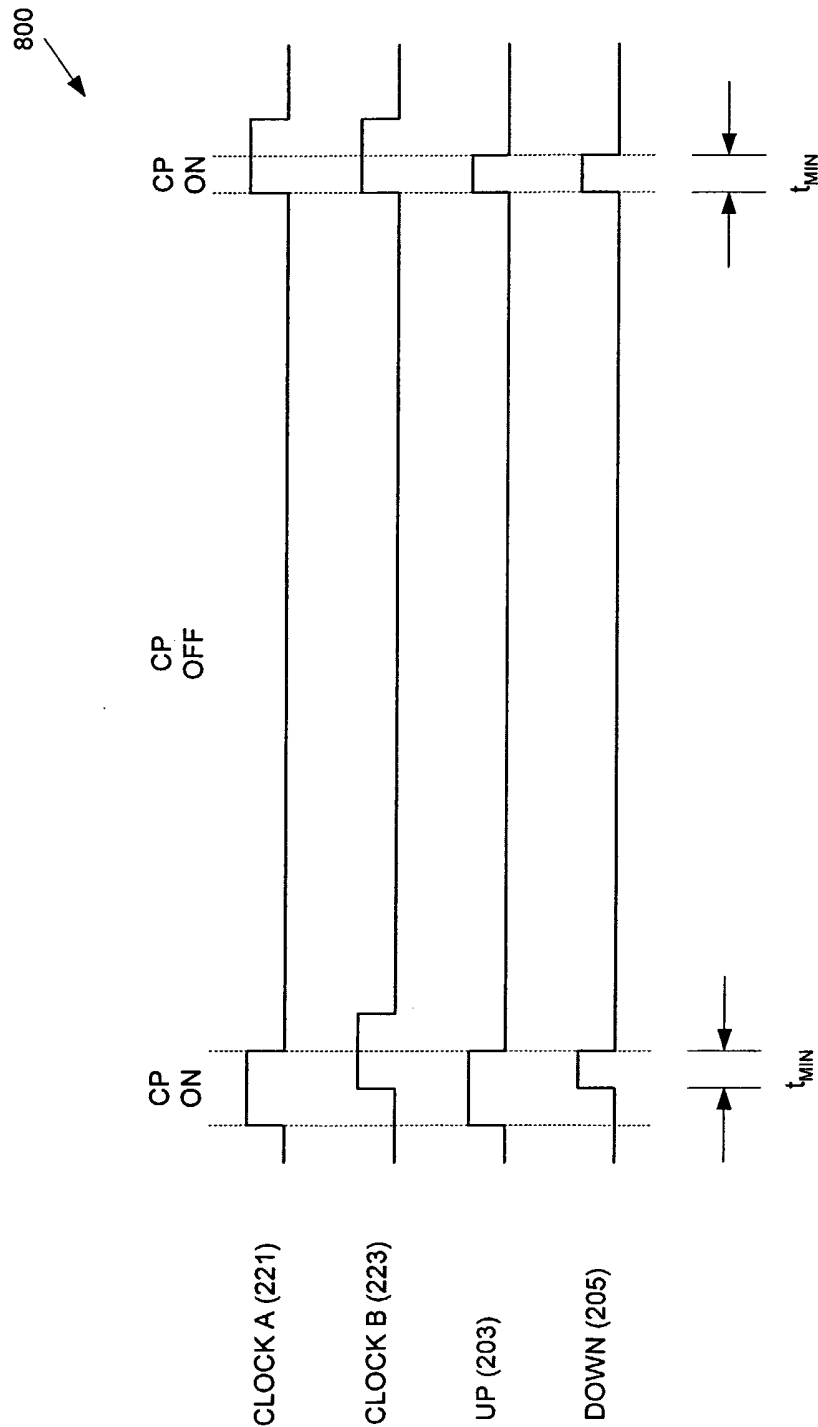


FIGURE 10

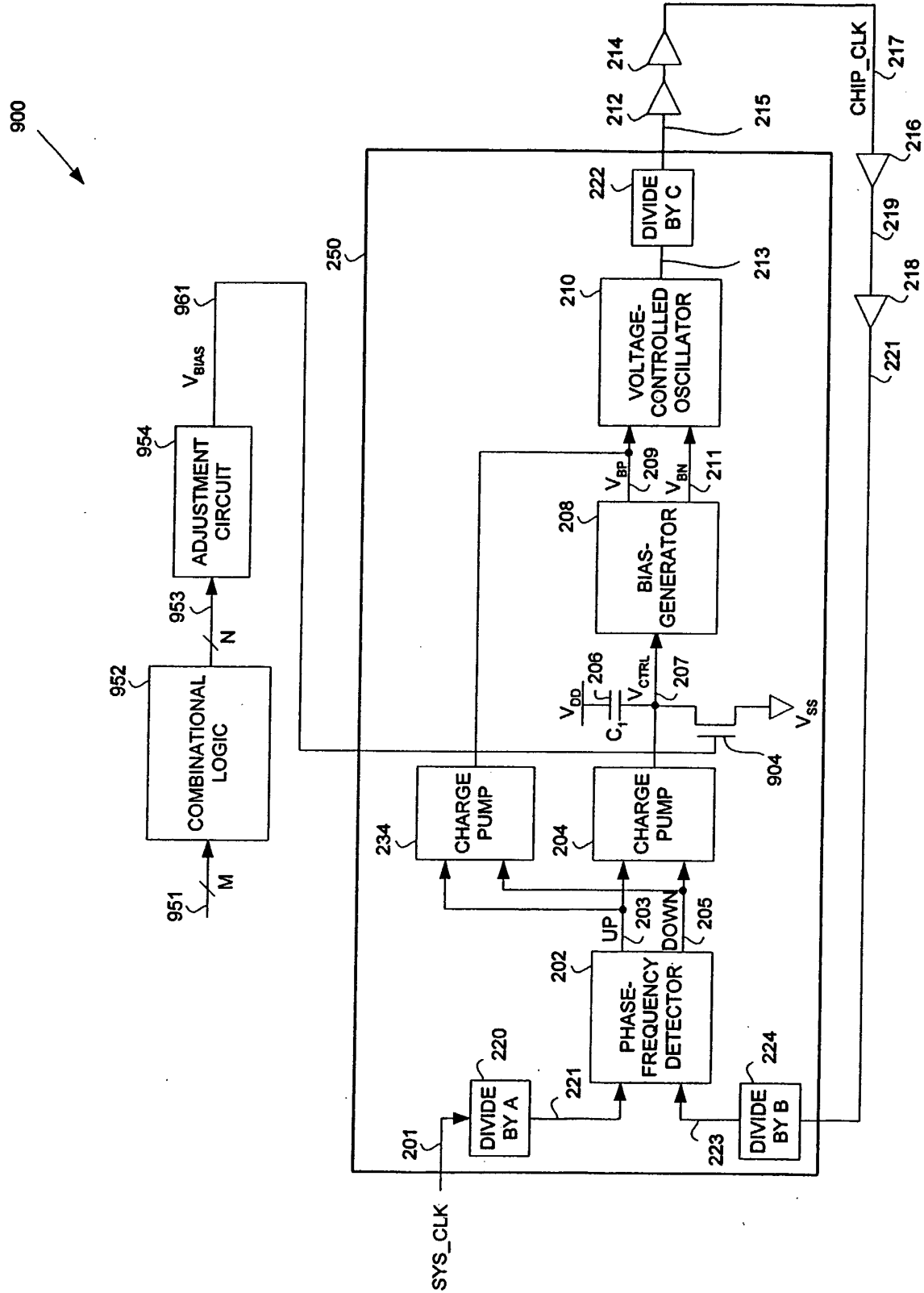


FIGURE 11

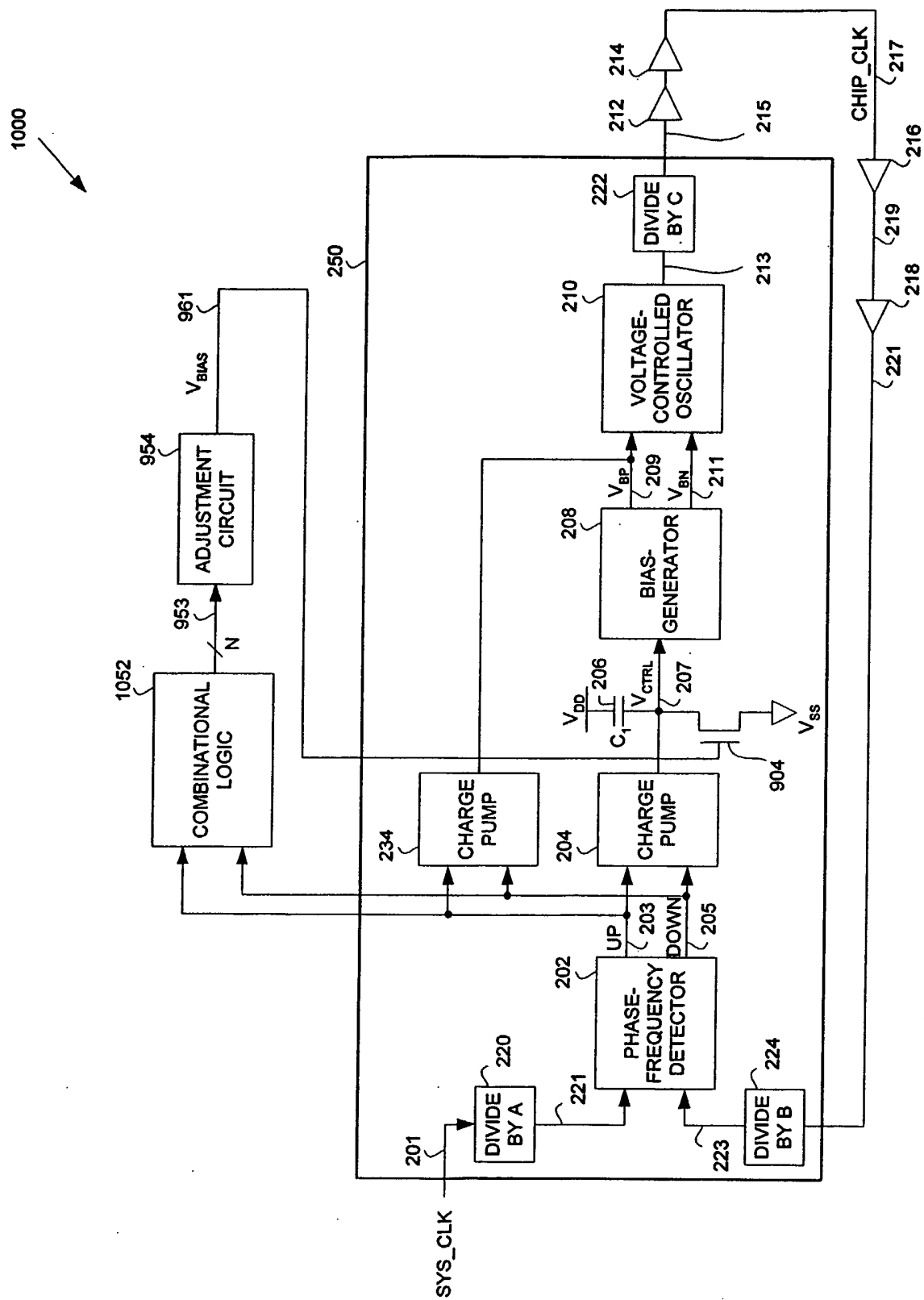


FIGURE 12

1100

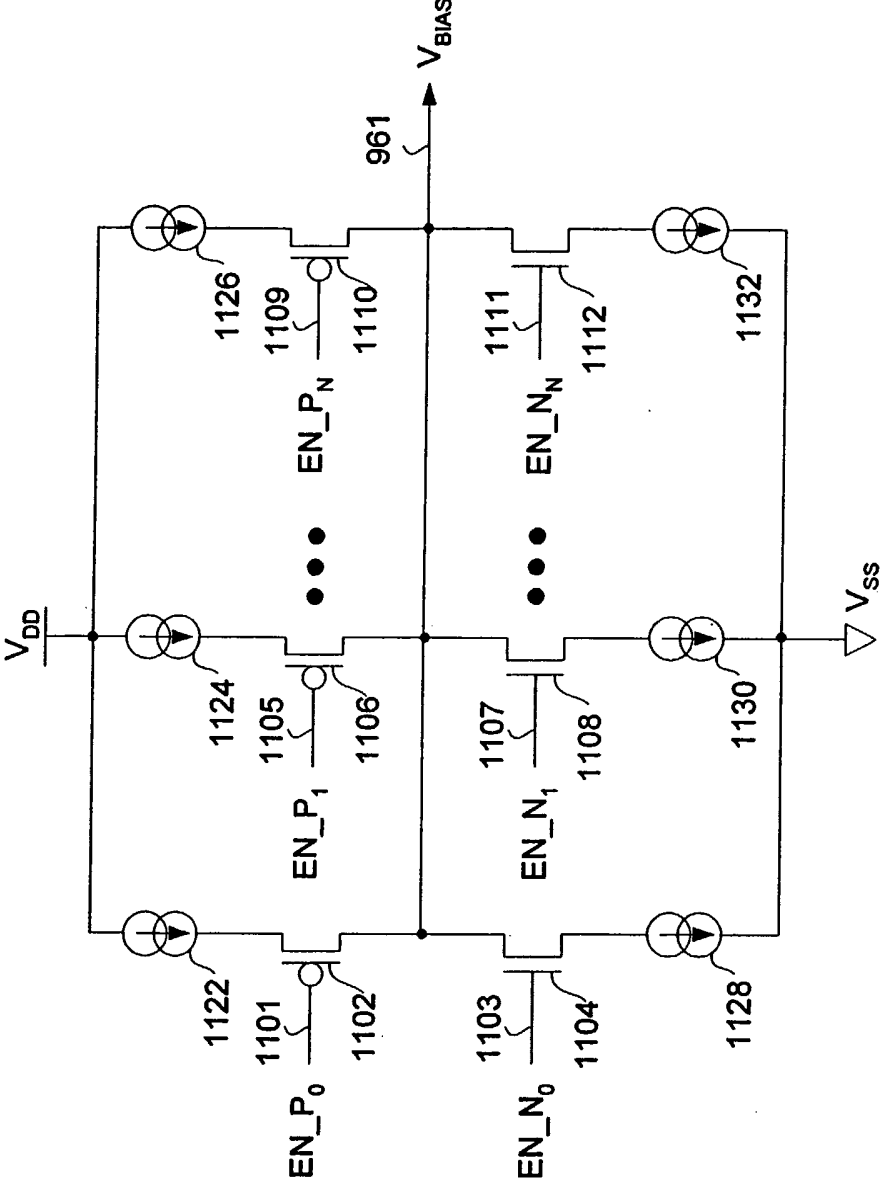


FIGURE 13

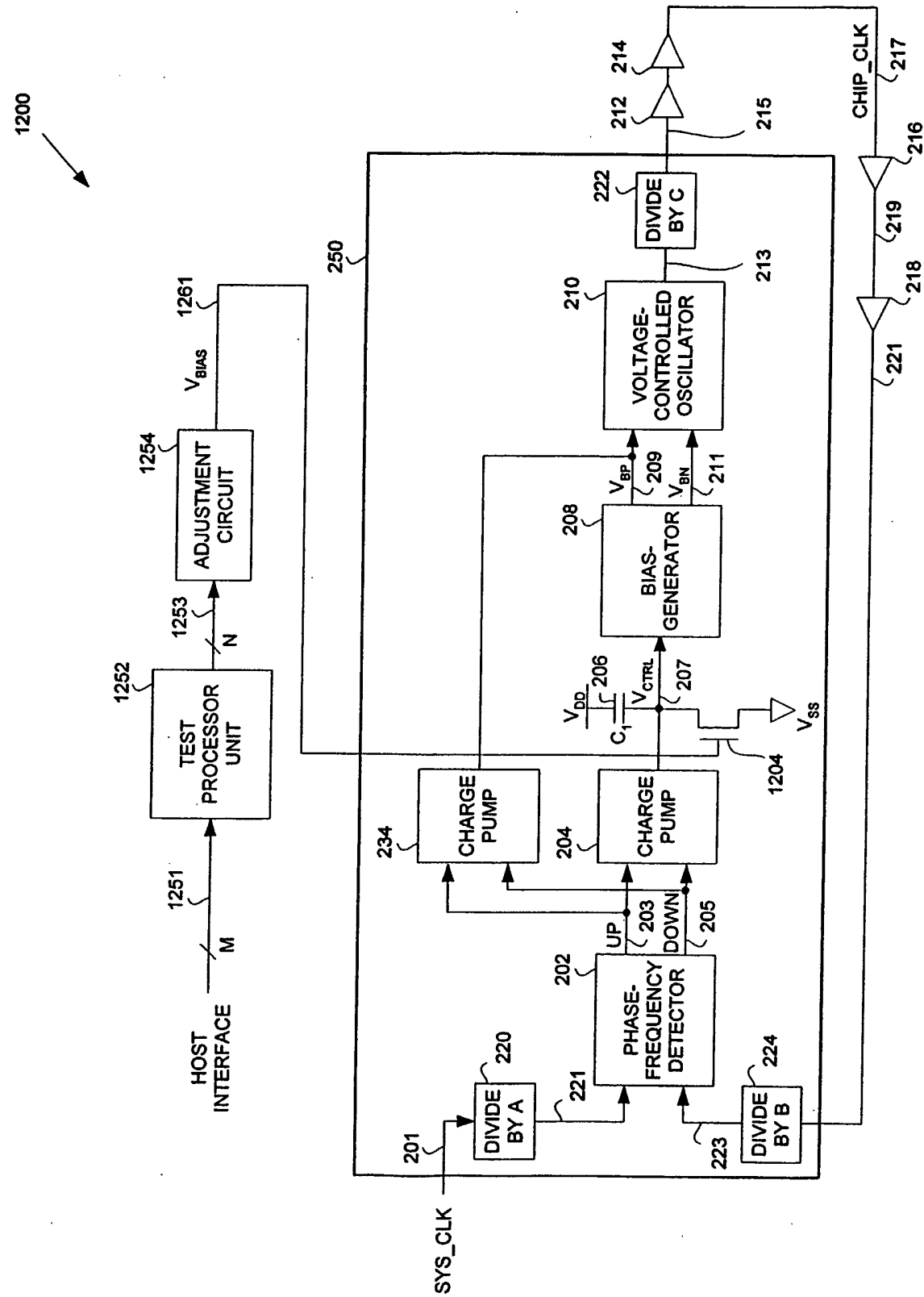


FIGURE 14

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 03/13108

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/089 H03L7/093

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 037 366 A (NIPPON ELECTRIC CO) 20 September 2000 (2000-09-20) paragraph '0002! - paragraph '0005!; figure 6 paragraph '0011! - paragraph '0023!; figure 1 ---	1,13
A	US 4 745 371 A (HAINE JOHN L) 17 May 1988 (1988-05-17) column 5, line 14 -column 5, line 30; figures 2,3E ---	1,13
A	US 6 011 822 A (DREYER STEPHEN F) 4 January 2000 (2000-01-04) column 1, line 24 -column 15, line 6; figures 1-5,9,16 --- -/--	1,13

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

11 July 2003

Date of mailing of the international search report

21/07/2003

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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