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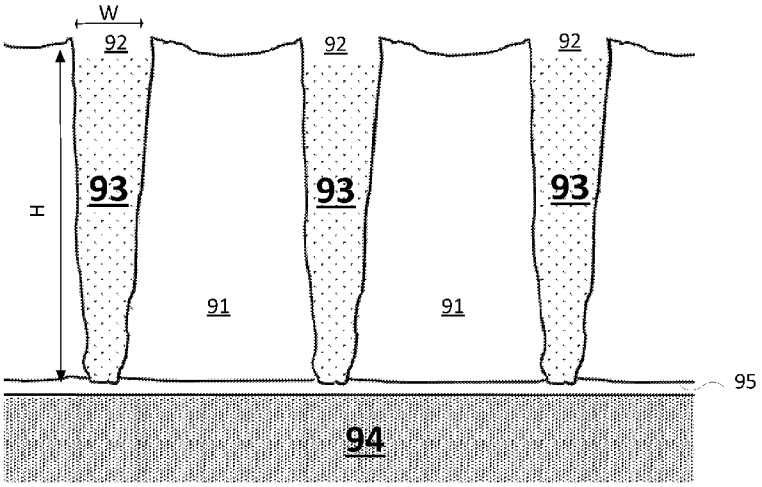


FIG. 9

(57) Abstract: Described herein are boron carbide (BC) based devices that include a structure comprising a plurality of openings or gaps, and a dielectric material disposed within the openings. The dielectric material comprises carborane-based units cross-linked to form a BC-based film. Methods of fabricating such devices are disclosed as well. Fabrication is based on synthesizing new air-stable precursors to BC using o-, m-, and p-carboranes functionalized at two carbon positions, followed by reaction with various electrophiles to create oligomers and polymers comprising carborane units linked by different functional groups. Such precursors deposited into the openings of a structure are then thermally, chemically, and/or photochemically cross-linked to form solid BC-based films.

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GAPFILL OF ETCH RESISTANT BORON CARBIDE

Technical Field

[0001] This disclosure relates generally to the field of integrated circuits and semiconductor manufacturing, and more specifically, to structures with fillable boron carbide and related dielectric materials and methods for manufacturing such structures.

Background

[0002] For the past several decades, the scaling of features in integrated circuits (ICs) has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor IC chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity.

[0003] IC chips are used in a variety of devices including automobiles, computers, appliances, mobile phones and consumer electronics. A plurality of IC chips can typically be formed on a single silicon wafer, i.e. a silicon disk having a diameter of, for example, 300 millimeters (mm), which is then diced apart to create individual chips. IC chips can include features sizes on the nanometer scale and can comprise hundreds of millions of components. Improved materials and manufacturing techniques have reduced features sizes to, for example, less than 45 nanometers (nm).

[0004] The drive for the ever-increasing capacity, however, is not without issue. The desire to make smaller IC chips continuously places demands on the methods and materials used to manufacture these devices. For example, in order to enable new patterning schemes, films with unique etch, gapfill and dielectric properties are needed.

[0005] In general, “etch properties” refer to conditions and characteristics related to etching of a material such as e.g. etch rate, etch resolution, etch resistance, compounds to be used for etching, etc. On the other hand, “gapfill properties” refer to conditions and characteristics related to ability of filling gaps with a material, e.g. methods that have to be

used to deposit a material into high aspect ratio structures, ability to deposit a material without forming voids or other defects, uniformity of a material filled within a gap, etc. Further, "dielectric properties" refer to conditions and characteristics such as dielectric values, thermal stability, and electrical leakage of a material, related to using the material as a dielectric material in IC chips, e.g. as an interlayer dielectric (ILD). As is well-known, an interlayer dielectric (ILD) or inter metal dielectric (IMD) film is the insulating material used between metal conductors and devices (such as transistors) in IC chips.

[0006] In particular, there is a need for films that have favorable dielectric properties, can be deposited into gaps or openings, and have etch properties different from those of silicon nitride (SiN), silicon dioxide (SiO_2), silicon carbide (SiC) and other silicon-based materials.

Brief Description of the Drawings

[0007] FIG. 1 provides a schematic flow chart illustrating formation of boron carbide and related dielectric films using carborane-based precursor formulation, according to some embodiments of the present disclosure.

[0008] FIG. 2 illustrates o-, m-, and p-carborane molecules, according to some embodiments of the present disclosure.

[0009] FIG. 3 illustrates polymers where carboranes are either in side chains or main chains, according to some embodiments of the present disclosure.

[0010] FIG. 4 illustrates a method of making oligomers/polymers by initial lithiation of the two acidic CH protons followed by reaction with various electrophiles, according to some embodiments of the present disclosure.

[0011] FIG. 5 illustrates direct synthesis of oligomers/polymers by lithiation of the two acidic CH protons followed by reaction with di- or multifunctional carbosilane electrophiles, according to some embodiments of the present disclosure.

[0012] FIG. 6 illustrates other polymeric materials that can be made through reaction of dilithium carboranes and difunctional electrophiles based on P, Si and B, according to some embodiments of the present disclosure.

[0013] FIG. 7 illustrates formation of mixed carborane-transition metal polymers through reaction of dilithium carboranes with metal chlorides, according to some embodiments of the present disclosure.

[0014] FIG. 8 illustrates a method of making alternating carborane-arene polymers using metal-catalysed coupling chemistry, according to some embodiments of the present disclosure.

[0015] FIG. 9 illustrates an exemplary structure comprising openings filled with boron carbide or other related dielectric materials, according to some embodiments of the present disclosure.

[0016] FIG. 10 provides a schematic illustration of an interposer, according to some embodiments of the present disclosure.

[0017] FIG. 11 provides a schematic illustration of a computing device built in accordance with some embodiments of the present disclosure.

Detailed Description

[0018] Described herein are boron carbide (BC) based devices that include a structure comprising a plurality of openings or gaps, and a dielectric material disposed within the openings. The dielectric material comprises carborane-based units cross-linked to form a BC-based film. Methods of fabricating such devices are disclosed as well. Fabrication is based on synthesizing new air-stable precursors to BC using o-, m-, and p-carboranes functionalized at two carbon positions, followed by reaction with various electrophiles to create oligomers and polymers comprising carborane units linked by different functional groups. Such precursors deposited into the openings of a structure are then thermally, chemically, and/or photochemically cross-linked to form solid BC-based films.

[0019] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present disclosure may be practiced with only some of the

described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present disclosure may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0020] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present disclosure, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0021] The terms "over," "under," "between," and "on" as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer "on" a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0022] Implementations of the disclosure may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation

upon which a semiconductor device may be built falls within the spirit and scope of the present disclosure.

[0023] In various embodiments, the interconnects as described herein may be used to connect various components associated with an integrated circuit. Components include, for example, transistors, diodes, power sources, resistors, capacitors, inductors, sensors, transceivers, receivers, antennas, etc. Components associated with an integrated circuit may include those that are mounted on an integrated circuit or those connected to an integrated circuit. The integrated circuit may be either analog or digital and may be used in a number of applications, such as microprocessors, optoelectronics, logic blocks, audio amplifiers, etc., depending on the components associated with the integrated circuit. The integrated circuit may be employed as part of a chipset for executing one or more related functions in a computer.

[0024] In the embodiments where at least some of the components associated with an integrated circuit are transistors, a plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the disclosure, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the disclosure may also be carried out using nonplanar transistors.

[0025] Each MOS transistor includes a gate stack formed of at least two layers, a gate interconnect support layer and a gate electrode layer. The gate interconnect support layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate interconnect support layer

include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate interconnect support layer to improve its quality when a high-k material is used.

[0026] The gate electrode layer is formed on the gate interconnect support layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0027] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[0028] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a "U"-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and

does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0029] In some implementations of the disclosure, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0030] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0031] One or more interlayer dielectrics may be deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0032] To provide context, conventionally, fabrication techniques used for integrating advanced interconnects require materials that can be deposited into gaps and that have unique compositions leading to different etch properties. Current solutions based largely on silicon (Si), carbon (C), and nitrogen (N) do not provide great enough contrast in etching properties with respect to one another.

[0033] Boron carbide (BC) is a material known to possess dielectric properties favorable for IC chip manufacturing. Furthermore, due to its unique elemental composition, BC expected to have unique etch properties relative to silicon-based materials such as SiN, SiO_2, SiC etc. Known methods for depositing BC are based on plasma-enhanced chemical vapor deposition (PECVD). However, PECVD requires use of damaging plasmas and does not allow gapfill, and there are no other methods for depositing this type of material into gaps or openings of relatively high aspect ratio structures.

[0034] Described herein are methods for providing BC-based materials into openings of a structure. The methods are based on synthesizing air-stable spin-on precursors of necessary size, solubility and glass transition temperature (Tg) to allow gapfill. These precursors are spun onto a wafer and, due to their low Tg, can fill or reflow into holes and gaps patterned on the wafer. After the fill is complete, the deposited precursors are subjected to some shock (thermal, chemical, UV, etc) that causes the precursors to crosslink into a solid thin film that fills the vertical features of the wafer. The material may be subsequently cured.

[0035] As used herein, the term "spin-on dielectric material" and variations thereof is used to describe dielectric materials formed using liquid precursors applied to a substrate using

any one of known coating techniques including, but not limited to e.g. spin-coating, dipcoating, dropcasting, solution immersion, or other similar coating techniques. Similarly, the term "spin-on precursor" and variations thereof is used to describe liquid precursors that could be applied to a substrate using any one of known coating techniques including, but not limited to e.g. spin-coating, dipcoating, dropcasting, solution immersion, or other similar coating techniques.

[0036] In various aspects, BC-based assemblies or devices are disclosed. The assemblies include a structure comprising a plurality of openings, and a BC-based dielectric material disposed within the plurality of openings. The plurality of openings may include openings, holes, or gaps (referred to herein as simply "openings") of various aspect ratios, where, as used herein, "aspect ratio" refers to a ratio between a height or a depth of an opening to a width of an opening. In various embodiments, openings described herein may have aspect ratios between 1 and 20, including all values and ranges therein, e.g. between 1 and 15, between 5 and 10, etc. Preferably, dimensions of the openings are on the nanometer scale, e.g. with a width of an opening being about 20 nm and a depth of an opening being about 100 nm, i.e. aspect ratio of 5. Therefore, such structures with openings are sometimes described as nanostructures or nanopatterned structures.

[0037] Nanostructures described herein could be a part of a semiconductor device or an IP package, e.g. a part of an interconnect, e.g. a backend interconnect, used for providing electrical conductivity in the semiconductor device or the IC package. As used herein, the term "backend interconnect" is used to describe a region of an IC chip containing wiring between transistors and other elements, while the term "frontend interconnect" is used to describe a region of an IC chip containing the rest of the wiring. Nanostructures described herein may be used in any devices or assemblies where one electrically conductive element of the wiring needs to be separated from another electrically conductive element, which could be done both in backend and frontend interconnects. Such devices or assemblies would typically provide an electronic component, such as e.g. a transistor, a die, a sensor, a processing device, or a memory device, and an interconnect for providing electrical connectivity to the component. The interconnect includes a plurality of conductive regions, e.g. trenches and vias filled with electrically conductive materials as known in the art. The

plurality of openings filled with dielectric materials as described herein could be used to electrically isolate at least some of the conductive regions from one another. For example, the structure in which the openings are made could be made of a conductive material.

[0038] The dielectric material provided within the openings includes carborane-based units, such as e.g. carborane-siloxane hybrids, carborane-boroxine hybrids, carborane-phosphine hybrids and metalopolymers, or carborane-arenes, cross-linked to form a BC-based film. The material can be, for example, a spin-on dielectric material, and may be used as an interlayer dielectric material and/or an etch-selective material. The material can be made from carborane-based precursors that can be applied to a nanopatterrned substrate, for example a silicon wafer, or any other structure with openings by techniques such as spin coating or other suitable deposition processes such as vapor phase deposition. In some embodiments, the resulting material can exhibit relatively low dielectric values (e.g., less than 2.2), may be hydrophobic, and can be resistant to chemical attack (such as chemicals used in typical IC fabrication processes).

[0039] Embodiments of the present disclosure describe difunctional carborane molecules that may be used to produce oligomers or polymers (precursors) that in turn can be disposed on a structure comprising a plurality of openings, to provide a BC-based dielectric film within the openings. A coating of the oligomeric/polymeric precursor material can be polymerized into a hard, cross-linked material. A flow chart illustrating some of the steps that can be used from carborane molecules to a BC-based dielectric material provided within openings of a structure, in accordance with some embodiments, is provided in FIG. 1. It should be noted that, while descriptions provided herein are particularly suitable for providing BC-based dielectrics within features of nanopatterned structures, these descriptions are equally applicable for forming BC-based dielectric films in bulk or blanket forms as well. Such approach would be advantageous over the PECVD approaches used in current state of the art because use of damaging plasmas may be avoided.

[0040] FIG. 1 provides a schematic flow chart 100 illustrating formation of boron carbide and related dielectric films using carborane-based precursor formulation, according to some embodiments of the present disclosure.

[0041] As shown with box 102 in FIG. 1, first, difunctional carborane molecules are synthesized from raw materials of o-, m-, or p-carborane molecules such as those illustrated in FIG. 4-7. In general, "difunctional molecule" is a molecule comprising two functional groups.

[0042] In an embodiment, difunctional carborane molecules may be synthesized by functionalizing the parent carborane molecules readily at two carbon positions, e.g. as those shown with black dots for each of the molecules in FIG. 2, via lithiation (also referred to as deprotonation) of the carborane molecules. In general, deprotonation refers to removal of a proton (H^+) from a molecule, forming a conjugate base.

[0043] Functionalizing the carborane molecules at two carbon positions ensures chemical reactivity that allows oligomers and polymers to be created (box 104 in FIG. 1), where individual carboranes are linked by different functional groups containing different elemental compositions. Such oligomerization/polymerization produces moderate to high molecular weight materials, e.g. materials having molecular weight in the range of 1000 to 10000 or even to 100000, which are suitable for spin-coating onto wafers as thin films and are sufficiently thermally stable to resist evaporation from the wafer during subsequent baking steps (described below).

[0044] In some embodiments, the oligomerization/polymerization of box 104 includes reacting the difunctional carborane molecules with one or more electrophiles to produce oligomers or/and polymers of the difunctional carborane molecules. In various embodiments, electrophiles may include one or more of dichlorosilanes, dichloroboranes, alkyl dichlorides, aryl dichlorides, dichlorostannanes, dichlorophosphines, metal halides or any other multifunctional molecules with two or more sites for reaction with nucleophiles of the difunctional carborane molecules. In general, electrophiles refer to reagents attracted to electrons. Electrophiles are typically positively charged or neutral species that have vacant orbitals that are attracted to an electron rich centre. On the other hand, nucleophiles refer to chemical species that donate an electron pair to an electrophile to form a chemical bond in relation to a reaction. Some examples of oligomers and polymers are illustrated in FIG. 5 as well as in FIGs. 6 and 7.

[0045] Next, oligomers/polymers of the difunctional carborane molecules that were created in box 104 are dissolved in one or more solvents, thus forming a chemical formulation that can be used as a liquid precursor for forming BC-based dielectric materials (box 106 in FIG. 1). In some embodiments, solvents such as toluene, cyclohexanone, 2-heptanone, or propyleneglycol monomethyl ether acetate may be used. In general, any common solvents used for spin-coating may be used.

[0046] Properties such as the average molecular weight of the oligomers/polymers can be pre-determined by controlling reaction conditions such as concentration of components (including starting carborane molecules and, optionally, catalyst), time of addition, solvent or co-solvents, and temperature. Molecular weights may be selected to improve the applicability of the precursor when spun onto a structure with a plurality of openings, e.g. on a substrate/wafer. Exemplary average molecular weights for precursors may be greater than or equal to 1000, greater than 1500, greater than 5000, greater than 7000 or greater than 9000. The oligomers may include, for instance, dimers, trimers, tetramers, pentamers, hexamers, heptamers, octomers, nonomers, or may contain greater than 10, greater than 20 or greater than 30 difunctional carborane molecules. In some embodiments, two, three, four or more different oligomers/polymers may be physically mixed together and then coated onto a nanopatterned structure. These oligomers/polymers may differ, for example, with regard to difunctional carborane molecule structure, average molecular weight, molecular weight distribution, atomic percent C, atomic percent B, atomic percent H, ratio of C:B:H, amount of branching, capping species, porogen content, etc.

[0047] In some embodiments, the organic solvent, any unreacted starting molecules, and low molecular weight oligomers/polymers can be removed in a rotary evaporator or a similar apparatus. Additionally or alternatively, higher molecular weight oligomers/polymers (e.g. with molecular weight above a certain threshold value) can be precipitated from solution or isolated by other methods.

[0048] Remaining high molecular weight oligomers/polymers can be re-dissolved into new solvents, e.g. 2-heptanone. At this point, a new solvent than the one used in the oligomer/polymer synthesis of box 104 may be used. However, use of new solvents other

than that used for reaction synthesis could have manufacturing, environmental health and safety (EHS), and fillability implications. Whether the rotary evaporator is used for solvent exchange or not, the precursor oligomers/polymers may then be diluted to target concentrations for spin coating. The dilution tunes the thickness of the film that results after spin coating. Depending upon the aspect ratio of the features needing to be filled, the dilution can be tuned for incomplete fill, nearly complete fill, or complete fill with various amounts of overburden (i.e. when not only all of the openings are filled, but also there is a layer of thin film over the structure).

[0049] Synthesis of box 102 and oligomerization and/or polymerization of box 104 produces new materials with carboranes connected by various cross-linkers. Some examples of resulting spin-on carboranes include carborane-siloxane hybrids, carborane-boroxine hybrids, carborane-phosphine hybrids, carborane-phosphine metalopolymers, and carborane-arenes.

[0050] In the embodiments involving carborane-siloxane hybrids, functionalizing the carborane molecules (box 102) may include installing reactive organosilane functionality on the carborane molecules to produce siloxanes. Subsequently oligomerizing and/or polymerizing the siloxanes (box 104), which could be performed according to any of well-known methods, all included within the scope of the present disclosure, leads to formation of carborane-siloxane hybrids which, when dissolved in a solvent (box 106), may be used as a precursor for BC-based materials.

[0051] In the embodiments involving carborane- boroxine hybrids, functionalizing the carborane molecules (box 102) may include functionalizing the carborane molecules in two carbon positions with boronic acid or boronate functionality. Subsequently oligomerizing and/or polymerizing these functionalized carboranes (box 104) leads to formation of carborane-boroxine hybrids which, when dissolved in a solvent (box 106), may also be used as a precursor for BC-based materials.

[0052] In the embodiments involving carborane-phosphine hybrids and metalopolymers, dilithiocarboranes (i.e. carborane molecules functionalized at two carbon sites) may be reacted with phosphorus trichloride (PCl_3) or alkyldichloro- and aminodichlorophosphines

($RPCl_2$) to form air-stable polymers. When reacted with $RPCl_2$, the resulting phosphine can be polymerized through coordination to various metal salts, such as e.g. nickel (II) chloride ($NiCl_2$), cobalt (II) chloride ($CoCl_2$), or copper (I) chloride (CuCl), allowing incorporation of metal uniformly through the film.

[0053] In the embodiments involving carborane-arenes, metal-catalysed coupling may be used to create carborane-arene bonds as illustrated in FIG. 8.

[0054] Based on the explanations provided herein, a person of ordinary skill in the art will recognize many other options that exist for linking carboranes together, allowing fine tuning of molecular weight and elemental composition of the resulting film, thereby, ultimately fine-tuning the etch, gapfill and dielectric properties of the film. Therefore, other options for linking carboranes together are within the scope of the present disclosure. Flexible fine tuning of etch properties in particular is essential to being able to integrate film with two or more other materials where it is impossible to predict a priori a specific composition that will work.

[0055] Turning back to FIG. 1, liquid precursor formulation of box 106 may then be coated onto the patterned wafer or any structure with openings that need to be filled with BC-based material (box 108). Precursor coating can happen by dispensing and spin coating of the precursor formulation described above using industry standard spin tracks. For example, in some embodiments, spin coating the precursor onto the structure with the openings may include spin coating for 1-60 seconds, including all values and ranges therein, at 500-6000 rotations per minute (rpm), including all values and ranges therein.

[0056] In other embodiments, precursor may be provided on the structure with opening by means other than spin coating, such as e.g. dipcoating, dropcasting, solution immersion, and flowable chemical vapor deposition (CVD) methods.

[0057] After spin coating, depending on the topography of the nanostructure, it is possible that the precursor materials do not properly and/or completely fill the openings provided in a structure. Dense fill of precursor oligomers/polymers can be accomplished by heating up the precursors above their glass transition temperature Tg, a process referred to herein as a

"reflow bake" to indicate that the structure with the openings onto which the precursor was coated is baked to allow complete and uniform reflow of the precursor into the openings. Reflow bake may help filling the openings without leaving any voids or at least reducing occurrence of such voids. A person of ordinary skill in the art would readily recognize that different molecular weight species can provide different Tg values and, therefore, different temperatures need to be applied for controlling the reflow bake process. For example, in some embodiments, a reflow bake process for the carborane-siloxane hybrid precursors may include heating the precursor to 125 degrees Celsius for 5 minutes, preferably under nitrogen gas.

[0058] After the oligomers/polymers have been adequately filled into the topographical features on the wafer, these precursors may be cross-linked into a solid BC-based material using any one of several methods (box 110 in FIG. 1). Cross-linking typically involves thermally and/or photochemically and/or via e-beam exposure transforming thin films produced by coating of box 108 into boron carbide films of various stoichiometries where carborane cages are broken up and transformed into final film.

[0059] In various embodiments, cross-linking agents may be selected based on the specific precursor oligomers/polymers that are being linked. In general, "cross-linking agent" (or simply "cross-linker") refers to a molecule introduced in some proportion to the primary boron carbide oligomer or polymer and designed to have reactivity with the oligomer or polymer being used. Cross-linkers allow further tuning the composition of the final BC-based films. For example, hybrid boron-carbide-siloxanes can be made using carbosiloxane cross-linkers.

[0060] The cross-linking can be facilitated, for example, by heat, radiation, a chemical catalyst, or any other excitation means that activate cross-linking, or a combination of various means. Furthermore, cross-linking may be preceded by baking the structure with coated precursor at 303 to 673 degrees Celsius for 30 seconds to 30 minutes (a process sometimes referred to as "soft-baking"), in order to get rid of solvents and low molecular weight components. Partial or full cross-linking may occur during this process.

[0061] In case of heat-assisted cross-linking, in some embodiments, the structure may be baked at higher temperatures, e.g. at 573 to 773 degrees Celsius (a process sometimes referred to as "hard-baking"). Hard-baking may be carried out under nitrogen or under a reactive gas such as e.g. ammonia, hydrogen, oxygen, diborane, or disilane.

[0062] Cross-linking in this context is a process of converting reactive functionality on the oligomer or polymer into new bonds that connect two oligomers or polymers leading to higher molecular weight polymers on the way to fully formed solid dielectric material network. The cross-linkable groups may be present entirely on the oligomer or polymer or may need to be introduced exogenously. Different schemes may be required depending on e.g. the specific functionality present on the oligomer and/or the cross-linking agent being used, if any. For example, Si-H functionality on oligomer or polymer can be initiated to react with C-O-Si bonds, water, C=C and other functionality either thermally, via agency of a catalyst or photochemically. B-H bonds present in the carborane cage can be similarly reacted at high temperature or through catalytic or photochemical activation process.

[0063] The crosslinking described here brings mechanical stability such as stiffness (high Young's modulus), reduced swelling in organic solvent, and reduced material shrinkage after exposure to UV photons, free electrons, or electron beams.

[0064] In case of radiation-assisted cross-linking, UV activation may be used, with UV radiation comprising a broad range of wavelengths. With some activators such as B-H, B-C and B-B bonds, any wavelength below 300 nm can be effective. Intensity of UV radiation should be selected to be adequate to fully cross-link the oligomers/polymers. In some embodiments an intensity of from 0.01 to 1.0 W/cm^2 has been found effective. Exposure time can be adjusted for specific carborane systems as well as specific wavelengths and radiation intensity. To achieve complete crosslinking, times from 5 seconds to 20 minutes have been used in many embodiments.

[0065] Once the solid BC-based material is set into a cross-linked network, the wafer could, optionally, be subjected to higher temperature outgassing bakes at 400-450 degrees Celsius, including all values and ranges therein, for 1-30 minutes, including all values and ranges therein, in order to remove any thermally labile species. Preferably, the outgassing bake is

carried out under nitrogen gas. As used herein, the term "outgassing" is used to describe release of zero or more gases that may have been dissolved, trapped, absorbed, or otherwise included within the cross-linked carbosilane material.

[0066] The material may also be subsequently cured (box 112 of FIG. 1), e.g. by using heat, UV photons or/and electron beams, in order to mechanically harden and/or change or fine-tune the etch properties of the BC-based material. In some embodiments, curing may involve heating the solid BC-based material between 200-450 degrees Celsius, including all values and ranges therein, while simultaneously exposing to optical radiation of 170-254 nm wavelengths (i.e., deep ultraviolet light), including all values and ranges therein. In other embodiments, curing may involve heating the solid BC-based material between 200-450 degrees Celsius, including all values and ranges therein, and exposing the solid BC-based material to electrons.

Exemplary Structure

[0067] FIG. 9 provides a schematic illustration of a cross-section of a structure 91 comprising a plurality of openings 92 filled with BC-based dielectric material 93, according to some embodiments of the present disclosure. As can be seen, FIG. 9 is drawn to reflect example real world process limitations, in that the features are not drawn with precise right angles and straight lines. The structure 91 can be disposed on a substrate 94, and an etch-stop layer 95 may be provided to ensure that when the openings 92 are made by etching the structure 91, etching does not extend into the substrate 94. Height H and width W of the openings 92 are also indicated in FIG. 9.

[0068] In a particular example shown in FIG. 9, the dielectric material 93 is shown to fill the features 92 to a large extend, but not completely – the upper parts of the openings 92 are not filled with the material 93. However, in other embodiments, the dielectric material may fill the features completely and may even form a thin film covering the entire structure 92.

[0069] In various embodiments, each one of the structure 91 and the substrate 94 may be comprised of one or more of silicon, silicon dioxide, germanium, indium, antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide and gallium antimonide. In

some embodiments, the structure 91 may be an interlayer dielectric (ILD). Two or more layers of the interlayer dielectric may be stacked to form an integrated circuit. In some embodiments, the ILD may include one or more sacrificial layers deposited over a dielectric substrate. The ILD may include one or more dielectric materials, which are understood to be materials that are insulators but are polarized upon application of an electric field. In some embodiments, the ILD may include a low-k dielectric material, that is, a material with a dielectric constant that is lower than 3.9, i.e., the dielectric constant of silicon dioxide, including all values and ranges from 1.5 to 3.8, such as 1.7, 1.9, 2.1, 2.8, 2.7, etc. Non-limiting examples from which the dielectric materials of the structure 91 may be selected include fluorine-doped silicon dioxide, carbon doped oxide (i.e., carbon-doped silicon dioxide), organo silicate glass, silicon oxycarbide, hydrogenated silicon oxycarbide, porous silicon dioxide, and organic polymer dielectrics such as polyimide, polytetrafluoroethylene, polynorbornenes, benzocyclobutene, hydrogen silsequioxane and methylsilsesquioxane. The structure 91 layer may have a thickness in the range of 50 nm to 300 nm, including all values and ranges therein, such as 100 nm to 300 nm, 100 nm to 200 nm, etc.

Implementation in an interposer

[0070] In accordance with embodiments of the disclosure, structures comprising openings filled with BC-based dielectric materials disclosed herein may be used in the fabrication of an interposer, such as e.g. the one shown in FIG. 10. In particular, the structures described herein may be used in the fabrication of various interconnects of the interposer shown in FIG. 10. For example, the structures described herein may be used in forming dielectric regions within the interposer 1000, e.g. regions between at least some of the trenches 1008 and vias 1010, which could be done instead of or in addition to a conventional dual damascene process. Use of the approaches and materials described herein may then be identified by the analysis of the localized dielectric material properties as described herein, such as e.g., density, porosity, propensity for film shrinkage, mechanical properties, and/or chemical composition.

[0071] FIG. 10 illustrates an interposer 1000 that includes one or more embodiments of the disclosure. The interposer 1000 is an intervening substrate used to bridge a first substrate

1002 to a second substrate 1004. The first substrate 1002 may be, for instance, an integrated circuit die. The second substrate 1004 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 1000 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 1000 may couple an integrated circuit die to a ball grid array (BGA) 1006 that can subsequently be coupled to the second substrate 1004. In some embodiments, the first and second substrates 1002/1004 may be attached to opposing sides of the interposer 1000. In other embodiments, the first and second substrates 1002/1004 may be attached to the same side of the interposer 1000. In further embodiments, three or more substrates may be interconnected by way of the interposer 1000.

[0072] The interposer 1000 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0073] The interposer may include metal interconnect trenches 1008 and vias 1010, including but not limited to through-silicon vias (TSVs) 1012. The vias 1010 may be enclosed by first and second diffusion barrier layers as described herein. The interposer 1000 may further include embedded devices 1014, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 1000.

Implementation in a computing device

[0074] In accordance with embodiments of the disclosure, structures comprising openings filled with BC-based dielectric materials disclosed herein may be used in the fabrication of a computing device, such as e.g. the one shown in FIG. 11. In particular, the structures

described herein may be used in the fabrication of various interconnects of the computing device shown in FIG. 11.

[0075] Figure 11 illustrates a computing device 1100 in accordance with one embodiment of the disclosure. The computing device 1100 may include a number of components. In one embodiment, these components may be attached to one or more motherboards. In an alternate embodiment, some or all of these components may be fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 1100 include, but are not limited to, an integrated circuit die 1102 and at least one communications logic unit 1108. In some implementations the communications logic unit 1108 may be fabricated within the integrated circuit die 1102 while in other implementations the communications logic unit 1108 may be fabricated in a separate integrated circuit chip that may be bonded to a substrate or motherboard that may be shared with or electronically coupled to the integrated circuit die 1102. The integrated circuit die 1102 may include a CPU 1104 as well as on-die memory 1106, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0076] Computing device 1100 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 1110 (e.g., DRAM), non-volatile memory 1112 (e.g., ROM or flash memory), a graphics processing unit 1114 (GPU), a digital signal processor 1116, a crypto processor 1142 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 1120, an antenna 1122, a display or a touchscreen display 1124, a touchscreen controller 1126, a battery 1128 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 1128, a compass 1130, a motion coprocessor or sensors 1132 (that may include an accelerometer, a gyroscope, and a compass), a speaker 1134, a camera 1136, user input devices 1138 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 1140 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0077] The communications logic unit 1108 enables wireless communications for the transfer of data to and from the computing device 1100. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 1108 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1100 may include a plurality of communications logic units 1108. For instance, a first communications logic unit 1108 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 1108 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0078] The processor 1104 of the computing device 1100 may include one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0079] The communications logic unit 1108 may also include one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0080] In further embodiments, another component housed within the computing device 1100 may contain one or more interconnects or other lithographically patterned features that are formed in accordance with embodiments of the present disclosure.

[0081] In various embodiments, the computing device 1100 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1100 may be any other electronic device that processes data.

[0082] Some Examples in accordance with various embodiments of the present disclosure are now described.

[0083] Example 1 provides a boron carbide (BC) - based device, the device including a structure including a plurality of openings; and a dielectric material disposed within the plurality of openings, the dielectric material including carborane-based units cross-linked to form a BC-based film.

[0084] Example 2 provides the device according to Example 1, where the carborane-based units include one or more of carborane-siloxane hybrids, carborane-carbosilane hybrids, carborane-boroxine hybrids, carborane-phosphine hybrids and metalopolymers, and carborane-arenes.

[0085] Example 3 provides the device according to any one of the preceding Examples, where the plurality of openings have aspect ratios of 1 or more, where an aspect ratio is a ratio of a depth of an opening to a width of the opening.

[0086] Example 4 provides the device according to Example 3, where the plurality of openings have aspect ratios between 1 and 20.

[0087] Example 5 provides a method of making a device including a structure with a plurality of openings filled with a BC-based material, the method including: providing onto the structure including the plurality of openings a precursor including a solution of oligomerized or polymerized difunctional carborane molecules; and providing an excitation to cross-link the precursor into a solid BC-based material within the plurality of openings.

[0088] Example 6 provides the method according to Example 5, where providing the precursor onto the structure includes spin-coating the precursor onto the structure for 1-60 seconds at 500-5000 rotations per minute (rpm).

[0089] Example 7 provides the method according to Examples 5 or 6, where providing the excitation to cross-link the precursor includes baking the structure at 303 to 673 degrees Celsius for 30 seconds to 30 minutes (soft-baking).

[0090] Example 8 provides the method according to any one of Examples 5-7, where providing the excitation to cross-link the precursor includes baking the structure at 573 to 773 degrees Celsius for 1-60 minutes (hard-baking).

[0091] Example 9 provides the method according to Example 8, where baking the structure at 573 to 773 degrees Celsius is performed under nitrogen.

[0092] Example 10 provides the method according to Example 8, where baking the structure at 573 to 773 degrees Celsius is performed under a reactive gas.

[0093] Example 11 provides the method according to Example 10, where the reactive gas includes ammonia, hydrogen, oxygen, diborane, or disilane.

[0094] Example 12 provides the method according to any one of Examples 5-11, where providing the excitation to cross-link the precursor includes providing an optical excitation.

[0095] Example 13 provides the method according to any one of Examples 5-12, further including curing the solid BC-based material.

[0096] Example 14 provides the method according to Example 13, where curing includes exposing the solid BC-based material to optical radiation of 170-300 nanometer wavelengths.

[0097] Example 15 provides the method according to Example 13, where curing includes heating the solid BC-based material between 200-450 degrees Celsius while simultaneously exposing to optical radiation of 170-300 nanometer wavelengths.

[0098] Example 16 provides the method according to Example 13, where curing includes heating the solid BC-based material between 200-450 degrees Celsius and exposing the solid carbosilane material to electrons.

[0099] Example 17 provides the method according to Example 13, where curing includes plasma-assisted curing of the solid BC-based material, performed with or without heating, e.g. heating to 200-400 degrees Celsius.

[00100] Example 18 provides the method according to any one of Examples 5-17, further including heating the precursor provided on the structure, prior to providing the excitation, to a temperature above a glass transition temperature of the precursor.

[00101] Example 19 provides the method according to Example 18, where heating the precursor provided on the structure to the temperature above the glass transition temperature of the precursor includes heating the precursor to 125 degrees Celsius for 5 minutes.

[00102] Example 20 provides the method according to Examples 18 or 19, where the heating is carried out under nitrogen gas.

[00103] Example 21 provides the method according to any one of Examples 5-20, further including performing an outgassing of the solid BC-based material, preferably done prior to curing, if curing is performed.

[00104] Example 22 provides the method according to Example 21, where the outgassing includes baking the structure at 400 to 450 degrees Celsius for 1 to 30 minutes.

[00105] Example 23 provides a method of preparing a precursor for forming BC – based materials, the method including functionalizing carborane molecules at two carbon positions to synthesize difunctional carborane molecules; reacting the difunctional carborane molecules with one or more electrophiles to produce oligomers or/and polymers of the difunctional carborane molecules, and dissolving the oligomers or/and polymers of the difunctional carborane molecules in one or more solvents to use as the precursor.

[00106] Example 24 provides the method according to Example 23, where functionalizing the carborane molecules includes deprotonation of the carborane molecules.

[00107] Example 25 provides the method according to Examples 23 or 24, where functionalizing the carborane molecules includes installing organosilane functionality on the carborane molecules to produce siloxanes.

[00108] Example 26 provides the method according to Examples 23 or 24, where functionalizing the carborane molecules includes functionalizing the carborane molecules with boronic acid or boronate functionality.

[00109] Example 27 provides the method according to Example 23, where the one or more electrophiles include dichlorosilanes, dichloroboranes, alkyl dichlorides, aryl dichlorides, dichlorostannanes, dichlorophosphines, and metal halides.

[00110] Example 28 provides the method according to Examples 23 or 24, where the one or more electrophiles include multifunctional molecules with two or more sites for reaction with nucleophiles of the difunctional carborane molecules.

[00111] Example 29 provides the method according to any one of Examples 23-28, where the one or more solvents include toluene, cyclohexanone, 2-heptanone, and propyleneglycol monomethyl ether acetate.

[00112] Example 30 provides a precursor for forming BC – based materials, the precursor including a solution of oligomers and/or polymers of carborane molecules functionalized at two carbon positions and reacted with one or more electrophiles.

[00113] Example 31 provides the precursor according to Example 30, where the solution includes a solution in one or more of toluene, cyclohexanone, 2-heptanone, and propyleneglycol monomethyl ether acetate.

[00114] Example 32 provides the precursor according to Examples 30 or 31, where the oligomers and/or polymers include carborane-siloxane hybrids.

[00115] Example 33 provides the precursor according to Examples 30 or 31, where the oligomers and/or polymers include carborane-boroxine hybrids.

[00116] Example 34 provides the precursor according to Examples 30 or 31, where the oligomers and/or polymers include carborane-phosphine hybrids.

[00117] Example 35 provides the precursor according to Examples 30 or 31, where the oligomers and/or polymers include carborane-phosphine metalopolymers.

[00118] Example 36 provides the precursor according to Examples 30 or 31, where the oligomers and/or polymers include carborane-arenes.

[00119] Example 37 provides the precursor according to any one of Examples 30-36, where molecular weight of the oligomers and/or polymers is between 500 and 100000.

[00120] Example 38 provides an integrated circuit package that includes a component, and an interconnect for providing electrical connectivity to the component, the interconnect including a plurality of conductive regions; a structure including a plurality of openings, the plurality of openings configured to electrically isolate at least some of the plurality of conductive regions; and a dielectric material disposed within the plurality of openings, the dielectric material including carborane-based units cross-linked to form a BC-based film.

[00121] Example 39 provides the integrated circuit package according to Example 38, where the component includes a transistor, a die, a sensor, a processing device, or a memory device.

[00122] Example 40 provides the integrated circuit package according to Examples 38 or 39, where the structure and the dielectric material form the device according to any one of Examples 2-4.

[00123] Example 41 provides a computing device including the integrated circuit package according to any one of Examples 38-40.

[00124] Example 42 provides a semiconductor device including the device according to any one of the Examples 1-4.

[00125] The above description of illustrated implementations of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[00126] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A boron carbide (BC) - based device, the device comprising:

a structure comprising a plurality of openings; and

a dielectric material disposed within the plurality of openings, the dielectric material comprising carborane-based units cross-linked to form a BC-based film.

2. The device according to claim 1, wherein the carborane-based units comprise one or more of carborane-siloxane hybrids, carborane-carbosilane hybrids, carborane-boroxine hybrids, carborane-phosphine hybrids and metalopolymers, and carborane-arenes.

3. The device according to claims 1 or 2, wherein the plurality of openings have aspect ratios between 1 and 20, wherein an aspect ratio is a ratio of a depth of an opening to a width of the opening.

4. A method of making a device comprising a structure with a plurality of openings filled with a BC-based material, the method comprising:

providing onto the structure comprising the plurality of openings a precursor comprising a solution of oligomerized or polymerized difunctional carborane molecules; and

providing an excitation to cross-link the precursor into a solid BC-based material within the plurality of openings.

5. The method according to claim 4, wherein providing the precursor onto the structure comprises spin-coating the precursor onto the structure at 500-5000 rotations per minute (rpm).

6. The method according to claims 4 or 5, wherein providing the excitation to cross-link the precursor comprises baking the structure at 303 to 673 degrees Celsius for 30 seconds to 30 minutes.

7. The method according to claims 4 or 5, wherein providing the excitation to cross-link the precursor comprises baking the structure at 573 to 773 degrees Celsius for 1-60 minutes.

8. The method according to claims 4 or 5, further comprising curing the solid BC-based material, wherein curing comprises exposing the solid BC-based material to optical radiation of 170-300 nanometer wavelengths.

9. The method according to claims 4 or 5, further comprising curing the solid BC-based material, wherein curing comprises heating the solid BC-based material between 200-450 degrees Celsius while simultaneously exposing to optical radiation of 170-300 nanometer wavelengths.

10. The method according to claims 4 or 5, further comprising curing the solid BC-based material, wherein curing comprises heating the solid BC-based material between 200-450 degrees Celsius and exposing the solid carbosilane material to electrons.

11. The method according to claims 4 or 5, further comprising heating the precursor provided on the structure, prior to providing the excitation, to a temperature above a glass transition temperature of the precursor.

12. A method of preparing a precursor for forming boron carbide (BC) – based materials, the method comprising:

functionalizing carborane molecules at two carbon positions to synthesize difunctional carborane molecules;

reacting the difunctional carborane molecules with one or more electrophiles to produce oligomers or/and polymers of the difunctional carborane molecules, and

dissolving the oligomers or/and polymers of the difunctional carborane molecules in one or more solvents to use as the precursor.

13. The method according to claim 12, wherein functionalizing the carborane molecules comprises deprotonation of the carborane molecules.

14. The method according to claims 12 or 13, wherein functionalizing the carborane molecules comprises installing organosilane functionality on the carborane molecules to produce siloxanes.

15. The method according to claims 12 or 13, wherein functionalizing the carborane molecules comprises functionalizing the carborane molecules with boronic acid or boronate functionality.

16. The method according to claim 12, wherein the one or more electrophiles comprise dichlorosilanes, dichloroboranes, alkyl dichlorides, aryl dichlorides, dichlorostannanes, dichlorophosphines, and metal halides.

17. The method according to claims 12 or 13, wherein the one or more electrophiles comprise multifunctional molecules with two or more sites for reaction with nucleophiles of the difunctional carborane molecules.

18. A precursor for forming boron carbide (BC) – based materials, the precursor comprising:

a solution of oligomers and/or polymers of carborane molecules functionalized at two carbon positions and reacted with one or more electrophiles.

19. The precursor according to claim 18, wherein the solution comprises a solution in one or more of toluene, cyclohexanone, 2-heptanone, and propyleneglycol monomethyl ether acetate.

20. The precursor according to claims 18 or 19, wherein the oligomers and/or polymers comprise carborane-siloxane hybrids.

21. The precursor according to claims 18 or 19, wherein the oligomers and/or polymers comprise carborane-boroxine hybrids.

22. The precursor according to claims 18 or 19, wherein the oligomers and/or polymers comprise carborane-phosphine hybrids.

23. The precursor according to claims 18 or 19, wherein the oligomers and/or polymers comprise carborane-phosphine metalopolymers.

24. The precursor according to claims 18 or 19, wherein the oligomers and/or polymers comprise carborane-arenes.

25. The precursor according to claims 18 or 19, wherein molecular weight of the oligomers and/or polymers is between 500 and 100000.

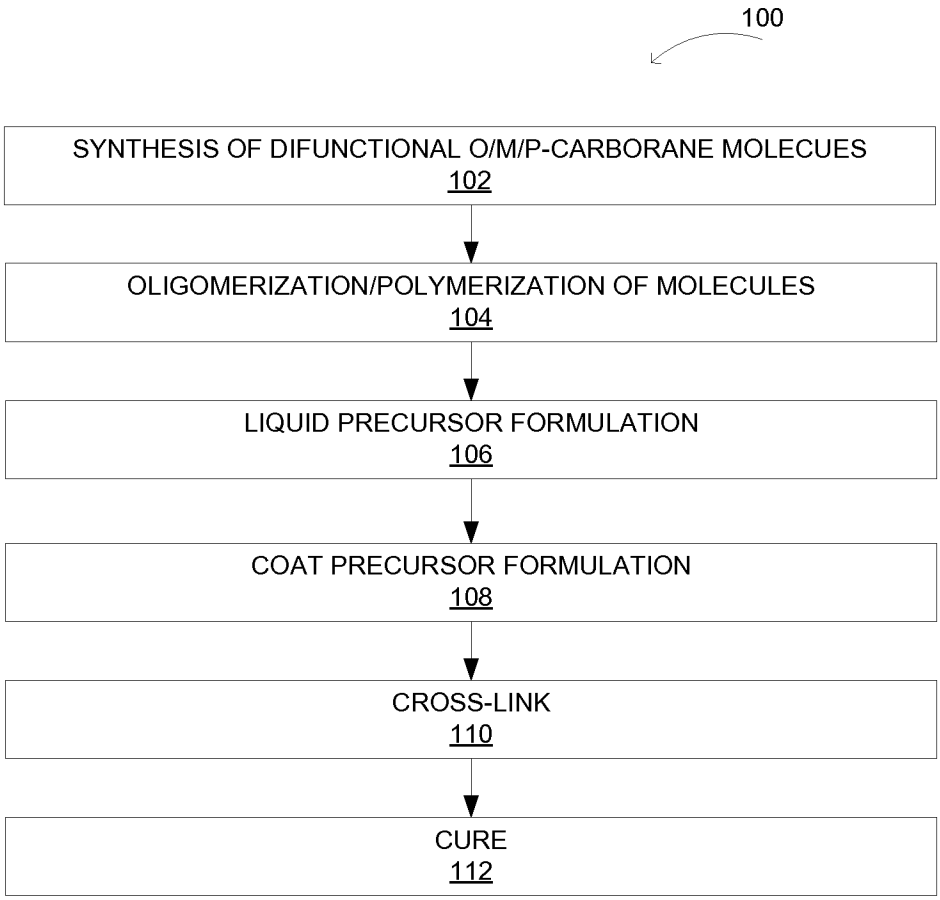
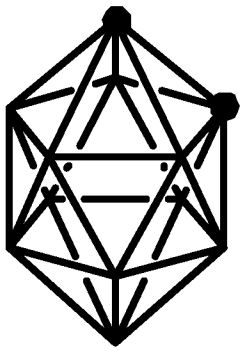
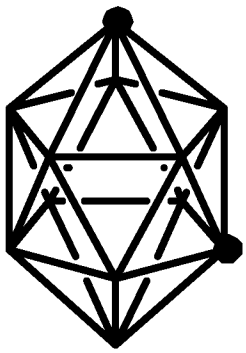

100
SYNTHESIS OF DIFUNCTIONAL O/M/P-CARBORANE MOLECUES
102
OLIGOMERIZATION/POLYMERIZATION OF MOLECULES
104
LIQUID PRECURSOR FORMULATION
106
COAT PRECURSOR FORMULATION
108
CROSS-LINK
110
CURE
112

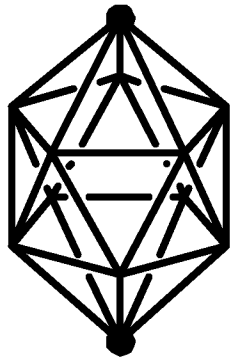
FIG. 1



o-Carborane
o-$C_2H_{12}B_{10}$

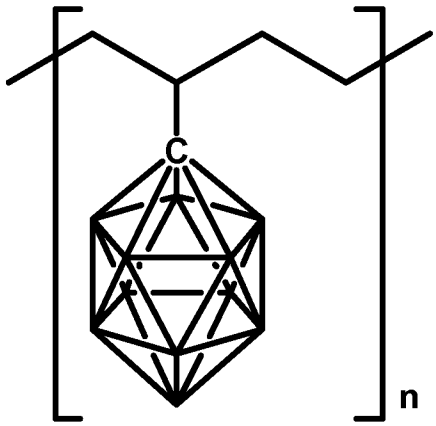


m-Carborane
m-$C_2H_{12}B_{10}$

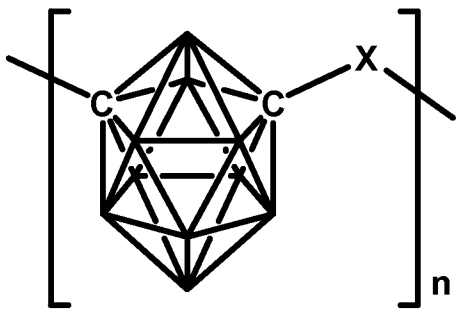


p-Carborane
p-$C_2H_{12}B_{10}$

FIG. 2



Side Chain



Main Chain

FIG. 3

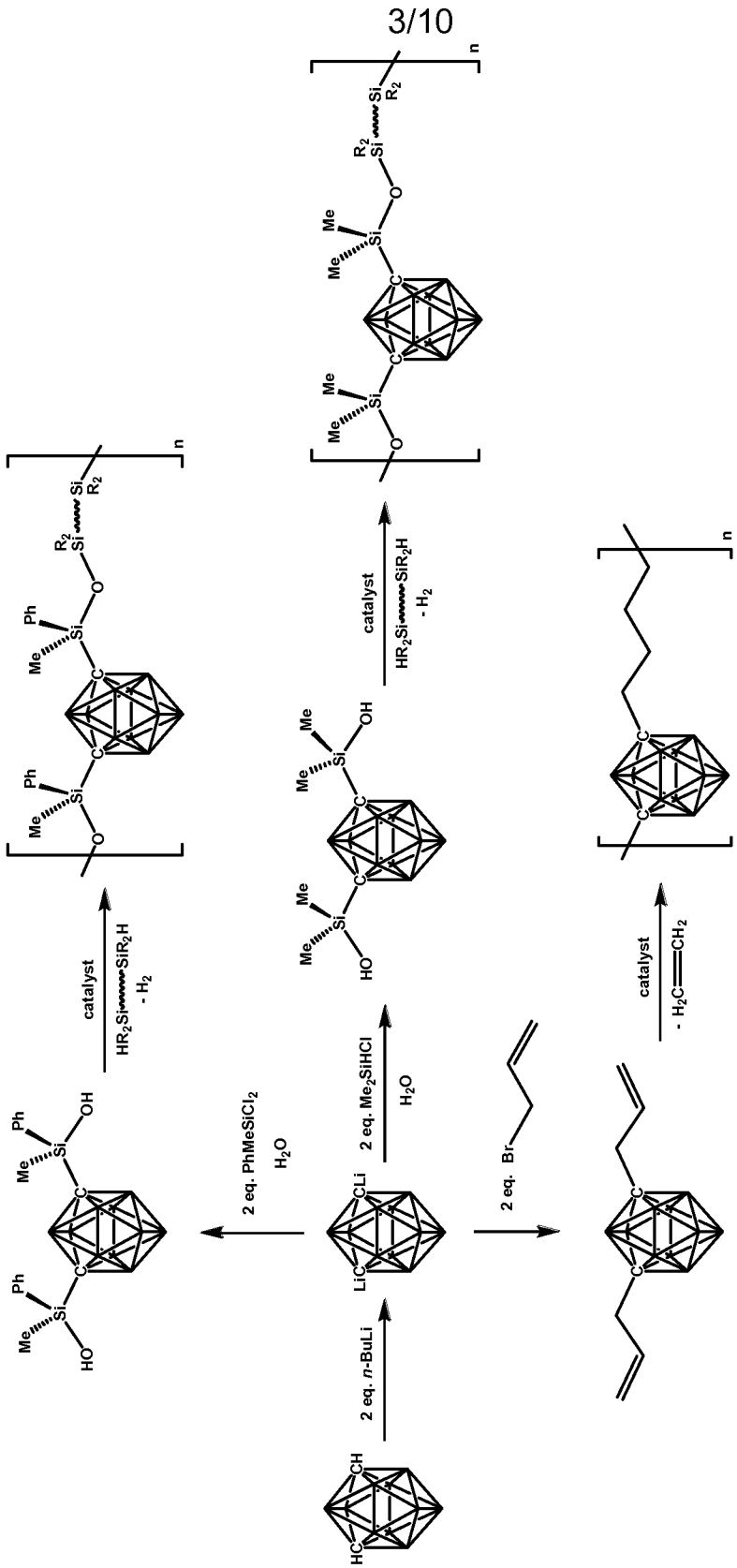

2 eq. n-BuLi
2 eq. PhMeSiCl2
H2O
2 eq. Me2SiHCl
H2O
2 eq. Br
catalyst
HR2Si-----SiR2H
- H2
catalyst
HR2Si-----SiR2H
- H2
catalyst
- H2C=CH2

FIG. 4

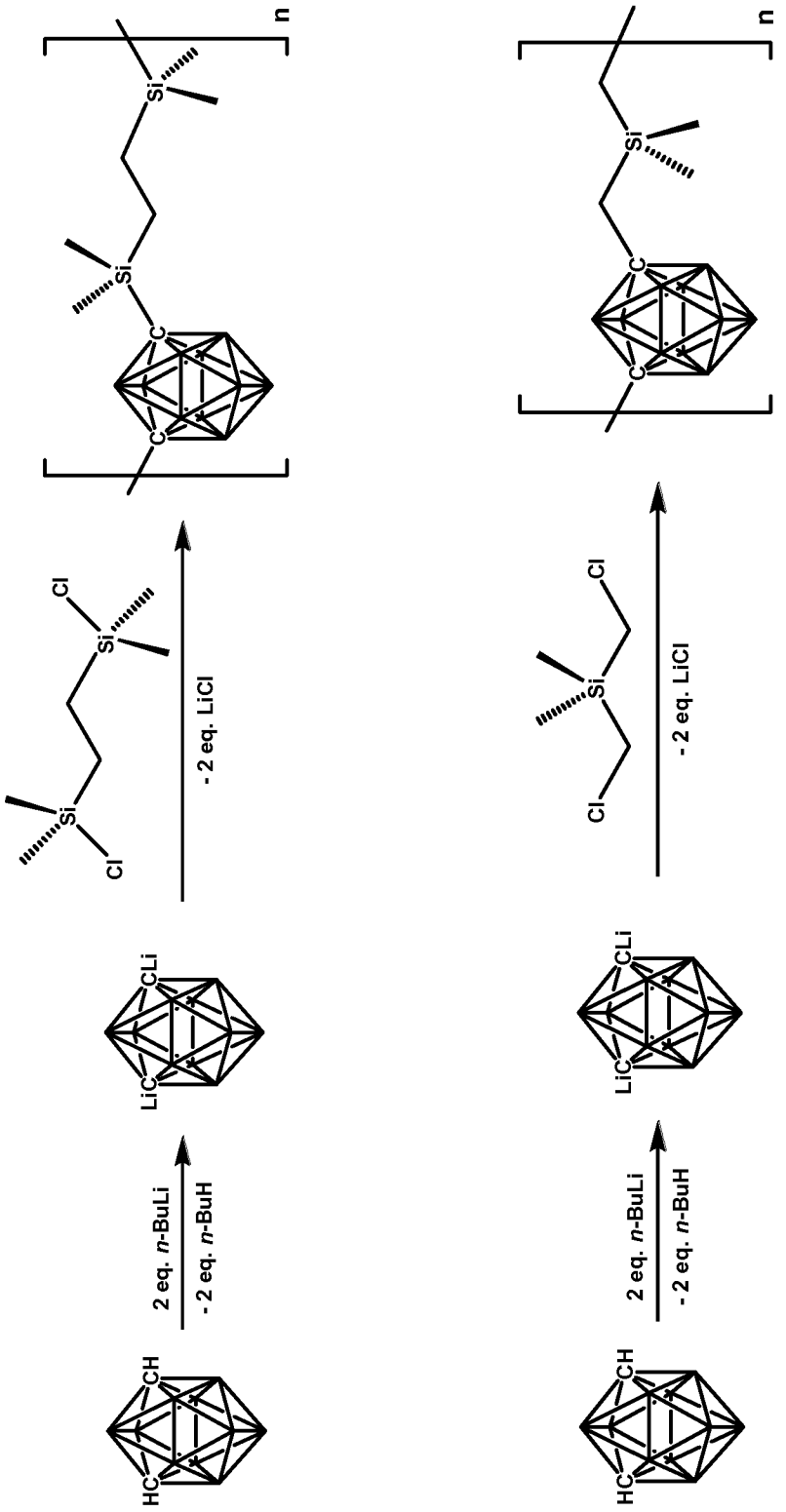


FIG. 5

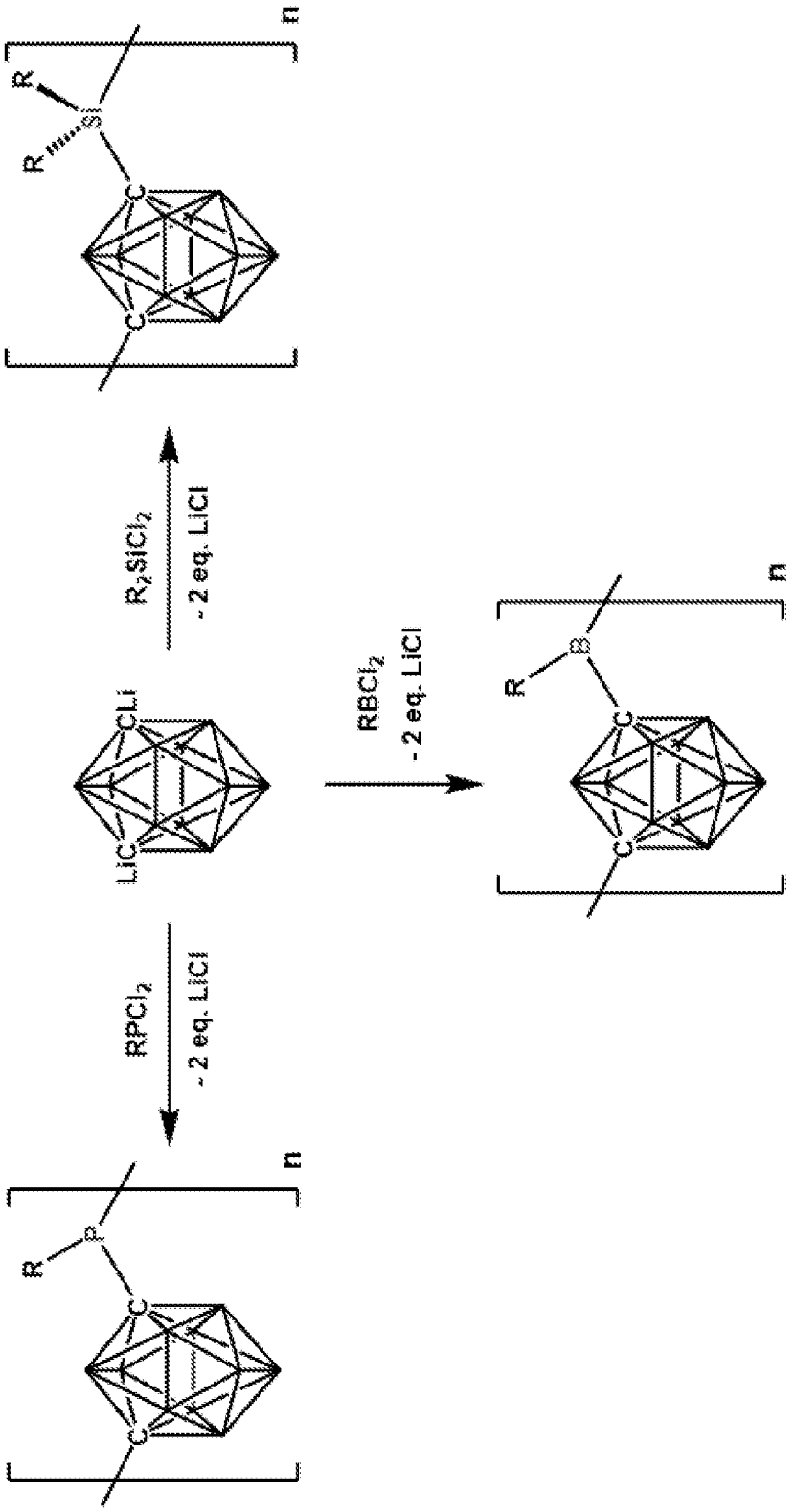

n
R
R
Si
C
C
R2SiCl2
- 2 eq. LiCl
CLi
LiC
RBCl2
- 2 eq. LiCl
n
R
B
C
C
RPCl2
- 2 eq. LiCl
n
R
P
C
C

FIG. 6

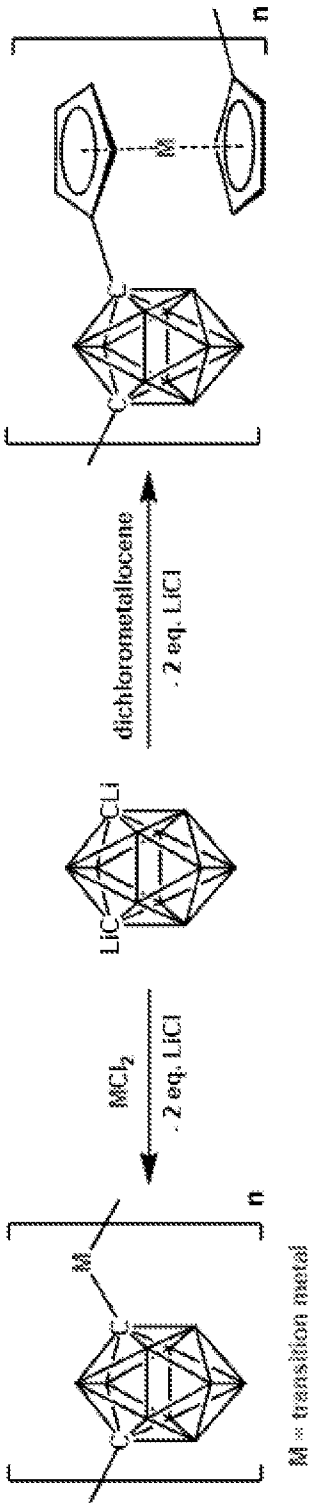

n
M
dichlorometallocene
- 2 eq. LiCl
CLi
LiC
MCl2
- 2 eq. LiCl
n
M
M = transition metal

FIG. 7

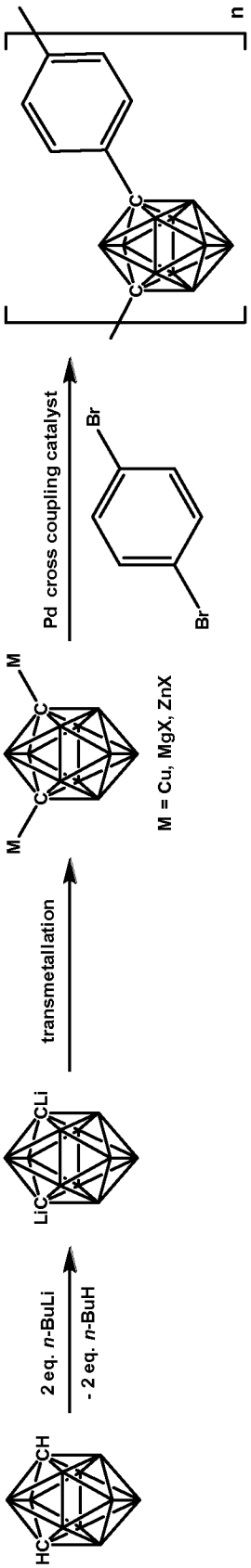

HC
CH
2 eq. n-BuLi
- 2 eq. n-BuH
LiC
CLi
transmetallation
M
C
C
M
M = Cu, MgX, ZnX
Pd cross coupling catalyst
Br
Br
n

FIG. 8

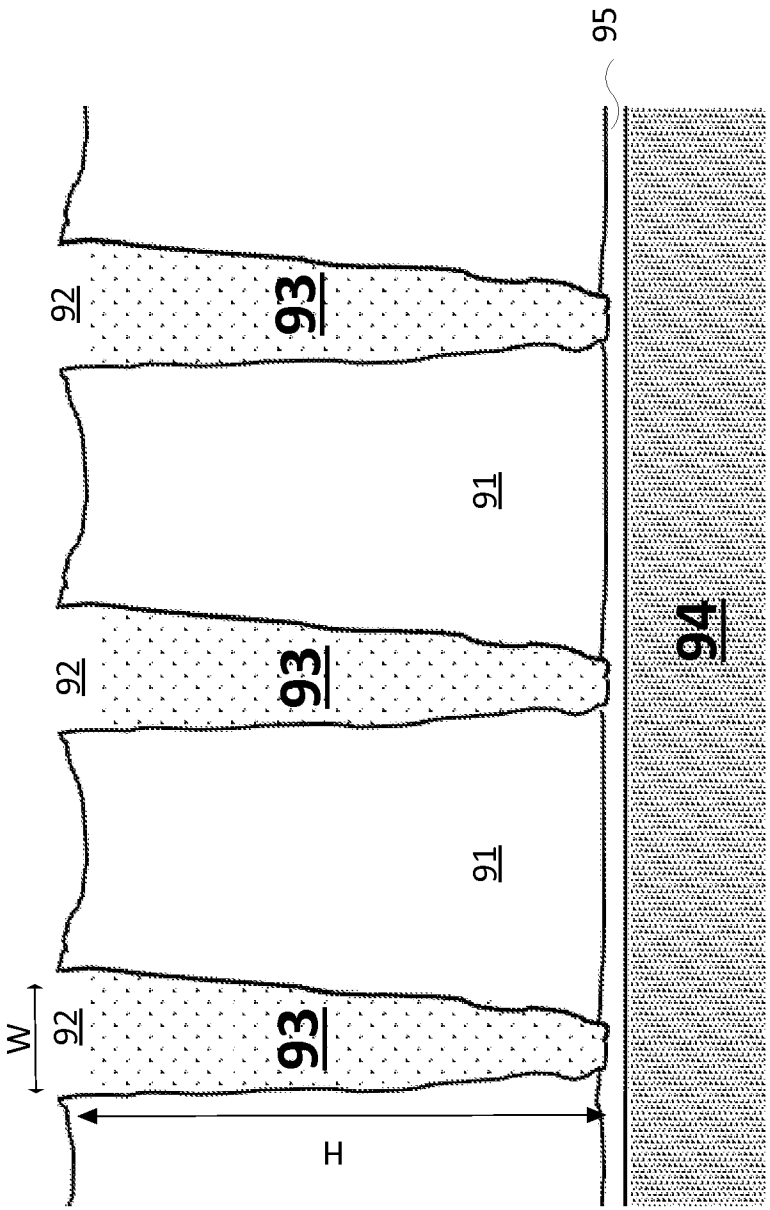


FIG. 9

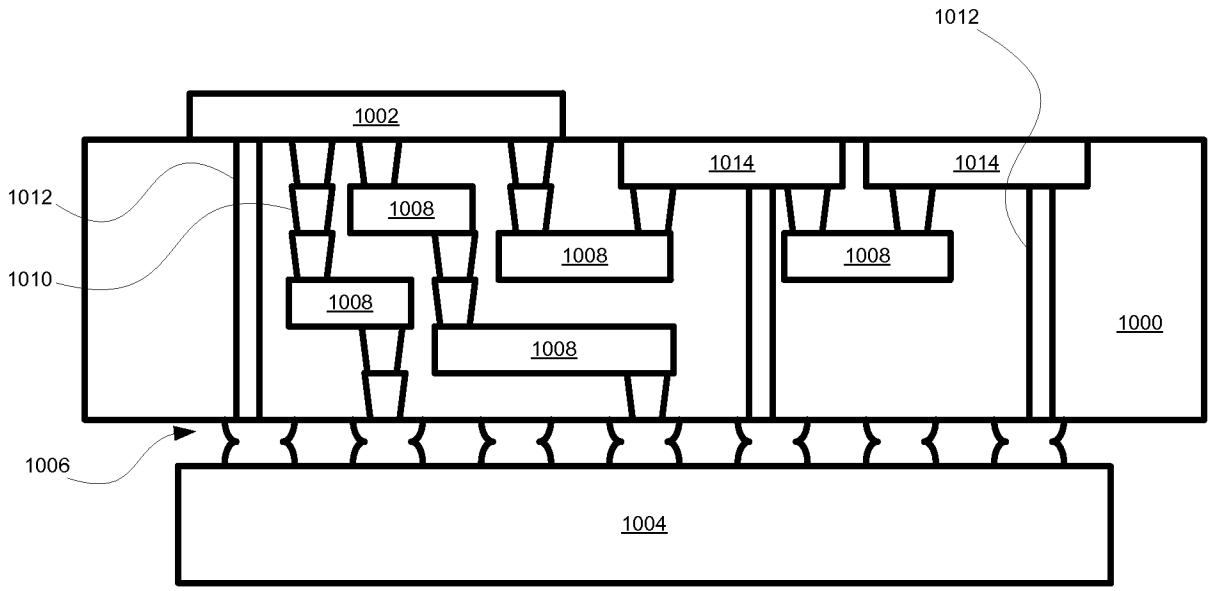

1012
1002
1014
1014
1012
1008
1008
1008
1010
1008
1000
1008
1006
1004

FIG. 10

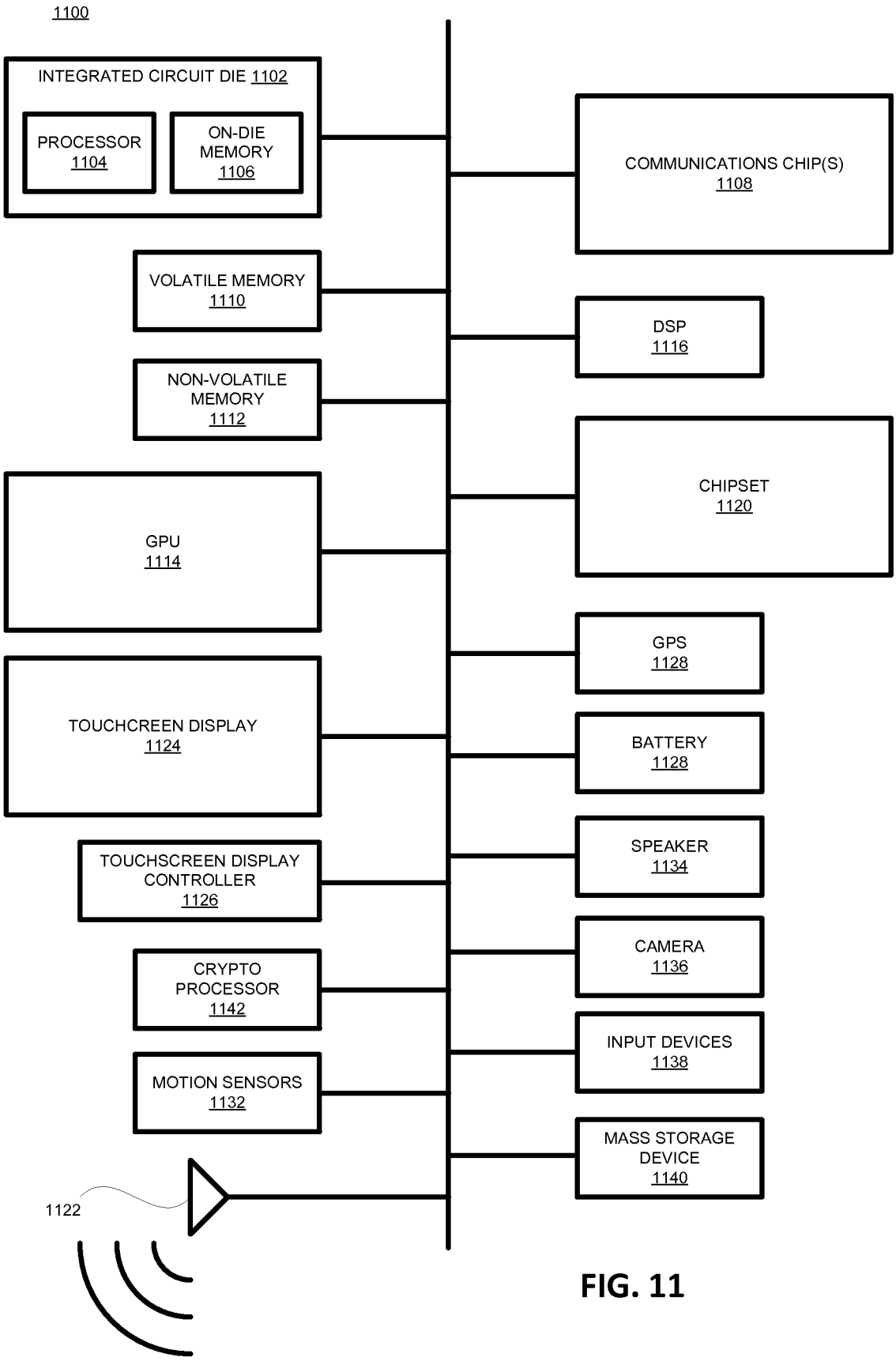

1100
INTEGRATED CIRCUIT DIE 1102
PROCESSOR 1104
ON-DIE MEMORY 1106
VOLATILE MEMORY 1110
NON-VOLATILE MEMORY 1112
GPU 1114
TOUCHCREEN DISPLAY 1124
TOUCHSCREEN DISPLAY CONTROLLER 1126
CRYPTO PROCESSOR 1142
MOTION SENSORS 1132
1122
COMMUNICATIONS CHIP(S) 1108
DSP 1116
CHIPSET 1120
GPS 1128
BATTERY 1128
SPEAKER 1134
CAMERA 1136
INPUT DEVICES 1138
MASS STORAGE DEVICE 1140

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/064158

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/31(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/31; H01L 23/52; H01L 21/469; H01L 21/4763; H01L 31/0328; H01L 21/762; H01L 29/06; C08F 2/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords:boron carbide, gapfill, carborane, oligomer, precursor, solution, crosslink

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6352921 B1 (LICHENG M. HAN et al.) 05 March 2002 See abstract, columns 5-7, claims 1, 2 and figures 2a-2f.	1-25
A	US 2009-0017640 A1 (JEONG-UK HUH et al.) 15 January 2009 See abstract and paragraphs [0019]-[0041].	1-25
A	US 2010-0099236 A1 (YOUNG SOO KWON et al.) 22 April 2010 See abstract, paragraphs [0029]-[0038] and figure 4.	1-25
A	US 2004-0084690 A1 (PETER A. DOWBEN et al.) 06 May 2004 See abstract, paragraph [0024] and figure 1.	1-25
A	US 2004-0130031 A1 (TIAN-AN CHEN et al.) 08 July 2004 See abstract, paragraphs [0020]-[0025], claims 1-7 and figures 5-13.	1-25
A	FRANK L. PASQUALE et al. "Novel Cross-Linked Ortho-Carborane and Ortho-Carborane:Y (Y=1,4-diaminobenzene, pyridine, benzene) Polymer Films: A New Class of Carborane-Based Materials with Tunable Electronic Structure." ECS Transaitions, 2013, Vol. 53, No. 1, pp. 303-310 See abstract, page 304 and figure 1.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 August 2016 (17.08.2016)	**17 August 2016 (17.08.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/064158

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US 2004-0130031 A1	08/07/2004	US 7029723 B2	18/04/2006