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(71) Applicant *(for all designated States except US)*: **RAMBUS INCORPORATED** [US/US]; 4440 El Camino Real, Los Altos, CA 94022 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PEREGO, Richard** [US/US]; 2902 E. 148th Place, Thornton, CO 80602 (US). **WARE, Fred** [US/US]; 13961 Fremont Pines Lane, Los Altos Hill, CA 94022 (US). **TSERN, Ely** [US/US]; 784 Dixon Way, Los Altos, CA 94022 (US). **HAMPEL, Craig** [US/US]; 340 Bellvue Court, Los Altos, CA 94024 (US).

(74) Agent: **DENIRO, Kirk, J.**; Vierra Magen Marcus Harmon & DeNiro, LLP, 685 Market Street, Suite 540, San Francisco, CA 94105 (US).

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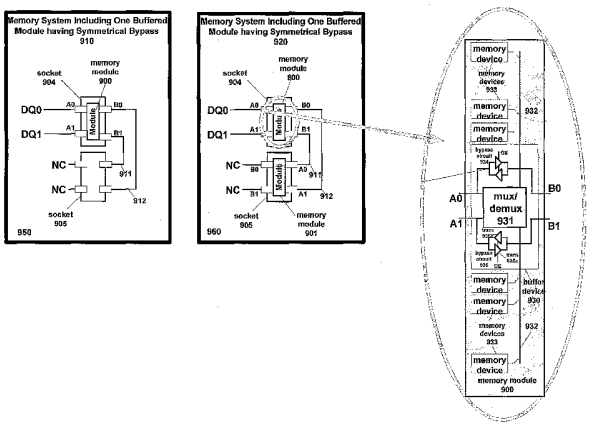
(54) Title: CONFIGURABLE WIDTH BUFFERED MODULE HAVING A BYPASS CIRCUIT



(57) Abstract: A memory system architecture/interconnect topology includes a configurable width buffered memory module having a configurable width buffer device with at least one bypass circuit. A buffer device, such as a configurable width buffer device, is positioned between or with at least one integrated circuit memory device positioned on a substrate surface of a memory module, such as a DIMM. The configurable width buffer device is coupled to at least one memory device (by way of an internal channel), entry pin and exit pin on the memory module. The configurable width buffer device includes a multiplexer/demultiplexer circuit coupled to the entry pin and the internal channel for accessing the memory device. A bypass circuit is coupled to the entry pin and the exit pin in order to allow information to be transferred through the memory module to another coupled memory module in the memory system by way of an external channel. In an alternate embodiment of the present invention, two bypass circuits are coupled to a pair of entry and exit pins. In an embodiment of the present invention, a memory system may include at least four interfaces, or sockets, for respective memory modules having configurable width buffer devices with bypass circuits that enable additional upgrade options while reducing memory system access delays.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CONFIGURABLE WIDTH BUFFERED MODULE HAVING A BYPASS CIRCUIT

This application is a continuation-in-part of U.S. Patent Application Serial No. 10/766,131 filed on January 28, 2004 (still pending); which is a continuation-in-part of U.S. Patent Application Serial No. 10/272,024 filed on October 15, 2002 (still pending); which is a continuation of U.S. Patent Application Serial No. 09/479,375 filed on January 5, 2000 (now U.S. Patent No. 6,502,161).

BACKGROUND OF THE INVENTION

This invention relates to memory systems, memory subsystems, memory modules or a system having memory devices. More specifically, this invention is directed toward memory system architectures that may include integrated circuit devices such as one or more controllers and a plurality of memory devices.

Some contemporary memory system architectures may demonstrate tradeoffs between cost, performance and the ability to upgrade, for example; the total memory capacity of the system. Memory capacity is commonly upgraded via memory modules or cards featuring a connector/socket interface. Often these memory modules are connected to a bus disposed on a backplane to utilize system resources efficiently. System resources include integrated circuit die area, package pins, signal line traces, connectors, backplane board area, just

to name a few. In addition to upgradeability, many of these contemporary memory systems also require high throughput for bandwidth intensive applications, such as graphics.

With reference to FIGURE 1, a representational block diagram of a conventional memory system employing memory modules is illustrated. Memory system 100 includes memory controller 110 and modules 120a-120c. Memory controller 110 is coupled to modules 120a-120c via control/address bus 130, data bus 140, and corresponding module control lines 150a-150c. Control/address bus 130 typically comprises a plurality of address lines and control signals (e.g., RAS, CAS and WE).

The address lines and control signals of control/address bus 130 are bussed and "shared" between each of modules 120a-120c to provide row/column addressing and read/write, precharge, refresh commands, etc., to memory devices on a selected one of modules 120a-120c. Individual module control lines 150a-150c are typically dedicated to a corresponding one of modules 120a-120c to select which of modules 120a-120c may utilize the control/address bus 130 and data bus 140 in a memory operation.

Here and in the detailed description to follow, "bus" denotes a plurality of signal lines, each having one or more connection points for "transceiving" (i.e., transmitting or receiving). Each connection point connects or couples to a transceiver (i.e., a transmitter-receiver) or one of a single transmitter or receiver circuit. A connection or coupling is provided electrically, optically, magnetically, by way of quantum entanglement or equivalently thereof.

With further reference to FIGURE 1, memory system 100 may provide an upgrade path through the usage of modules 120a-120c. A socket and connector interface may be employed which allows each module to be removed and replaced by a memory module that is faster

or includes a higher capacity. Memory system 100 may be configured with unpopulated sockets or less than a full capacity of modules (i.e., empty sockets/connectors) and provided for increased capacity at a later time with memory expansion modules. Since providing a separate group of signals (e.g., address lines and data lines) to each module is avoided using the bussed approach, system resources in memory system 100 are efficiently utilized.

U.S. Patent 5,513,135 discloses a contemporary dual inline memory module (DIMM) having one or more discrete buffer devices.

Examples of contemporary memory systems employing buffered modules are illustrated in FIGURES 2A and 2B. FIGURE 2A illustrates a memory system 200 based on a Rambus® channel architecture and FIGURE 2B illustrates a memory system 210 based on a Synchronous Link architecture. Both of these systems feature memory modules having buffer devices 250 disposed along multiple transmit/receive connection points of bus 260.

In an upgradeable memory system, such as conventional memory system 100, different memory capacity configurations become possible. Each different memory capacity configuration may present different electrical characteristics to the control/address bus 130. For example, load capacitance along each signal line of the control/address bus 130 may change with two different module capacity configurations. However, using conventional signaling schemes, the bussed approaches lend efficiency towards resource utilization of a system and permits module interfacing for upgradeability.

There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

In the course of the detailed description to follow, reference will be made to the attached drawings, in which:

FIGURE 1 illustrates a representational block diagram of a conventional memory system employing memory modules;

FIGURES 2A and 2B illustrate contemporary memory systems employing buffered modules;

FIGURES 3A and 3B illustrate a block diagram representing memory systems according to embodiments of the present invention;

FIGURE 3C illustrates a block diagram representing a memory module that includes a configurable width buffer device according to an embodiment of the present invention;

FIGURES 4A, 4B, and 4C illustrate buffered memory modules according to embodiments of the present invention;

FIGURE 5A illustrates a block diagram of a buffer device according to another embodiment of the present invention;

FIGURE 5B illustrates a block diagram of a configurable width buffer device according to an embodiment of the present invention;

FIGURE 5C illustrates a block diagram showing multiplexing and demultiplexing logic used in a configurable width interface of a buffer device shown in FIGURE 5B according to an embodiment of the present invention;

FIGURE 5D is a table showing control input states to achieve specified data widths in the configurable width buffer device shown in FIGURE 5B;

FIGURES 5E and 5F illustrate configurable width buffered modules including a configurable width buffer device coupled to memory devices according to an embodiment of the present invention;

FIGURES 6A and 6B illustrate block diagrams of a memory system according to other embodiments of the present invention;

FIGURE 7 illustrates a block diagram of a memory system employing a buffered quad-channel module according to an embodiment of the present invention;

FIGURE 8A illustrates a block diagram of a large capacity memory system according to another embodiment of the present invention; and

FIGURES 8B and 8C illustrate another approach utilized to expand the memory capacity of a memory system in accordance to yet another embodiment of the present invention;

FIGURE 9 illustrates a memory system including a buffered memory module having symmetric bypass circuits in accordance to an embodiment of the present invention;

FIGURE 10A illustrates an address space for a single buffered memory module having symmetric bypass circuits in accordance to an embodiment of the present invention;

FIGURE 10B illustrates an address space for two buffered memory modules having respective symmetric bypass circuits in accordance to an embodiment of the present invention;

FIGURE 11 illustrates a memory system including four buffered memory modules having respective symmetric bypass circuits in accordance to an embodiment of the present invention;

FIGURE 12A illustrates an address space for a single buffered memory module having asymmetric bypass circuit in accordance to an embodiment of the present invention;

FIGURE 12B illustrates an address space for two buffered memory modules having respective asymmetric bypass circuits in accordance to an embodiment of the present invention;

FIGURE 13A illustrates an address space for a single buffered memory module having asymmetric bypass circuit in accordance to an embodiment of the present invention;

FIGURE 13B illustrates an address space for two buffered memory modules having respective asymmetric bypass circuits when the two buffer memory modules do not have equal storage capacity in accordance to an embodiment of the present invention;

FIGURE 14A illustrates managing an address space for a single buffered memory module having asymmetric bypass circuit in a memory system having buffered memory modules with unequal storage capacity in accordance to an embodiment of the present invention;

FIGURE 14B illustrates managing an address space for two buffered memory modules having respective asymmetric bypass circuits when the two buffered memory modules have unequal storage capacity in accordance to an embodiment of the present invention;

FIGURE 15 illustrates a buffered memory module having bypass circuits for coupling to four channels in accordance to an embodiment of the present invention;

FIGURE 16A illustrates how a single buffered memory module, as shown in FIGURE 15, is used in a four-socket memory system in accordance to an embodiment of the present invention;

FIGURE 16B illustrates how two buffered memory modules, as shown in FIGURE 15, are used in a four-socket memory system in accordance to an embodiment of the present invention;

FIGURE 16C illustrates how three buffered memory modules, as shown in FIGURE 15, are used in a four-socket memory system in accordance to an embodiment of the present invention;

FIGURE 16D illustrates how four buffered memory modules, as shown in FIGURE 15, are used in a four-socket memory system in accordance to an embodiment of the present invention;

FIGURES 17 and 19 illustrate different modes of operation of a buffered memory module in accessing storage cells in a memory device in accordance to an embodiment of the present invention;

FIGURES 18 and 20 illustrate different modes of operation of a buffered memory module in accessing respective storage cells in respective memory devices in accordance to an embodiment of the present invention;

FIGURES 21 and 22 illustrate different views of a memory module having a buffer device positioned between a substrate and an integrated circuit memory device in accordance to embodiments of the present invention.

DETAILED DESCRIPTION

The present invention relates to a memory system which includes one or more semiconductor memory devices coupled to a buffer device having a bypass circuit. The buffer device may be disposed on a memory module, housed in a common package along with memory devices, or situated on a motherboard, for example, main memory in a personal computer or server. The buffer device may also be employed in an embedded memory subsystem, for example such as one found on a computer graphics card, video game console or a printer.

In several embodiments, the buffer device having a bypass circuit provides for flexible system configurations, and several performance benefits. For example, a buffer device having a bypass circuit enables adding memory module upgrades to a memory system while reducing system delays for accessing information from the memory module upgrades. Further, the buffer device may be a configurable width buffer device to provide upgrade flexibility and/or provide high bandwidth among a variety of possible module configurations in the system. A plurality of buffer devices, configurable or otherwise, may be utilized in

the memory system to provide high capacity, without compromising performance. A buffer device having configurable width functionality may be employed to allow memory subsystem bandwidth to scale as the system is upgraded or to allow theoretical maximum memory subsystem bandwidth to be achieved among possible memory module configurations. As specified herein, "configurable width" is used to denote that interfacing to the buffer device may be configured in a flexible manner, for example, by configuring how many parallel bits of data may be transferred with the buffer device.

In several embodiments, one or more busses or a plurality of point-to-point links may be used to couple one or more buffer devices to a master (e.g., a controller or microprocessor device). A dynamic point-to-point link topology or any combination of point-to-point links or busses may be used to interface the master device and a corresponding buffer device.

In a specific embodiment, at least one point-to-point link connects at least one memory subsystem to the master, (e.g., a processor or controller). The memory system may be upgraded by coupling memory subsystems to the master via respective dedicated point-to-point links. Each memory subsystem includes a buffer device (e.g., a configurable width buffer device) that communicates to a plurality of memory devices. The master communicates with each buffer device via each point-to-point link. The buffer device may be disposed on a memory module along with the plurality of memory devices and connected to the point-to-point link via a connector. Alternatively, the buffer device may be disposed on a common printed circuit board or backplane link along with the corresponding point-to-point link and master.

"Memory devices" are a common class of integrated circuit devices that have a plurality of storage cells, collectively referred to as a memory array. A memory device stores data (which may be retrieved)

associated with a particular address provided, for example, as part of a write or read command. Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR). A memory device typically includes request decode and array access logic that, among other functions, decodes request and address information, and controls memory transfers between a memory array and routing path. A memory device includes a transceiver for transmitting and receiving data in an embodiment of the present invention. A transceiver includes a transmitter circuit to output data synchronously with respect to rising and falling edges of a clock signal as well as a receiver circuit in an embodiment of the present invention.

A "memory subsystem" is a plurality of memory devices, which may be interconnected with an integrated circuit device (e.g., a buffer device) providing access between the memory devices and an overall system, for example, a computer system. It should be noted that a memory system is distinct from a memory subsystem in that a memory system may include one or more memory subsystems. A "memory module" or simply just "module" denotes a substrate package housing or structure having a plurality of memory devices employed with a connector interface. For example, a memory module may be included in a single unitary package, as in a "system in package" ("SIP") approach. In one type of SIP approach, the module may include a series of integrated circuit dies (i.e., memory devices and buffer device) stacked on top of one another and coupled via conductive interconnect. Solder balls or wire leads may be employed as the connector interface such that the module may be fixedly attached to a printed circuit board substrate. The connector interface may also be of a physically separable type that includes, for example, male and female portions such that the module is detachable from the rest of the system. Another

SIP approach may include a number of memory devices and buffer device disposed, in a two dimensional arrangement, on a common substrate plane and situated inside a single package housing.

It follows from these definitions that a memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface may be a memory subsystem. As referred to herein, the term "buffer device" may be interchangeable with "configurable width buffer device", although this does not expressly imply that a "buffer device" must have a "configurable width" feature.

A connector interface as described herein, such as a memory module connector interface, is not limited to physically separable interfaces where a male connector or interface engages a female connector or interface. A connector interface also includes any type of physical interface or connection, such as an interface used in a SIP where leads, solder balls or connections from a memory module are soldered to a circuit board. For example, in the stacked die approach, a number of integrated circuit die (i.e., memory devices and buffer device) may be stacked on top of one another with a substrate forming the base and interface to a memory controller or processor via a ball grid array type of connector interface. As another example, the memory devices and buffer device may be interconnected via a flexible tape interconnect and interface to a memory controller via one of a ball grid array type connector interface or a physically separable socket type connector interface.

With reference to FIGURES 3A and 3B, block diagrams of a memory system according to embodiments of the present invention are illustrated. Memory systems 300 and 305 include a controller 310, a plurality of point-to-point links 320a-320n, and a plurality of memory subsystems 330a-330n. For simplicity, a more detailed embodiment of

memory subsystem 330a is illustrated as memory subsystem 340. Buffer device 350 and a plurality of memory devices 360 are disposed on memory subsystem 340. Buffer device 350 is coupled to the plurality of memory devices 360 via channels 370. Interface 375 disposed on controller 310 includes a plurality of memory subsystem ports 378a-378n. A "port" is a portion of an interface that serves a congruent I/O functionality. The memory subsystem ports 378a-378n may be included as a portion of a configurable width interface, for example as is described in some of the embodiments below.) One of memory subsystem ports 378a-378n includes I/Os, for sending and receiving data, addressing and control information over one of point-to-point links 320a-320n.

According to an embodiment of the present invention, at least one memory subsystem is connected to one memory subsystem port via one point-to-point link. The memory subsystem port is disposed on the memory controller interface, which includes a plurality of memory subsystem ports, each having a connection to a point-to-point link. In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines). A combination of bus and point-to-point connections may be used to connect the memory subsystem ports to each memory subsystem, for example, point-to-point links may be employed to transport data between the memory subsystem ports and each memory subsystem, and one or more busses may be used to transport control and/or addressing information between the memory subsystem ports and each memory subsystem.

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory

module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.

In FIGURE 3A, point-to-point links 320a-320n, memory subsystems 330a-330c (including mating connectors 380a-n), and controller 310, are incorporated on a common substrate (not shown) such as a wafer or a printed circuit board (PCB) in memory system 300. In an alternate embodiment, memory subsystems are incorporated onto individual substrates (e.g., PCBs). The memory subsystems are then fixedly attached to a single substrate that incorporates point-to-point links 320a-320n and controller 310. In another alternate embodiment illustrated in FIGURE 3B, memory subsystems 330a-330c are incorporated onto individual substrates that include connectors 390a-390c to support upgradeability in memory system 305. Corresponding mating connectors 380a-380n are connected to a connection point of each point-to-point link 320a-320n. Each of mating connectors 380a-380n interface with connectors 390a-390c to allow removal/inclusion of

memory subsystems 330a-330c in memory system 305. In one embodiment, mating connectors 380a-380n are sockets and connectors 390a-390c are edge connectors disposed on an edge of each memory subsystems 330a-330c. Mating connectors 380a-380n, are attached to a common substrate shared with point-to-point links 320a-320n and controller 310.

With further reference to FIGURES 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a. Controller 310 receives the signals corresponding to the data at corresponding ports 378a-378n. In this embodiment, memory subsystems 330a-330n are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Patent 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system 100).

Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new

generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

Buffer device 350 effectively reduces the number of loading permutations on the corresponding point-to-point link to one, thus simplifying test procedures. For example, characterization of a point-to-point link may involve aspects such as transmitters and receivers at opposite ends, few to no impedance discontinuities, and relatively short interconnects. By way of contrast, characterization of control/address bus 130 (see FIGURE 1) may involve aspects such as multiple transmit and receive points, long stub lines, and multiple load configurations, to name a few. Thus, the increased number of electrical permutations tends to add more complexity to the design, test, verification and validation of memory system 100.

With further reference to FIGURE 3B an exemplary system that uses configurable width modules coupled in a dynamic point-to-point configuration may be described. In this exemplary embodiment, each of memory subsystems 330a-330c is a buffered memory module having a configurable width interface. In this embodiment, system capacity may scale without compromising performance when memory modules are added to the system to increase total memory capacity. For example, memory system may be populated with a single buffered memory module located, for example in mating connector 380a (e.g., a socket connector), thus leaving point-to-point links 320b-320n coupled to unpopulated mating connectors 380b-380n. In this configuration, point-to-point links 320b-320n may be routed to access the single buffered memory module located in mating connector 380a and routed using electrical or mechanical switches. The single buffered memory module located in mating connector 380a is programmed to include an interface width that may accommodate the routed point-to-point links 320b-320n.

U.S. Patent Application Serial No. 09/797,099, (the Upgradeable Application") entitled "Upgradeable Memory System with Reconfigurable Interconnect," filed on February 28, 2001, Attorney Docket No. RB1-017US which application is incorporated by reference herein and which application is assigned to the owner of the present application, describes a configurable memory module that is used in embodiments of the present invention to provide a dynamic point-to-point configuration. In particular, the configurable memory module taught by the Upgradeable Application is used with a configurable buffer device 391, as described below, in embodiments of the present invention. In a point-to-point system, the minimum number of links per memory module is limited by the number of memory devices in a memory module that does not include a buffer device, but can be as low as one link for a memory module having a configurable width buffer device 391. Because memory modules having configurable width buffer devices allow for fewer links per memory module, more memory modules can be supported for a particular number of links from a master device.

FIGURE 3C shows an example of a configurable width buffered module 395 that can be used in conjunction with the system described above. Configurable width buffered module 395 includes memory devices 360, channels 370, configurable width buffer device 391 and connector 390. Configurable width buffered module 395 is configurable or programmable such that information may be transferred using different numbers of interface connections 390a in connector 390 provided by configurable width buffer device 391. In an embodiment of the present invention, interface connections 390a includes a plurality of contacts, conducting elements or pins. In an embodiment illustrated by FIGURE 3C, there are four possible configurations for configurable width buffer device 391. As used in the circuit described above, however, each module will be configured in one of two ways: (a) to use its full set

of available interface connections 390a, or (b) to use only a limited subset (half in the described example) of its interface connections 390a.

In the following discussion, the modules' alternative configurations, and in particular the configurable width buffer device 391 alternate configurations, are referred to as having or using different "widths". However, it should be noted that the capacities of the memory modules may or may not change with the different data widths, at least in an embodiment of the present invention. A module's full set of data stored on the associated memory devices is available regardless of the buffer interface width being used. With wider interface widths, different subsets of memory devices and memory cells may be accessed through different sets of interface connections. With narrower data or interface widths, the different subsets of memory devices and memory cells are accessed through a common set of interface connections. At such narrower interface widths, larger addressing ranges may be used to access data from one or more of the memory devices.

Configurable width buffered module 395 includes at least one memory device 360a, of memory devices 360, that receive and transmit data bit signals through channels 370 (e.g., a plurality of signal lines). In the described embodiment, memory devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices, Direct Rambus® memory devices (DRDRAM), or "XDR™" memory devices, although the memory devices might be any of a number of other types, including but not limited to SRAM, FRAM (Ferroelectric RAM), MRAM (Magnetoresistive or Magnetic RAM), Flash, or ROM. singly or in combination.

In the embodiment illustrated in FIGURE 3A, buffered modules added to upgrade memory system 300 (e.g., increase memory capacity) are accommodated by independent point-to-point links. Relative to a bussed approach, system level design, verification and validation

considerations are reduced, due to the decreased amount of module inter-dependence provided by the independent point-to-point links. Additionally, the implementation, verification and validation of buffered modules may be performed with less reliance on system level environment factors.

Several embodiments of point-to-point links 320a-320n include a plurality of link architectures, signaling options, clocking options and interconnect types. Embodiments having different link architectures include simultaneous bi-directional links, time-multiplexed bi-directional links and multiple unidirectional links. Voltage or current mode signaling may be employed in any of these link architectures.

Clocking methods employed in the synchronization of events in point-to-point link or bussed topologies include any of globally synchronous clocking (i.e., where a single clock frequency source is distributed to various devices in the system); source synchronous clocking (i.e., where data is transported alongside the clock from the source to destination such that the clock and data become skew tolerant) and encoding the data and the clock together. In one embodiment, differential signaling is employed and is transported over differential pair lines. In alternate embodiments, one or more common voltage or current references are employed with respective one or more current/voltage mode level signaling. In yet other embodiments, multi-level signaling-where information is transferred using symbols formed from multiple signal (i.e., voltage/current) levels is employed.

Signaling over point-to-point links 320a-320n or alternatively, over bussed topologies, may incorporate different modulation methods such as non-return to zero (NRZ), multi-level pulse amplitude modulation (PAM), phase shift keying, delay or time modulation, quadrature amplitude modulation (QAM) and Trellis coding. Other signaling

methods and apparatus may be employed in point-to-point links 320a-320n, for example, optical fiber based apparatus and methods.

The term "point-to-point link" denotes one or a plurality of signal lines, each signal line having only two transceiver connection points, each transceiver connection point coupled to transmitter circuit, receiver circuit or transceiver circuit. For example, a point-to-point link may include a transmitter coupled at or near one end and a receiver coupled at or near the other end. The point-to-point link may be synonymous and interchangeable with a point-to-point connection or a point-to-point coupling.

In keeping with the above description, the number of transceiver points along a signal line distinguishes between a point-to-point link and a bus. According to the above, the point-to-point link consists of two transceiver connection points while a bus consists of more than two transceiver points.

One or more terminators (e.g., a resistive element) may terminate each signal line in point-to-point links 320a-320n. In several embodiments of the present invention, the terminators are connected to the point-to-point link and situated on buffer device 350, on a memory module substrate and optionally on controller 310 at memory subsystem ports 378a-378n. The terminator(s) connect to a termination voltage, such as ground or a reference voltage. The terminator may be matched to the impedance of each transmission line in point-to-point links 320a-320n, to help reduce voltage reflections. Signal lines of bussed topologies may also benefit from terminating end points or connection points where devices, such as buffer devices connect to those signal lines.

In an embodiment of the present invention employing multi-level PAM signaling, the data rate may be increased without increasing either the system clock frequency or the number of signal lines by employing

multiple voltage levels to encode unique sets of consecutive digital values or symbols. That is, each unique combination of consecutive digital symbols may be assigned to a unique voltage level, or pattern of voltage levels. For example, a 4-level PAM scheme may employ four distinct voltage ranges to distinguish between a pair of consecutive digital values or symbols such as 00, 01, 10 and 11. Here, each voltage range would correspond to one of the unique pairs of consecutive symbols.

With reference to FIGURES 4A, 4B and 4C, buffered memory modules according to embodiments of the present invention are shown. Modules 400 and 450 include buffer device 405 and a plurality of memory devices 410a-410h communicating over a pair of channels 415a and 415b. In these embodiments channel 415a communicates to memory devices 410a-410d and channel 415b communicates to memory devices 410e-410h.

In an embodiment, channels 415a and 415b consist of a plurality of signal lines in a relatively short multi-drop bus implementation. The plurality of signal lines may be controlled impedance transmission lines that are terminated using respective termination elements 420a and 420b. Channels 415a and 415b are relatively short (i.e., are coupled to relatively few memory devices relative to a conventional memory system, for example see FIGURES 2A and 2B) and connect to an I/O interface (not shown) of each memory device via a short stub. Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM). The varieties of interconnect topologies, interconnect types, clocking methods, signaling references, signaling methods, and signaling apparatus described above in reference to point-to-point links 320a-320n may equally apply to channels 415a and 415b.

In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge...) information and address (e.g., row and column) information contained in packets. By bundling control and address information in packets, protocols required to communicate to memory devices 410a-410h are independent of the physical control/address interface implementation.

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow "packet protocol" approach. In one alternate embodiment illustrated in FIGURE 6A, individual device select lines 633a and 633b are employed to perform device selection. Individual device select lines 633a and 633b decrease some latency consumed by decoding device identification that normally is utilized when multiple devices share the same channel and incorporate individual device identification values.

Clock lines of channels 415a and 415b include a terminated clock-to-master (CTM) (i.e., clock to buffer) and clock-from-master (CFM) (i.e., clock from buffer) line. In a source synchronous clocking method, CTM may be transition or edge aligned with control and/or data communicated to buffer device 405 from one or more of memory devices 410a-410d in, for example, a read operation. CFM may be aligned with or used to synchronize control and/or data from the memory buffer-to-buffer device 405 in, for example, a write operation.

Although two channels 415a and 415b are shown in FIGURE 4A, a single channel is also feasible. In other embodiments, more than two channels may be incorporated onto module 400. It is conceivable that if each channel and memory device interface is made narrow enough,

then a dedicated channel between each memory device and the buffer device may be implemented on the module. The width of the channel refers to the number of parallel signal paths included in each channel. FIGURE 4B illustrates a quad-channel module 450 having channels 415a-415d. In this embodiment, channels 415c and 415d are routed in parallel with channels 415a and 415b to support more memory devices (e.g., 32 memory devices). By incorporating more channels and additional memory devices, module 450 (FIGURE 4B) may be implemented in memory systems that require large memory capacity, for example, in server or workstation class systems.

In alternate embodiments, channels 415a and 415b may operate simultaneously with channels 415c and 415d to realize greater bandwidth. By operating a plurality of channels in parallel, the bandwidth of the module may be increased independently of the memory capacity. The advantages of greater bandwidth may be realized in conjunction with larger capacity as more modules incorporated by the memory system 305 (see FIGURE 3B) increase the system memory capacity. In other alternate embodiments, the modules are double sided and channels along with corresponding pluralities of memory devices are implemented on both sides. Using both sides of the module increases capacity or increases bandwidth without impacting module height. Both capacity and bandwidth may increase using this approach. Indeed, these techniques may increase capacity and bandwidth singly or in combination.

Other features may also be incorporated to enhance module 400 in high capacity memory systems, for example, additional memory devices and interface signals for error correction code storage and transport (ECC). Referring to FIGURE 4C, memory devices 410i and 410r intended for ECC are disposed on module 470.

In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIGURE 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

With reference to FIGURE 5A, a block diagram of a buffer device according to an embodiment of the present invention is illustrated. Buffer device 405 includes interface 510, interfaces 520a and 520b, multiplexers 530a and 530b, request & address logic 540, write buffer 550, optional cache 560, computation block 565, clock circuit 570a-b and operations circuit 572.

In an embodiment, interface 510 couples to external point-to-point link 320 (e.g., point-to-point links 320a-320n in FIGURES 3A and 3B). Interface 510 includes a port having transceiver 575 (i.e. transmit and receive circuit) that connects to a point-to-point link. Point-to-point link 320 comprises one or a plurality of signal lines, each signal line having no more than two transceiver connection points. One of the two transceiver connection points is included on interface 510. Buffer device 405 may include additional ports to couple additional point-to-point links between buffer device 405 and other buffer devices on other memory modules. These additional ports may be employed to expand memory capacity as is described in more detail below. Buffer device 405 may function as a transceiver between point-to-point link 320 and other point-

to-point links. FIGURES 8B and 8C illustrate some buffer-to-buffer connection topology embodiments, while one of ordinary skill in the art would appreciate that there many more embodiments.

In one embodiment, termination 580 is disposed on buffer device 405 and is connected to transceiver 575 and point-to-point link 320. In this embodiment, transceiver 575 includes an output driver and a receiver. Termination 580 may dissipate signal energy reflected (i.e., a voltage reflection) from transceiver 575. Termination 580 may be a resistor or capacitor or inductor, singly or a series/parallel combination thereof. In alternate embodiments, termination 580 may be external to buffer device 405. For example, termination 580 may be disposed on a module substrate or on a memory system substrate.

In another approach, signal energy reflected from transceiver 575 may be utilized in a constructive manner according to an embodiment. By correctly placing a receive point spaced by a distance from the end of point-to-point link 320, a reflected waveform is summed with an incident waveform to achieve a greater signal amplitude. In this approach, layout space may be saved by eliminating termination 580. System power may also be saved using this approach since smaller incident voltage amplitude waveforms may be employed. This approach may be equally applicable to the transceiver end of the point-to-point link, or to channels 415a and 415b (see FIGURES 4A to 4C).

With further reference to FIGURE 5A, interfaces 520a and 520b receive and transmit to memory devices disposed on the module (e.g., see FIGURES 4A, 4B and 4C) via channels. Ports included on interfaces 520a and 520b connect to each channel. In alternate embodiments of the present invention, interfaces 520a and 520b include any number of channels e.g., two, four, eight or more channels.

According to an embodiment of the present invention, multiplexers 530a and 530b perform bandwidth-concentrating

operations, between interface 510 and interfaces 520a and 520b, as well as route data from an appropriate source (i.e. target a subset of channels, internal data, cache or write buffer). The concept of bandwidth concentration involves combining the (smaller) bandwidth of each channel in a multiple channel embodiment to match the (higher) overall bandwidth utilized in a smaller group of channels. This approach typically utilizes multiplexing and demultiplexing of throughput between the multiple channels and smaller group of channels. In an embodiment, buffer device 405 utilizes the combined bandwidth of interfaces 520a and 520b to match the bandwidth of interface 510. Bandwidth concentration is described in more detail below.

Cache 560 is one performance enhancing feature that may be incorporated onto buffer device 405. Employing a cache 560 may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with lower access latency characteristics than those of the memory devices. Computation block 565 may include a processor or controller unit, a compression/decompression engine, etc, to further enhance the performance and/or functionality of the buffer device. In an embodiment, write buffer 550 may improve interfacing efficiency by utilizing available data transport windows over point-to-point link 320 to receive write data and optional address/mask information. Once received, this information is temporarily stored in write buffer 550 until it is ready to be transferred to at least one memory device over interfaces 520a and 520b.

A serial interface 574 may be employed to couple signals utilized in initialization of module or memory device identification values, test function, set/reset, access latency values, vendor specific functions or calibration. Operations circuit 572 may include registers or a read-only memory (ROM) to store special information (e.g., vendor, memory device parameter or configuration information) that may be used by the

controller. Operations circuit may reduce costs by eliminating the need for separate devices on the module conventionally provided to perform these features (e.g., serial presence detect (SPD) employed in some conventional DIMM modules). An SPD device is a non-volatile memory device included on a memory module. The SPD stores information used by the remainder system to properly configure the memory devices upon boot of the system.

According to an embodiment of the present invention, sideband signals are employed to handle special functions such as reset, initialization and power management functions. In addition, sideband signals may be employed to configure the width of the buffer device. Sideband signals are connected via serial interface 574 and are independent from point-to-point link 320 for handling the special functions. In other embodiments sideband signals are independently coupled to memory devices 410a-410h to directly promote initialization, reset, power-up or other functionality independently of buffer device 405. Other interconnect topologies of sideband signals are possible. For example, sideband signals may be daisy chained between buffer devices and coupled to the memory controller or daisy chained between all memory devices to the memory controller. Alternatively, dedicated sideband signals may be employed throughout.

Clock circuit 570a-b may include clock generator circuit (e.g., Direct Rambus® Clock Generator), which may be incorporated onto buffer device 405 and thus may eliminate the need for a separate clock generating device. Here, module or system costs may be decreased since the need for a unique clock generator device on the module or in the system may be eliminated. Since reliability to provide adequate clocking on an external device is eliminated, complexity is reduced since the clock may be generated on the buffer device 405. By way of comparison, some of the conventional DIMM modules require a phase

lock loop (PLL) generator device to generate phase aligned clock signals for each memory device disposed on the module. In an embodiment of the present invention, clock circuit 570a-b is used to resynchronize information transferred by bypass circuits described below.

According to an embodiment of the present invention, clock circuit 570a-b includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship.

FIGURE 5B illustrates a configurable width buffer device 391 as seen in FIGURE 3C in an embodiment of the present invention. Configurable width buffer device 391 includes like numbered components as shown in FIGURE 5A and, in an embodiment, may operate as described above. Configurable width buffer device 391 also includes configurable width interface 590, state storage 576, configurable serialization circuit 591 and interface 596. In an embodiment, a plurality of contacts, solder balls or pins are included to provide electrical connections between interface 596 and connector 390 (FIGURE 3C) via signal line traces routed on or through out a substrate portion of the module.

Also, in an embodiment of the present invention, one or more transceiver 575 (FIGURE 5B) and termination 580 are associated with each port in interface 596. In this specific embodiment, transceiver 575 includes a transmit circuit to transmit data onto a signal line (external to configurable width buffer device 391) and a receiver circuit to receive a data signal on the same signal line. In an alternate embodiment, the transmit circuit is multiplexed with the data received by the receiver circuit. In still a further embodiment of the present invention, the transmit

circuit transmits data and the receiver circuit receives data simultaneously.

In another embodiment, the transceiver 575 includes separate unidirectional transmit and receive circuits, each having dedicated resources for communicating data on and off configurable width buffer device 391. In this embodiment, unidirectional transmitter circuit transmits data onto a first signal line disposed on (external to configurable width buffer device 391, for example, disposed on configurable width buffered module 395). In addition, unidirectional receiver circuit receives data from a second signal line.

In another embodiment of the present invention, a transmit circuit transmits a differential signal that includes encoded clock information and a receiver circuit receives a differential signal that includes encoded clock information. In this embodiment, clock and data recovery circuit is included to extract the clock information encoded with the data received by the receiver circuit. Furthermore, clock information is encoded with data transmitted by the transmit circuit. For example, clock information may be encoded onto a data signal, by ensuring that a minimum number of signal transitions occur in a given number of data bits.

In an embodiment of the present invention, any multiplexed combination of control, address information and data intended for memory devices coupled to configurable width buffer device 391 is received via configurable width interface 590, which may, for example extract the address and control information from the data. For example, control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596. The data may then be provided to configurable serialization circuit 591. Request & address logic 540 generates one or more output enable (OE) signals to enable bypass circuits as described below.

Interfaces 520a and 520b include programmable features in embodiments of the present invention. A number of control lines between configurable width buffer device 391 and memory devices are programmable in order to accommodate different numbers of memory devices on a configurable width buffered module 395 in an embodiment of the present invention. Thus, more dedicated control lines are available with increased memory device memory module configuration. Using programmable dedicated control lines avoids any possible load issues that may occur when using a bus to transfer control signals between memory devices and a configurable width buffer device 391. In another embodiment of the present invention, an additional complement data strobe signal for each byte of each memory device may be programmed at interfaces 520a and 520b to accommodate different types of memory devices on a configurable width memory module 395, such as legacy memory devices that require such a signal. In still a further embodiment of the present invention, interfaces 520a and 520b are programmable to access different memory device widths. For example, interfaces 520a and 520b may be programmed to connect to 16 "x4" width memory devices, 8 "x8" width memory devices or 4 "x16" width memory devices.

Configurable width buffer device 391 has a maximum buffer device interface width equivalent to the number of data pins or contacts provided on the buffer device's package or interface 596. In an embodiment of the present invention, interface 596 includes 128 pins of which selectable subsets of 1, 2, 4, 8, 16, 32, 64 or all 128 pins (W_{DP}) may be used in order to configure the width of configurable width buffer device 391. Configurable width buffer device 391 also has a maximum memory device access width defined as the largest number of bits that can be accessed in a single memory device transfer operation to or from configurable width buffer device 391. Using the techniques described herein, the configurable width buffer device 391 may be programmed or

configured to operate at interface widths and memory device access widths other than these maximum values.

In an embodiment illustrated by FIGURE 5B, a serialization ratio is defined as follows:

$$R_S = W_A : W_{DP}$$

Where:

R_S = Serialization Ratio

W_A = Memory Device Access Width

W_{DP} = Configured Buffer Device Interface Width

For example, if the memory device access width W_A is 128-bits and the configurable width buffer device interface width W_{DP} is 16-bits, the serialization ratio is 8:1. For the described embodiment, the serialization ratio remains constant for all configured buffer device interface widths, so that the memory device access width scales proportionally with configured buffer device interface width. In other embodiments, the serialization ratio could vary as the configured buffer device interface width varies. In other embodiments, the serialization ratio may change and the memory device access width may remain constant.

Configurable serialization circuit 591 performs serialization and deserialization functions depending upon the desired serialization ratio as defined above. As the memory device access width is reduced from its maximum value, memory device access granularity (measured in quanta of data) is commensurately reduced, and an access interleaving or multiplexing scheme may be employed to ensure that all storage locations within memory devices 360 can be accessed. The number of signal lines of channels 370 may be increased or decreased as the memory device access width changes. Channels 370 (FIGURE 3C)

may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction. In addition, the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio. Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device 391.

In an embodiment of the present invention, a serialization ratio SR between a primary channel and secondary channels is defined below. In an embodiment of the present invention, communications between primary (e.g. link or bus) and secondary channels (e.g. channel 370 having a plurality of signal lines) have matched bandwidth (i.e. no compression, coding/ECC overhead, or caching).

$$SR = BW_P : BW_S$$

where:

BW_P = bandwidth of primary channel (bits / sec / signal line)
BW_S = bandwidth of secondary channel (bits / sec / signal line)

The minimum number of secondary channel signal lines required to participate per transaction between primary and secondary channels is:

$$W_{DPT,S} = W_{DP,P} * SR$$

where:

$W_{DP,P}$ = programmed data path width for primary channel
$W_{DP,S}$ = total data path width for secondary channel

$W_{DPT,S}$ = minimum number of secondary channel signal lines required to participate in each transaction

If the total number of secondary channel signal lines per configurable width buffer device 391, $W_{DP,S}$ is greater than the minimum number required per transaction, $W_{DPT,S}$, then configurable width buffer device 391 may employ a configurable datapath router within interface 590 to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

Operations circuit 572 (similarly, as described above) is included in configurable width buffer device 391 in an embodiment of the present invention. Operations circuit 572 includes storage circuit to store information used by the system in which the configurable width buffer device 391 is situated in, for example, to perform configuration operations. Alternatively the information may be stored in a serial presence detect device (SPD). Alternatively, the information may be stored in a number of different physical locations, for example, in a register within a memory controller or a separate integrated circuit on a system motherboard. Operations circuit 572 may store information representing a possible number of configurations of configurable width

buffer device 391 and/or configurable width buffered module 395 in embodiments of the present invention. Other information, which may be stored includes, but is not limited to memory device parameters, such as access times, precharge times, setup and hold times, allowable skew times, etc. The functionality of operations circuit 572 may be included on an SPD device for example, an EEPROM device, that is readable by the system, such as a controller, to determine the capabilities of a configurable width buffer device 391 and/or configurable width buffered module 395. A controller can then initialize or set system parameters, such as a data path or interface width, based on the values stored in the SPD device by generating control signals to a control terminal of configurable width buffered module 395. For example, the SPD device may indicate to a controller that configurable width buffer device 391 has a maximum width of 64 as opposed to a maximum width of 128. In an alternate embodiment of the present invention, the SPD device stores a number of serialization ratios, for example, which may be programmed into a register, located on configurable width buffer device 391.

State storage 576 may store a value that is repeatedly programmable or changeable to indicate different buffer device interface widths. The value stored in state storage 576 may be decoded to establish the desired configuration of configurable width interface 590. In addition, state storage may store a plurality of values, for example, a first value that represents the desired width of configurable width interface 590, and a second value that represents the desired width of one or more of interfaces 520a and 520b.

State storage may be programmed upon initialization by a controller device that communicates, to the configurable width buffer device, a value, which corresponds to the width of controller. The configurable width buffer device 391 may also automatically detect what

the width of the interface of the controller device is upon power-up and set it's own value in state storage 576 accordingly.

In an embodiment of the present invention as illustrated by FIGURE 5B, state storage 576 is a programmable register comprising two programmable memory cells, latches, or other mechanisms for storing state information. Within the two cells, two bits are stored. The two bits can represent four different values, through different combinations of bit values (Ex: 00 = x1, 01 = x2, 10 = x4, 11 = x8). The different stored values correspond to different programmed buffer device widths. In an embodiment of the present invention, state storage 576 outputs to request & address logic 540 and configurable width interface 590. In FIGURE 5B, a state storage 576 is fabricated within each of configurable width buffer device 391. However, state storage 576 can alternatively be located in a number of different physical locations. For example, stage storage 576 might be a register within a memory controller or on a system motherboard. If the storage register is external to configurable width buffer device 391, the width selection information is communicated to configurable width buffer device 391 via electrical signals propagated through module connector 390. In an alternate embodiment of the present invention, a controller transfers width selection information by way of control signals to a control terminal of configurable width buffer device 391.

Various types of state storage are possible. In the described embodiment, the state storage takes the form of a width selection register or latch. This type of state can be easily changed via software during system operation, allowing a high degree of flexibility, and making configuration operations that are transparent to the end user. However, other types of state storage are possible, including but not limited to manual jumper or switch settings and module presence detection or type detection mechanisms. The latter class of mechanisms may employ

pull-up or pull-down resistor networks tied to a particular logic level (high or low), which may change state when a module is added or removed from the system.

State storage 576 can be repeatedly programmed and changed during operation of configurable width buffer device 391 to indicate different interface widths. Changing the value or values of state storage 576 changes the interface width of configurable width buffer device 391; even after configurable width buffer device 391 has already been used for a particular width. In general, there is no need to power-down or reset configurable width buffer device 391 when switching between different interface widths, although this may be required due to other factors.

There are many possible ways to implement a state storage 576. Commonly, a register is defined as a state storage 576 that receives a data input and one or more control inputs. The control inputs determine when the storage node within the register will sample the data input. Some time after the register has sampled the input data, which data will appear on the output of the register.

The term register may apply either to a single-bit-wide register or multi-bit-wide register. In general, the number of bits in the width selection register is a function of the number of possible widths supported by the memory device, although there are many possible ways to encode this information.

FIGURE 5C illustrates another embodiment of configurable width interface 590 shown in FIGURE 5B. FIGURE 5C illustrates a multiplexer/demultiplexer circuit 597, for example that may be disposed in configurable serialization circuit 591 (FIGURE 5B) to perform multiplexing/demultiplexing functions. For the embodiment illustrated by FIGURE 5C, the serialization ratio is 1:1. Serialization ratios greater than 1:1 are possible with the addition of serial-to-parallel (e.g., during

write operations, for data intended to be written to the memory devices) and parallel-to-serial (e.g., during read operations, for data read from the memory device to be provided to the controller device) conversion circuits.

Multiplexer/demultiplexer circuit 597 includes four pairs of read and write data line pairs 594a-d coupled, by way of configurable width buffer device 391, to respective memory devices 360. In an alternate embodiment of the present invention, data line pairs 594a-d are coupled to a memory array in a memory device 360a by way of configurable width buffer device 391.

Generally, multiplexer/demultiplexer circuit 597 contains multiplexing logic and demultiplexing logic. The multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations. The multiplexing logic and demultiplexing logic are designed to allow one, two, or four (0-3) buffer device connections or pins in interface 596 to be routed to memory devices, and in particular individual memory cells.

In the one-bit wide configuration, buffer device data connection 0 can be routed to/from any of the four data line pairs 594a-d, which may be coupled to respective memory devices or memory cells in a memory device. In the 2-bit wide configuration, buffer device data connections 0 and 1 can be routed to/from data line pairs 594a-b or 594c-d, respectively. In the 4-bit wide configuration, buffer device data connections 0, 1, 2, and 3 route straight through to/from data line pairs 594a-d, respectively.

Likewise, further data paths may be constructed to couple greater than four configurable width buffer device 391 data connections in an embodiment of the present invention.

Multiplexer/demultiplexer circuit 597 includes input and output latches 597f-m, two for each configurable width buffer device data

connection in interface 596. Multiplexer/demultiplexer circuit 597 also comprises five multiplexers 597a-e. Multiplexers 597a-d are two-input multiplexers controlled by a single control input. Multiplexer 597e is a four input multiplexer controlled by two control inputs.

Multiplexer/demultiplexer circuit 597 is configured to use two write control signals W_A and W_B, and two read control signals R_A and R_B. These signals control multiplexers 597a-e. They are based on the selected data path width and bits of the requested memory address or transfer phase (see FIGURE 5D, described below). State storage 576 (FIGURE 5B) produces these signals in response to the programmed data width, whether the operation is a read or write operation, and appropriate addressing information.

FIGURE 5D shows the control values used for data path widths of one, two, and four. FIGURE 5D also indicates which of interface 596 connections are used for each data width.

When a width of one is selected during a read operation, the circuit allows data from any one of the four data line pairs 594a-d (in particular, the read line) to be presented at interface 596 connection 0. Control inputs R_A and R_B determine which of data bit signals will be presented at any given time. R_A and R_B are set (at this data width) to equal the least significant two bits (A_1, A_0) of the memory address corresponding to the current read operation.

When a width of one is selected during a write operation, the circuit accepts the data bit signal from interface 596 data connection 0 and routes it to all of the four data line pairs 594a-d (in particular, the write lines), simultaneously. Control inputs W_A and W_B are both set to a logical value of one to produce this routing.

When a width of two is selected during a read operation, the circuit allows any two of the four data bit signals associated with data line pairs 594a-d (in particular, the read lines) to be present at interface

596 connections 0 and 1. To obtain this result, R_A is set to 0, and R_B is equal to the lower bit (A_0) of the memory address corresponding to the current read operation. R_B determines which of two pairs of data bit signals (594a and 594b or 594c and 594d) are presented at interface 596 connections 0 and 1 during any given read operation.

When a width of two is selected during a write operation, the circuit accepts the data bit signals from interface 596 connections 0 and 1, and routes them either to data line pairs 594a and 594b (in particular, write lines), or to data line pairs 594c and 594d (in particular, write lines). W_A and W_B are set to 0 and 1, respectively, to obtain this result.

When a width of four is selected by setting all of the control inputs (R_A, R_B, W_A, and W_B) to 0, read and write data signals are passed directly between data line pairs 594a-d and corresponding interface 596 data connections 3-0.

The circuit of FIGURE 5C is just one example out of many possible embodiments of the present invention. At the expense of increased logic and wiring complexity, an embodiment of the present invention uses a more elaborate crossbar-type scheme that could potentially route any single data bit signal to any data pair line or to any of the interface 596 data connections. In still further embodiments of the present invention, the number and width of memory devices, number of buffer device data connections per buffer device, serialization ratios, and width of data paths may be varied, singly or in combination, from the exemplary numbers and widths provided in describing particular embodiments of the present invention.

In embodiments of the present invention, a master device, such as memory controller 110, includes configurable width interface 590, as described herein, to access at least one configurable width buffered module.

In embodiments of the present invention, interfaces 520a and 520b include multiplexer/demultiplexer circuit 597, also known as a type of partial crossbar circuit, for transferring signals between configurable width buffer device 391 and memory devices on configurable width buffered module 395. In an alternate embodiment of the present invention, a full crossbar circuit is used.

FIGURE 5E illustrates a configurable width buffered module 650 including a configurable width buffer device 651 coupled to memory devices 652 and 653 in an embodiment of the present invention. Memory devices 652 and 653 include memory cells 652a-b and 653a-b, respectively.

Channels DQ1 and DQ2 are coupled to configurable width buffered module 650 at a connector interface that includes at least a first contact and a second contact, and in particular to configurable width buffer device 651. Channels DQ1 and DQ2 include a plurality of signal lines for providing signals to and from configurable width buffered module 650. In an alternate embodiment of the present invention, a single or more channels are coupled to configurable width buffered module 650. In an embodiment of the present invention, channels DQ1 and DQ2 are coupled to a master device, such as a controller.

Channels DQ3 and DQ4 are also coupled to configurable width buffer device 651 and are positioned in configurable width buffered module 650 in an embodiment of the present invention. Channels DQ3 and DQ4 couple configurable width buffer device 651 to memory devices 652 and 653. Channels DQ3 and DQ4 include a plurality of signal lines for providing signals to and from memory devices 652 and 653, and in particular memory cells 652a-b and 653a-b. In an alternate embodiment of the present invention, a single or more channels are coupled to memory devices 652 and 653. In alternate embodiments of the present

invention, more or less memory devices are included in configurable width buffered module 650.

Configurable width buffer device 651 includes a plurality of transceiver circuits 651a-f capable of transmitting and receiving signals on channels DQ1-4. Each transceiver circuit 651a-f includes a transmitter circuit and a receiver circuit in an embodiment of the present invention. Transceiver 651a is coupled to channel DQ1 and provides signals on channel DQ3. Transceiver 651b is coupled to channel DQ3 and provides signals on channel DQ1. Transceiver 651c is coupled to channel DQ1 and provides signals on channel DQ4. Transceiver 651d is coupled to channel DQ4 and provides signals on channel DQ1. Transceiver 651e is coupled to channel DQ2 and provides signals on channel DQ4. Transceiver 651f is coupled to channel DQ4 and provides signals on channel DQ2. Both memory cells 652a and 652b are not accessed via channel DQ1 during a single access operation in an embodiment of the present invention.

In an embodiment of the present invention, configurable width buffered module 650 operates in at least two modes of operation. In a first mode of operation, memory cell 652a and memory cell 652b in memory device 652 are accessible from a first contact coupled to channel DQ1. In particular, signals are transferred between channel DQ1 and memory cell 652a by using transceiver 651a, transceiver 651b and channel DQ3. Transceiver 651a is used to write data signals to memory cell 652a and transceiver 651b is used to read data signals from memory cell 652a. Signals are transferred between channel DQ1 and memory cell 652b using transceiver 651c, transceiver 651d and channel DQ4. Transceiver 651c is used to write data signals to memory cell 652b and transceiver 651d is used to read data signals from memory cell 652b.

In a second mode of operation, memory cell 652a and memory cell 652b in memory device 652 are accessible from a first contact coupled to channel DQ1 and a second contact coupled to channel DQ2, respectively. In particular, signals are transferred between channel DQ1 and memory cell 652a by using transceiver 651a, transceiver 651b and channel DQ3. Transceiver 651a is used to write data signals to memory cell 652a and transceiver 651b is used to read data signals from memory cell 652a. Signals are transferred between channel DQ2 and memory cell 652b using transceiver 651e, transceiver 651f and channel DQ4. Transceiver 651e is used to write data signals to memory cell 652b and transceiver 651f is used to read data signals from memory cell 652b.In another embodiment of the present invention, memory device 653 is also coupled to channels DQ3 and DQ4 and includes memory cells 653a and 653b that are likewise accessible in at the two modes of operation described above.

FIGURE 5F illustrates a configurable width buffered module 660 where channel DQ3 is coupled to memory cell 652a in memory device 652 and channel DQ4 is coupled to memory cell 653b in memory device 653. Like referenced components shown in FIGURE 5F operate and are described above in regard to FIGURE 5E. In this embodiment of the present invention, Configurable width buffer device 651 accesses two memory devices that do not share channels DQ3 and DQ4. There are two modes of operation in an embodiment of the present invention. In a first mode of operation, memory cell 652a is accessed via channel DQ1 and memory cell 653b is accessed via channel DQ2. In a second mode of operation, memory cell 652a is accessed via channel DQ1 and memory cell 653b is accessed via channel DQ1. Both memory cells 652a and 653b are not accessed via channel DQ1 during a single access operation in an embodiment of the present invention. FIGURE 5F conceptually illustrates accessing memory cells by a configurable

width buffer device 651. In order to clearly describe the present invention, one of ordinary skill in the art would appreciate that may components used in a buffer device and memory devices are not shown, such as memory device access logic and transceivers as well as configurable width buffer device 651 logic.

According to embodiments of the present invention, subsets of available memory devices on configurable width buffered module 395 are activated or powered-on during various modes of operation. Thus, configurable width buffered module 395 is able to achieve power savings by only powering particular memory devices.

With reference to FIGURES 6A, and 6B, block diagrams of a memory system according to embodiments of the present invention are illustrated. Memory system 600 includes modules 400a and 400b, controller 610, and populated primary point-to-point links 620a and 620b. Unpopulated primary point-to-point links 630 are populated by coupling additional modules (not shown) thereto. The additional modules may be provided to upgrade memory system 600. Connectors may be disposed at an end of each primary point-to-point link to allow insertion or removal of the additional modules. Modules 400a and 400b may also be provided with a connector or may be fixedly disposed (i.e., soldered) in memory system 600. Although only two populated primary point-to-point links are shown in FIGURE 6A, any number of primary point-to-point links may be disposed in memory system 600, for example, three primary point-to-point links 400a-400c, as shown in FIGURE 6B.

With reference to FIGURE 7 and FIGURE 4B, a block diagram of a memory system employing a buffered quad-channel module according to an embodiment of the present invention is illustrated. Memory systems 700 incorporate quad-channel modules 450a-450d, each coupled via point-to-point links 620a-620d respectively.

Referring to FIGURE 4B, buffer device 405 may operate in a bandwidth concentrator approach. By employing quad channels 415a-415d on each of modules 450a-450d, bandwidth in each module may be concentrated from all quad channels 415a-415d on each module to corresponding point-to-point links 620a-620d. In this embodiment, throughput on each of point-to-point links 620a-620d is concentrated to four times the throughput achieved on each of quad channels 415a-415d. Here, each of channels 415a-415d transfers information between one or more respective memory devices on each channel and buffer device 405 simultaneously.

Any number of channels 415a-415d, for example; two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations. Different applications may have different processing throughput requirements. In addition, the throughput requirements of a particular application may dynamically change during processing. Typically, more power is consumed as throughput is increased as power consumption relates in proportion to operation frequency. The amount of throughput in a system may be implemented on a dynamic throughput requirement basis to save on power consumption. In this embodiment, memory system 700 may concentrate bandwidth as it is required while in operation. For example, memory system 700 may employ only one of channels 415a-415d and match throughput to the corresponding point-to-point link. As bandwidth requirements increase, memory system 700 may dynamically activate more of channels 415a-415d and increase the throughput on the point-to-point link along with the number of channels accordingly to meet the bandwidth requirements for a given operation.

With reference to FIGURE 8A, a block diagram of a large capacity memory system according to an embodiment of the present invention is

illustrated. Memory system 800 includes modules 470a-470p, coupled to controller 610 via repeaters 810a-810d, primary links 820a-820d, and repeater links 830a-830p. Primary links 820a-820d provide a point-to-point link between controller 610 and a respective repeater 810a-810d. In an embodiment of the present invention, each of repeaters 810a-810d decode packets transmitted from controller 610 which are then directed over one or more, or none of repeater links 830a-d, depending on the type of access configured. Each repeater link 830a-830p may utilize a point-to-point link configuration. By incorporating, repeated links 830a-830p and repeaters 810a-810d, a larger number of modules may be accessed and a larger capacity memory system may be realized. Such a large capacity may be suited in a computer server system.

FIGURE 8B illustrates another approach utilized to expand the memory capacity of a memory system in accordance to yet another embodiment. Here, a plurality of buffered modules 850a-850d are "daisy chained" via a plurality of point-to-point links 860a-860d to increase the overall memory capacity. Connection points of each point-to-point link are connected to two adjacent buffered modules. Each of buffered modules 850a-850d transceive signals between adjacent point-to-point links 860a-860d. Point-to-point link 860a may be coupled to a controller or another buffered module. Additional point-to-point links may be coupled to a buffer device in a tree configuration approach. For example, three point-to-point links 870a-870c each having a single end connected to one buffer device 880 may be employed as shown in FIGURE 8C.

Other point-to-point topologies include a "ring" in which a plurality of buffered modules are connected in a ring by a respective plurality of point-to-point links and a "star" where a plurality of memory modules are connected to a center memory module by a respective plurality of point-to-point links.

In various embodiment of the present invention, point-to-point links are unidirectional, bidirectional or a combination thereof. A unidirectional link transfers a signal in a single direction to or from a connection point. A bidirectional link transfers signals both to and from a connection point.

FIGURES 9-20 illustrate a memory system, or portions of a memory system, for allowing an upgrade option for memory modules. In particular, FIGURES 9-20 illustrate a memory system including a buffered memory module having at least one bypass circuit that allows for memory module upgrades while reducing memory system delays in accessing information from the memory module upgrades.

Figure 9 illustrates a memory system 910 including a single buffered memory module having symmetrical bypass circuits (unpopulated or unfilled socket 905) and a memory system 920 including two buffered memory modules having symmetrical bypass circuits. Memory systems 910 and 920 include substrates 950 and 960, respectively, for positioning an interface, such as sockets 904 and 905 that may or may not be populated with buffered memory modules 900 and 901. The choice of populating sockets 904 and 905 with buffered memory modules 900 and 901 may be made at the time of manufacture, or after a memory system has been manufactured.

Memory modules 900 and 901 include a connector interface having contacts, such as pins A0, A1, B0 and B1 that are used to provide signals between memory modules 900 and 901 and sockets 904 and 905, respectively. Pins A0, A1, B0 and B1, respectively, represent one or more contacts or pins in embodiments of the present invention.

Data and/or control signals are transferred between buffered modules 900 and 901 by channels DQ0, DQ1, 911 and 912. In an alternate embodiment of the present invention, control and/or address signals are transferred on separate signal lines or channels. Channels

DQ0, DQ1, 911 and 912,respectively, include one or more signal lines in embodiments of the present invention. In an embodiment of the present invention, channels DQ0, DQ1, 911, 912 as well as other channels described herein, are unidirectional (information can travel in one direction) and/or bidirectional (information can travel in either direction). Channels DQ0 and DQ1 are coupled to a master device, such as memory controller 310 shown in FIGURE 3B, in an embodiment of the present invention. Channel DQ0 is also coupled to pin A0 of memory module 900 by way of socket 904. Channel DQ1 is also coupled to pin A1 of memory module 900 by way of socket 904. Similarly, pin B0 of memory module 900 is coupled to channel 912 and pin B1 of memory module 900 is coupled to channel 911. In memory system 920, memory module 901 has pins A0 and A1 that are also coupled to channels 911 and 912, respectively, by way of socket 905. Pins B0 and B1 of memory module 901 are not coupled to a channel in an embodiment of the present invention shown in FIGURE 9.

In an embodiment of the present invention, memory modules 900 and 901, singly or in combination, include a buffer device 930 having bypass circuits 934 and 935 as indicated by the expanded view of buffered memory module 900 shown in FIGURE 9. Bypass circuit 934 is coupled to pins A0 and B0; while bypass circuit 935 is coupled to pins A1 and B1. In an embodiment of the present invention, a bypass circuit, such as bypass circuit 935, includes a first transmitter ("trans") 935a for transmitting signals received on pin A1 to pin B1. Likewise, a bypass circuit also includes a second transmitter 935b for transmitting signals received on pin B1 to pin A1 and/or multiplexer/demultiplexer ("mux/demux") circuit 931.

In an embodiment of the present invention, transmitters 935a and 935b are enabled responsive to one or more OE signals. In an embodiment of the present invention, an OE signal is generated by

request & address logic 540 of configurable width buffer device 391, as shown in FIGURE 5B, responsive to address information on lines 595.

In an embodiment of the present invention, information transmitted by transmitters 935a and 935b is resynchronized using clock circuit 570a-b in configurable width buffer device 391 shown in FIGURE 5B. In an embodiment of the present invention, clock circuit 570a-b includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock (not shown). The clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronization clock signals for transmitters 935a and 935b having predetermined temporal relationships that allow for the resynchronization of information transferred between memory modules having bypass circuits. In particular, generated internal synchronization clock signals are used to receive or sample information provided to bypass circuits and drive or transmit information from bypass circuits.

Buffer device 930 also includes mux/demux circuit 931 for selectively connecting pins A0 and A1 to memory devices 933, in particular memory cells, by way of internal channel 932. Mux/demux circuit 931 corresponds to multiplexer/demultiplexer circuit 597 shown in FIGURE 5C in an embodiment of the present invention. Mux/demux circuit 931 performs transfers between timing slots on pins A0 and A1 and memory devices 933. In a write transfer embodiment of the present invention, mux/demux circuit 931 will receive information from pins A0 and A1, and will retransmit the information to the memory devices 933 where it is written into storage cells. In a read transfer embodiment of the present invention, mux/demux circuit 931 will receive information that is read from storage cells in memory devices 933, and will retransmit the information onto pins A0 and A1.

Bypass circuits 934 and 935 perform transfers between timing slots on pins A0 and A1 and timing slots on pins B0 and B1. In a write transfer embodiment of the present invention, bypass circuits 934 and 935 will receive information from pins A0 and A1, and will retransmit the information onto pins B0 and B1. In a read transfer embodiment of the present invention, mux/demux circuit 931 will receive information from pins B0 and B1, and will retransmit the information onto pins A0 and A1.

In an embodiment of the present invention, bypass circuits 934, 935 and mux/demux circuit 931 are used in configurable width buffer device 391 shown in FIGURE 5B.

A channel or signal line between master device pins, such as memory controller pins, and the pins A0/A1 of memory module 900 is known as a point-to-point wiring topology. This point-to-point topology has the principle benefit that the parasitic resistance, capacitance, and inductance elements in the controlled impedance path are minimized, maximizing signaling bandwidth.

The signaling bandwidth is kept high by the use of on-component termination elements, which provide a termination resistance that approximates the impedance value of the signal path or line.

One disadvantage of the point-to-point topology is that each signal path must use pins to enter and exit a memory module. So when bypass circuits 934 and 935 are included in buffer device 930, a delay in the signal path between entry and exit pins is created. This delay increases as memory modules are added to a memory system without using a buffer device with a bypass circuit. Each memory module sees the accumulated delay of all bypass circuits between it and the controller.

FIGURE 10A illustrates the use of address space when using a single memory module 900 and FIGURE 10B illustrates the use of address space when using two memory modules 900 and 901. When

memory module 900 is present, both channels DQ0 and DQ1 connect to memory module 900. When memory modules 900 and 901 are present, channels DQ0 and DQ1 connect to memory module 900 and also connect to memory module 901 using the A0/B0 and A1/B1 connection paths of memory module 900. The address spaces of the modules 900 and 901 can be stacked, with an access to a particular address location involving only the memory devices of either memory module 900 or module 901.

FIGURE 11 illustrates a memory system 1100 having four memory modules 1101-1104 coupled to sockets 1105-1108 positioned on substrate 1150. Socket 1105 is coupled to channels DQ0-3 and 1120. Socket 1106 is coupled to channels 1120 and 1121. Socket 1107 is coupled to channels 1121 and 1122. Socket 1108 is coupled to channels 1122. The cost of increasing the number of upgrade memory modules is that the signal path from a master device coupled to channels DQ0-3 to the furthest memory module 1104 includes more delay.

In an embodiment of the present invention, an upgradeable memory system includes four or more memory modules without creating more delay than is provided by system 920 shown in FIGURE 9. FIGURE 12A illustrates a memory module 1200 that enables the reduced signal path delay in memory systems having four or more memory modules. Memory module 1200 includes a buffer device 1210 with an asymmetrical bypass circuit 1212. In particular, buffer device 1210 includes mux/demux circuit 1211 that operates similar to mux/demux circuit 931 and a single bypass circuit 1212 coupled to pins A1 and B1. A difference between buffer device 1210 and 930 is that a bypass path is only provided between pins A1 and B1. There is no path between pins A0 and B0. In an embodiment of the present invention, there is not any pin B0.

FIGURES 12A-B also shows the address spaces for the one and two memory module cases with an asymmetrical bypass circuit. The address space for memory module 1200 is the same in memory module 900 shown in FIGURE 9. But in memory modules 1200 and 1201, the address spaces of the two memory modules are parallel rather than stacked. This means that when an address is accessed, memory devices 933 on memory module 1201 will be used for the transfer timing slots on the channel DQ1, and memory devices 933 on module 1200 will by used for the transfer timing slots on channel DQ0.

In embodiments of the present invention, some (or all) of the storage locations or cells of memory devices 933 in memory module 1200 or 1201 must be accessible through either channel DQ0 or DQ1, depending upon the number of memory modules present. Mux/demux circuit 1211 in buffer device 1210 manages this accessing of storage locations/cells.

In an embodiment of the present invention, information from memory devices 933 that are accessed through a shorter path (without the bypass circuit) must be delayed at some point so that the access paths are matched. This delay can be added at a master device, or could be added in the mux/demux circuit 1211 of buffer device 1210 in embodiments of the present invention.

When using only memory module 1200 shown in FIGURE 12A, an access to a particular address in memory devices 933 causes a transfer between timing slots on channels DQ0 and DQ1 and storage locations in all memory devices 933 on memory module 1200. Buffer device 1210 handles the multiplexing and demultiplexing needed for performing this transfer.

When using two memory modules 1200 and 1201(with equal-size storage capacity) shown in FIGURE 12B, an access to a particular address causes a transfer between timing slots on channel DQ0 and

storage locations in half of the memory devices 933 on memory module 1200, and between timing slots on channel DQ1 and storage locations in half of the memory devices 933 on memory module 1201. Buffer device 1210, and in particular mux/demux 1211, handles the multiplexing and demultiplexing needed for performing this transfer. Address and control signals from a master device will manage mux/demux 1211 in an embodiment of the present invention.

In an embodiment of the present invention, the address space of memory modules 1200 and 1201, respectively, is twice as large as the address space of memory module 900, because only half of the memory devices 933 are being accessed in each transaction.

When memory modules 1300 and 1301, as shown in FIGURE 13A-B do not have equal storage capacities, then the management of the address space becomes more complicated. For example, when the upgrade memory module 1301 has half the storage capacity of memory module 1300, the address space increases in size by a factor of 1.5. Accesses to address locations in the first 2/3 of the address space cause transfers from both memory modules 1300 and 1301.

When the upper 1/3 of the address space is accessed, only memory module 1300 is accessed in an embodiment of the present invention. There are at least two ways in which access can be performed in embodiments of the present invention.

First, the timing slots on channels DQ0 and DQ1 are both used by memory module 1300 in an embodiment of the present invention. A master device uses address and control signals to cause memory module 1300 to perform double-width transfers in this region of the address space as illustrated by FIGURE 14A.

Second, the timing slot on channel DQ0 is filled from memory module 1300, and the timing slot on channel DQ1 is not used. A master device knows that access to this part of the address space will be at half

the nominal bandwidth, and that the master device performs the appropriate multiplexing and demultiplexing to the master device's internal signal paths as shown by FIGURE 14B.

FIGURE 15 illustrates a buffered memory module 1500 that can be used in a memory system such that memory module upgrades can be extended to more than two memory modules with no additional bypass delay. Memory module 1500 includes memory devices 933 coupled to buffer device 1501 by channel 932. Buffer device 1501 includes mux/demux circuit 1502 similar to mux/demux circuit 1211 described above. Channels DQ0, DQ1, DQ2, and DQ3 are coupled to pins A0, A1, A2 and A3 which are coupled to bypass circuits 1503, 1504, 1505, and 1506, respectively. Pins B0, B1, B2 and B3 are also coupled to bypass circuits 1503, 1504, 1505, and 1506, respectively. Accordingly, information may selectively enter on pins A0-A3 and exit on pins B0-B1.

FIGURES 16A-D illustrate how a memory module, such as memory module 1500, is used in a four socket memory system, allowing one, two, three or four memory modules to be inserted, as shown by FIGURES 16A, 16B, 16C and 16D, respectively.

FIGURE 16A shows a one-module case 1600 where memory module 1601 is coupled to socket 1605 and sockets 1606-08 are unpopulated. Channels DQ0, DQ1, DQ2 and DQ3 are coupled to socket 1605 that has memory module 1601 inserted. Channel 1620 couples socket 1605 to socket 1606. Channel 1621 also couples socket 1605 to socket 1606. Channel 1622 couples socket 1605 to socket 1607 and channel 1623 couples socket 1605 to socket 1608. In a one-module case, an access causes a transfer between a timing slot on all four channels DQ0, DQ1, DQ2, and DQ3 and storage locations in memory module 1601 (the top socket 1605).

FIGURE 16B shows a two-module case 1630 where a memory module 1601 and 1602 is coupled to sockets 1605 and 1606, respectively, and sockets 1607-08 are unpopulated. An access causes a transfer between a timing slot on two channels DQ2 and DQ3 and storage locations in memory module 1601 (the top socket 1606) and between a timing slot on two channels DQ0 and DQ1 and storage locations in memory module 1602 (the second socket 1606 from the top).

FIGURE 16C shows a three-module case 1650 where a memory module 1601, 1602 and 1603 is coupled to sockets 1605, 1606 and 1607, respectively, and socket 1608 is unpopulated. An access causes a transfer between a timing slot on two channels DQ0 and DQ3 and storage locations in memory module 1601 (the top socket 1605), between a timing slot on channel DQ1 and storage locations in memory module 1602 (the second socket 1607 from the top), and between a timing slot on channel DQ2 and storage locations in memory module 1603 (the third socket 1607 from the top).

FIGURE 16D shows a four-module case 1670 where a memory module 1601, 1602, 1603 and 1604 is coupled to sockets 1605, 1606, 1607 and 1608, respectively. An access causes a transfer between a timing slot on channel DQ0 and storage locations in memory module 1601 (the top socket 1605), between a timing slot on one channel DQ1 and storage locations in memory module 1602 (the second socket 1606 from the top), between a timing slot on channel DQ2 and storage locations in memory module 1603 (the third socket 1607 from the top), and between a timing slot on channel DQ3 and storage locations in memory module 1604 (the fourth socket 1608 from the top).

Each memory system shown in FIGURES 16C-D has the same number of bypass delays in a particular signal path as in the two-module case shown in FIGURES 9 and 12B. However, the four-module case of

FIGURE 16D provides greater capacity and more upgrade opportunities. In alternate embodiments of the present invention, more than four modules are used in a memory system.

In various embodiments of the present invention, each memory system shown in FIGURES 16A-D will have many combinations of memory module storage capacity; i.e. all the memory modules have the same storage capacity, some memory modules have twice the storage capacity of other memory modules, some memory modules have four times the storage capacity of other memory modules, and so forth. In a preferred embodiment, a memory module with the largest storage capacity will be inserted into a higher socket position; i.e. towards the top of FIGURES 16-D. This will enable higher storage capacity memory modules the opportunity to use a larger number of channels.

For some memory module storage capacity combinations, it will be possible to provide uniform access bandwidth across the entire combined address space. For example, for a three-module case shown in FIGURE 16C, if the top memory module 1601 has twice the storage capacity of the other two memory modules 1602 and 1603, then uniform access bandwidth is available at any address location. This is because memory module 1601 has two timing slots (channels DQ0 and DQ3) for every single timing slot of memory module 1602 (channel DQ1) and memory module 1603 (channel DQ2).

For some of the storage capacity combinations, it will not be possible to provide uniform access bandwidth across the entire combined address space using the fixed channels shown in FIGURES 16A-D in an embodiment of the present invention. For example, for the three-module case 1650 shown in FIGURE 16C, if the top memory module 1601 has four times the storage capacity of the other two memory modules 1602 and 1603, then there will be a bandwidth mismatch when the upper half of memory module 1601 is accessed.

There are at least two ways in which access can be performed in embodiments of the present invention.

First, the timing slots on channels DQ0, DQ1, DQ2 and DQ3 are all filled from memory module 1601 when the address locations in the upper half of memory module 1601 are accessed. This requires that a master device use the address and control signals to cause memory module 1601 to perform double-width transfers in this region of the address space, similar to the two-module case shown in FIGURE 14A.

Second, the timing slots on channels DQ0 and DQ3 are filled from memory module 1601, and the timing slots on channel DQ1 and DQ2 are not used. In this embodiment of the present invention, a master device knows that access to this part of the address space will be at half the nominal bandwidth, and that it performs the appropriate multiplexing and demultiplexing to its internal signal paths. This embodiment is similar to the two-module case shown in FIGURE 14B.FIGURES 17-20 illustrates coupling external channels such as channels DQ0, DQ1, 1120 and 1121 to internal channels, such as channel 932, by a buffer device, such as buffer device 930, in a buffered memory module in embodiments of the present invention.

FIGURE 17 illustrates operation modes of a memory module 1700 that couples external signal lines data 1 and data 2 to internal signal line data A, internal signal line data B and external signal line data 3. In embodiments of the present invention, memory module 1700 corresponds to memory module 900 or 1200 described above. In embodiments of the present invention, signal lines data 1 and data 2 are included in a single external channel, such as channel DQ0, or respective external channels. In an embodiment of the present invention, external signal line data 3 is included in an external channel that is different than either external signal lines data 1 or data 2. In still a further embodiment of the present invention, an external signal line is

positioned on a memory module substrate between a buffer device and a memory module contact. Likewise, signal lines data A and data B are included in a single internal channel, such as channel 932, or respective internal channels in embodiments of the present invention.

Memory module 1700 is used as a memory module having a bypass circuit as described herein in an embodiment of the present invention. Memory module 1700 includes memory device 1702 including storage cells Sa and Sb that represents a memory device in memory devices 933 as described herein in an embodiment of the present invention. Likewise, buffer device 1701 represents a buffer device as described herein, such as buffer device 930 or 1210, in embodiments of the present invention.

In a first mode of operation at a first time, coupling circuit C1 in buffer device 1701 couples signal line data 1 to storage cell Sa by way of signal line data A and coupling circuit C2 couples signal line data 2 to storage cell Sb by way of signal line data B. In embodiments of the present invention, coupling circuits C1 and C2 include, respectively, a mux/demux circuit, bypass circuit and/or delay circuit, singly or in combination.

In a second mode of operation at a second time, coupling circuit C1 couples signal line data 1 to storage cell Sa by way of signal line data A and coupling circuit C2 couples signal line data 2 to signal line data 3.

In a third mode of operation at a third time, coupling circuit C1 couples signal line data 1 to storage cell Sb by way of signal line data B and coupling circuit C2 couples signal line data 2 to signal line data 3.

FIGURE 18 illustrates operation modes of a memory module 1800 that couples external signal lines data 1 and data 2 to internal signal lines data A, internal signal line data B, and external signal line data 3. In embodiments of the present invention, external signal lines

data 1 and data 2 are included in a single external channel, such as channel DQ0, or respective external channels. In an embodiment of the present invention, external signal line data 3 is included in an external channel that is different than either external signal lines data 1 or data 2. In still a further embodiment of the present invention, an external signal line is positioned on a memory module substrate between a buffer device and a memory module contact. Likewise, internal signal lines data A and data B are included in a single internal channel, such as channel 932, or respective internal channels in embodiments of the present invention. Memory module 1800 is used as a memory module having a bypass circuit as described herein in an embodiment of the present invention. Memory module 1800 includes a memory device 1802 including storage cell Sa and a memory device 1803 including storage cell Sb that represents respective memory devices in memory devices 933 as described herein in an embodiment of the present invention.

Memory module 1800 operates similar to memory module 1700, as described above, except that two memory devices 1802 and 1803 having respective storage cells Sa and Sb are accessed instead of storage cells from a single memory device.

FIGURE 19 illustrates operation modes of a memory module 1900 that couples external signal lines data 1 and data 2 to internal signal line data A, internal signal line data B and external signal line data 3. In embodiments of the present invention, signal lines data 1 and data 2 are included in a single external channel, such as channel DQ0, or respective external channels. In an embodiment of the present invention, external signal line data 3 is included in an external channel that is different than either external signal lines data 1 or data 2. In still a further embodiment of the present invention, an external signal line is positioned on a memory module substrate between a buffer device and a memory module contact. Likewise, signal lines data A and data B are

included in a single internal channel, such as channel 932, or respective internal channels in embodiments of the present invention. Memory module 1900 is used as a memory module having a bypass circuit as described herein in an embodiment of the present invention. Memory module 1900 includes memory device 1902 including storage cells Sa, Sb and Sc that represents a memory device in memory devices 933 as described herein in an embodiment of the present invention. Likewise, buffer device 1901 represents a buffer device, such as buffer device 930 or 1210, as described herein in embodiments of the present invention.

In a first mode of operation at a first time, coupling circuit C1 in buffer device 1901 couples signal line data 1 to storage cell Sa by way of signal line data A and coupling circuit C2 couples signal line data 2 to storage cell Sb by way of signal line data B.

In a second mode of operation at a second time, coupling circuit C1 couples signal line data 1 to storage cell Sc by way of signal line data A and coupling circuit C2 couples signal line data 2 to signal line data 3.

In a third mode of operation at a third time, coupling circuit C1 couples signal line data 1 to storage cell Sc by way of signal line data B and coupling circuit C2 couples signal line data 2 to signal line data 3.

FIGURE 20 illustrates operation modes of a memory module 2000 that couples external signal lines data 1 and data 2 to internal signal line data A, internal signal line data B and external signal line data 3. In embodiments of the present invention, signal lines data 1 and data 2 are included in a single external channel, such as channel DQ0, or respective external channels. In an embodiment of the present invention, external signal line data 3 is included in an external channel that is different than either external signal lines data 1 or data 2. In still a further embodiment of the present invention, an external signal line is positioned on a memory module substrate between a buffer device and a memory module contact. Likewise, signal lines data A and data B are

included in a single internal channel, such as channel 932, or respective internal channels in embodiments of the present invention. Memory module 2000 is used as a memory module having a bypass circuit as described herein in an embodiment of the present invention. Memory module 2000 includes a first memory device 2002 including storage cells Sa and Sc; and a second memory device 2003 including storage cells Sb and Sd that represent respective memory devices in memory devices 933 as described herein in an embodiment of the present invention. Likewise, buffer device 2001 represents a buffer device, such as buffer device 930 or 1210, as described herein in embodiments of the present invention.

In a first mode of operation at a first time, coupling circuit C1 in buffer device 2001 couples signal line data 1 to storage cell Sa by way of signal line data A and coupling circuit C2 couples signal line data 2 to storage cell Sc by way of signal line data B.

In a second mode of operation at a second time, coupling circuit C1 couples signal line data 1 to storage cell Sc by way of signal line data A and coupling circuit C2 couples signal line data 2 to signal line data 3.

In a third mode of operation at a third time, coupling circuit C1 couples signal line data 1 to storage cell Sd by way of signal line data B and coupling circuit C2 couples signal line data 2 to signal line data 3.

FIGURE 21 illustrates a top view of a memory module 2100 according to an embodiment of the present invention. Memory module 2100 includes a plurality of integrated circuit memory devices 2133 and a buffer device 2130 positioned on or about surface 2150a of substrate 2150. In an embodiment of the present invention, memory devices 2133a-c, 2133g-i and 2133j-r as well as buffer device 2130 is coupled directly to surface 2150a.

Memory module 2100 positions at least a portion of one integrated circuit memory device (i.e. memory devices 2133d-f) of

memory devices 2133 above or with buffer device 2130 in embodiments of the present invention. One or more memory devices 2133d-f are integrated, housed or included with buffer device 2130 in a common or single discrete package 2250, as shown in Fig. 22, in embodiments of the present invention. Package 2250 is coupled to surface 2150a by a connector interface 2251 including a plurality of contacts as described herein. One or more memory devices 2133d-f are located above, adjacent or below buffer device 2130 in package 2250 in embodiments of the present invention. One or more memory devices 2133d-f are located on a different die or semiconductor substrate than buffer device 2130 or on the same die, but both one or more memory devices 2133d-f and buffer device 2130 are included in package 2250, in embodiments of the present invention.

In an alternate embodiment of the present invention, one or more memory devices 2133d-f have their own respective packages and buffer device 2130 has a separate package. In this embodiment of the present invention, one or more discretely packaged memory devices 2133d-f are positioned on top or above and connected to a discretely packaged buffer device 2130.

This packaging architecture enables numerous benefits. First, when using a buffer device 2130 in a memory module, more integrated circuit memory devices may be included in a standard form factor memory module, such as a DIMM. Second, the present packaging architecture allows for a larger or enhanced buffer device 2130 while not reducing the number of memory devices in memory module 2100. If buffer device 2130 functionality and/or size increases, memory devices will not have to be removed to accommodate a large sized buffer device or one which requires additional interface contacts.

In embodiments of the present invention, buffer device 2130 is a configurable width buffer device, such as configurable width buffer device 391, as described herein.

In embodiments of the present invention, memory devices 2133 are discretely packaged DRAM devices or other types of memory devices, singly or in combination, described herein. In an alternate embodiment of the present invention, memory devices 2133d-f are not discretely packaged and are included in package 2250. FIGURE 22 illustrates a cross section view of memory module 2100 shown in FIGURE 21 having memory devices 2133 positioned on both surfaces of substrate 2150. In an embodiment of the present invention, memory devices 2133j-r are positioned on surface 2150b of substrate 2150, memory devices 2133a-c and 2133g-i are positioned on surface 2150a and memory devices 2133d-f are positioned on or with buffer device 2130 that is positioned on surface 2150a of substrate 2150. Accordingly, at least eighteen memory devices are positioned on memory module 2100.

In an alternate embodiment of the present invention, ten memory devices are positioned on surface 2150b, 6 memory devices are positioned on surface 2150a, and 2 memory devices are positioned on or with buffer device 2130 in a single package.

In embodiments of the present invention, substrate 2150 is a supporting material, printed circuit board, backplane link or wafer.

Memory module 2100 includes a connector interface 2180, such as a connector interface as described herein, for mating to an unpopulated socket in a memory system. In an embodiment of the present invention, connector interface 2180 includes a plurality of contacts, such as contact 2180a, for transferring signals. In embodiments of the present invention, a contact in connector interface

2180 is a conducting element, pin or solder ball. In an embodiment of the present invention, connector interface 2180 is a DIMM connector.

Connector interface 2180 is coupled to buffer device 2130 by channel 2170. Similarly, memory devices 2133a-c and 2133g-i are coupled to buffer device 2130 by channels 2140 and 2150, respectively, in an embodiment of the present invention. Memory devices 2133a-c and 2133g-i are coupled to buffer device 2130 by a single channel or more than two channels in alternate embodiments of the present invention. Memory devices 2133d-f are coupled to buffer device 2130 by channel 2160 in an embodiment of the present invention. Memory devices 2133d-f are coupled to buffer device 2130 in a SIP approach, as described above, in an alternate embodiment of the present invention. For example, memory devices 2133d-f are coupled to buffer device by at least one conducting interconnect. Memory devices 2133j-r are coupled to buffer device 2130 by channels 2140 and 2150. In an alternate embodiment of the present invention, memory devices 2133j-r are coupled to buffer device 2130 by a single channel or separate channels from channels 2140 and 2150.

While this invention has been described in conjunction with what is presently considered the most practical embodiments, the invention is not limited to the disclosed embodiments. In the contrary, the embodiments disclosed cover various modifications that are within the scope of the invention as set forth in the following claims.

What is claimed is:

1. A memory module comprising:

a connector interface which includes a first contact, a second contact and a third contact;

a first integrated circuit having memory including a first storage cell and a second storage cell; and

a buffer device coupled to the first integrated circuit and the connector interface, wherein the buffer device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first storage cell and the second storage cell are accessible from the first contact and the second contact, respectively; and

during the second mode of operation, at a first time the first storage cell is accessible from the first contact and the second contact is coupled to the third contact.

2. The memory module of claim 1, wherein:

during the second mode of operation, at a second time the second storage cell is accessible from the first contact and the second contact is coupled to the third contact.

3. The memory module of claim 1, wherein a delay is provided when accessing the first storage cell in the second mode of operation.

4. The memory module of claim 1, wherein during the first mode of operation,

a first coupling circuit couples a first external signal line coupled to the first contact to a first internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a second internal line coupled to the second storage cell.

5. The memory module of claim 1, wherein during the second mode of operation at the first time,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

6. The memory module of claim 2, wherein during the second mode of operation at the second time,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the second storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

7. The memory module of claim 1, wherein the buffer device further comprises a multiplexer/demultiplexer circuit coupled to the first and second contacts to access the first and second storage cells.

8. The memory module of claim 1, wherein the buffer device further comprises a bypass circuit capable to transfer information between the first and third contacts.

9. The memory module of claim 1, further comprising a fourth contact and wherein the buffer device includes:

a first bypass circuit capable to transfer information between the first and fourth contacts: and,

a second bypass circuit capable to transfer information between the second and third contacts.

10. The memory module of claim 9, further comprising a fifth, a sixth, a seventh and a eighth contact and wherein the buffer device includes:

a third bypass circuit capable to transfer information between the fifth and seventh contacts: and,

a fourth bypass circuit capable to transfer information between the sixth and seventh contacts.

11. The memory module of claim 1, wherein the first, second and third contacts are pins for mating to a socket.

12. The memory module of claim 1, wherein in a master device generates a control signal to the memory module to determine the mode of operation.

13. A memory module comprising:

a connector interface which includes a first contact, a second contact and a third contact;

a first integrated circuit having memory including a first storage cell;

a second integrated circuit memory having a second storage cell; and

a buffer device coupled to the first integrated circuit, the second integrated circuit and the connector interface, wherein the buffer device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first storage cell and the second storage cell are accessible from the first contact and the second contact, respectively; and

during the second mode of operation, at a first time the first storage cell is accessible from the first contact and the second contact is coupled to the third contact.

14. The memory module of claim 13, wherein:

during the second mode of operation, at a second time the second storage cell is accessible from the first contact and the second contact is coupled to the third contact.

15. The memory module of claim 13, wherein a delay is provided when accessing the first storage cell in the second mode of operation.

16. The memory module of claim 13, wherein during the first mode of operation,

a first coupling circuit couples a first external signal line coupled to the first contact to a first internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a second internal line coupled to the second storage cell.

17. The memory module of claim 13, wherein during the second mode of operation at the first time,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

18. The memory module of claim 14, wherein during the third mode of operation,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the second storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

19. The memory module of claim 13, wherein the buffer device further comprises a multiplexer/demultiplexer circuit coupled to the first and second contacts to access the first and second storage cells.

20. The memory module of claim 13, wherein the buffer device further comprises a bypass circuit capable to transfer information between the first and third contacts.

21. The memory module of claim 13, further comprising a fourth contact and wherein the buffer device includes:

a first bypass circuit capable to transfer information between the first and third contacts: and,

a second bypass circuit capable to transfer information between the second and fourth contacts.

22. The memory module of claim 21, further comprising a fifth, a sixth, a seventh and a eighth contact and wherein the buffer device includes:

a third bypass circuit capable to transfer information between the fifth and seventh contacts: and,

a fourth bypass circuit capable to transfer information between the sixth and seventh contacts.

23. The memory module of claim 13, wherein the first, second and third contacts are pins for mating to a socket.

24. The memory module of claim 13, wherein in a master device generates a control signal to the memory module to determine the mode of operation.

25. A memory module comprising:

a first integrated circuit having memory including a first storage cell, a second storage cell and a third storage cell;

a plurality of internal signal lines including a first and a second internal signal line coupled to the first integrated circuit;

a plurality of external signal lines including a first external signal line, a second external signal line, and a third external signal line; and,

a buffer device coupled to the plurality of internal signal lines and the plurality of external signal lines, wherein:

at a first time the first storage cell is accessible from the first external signal line coupled to the first internal signal line and the second storage cell is accessible from the second external signal line coupled to the second internal signal line; and

at a second time the third storage cell is accessible from the first external signal line coupled to the first internal signal line and the second external signal line is coupled to the third external signal line.

26. The memory module of claim 25, wherein :

at a third time, the third storage cell is accessible from the first external signal line coupled to the second internal signal line and the second external signal line is coupled to the third external signal line.

27. The memory module of claim 25, wherein a delay is provided when accessing the third storage cell in the second mode of operation.

28. The memory module of claim 25, wherein the buffer device further comprises a multiplexer/demultiplexer circuit coupled to the first and second external signal lines to access the first, second, and third storage cells.

29. The memory module of claim 25, wherein the buffer device further comprises a bypass circuit capable to transfer information between the first and third external signal lines.

30. The memory module of claim 25, wherein the first, second and third external signal lines are coupled to a socket for positioning the memory module.

31. The memory module of claim 25, wherein in a master device generates a control signal to the memory module to determine the mode of operation.

32. A memory module comprising:

a first integrated circuit having memory including a first storage cell and a second storage cell;

a second integrated circuit having memory including a third storage cell and a fourth storage cell;

a plurality of internal signal lines including a first and a second internal signal line coupled to the first and second integrated circuits;

a plurality of external signal lines including a first external signal line, a second external signal line, and a third external signal line; and,

a buffer device coupled to the plurality of internal signal lines and the plurality of external signal lines, wherein:

at a first time, the first storage cell is accessible from the first external signal line coupled to the first internal signal line and the second storage cell is accessible from the second external signal line coupled to the second internal signal line; and

at a second time, the second storage cell is accessible from the first external signal line coupled to the first internal signal line and the second external signal line is coupled to the third external signal line.

33. The memory module of claim 32, wherein:

at a third time, the fourth storage cell is accessible from the first external signal line coupled to the second internal signal line and the second external signal line is coupled to the third external signal line.

34. The memory module of claim 32, wherein a delay is provided when accessing the second storage cell in the second mode of operation.

35. The memory module of claim 32, wherein the buffer device further comprises a multiplexer/demultiplexer circuit coupled to the first and second external signal lines to access the first, second, third and fourth storage cells.

36. The memory module of claim 32, wherein the buffer device further comprises a bypass circuit capable to transfer information between the first and third external signal lines.

37. The memory module of claim 32, wherein the first, second and third external signal lines are coupled to a socket for positioning the memory module.

38. The memory module of claim 32, wherein in a master device generates a control signal to the memory module to determine the mode of operation.

39. A system comprising,

a first memory module coupled to a first external channel, a second external channel, and a third external channel, wherein information is transferred through the first memory module having a first delay;

a second memory module coupled to the second external channel; and,

a third memory module coupled to a third external channel, wherein information retrieved from the first, the second and the third

memory modules is provided on the first external channel having the first delay.

40. The system of claim 39, wherein the first memory module is coupled to a fourth external channel, further comprising:

a fourth memory module coupled to the fourth external channel, wherein information retrieved from the first, second, third and fourth memory modules is provided on the first external channel having the first delay.

41. The system of claim 39, wherein the first memory module includes a buffer device, coupled to the first and second external channels, having a multiplexer/demultiplexer circuit for accessing a plurality of storage cells in the first memory module.

42. The system of claim 41, wherein the buffer device comprises a first bypass circuit capable to transfer information between the first external channel and the second external channel.

43. The system of claim 42, wherein the buffer device further comprises a second bypass circuit capable to transfer information between the first external channel and the third external channel.

44. The system of claim 39, further comprising:

a master device, coupled to the first external channel, capable to generate a control signal to the first, second and third memory modules to determine the mode of operation of the first, second and third memory modules.

45. A buffer device, comprising:

a configurable width interface;

a multiplexer/demultiplexer circuit capable to access a first storage cell in a plurality of storage cells; and,

a first bypass circuit capable to transfer information through the buffer device from a first contact to a second contact.

46. The buffer device of claim 45, further comprising:

second bypass circuit capable to transfer information through the buffer device from a third contact to a fourth contact.

47. The buffer device of claim 46, further comprising:

a third bypass circuit capable to transfer information through the buffer device from a fifth contact to a sixth contact; and,

a fourth bypass circuit capable to transfer information through the buffer device from a seventh contact to a eighth contact.

48. A buffer device, comprising:

a multiplexer/demultiplexer circuit capable to access a first storage cell in a plurality of storage cells; and,

means for transferring information between the buffer device.

49. The buffer device of claim 48, wherein the buffer device is positioned in a memory module.

50. The buffer device of claim 49, wherein the memory module is positioned in a memory system having a controller.

51. A memory module, comprising:

a substrate having a first and second surface;

a first integrated circuit memory device positioned about the first surface;

a buffer device positioned about the first surface; and,

a second integrated circuit memory device positioned with the buffer device.

52. The memory module of claim 51, wherein the buffer device and second integrated circuit memory device is included in a package.

53. The memory module of claim 51, wherein the package includes a connector coupled to the first surface.

54. The memory module of claim 52, wherein the buffer device is positioned on a first die and the second integrated circuit memory device is positioned on a second die, wherein the first and second dies are included in the package.

55. The memory module of claim 51, wherein the second integrated circuit memory device is included in a first package and the buffer device is included in a second package, and wherein the second integrated circuit memory device is positioned above the buffer device coupled to the first surface.

56. The memory module of claim 51, wherein the memory module is a dual inline memory module.

57. The memory module of claim 51, wherein the first and second integrated circuits are dynamic random access memory ("DRAM") devices.

58. The memory module of claim 51, wherein the memory module includes 18 integrated circuit memory devices, wherein 9 integrated circuit memory devices are positioned on the second surface, 6 integrated circuit memory devices are positioned on the first surface, and 3 integrated circuit memory devices are positioned on the buffer device.

59. The memory module of claim 51, wherein the memory module includes 18 integrated circuit memory devices, wherein 10 integrated circuit memory devices are positioned on the second surface, 6 integrated circuit memory devices are positioned on the first surface, and 2 integrated circuit memory devices positioned with the buffer device, wherein the 2 integrated circuit memory devices and the buffer device are included in a package positioned on the first surface.

60. The memory module of claim 51, wherein the buffer device includes a configurable width interface.

61. The memory module of claim 51, wherein the buffer device includes a bypass circuit.

62. The memory module of claim 51, wherein the memory module is coupled to a master device.

63. A memory module, comprising:

a substrate;

a connector interface, coupled to the substrate, which includes a first contact, a second contact and a third contact;

a first integrated circuit having memory including a first storage cell and a second storage cell; and

a buffer device with the first integrated circuit positioned in a package coupled to the substrate, wherein the buffer device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first storage cell and the second storage cell are accessible from the first contact and the second contact, respectively; and

during the second mode of operation, at a first time the first storage cell is accessible from the first contact and the second contact is coupled to the third contact.

64. The memory module of claim 63, wherein:

during the second mode of operation, at a second time the second storage cell is accessible from the first contact and the second contact is coupled to the third contact.

65. The memory module of claim 63, wherein a delay is provided when accessing the first storage cell in the second mode of operation.

66. The memory module of claim 63, wherein during the first mode of operation,

a first coupling circuit couples a first external signal line coupled to the first contact to a first internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a second internal line coupled to the second storage cell.

67. The memory module of claim 63, wherein during the second mode of operation at the first time,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the first storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

68. The memory module of claim 63, wherein during the second mode of operation at the second time,

a first coupling circuit couples a first external signal line coupled to the first contact to an internal signal line coupled to the second storage cell; and,

a second coupling circuit couples a second external signal line coupled to the second contact to a third external line coupled to the third contact.

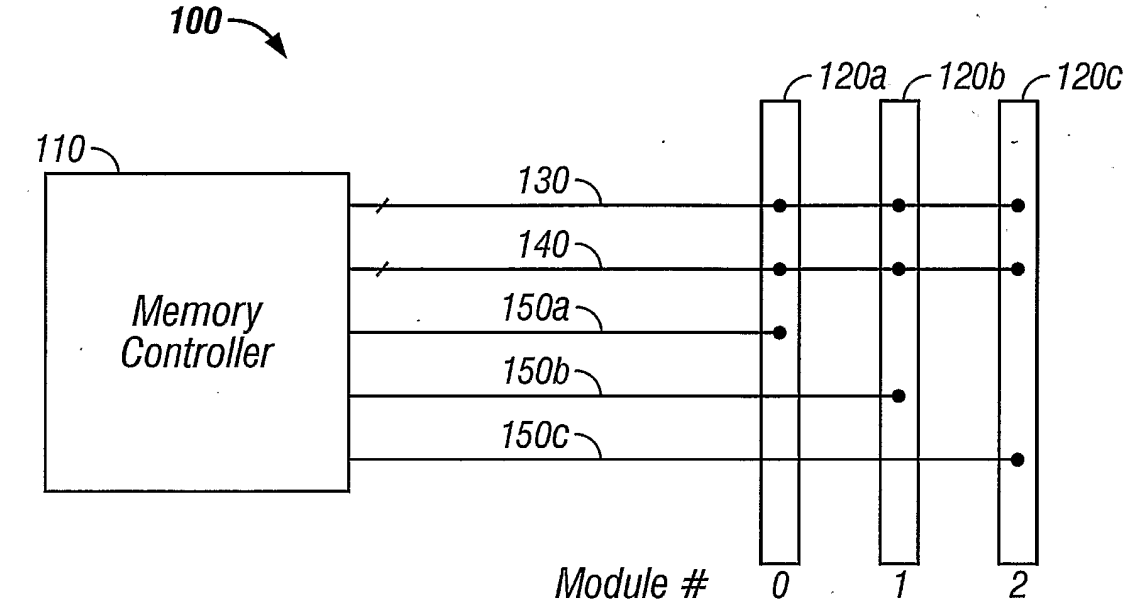


FIG. 1
(Prior Art)

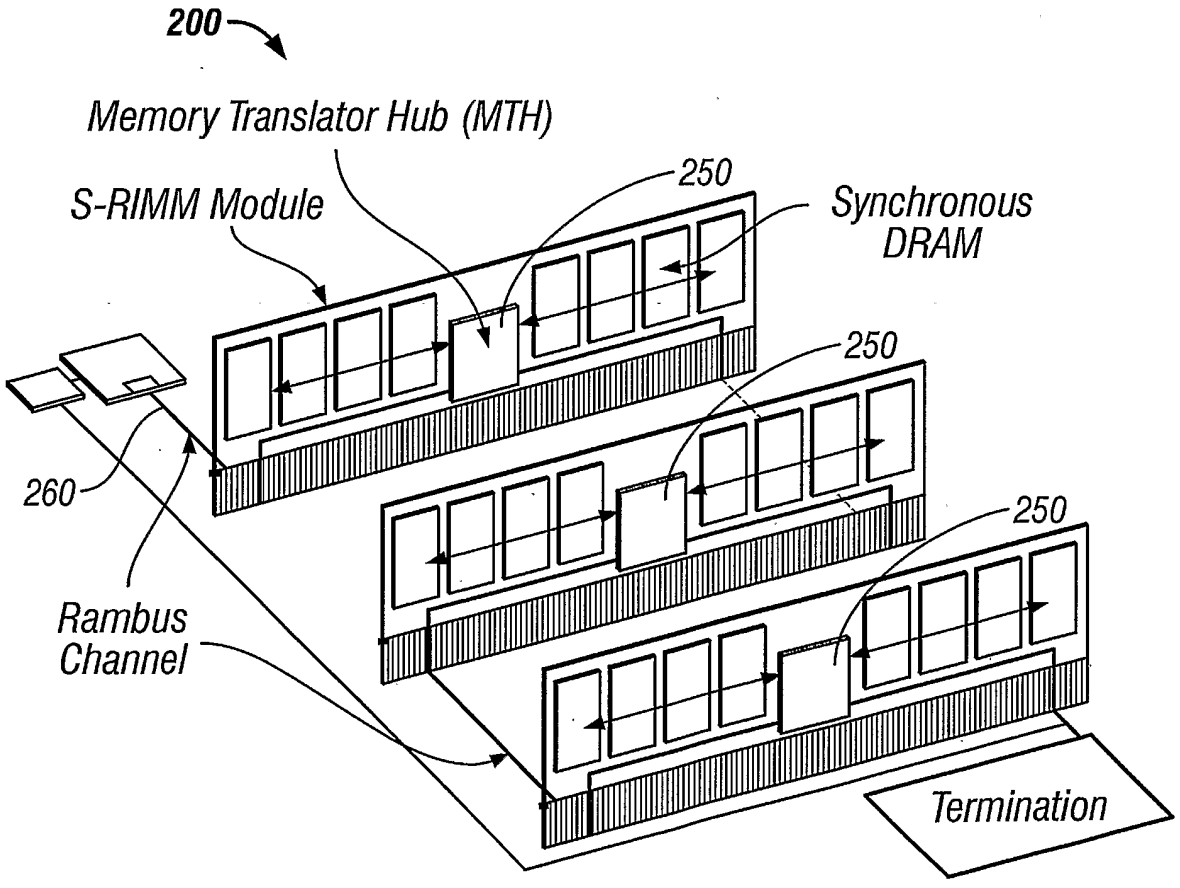


FIG. 2A
(Prior Art)

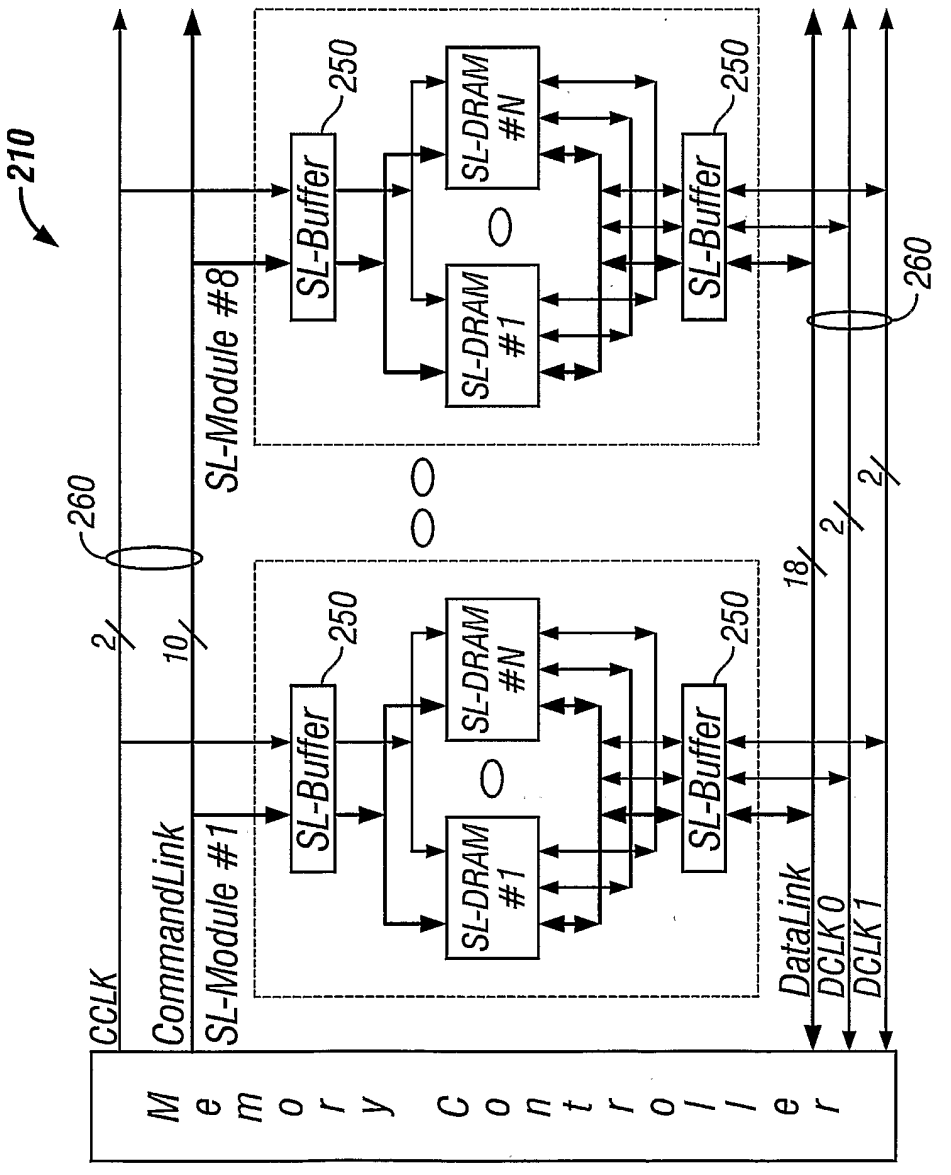


FIG. 2B
(Prior Art)

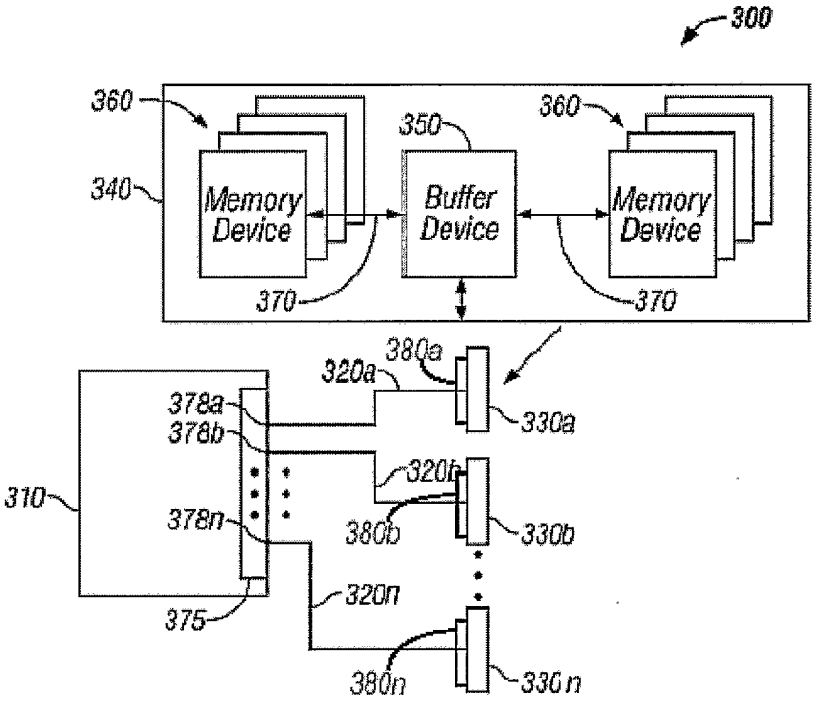

300
360
340
Memory Device
350
Buffer Device
360
Memory Device
370
370
380a
320a
330a
378a
378b
320b
310
378n
380b
330b
320n
375
380n
330n

FIG. 3A

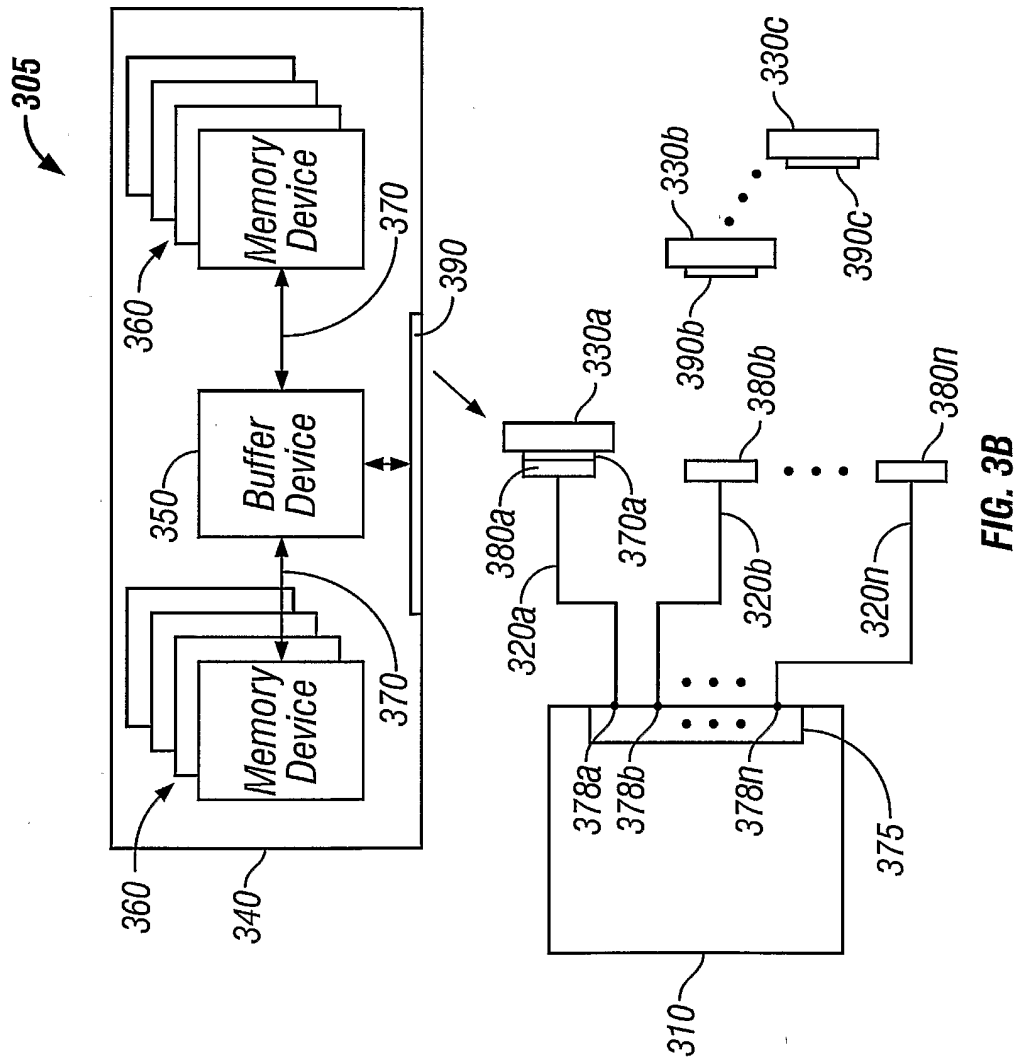

305
Memory Device
Buffer Device
Memory Device
360
370
390
350
370
360
340
330a
330b
330c
380a
380b
380n
370a
390b
390c
320a
320b
320n
378a
378b
378n
375
310

FIG. 3B

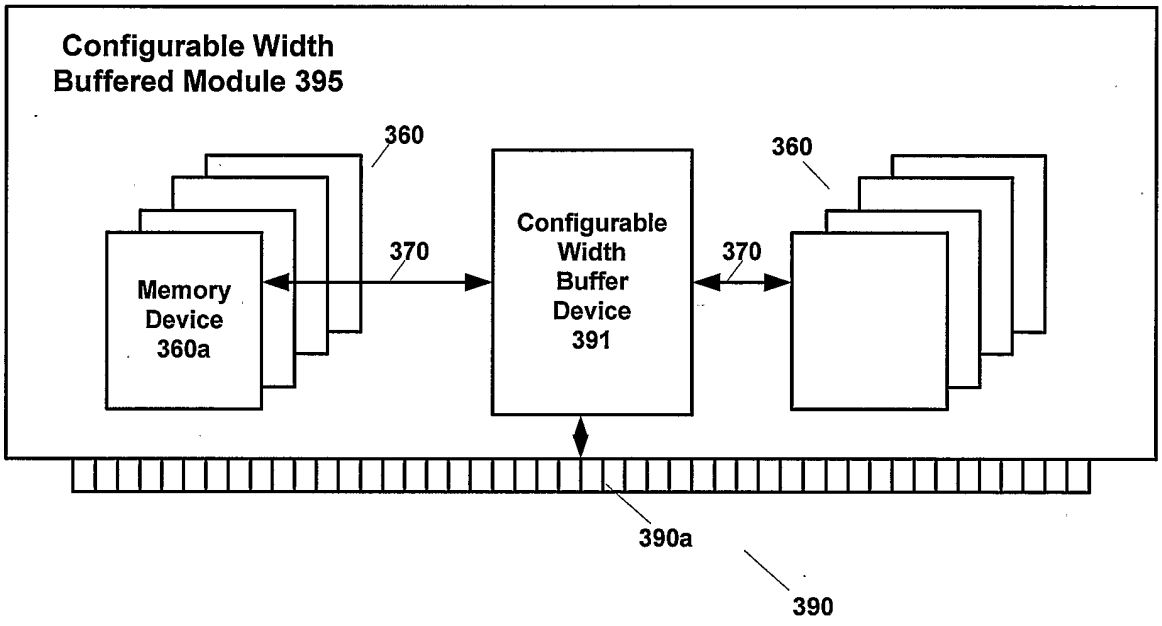

Configurable Width
Buffered Module 395
360
370
Memory
Device
360a
Configurable
Width
Buffer
Device
391
370
360
390a
390

Fig. 3C

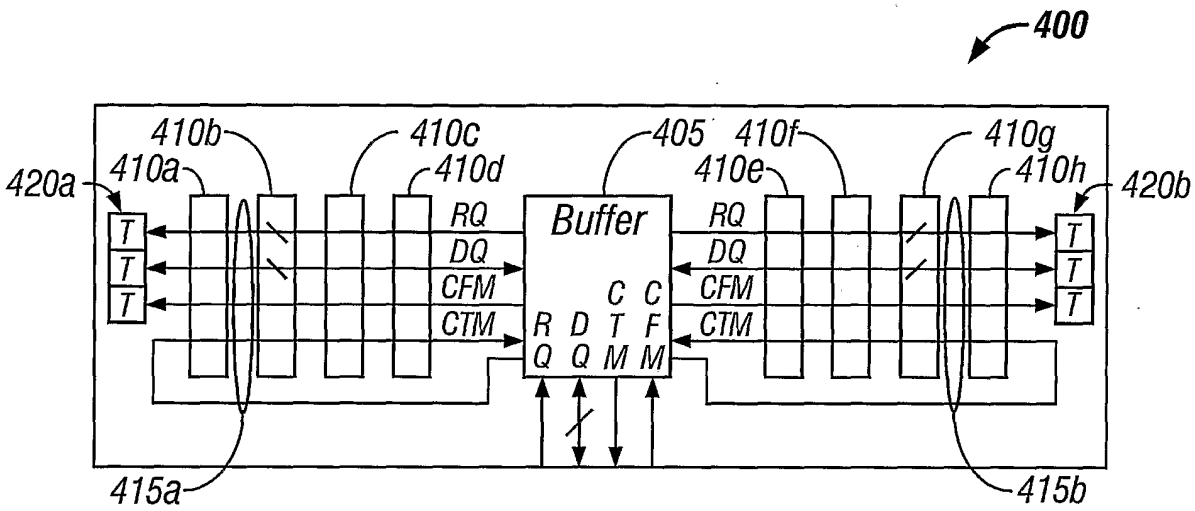

400
410b
410c
405
410f
410g
420a
410a
410d
410e
410h
420b
T
T
T
RQ
DQ
CFM
CTM
Buffer
C C
R D T F
Q Q M M
415a
415b

FIG. 4A

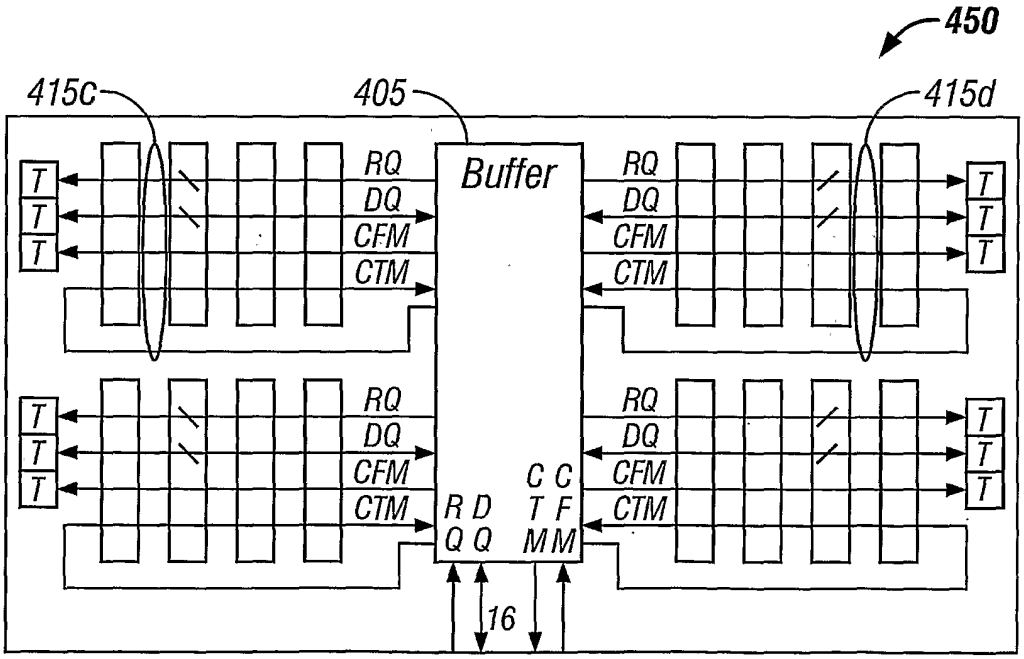

450
415c
405
415d
T
T
T
RQ
DQ
CFM
CTM
Buffer
C C
R D T F
Q Q M M
16

FIG. 4B

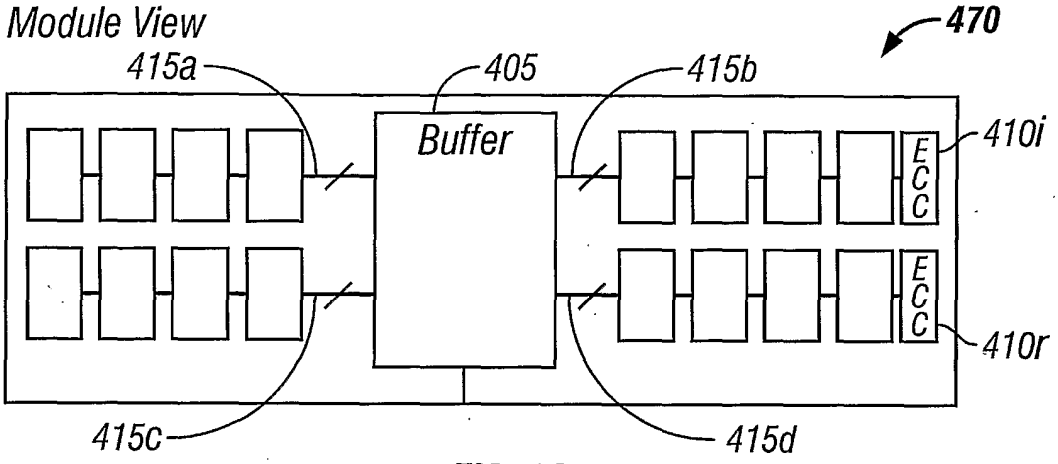

Module View
470
415a
405
415b
Buffer
410i
ECC
ECC
410r
415c
415d

FIG. 4C

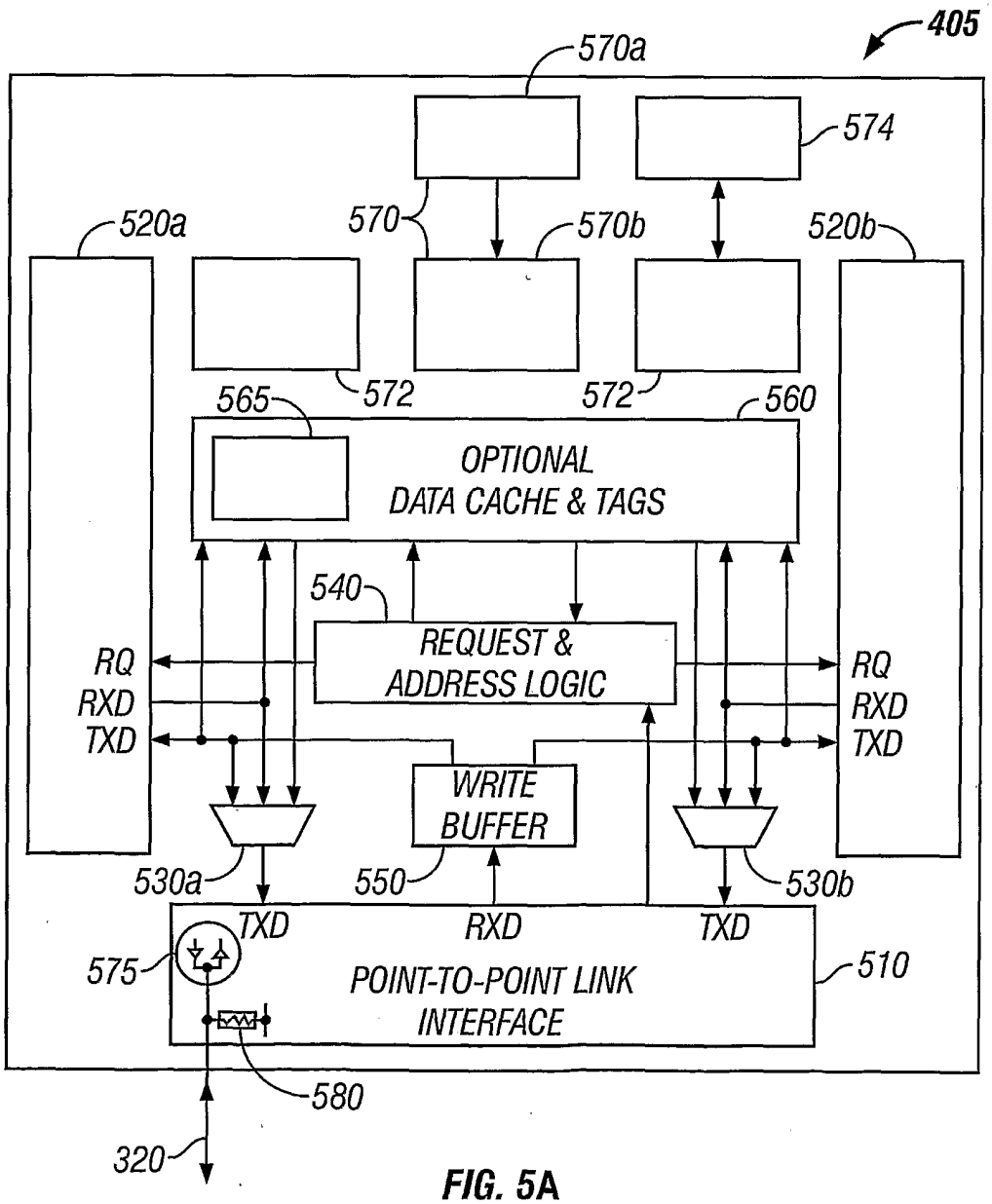

405
570a
574
520a
570
570b
520b
572
572
565
560
OPTIONAL
DATA CACHE & TAGS
540
REQUEST &
ADDRESS LOGIC
RQ
RXD
TXD
RQ
RXD
TXD
WRITE
BUFFER
530a
550
530b
TXD
RXD
TXD
575
POINT-TO-POINT LINK
INTERFACE
510
580
320

FIG. 5A

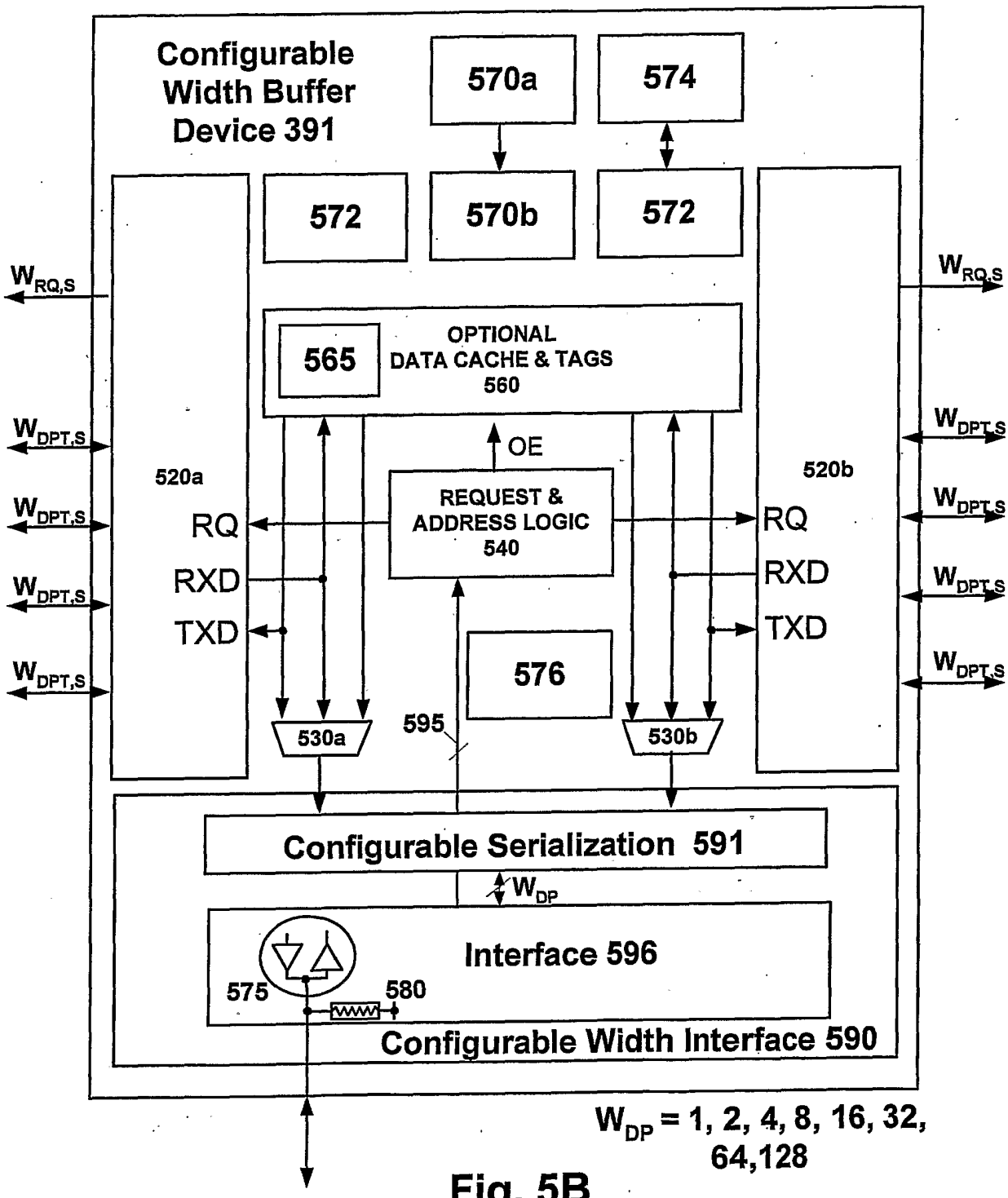

Configurable Width Buffer Device 391
570a
574
572
570b
572
$W_{RQ,S}$
$W_{RQ,S}$
565
OPTIONAL DATA CACHE & TAGS 560
$W_{DPT,S}$
$W_{DPT,S}$
OE
520a
520b
$W_{DPT,S}$
$W_{DPT,S}$
REQUEST & ADDRESS LOGIC 540
RQ
RXD
TXD
RQ
RXD
TXD
$W_{DPT,S}$
$W_{DPT,S}$
576
595
530a
530b
Configurable Serialization 591
W_{DP}
Interface 596
575
580
Configurable Width Interface 590
W_{DP} = 1, 2, 4, 8, 16, 32, 64,128

Fig. 5B

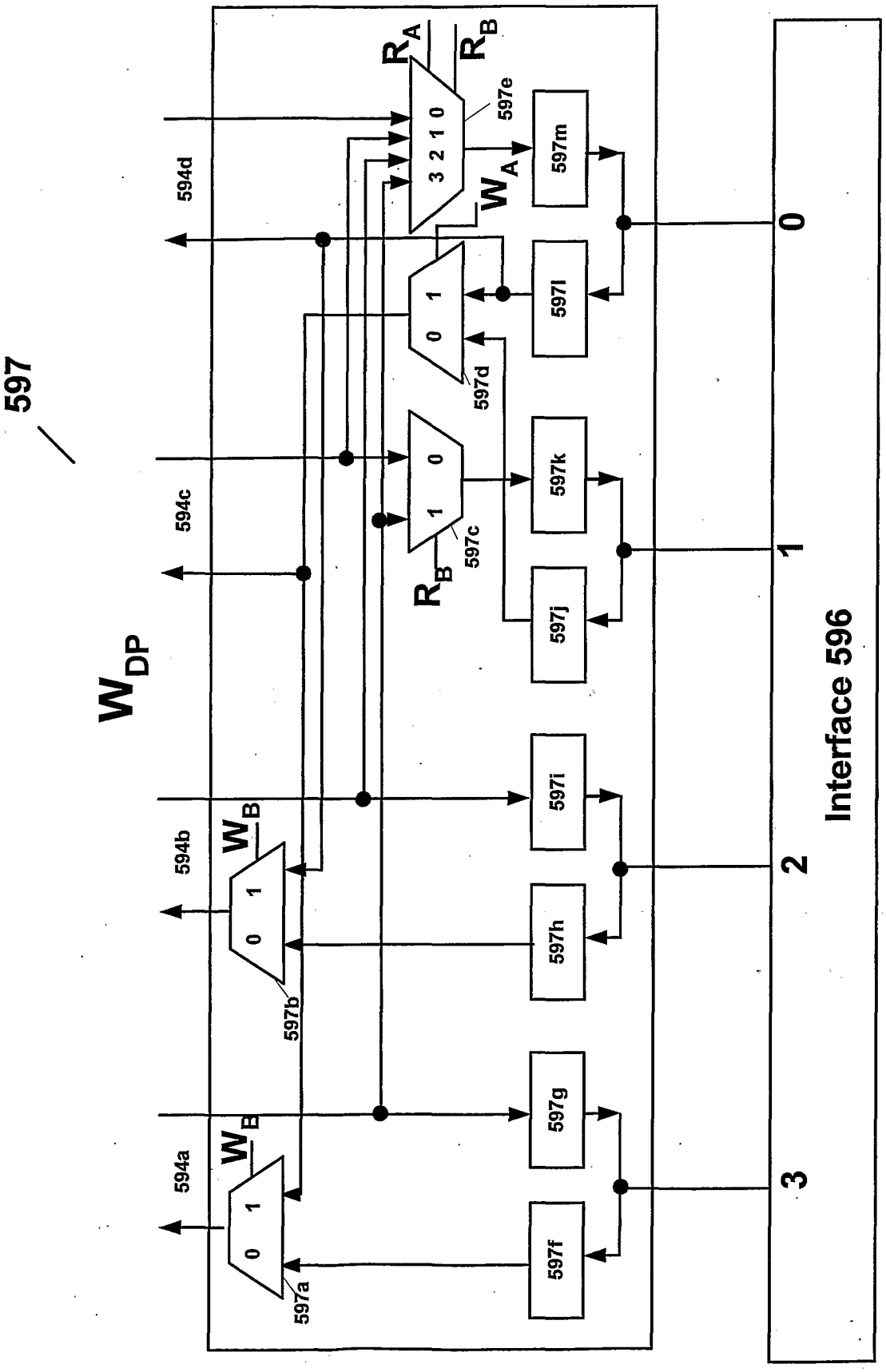

597
W_{DP}
R_A
R_B
W_A
W_B
W_B
W_B
R_B
3 2 1 0
0 1
0 1
0 1
0 1
1 0
597e
597d
597c
597b
597a
594d
594c
594b
594a
597m
597l
597k
597j
597i
597h
597g
597f
0
1
2
3
Interface 596

Fig. 5C

Width	Write		Read		Interface 596 Connections
	W_A	W_B	R_A	R_B	
1	1	1	A_0	A_1	0
2	0	1	0	A_0	0 and 1
4	0	0	0	0	3, 2, 1 and 0

Fig. 5D

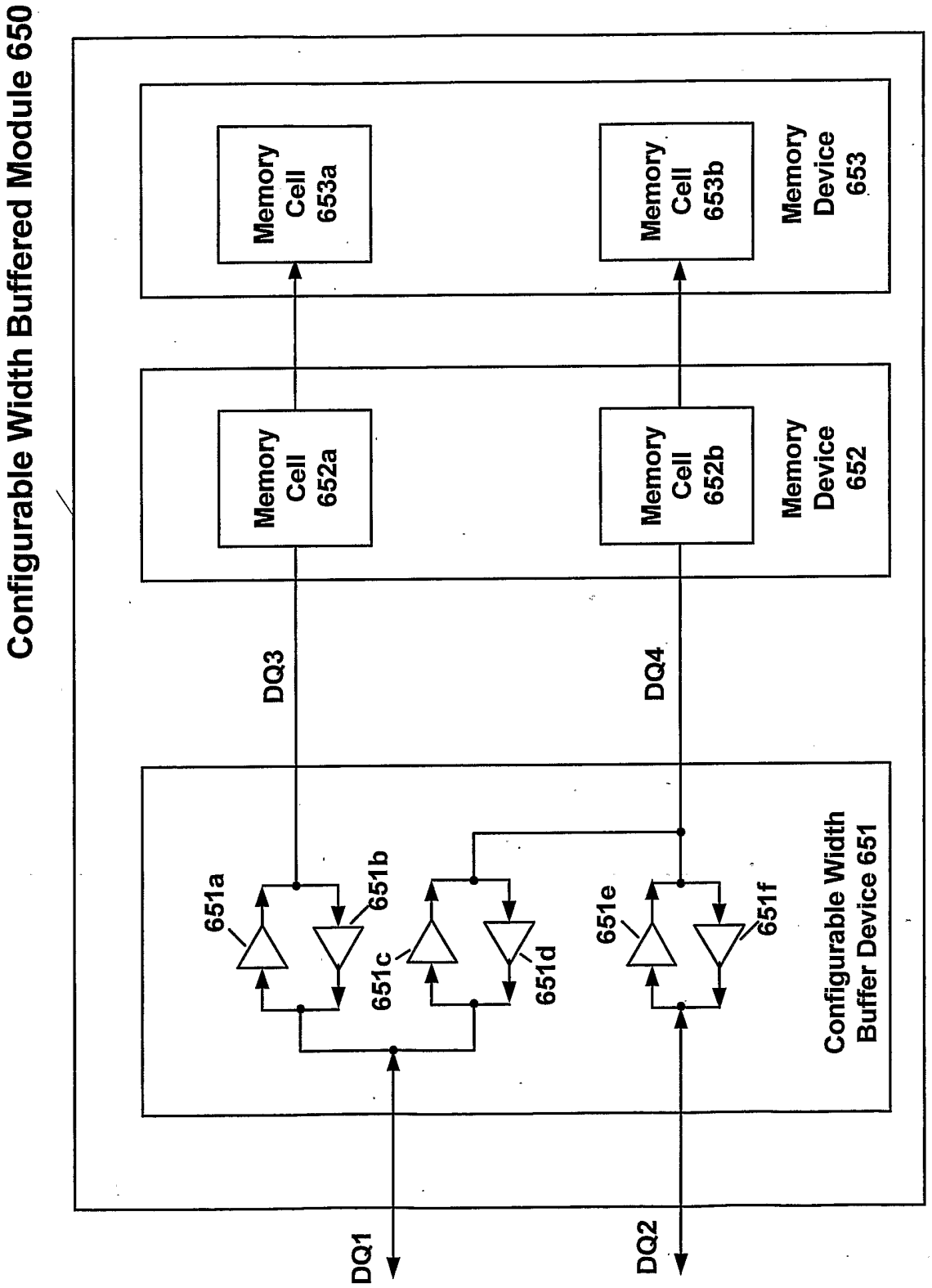

Configurable Width Buffered Module 650
Memory Cell 653a
Memory Cell 653b
Memory Device 653
Memory Cell 652a
Memory Cell 652b
Memory Device 652
DQ3
DQ4
651a
651b
651c
651d
651e
651f
Configurable Width Buffer Device 651
DQ1
DQ2

Fig. 5E

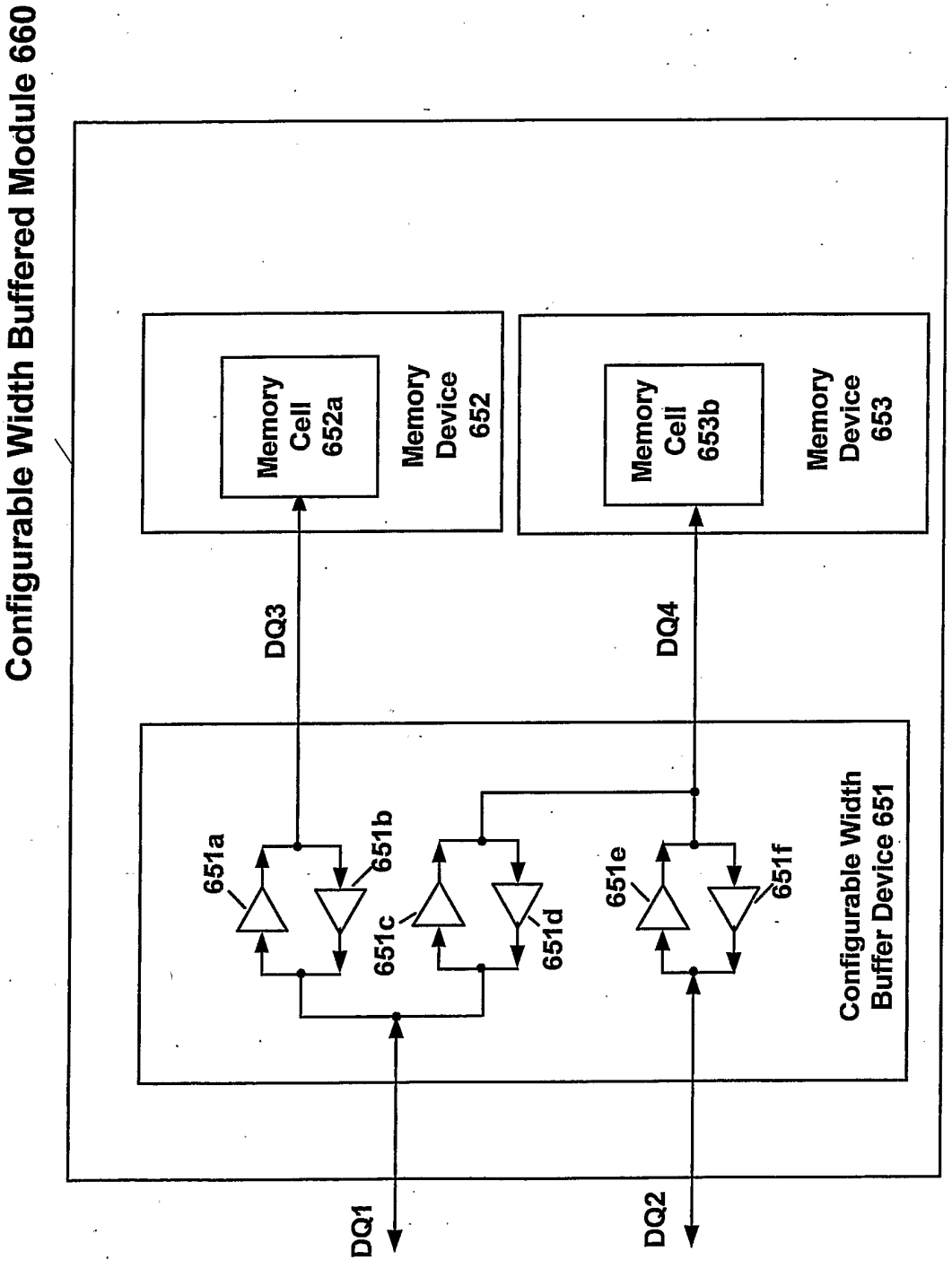

Configurable Width Buffered Module 660
Memory Cell 652a
Memory Device 652
Memory Cell 653b
Memory Device 653
DQ3
DQ4
651a
651b
651c
651d
651e
651f
Configurable Width Buffer Device 651
DQ1
DQ2

Fig. 5F

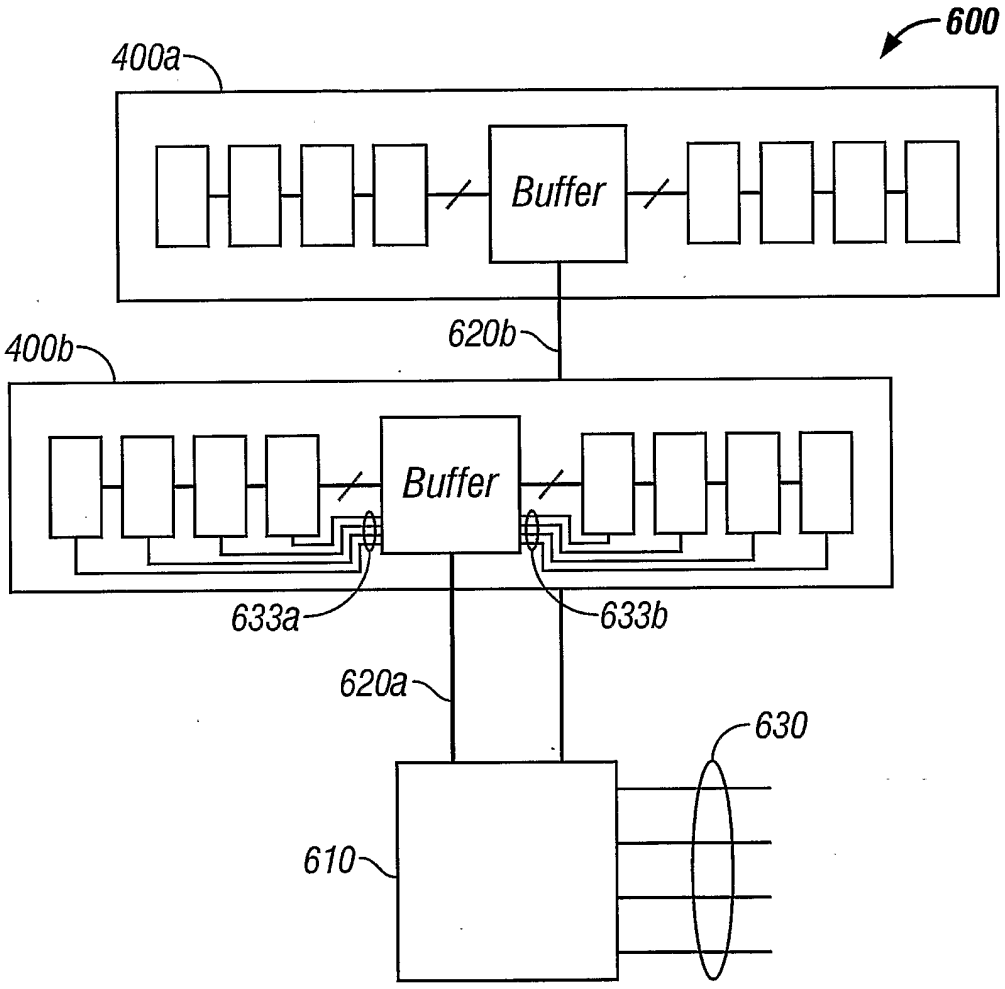


FIG. 6A

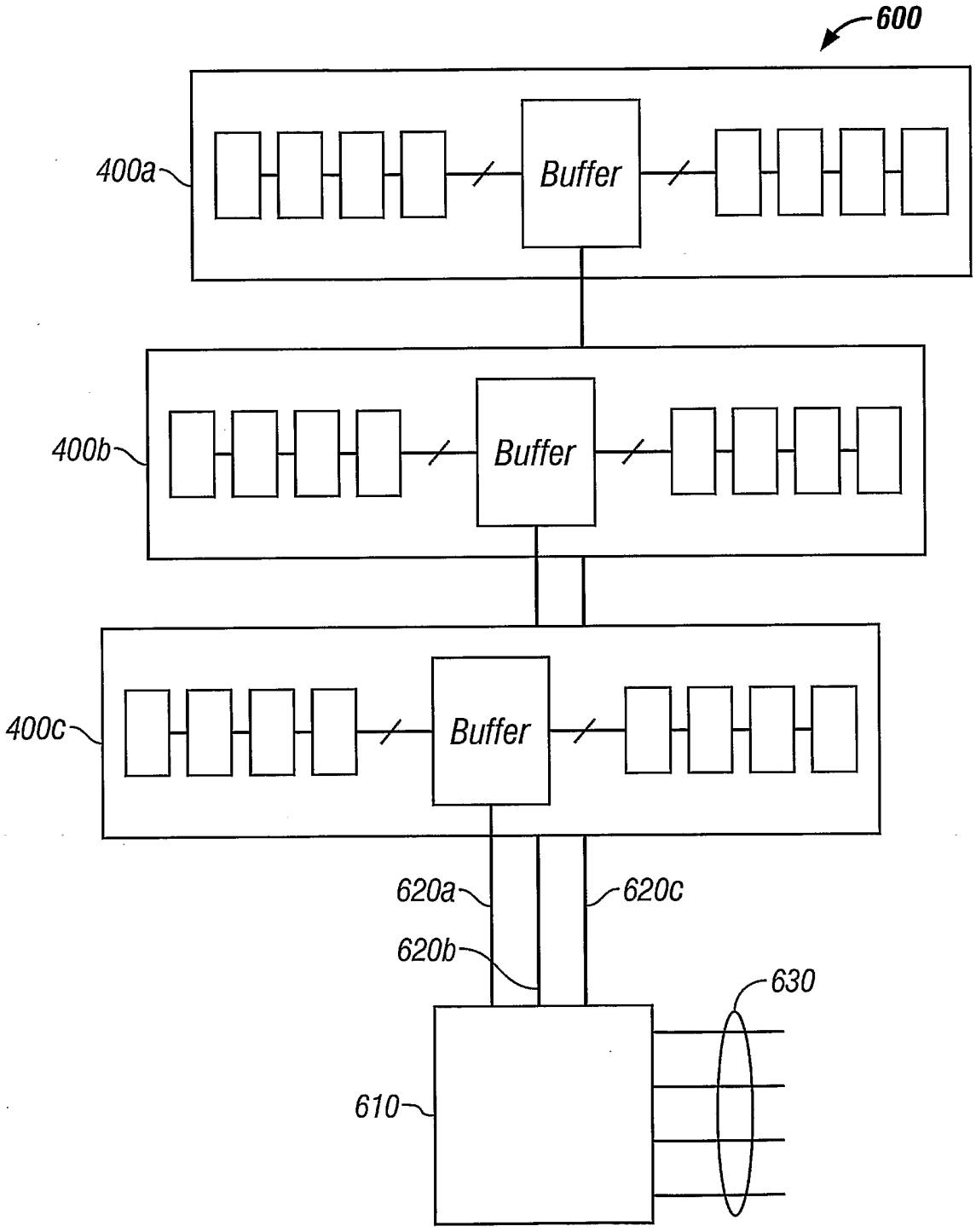

600
400a
Buffer
400b
Buffer
400c
Buffer
620a
620b
620c
630
610

FIG. 6B

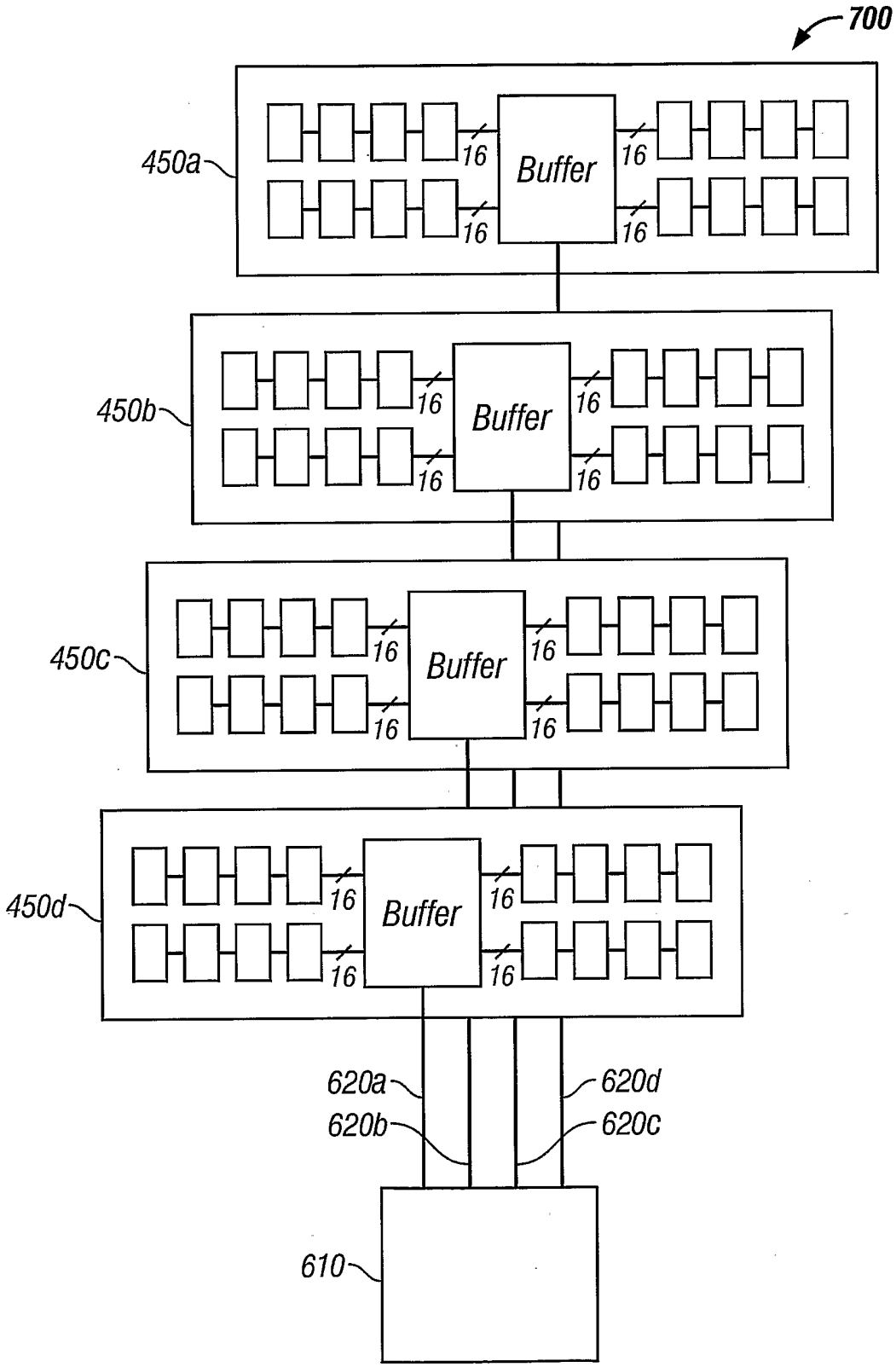

700
450a
Buffer
16
450b
Buffer
16
450c
Buffer
16
450d
Buffer
16
620a
620b
620c
620d
610

FIG. 7

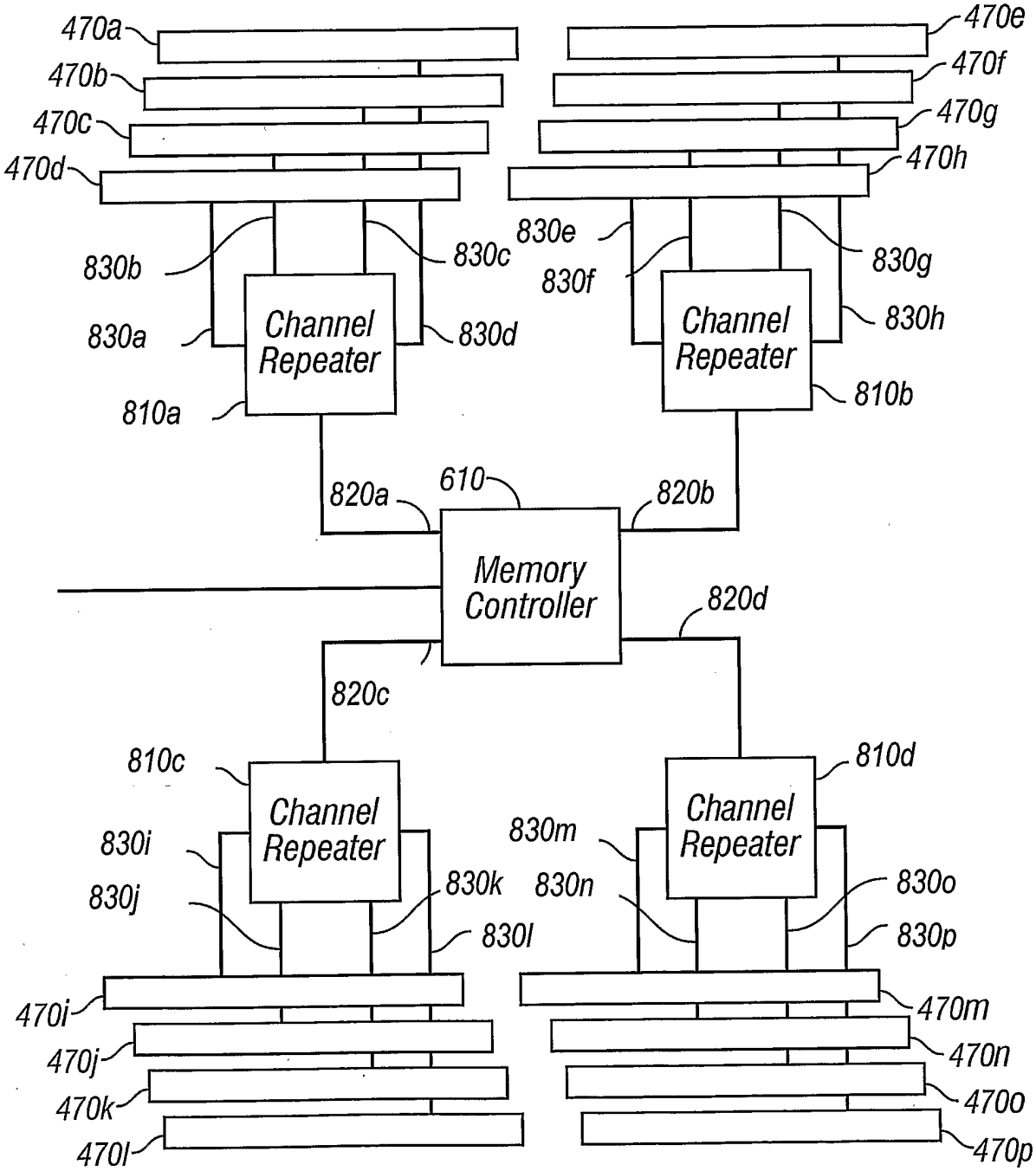

470a
470b
470c
470d
470e
470f
470g
470h
830b
830c
830e
830f
830g
830a
830d
830h
Channel Repeater
Channel Repeater
810a
810b
820a
610
820b
Memory Controller
820d
820c
810c
810d
830i
830j
830k
830l
830m
830n
830o
830p
Channel Repeater
Channel Repeater
470i
470j
470k
470l
470m
470n
470o
470p

FIG. 8A

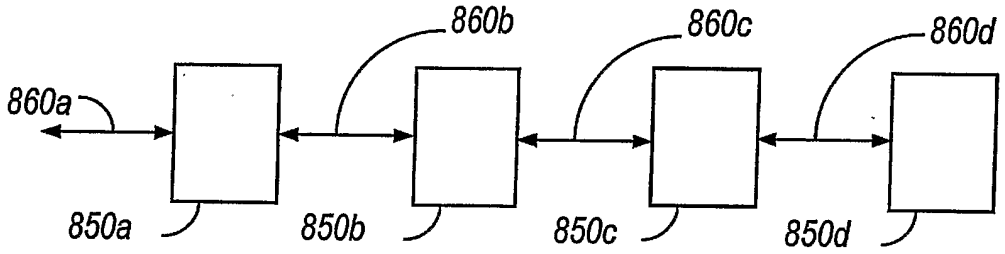


FIG. 8B

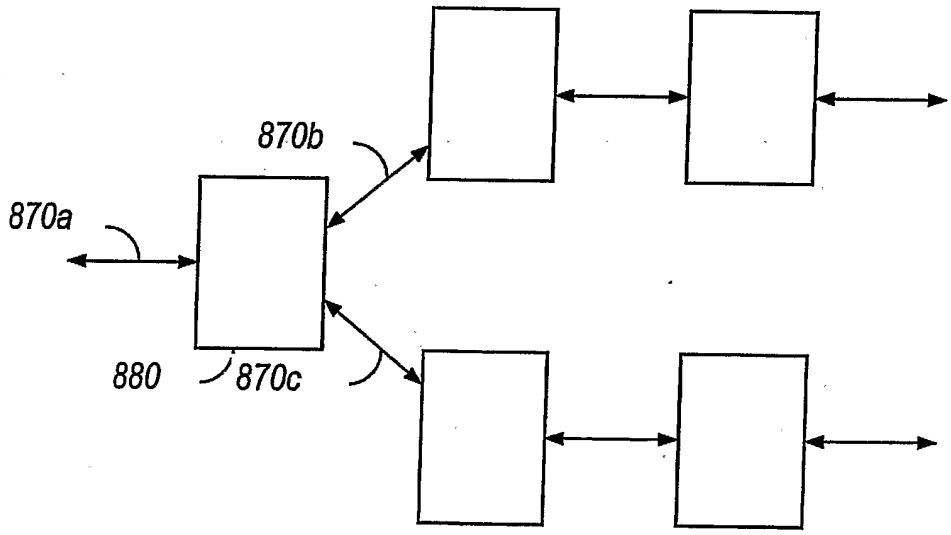


FIG. 8C

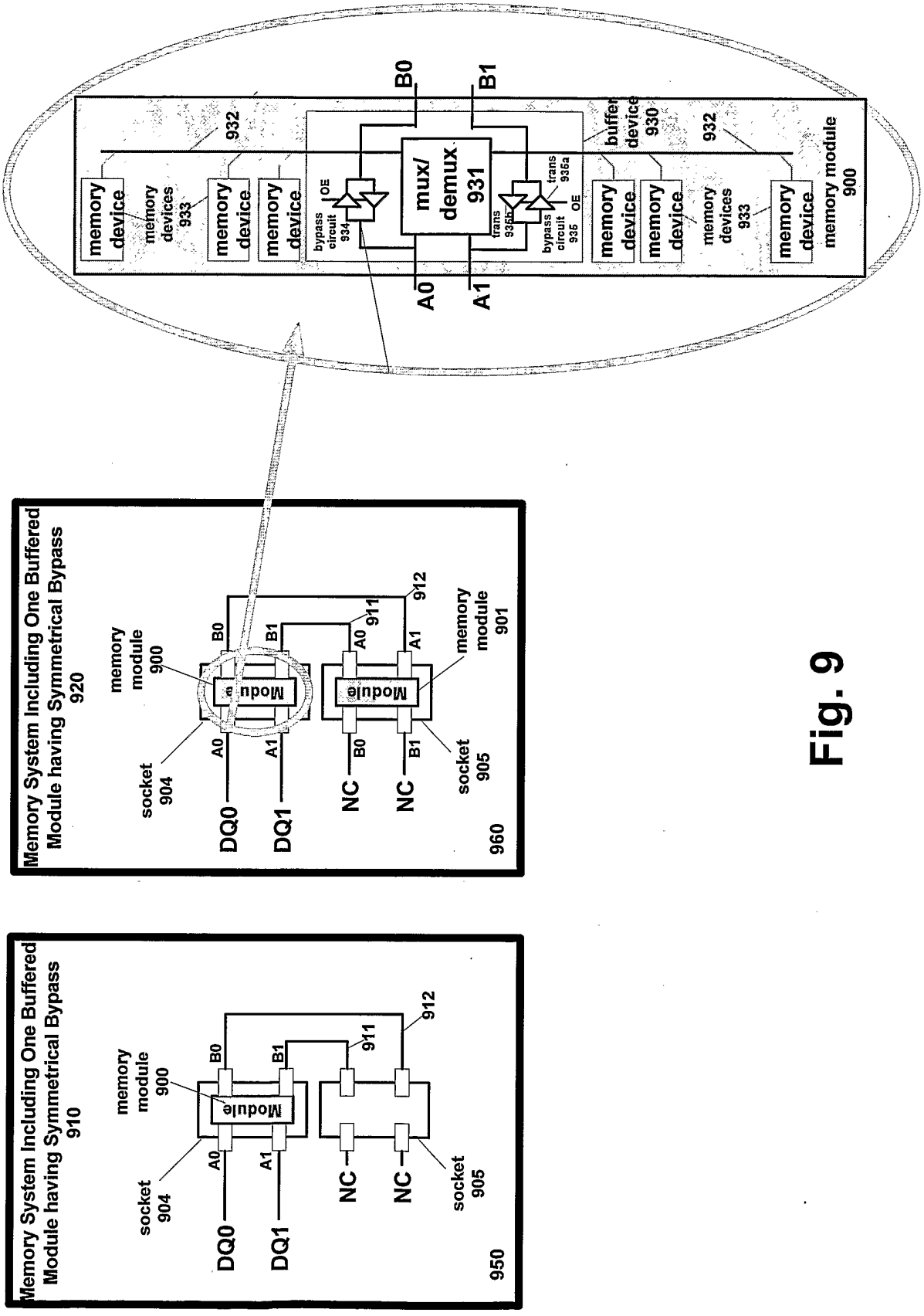

Memory System Including One Buffered Module having Symmetrical Bypass
910
memory module 900
socket 904
A0
A1
B0
B1
Module
DQ0
DQ1
NC
NC
911
912
socket 905
950
Memory System Including One Buffered Module having Symmetrical Bypass
920
memory module 900
socket 904
A0
A1
B0
B1
Module
DQ0
DQ1
NC
NC
911
912
memory module 901
socket 905
960
B0
B1
A0
A1
mux/ demux 931
bypass circuit 934
OE
trans 935b
trans 935a
bypass circuit 935
OE
buffer device 930
memory device
memory devices 933
932
memory module 900

Fig. 9

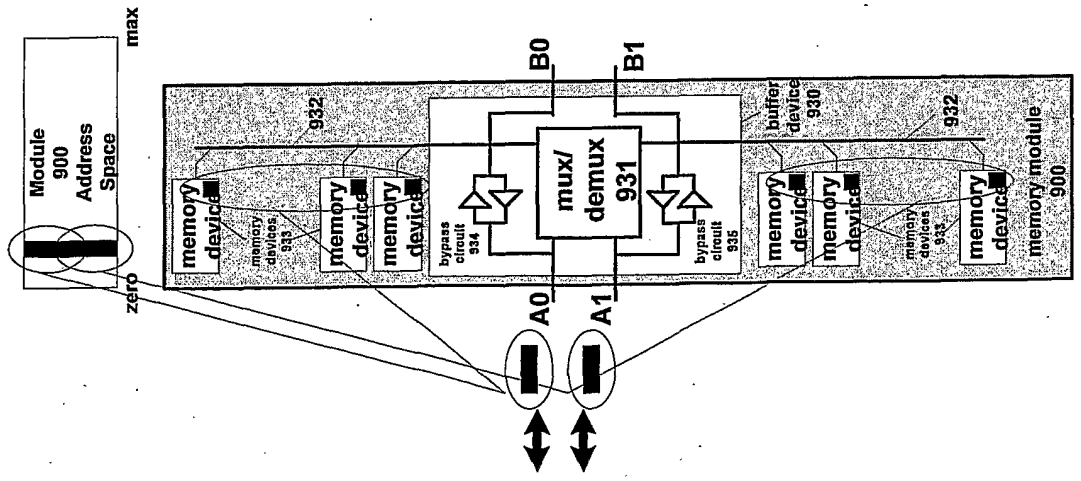


Fig. 10A

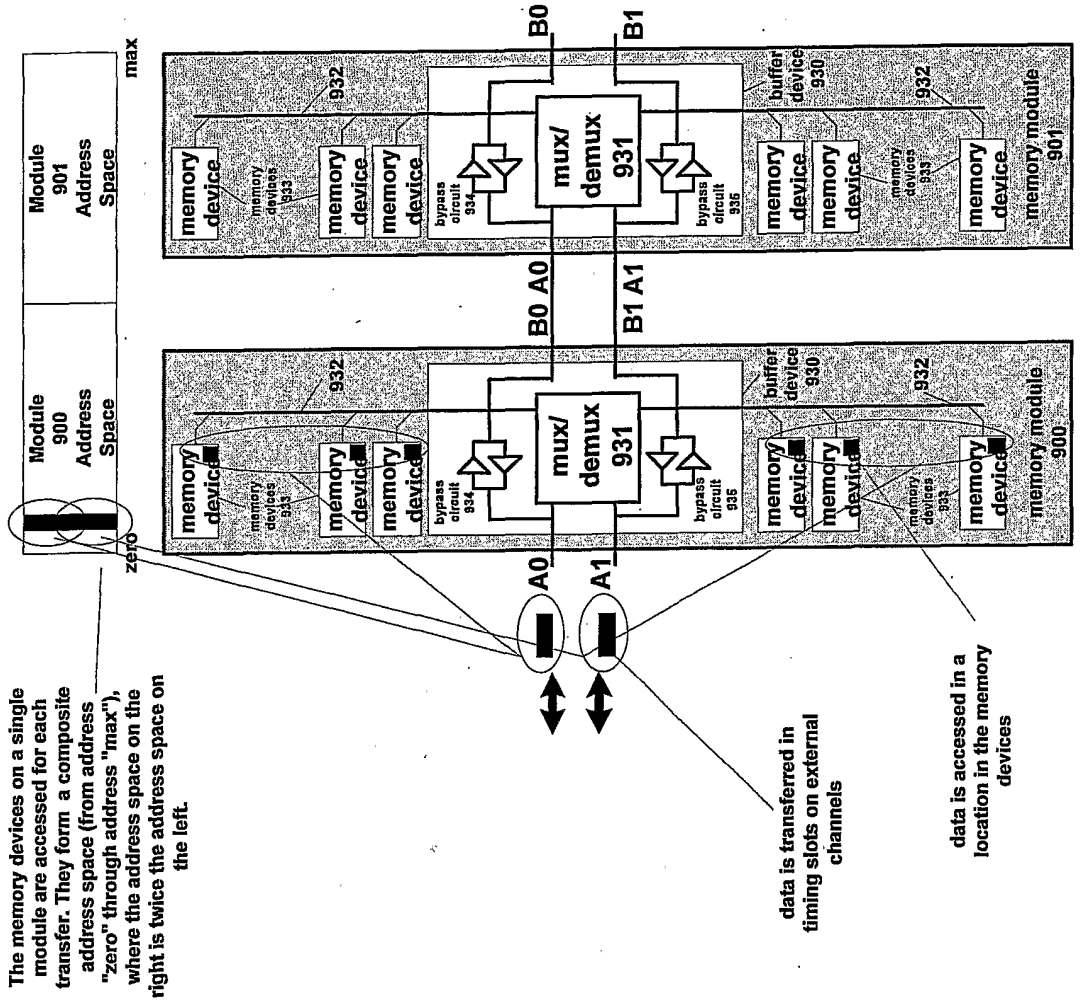


Fig. 10B

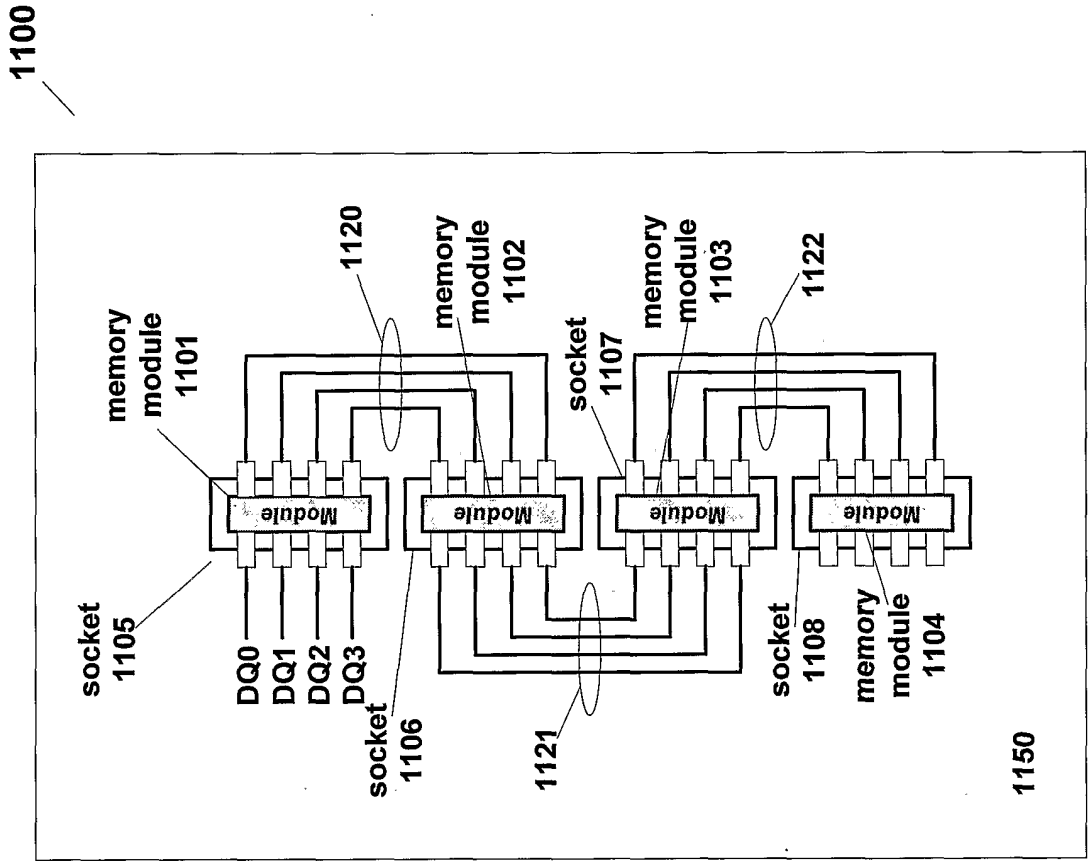

1100
memory module 1101
1120
memory module 1102
socket 1107
memory module 1103
1122
socket 1105
DQ0
DQ1
DQ2
DQ3
socket 1106
1121
socket 1108
memory module 1104
1150

Fig. 11

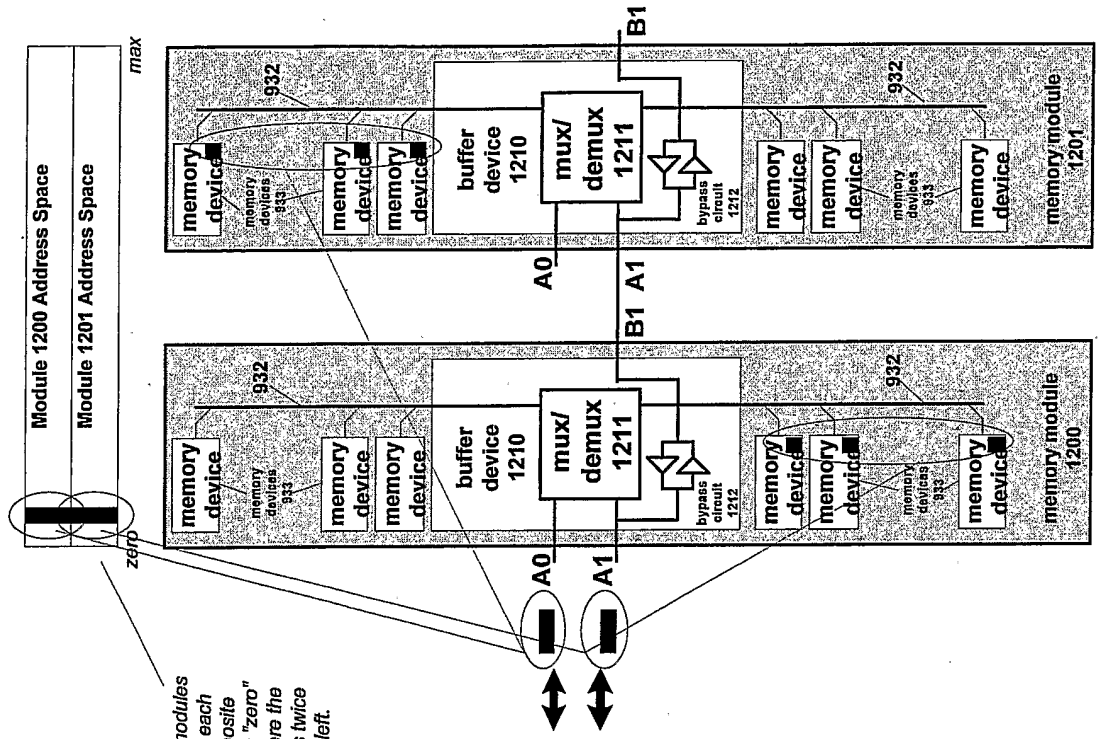


Fig. 12B

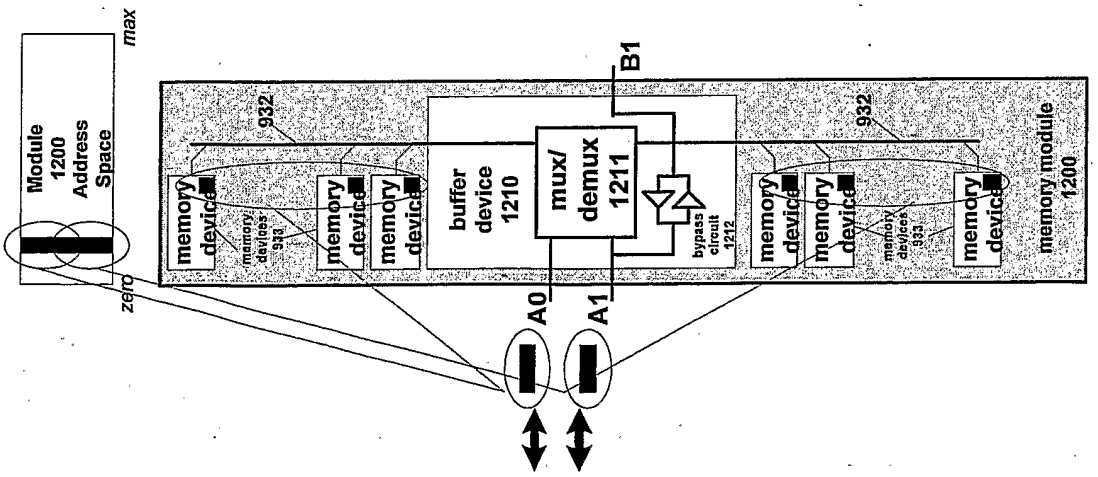


Fig. 12A

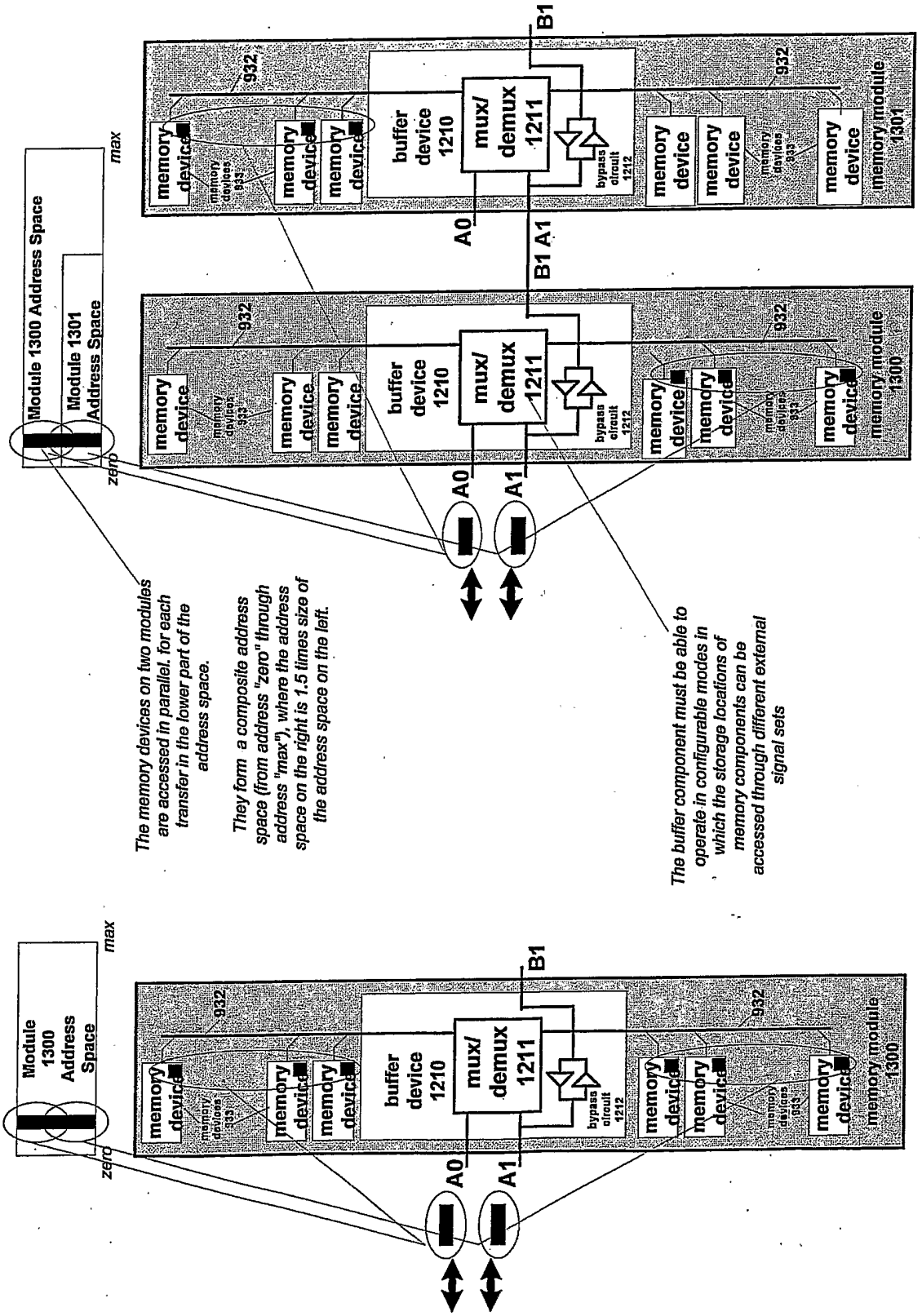


Fig. 13B

Fig. 13A

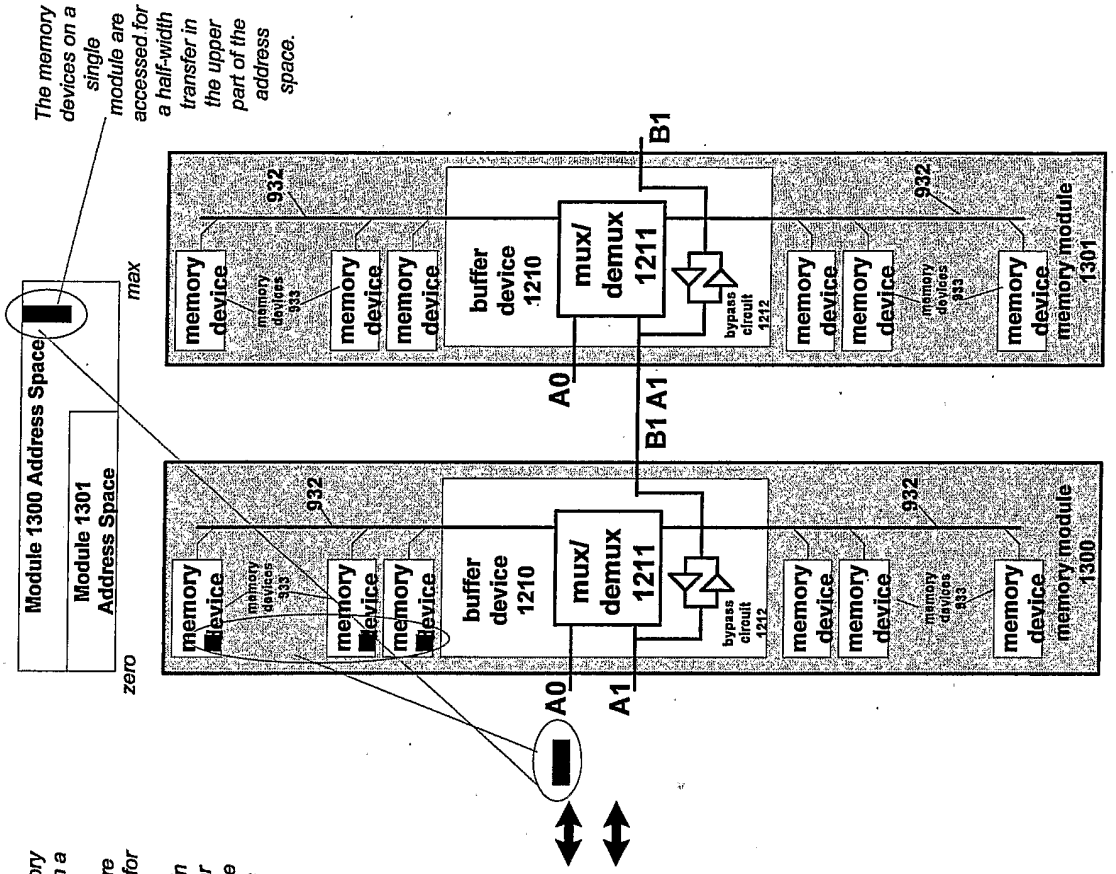


Fig. 14B

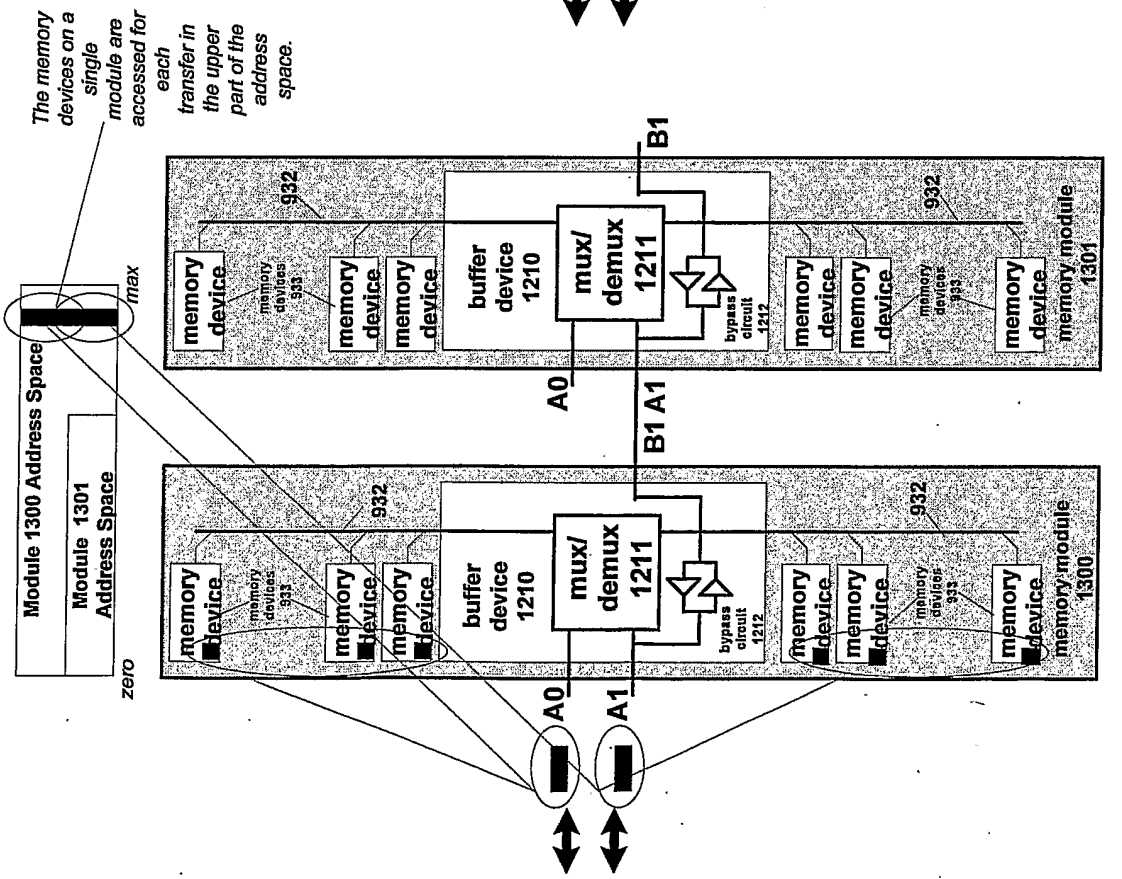
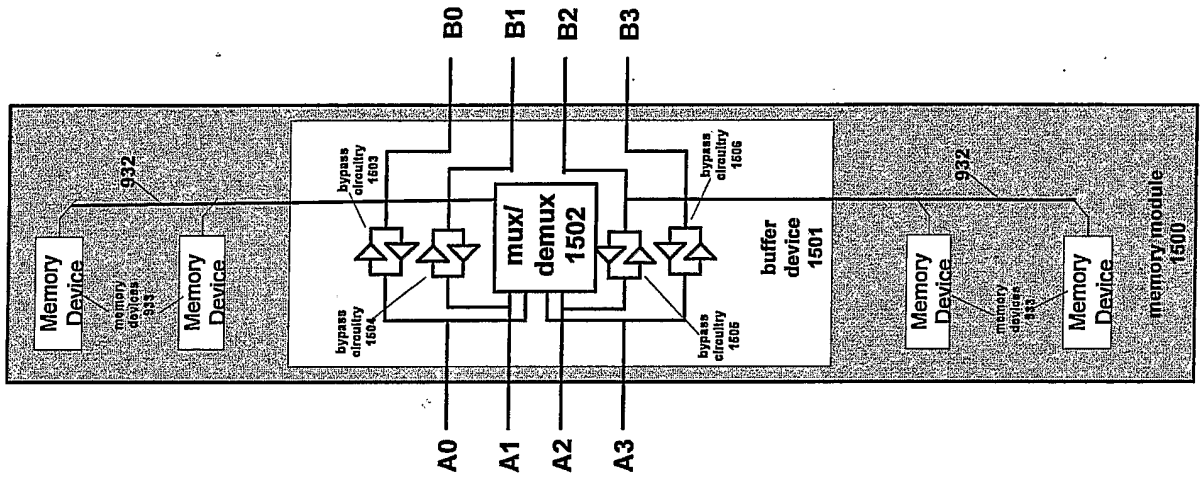


Fig. 14A

Fig. 15


B0
B1
B2
B3
bypass circuitry 1603
bypass circuitry 1606
932
mux/ demux 1502
buffer device 1501
Memory Device
memory devices 933
bypass circuitry 1604
bypass circuitry 1605
memory module 1500
A0
A1
A2
A3

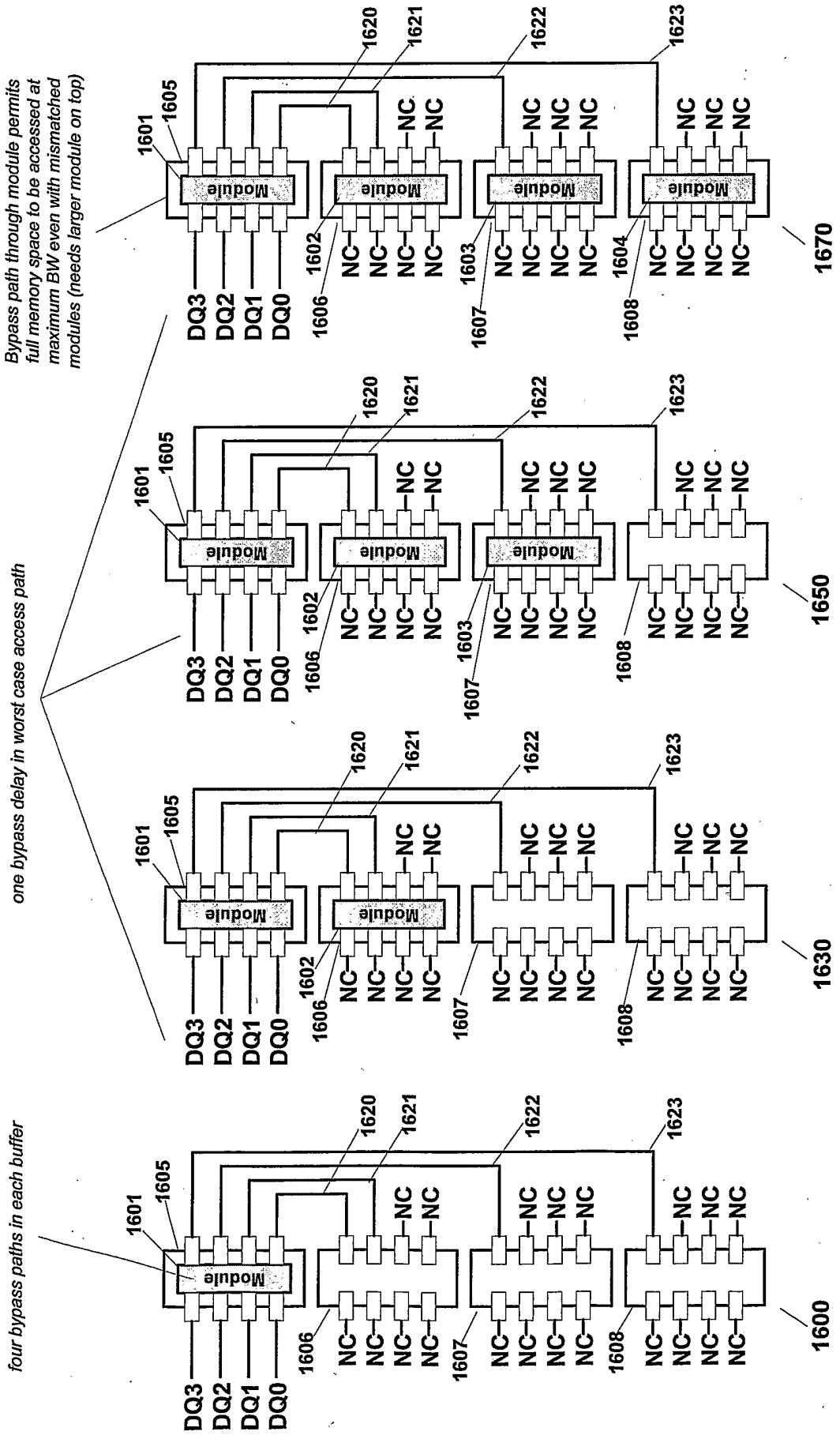


Fig. 16A

Fig. 16B

Fig. 16C

Fig. 16D

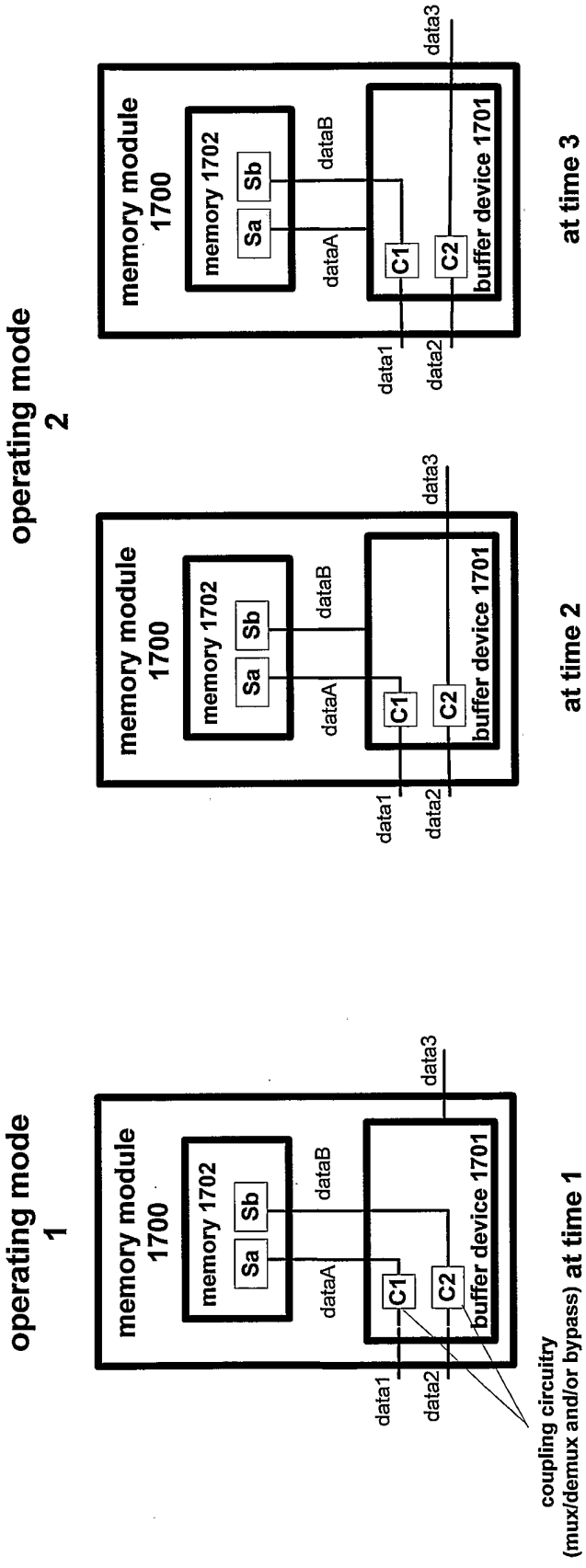

operating mode 1
memory module 1700
memory 1702
Sa
Sb
dataA
dataB
C1
C2
buffer device 1701
data1
data2
data3
coupling circuitry (mux/demux and/or bypass)
at time 1
operating mode 2
at time 2
at time 3

Fig. 17

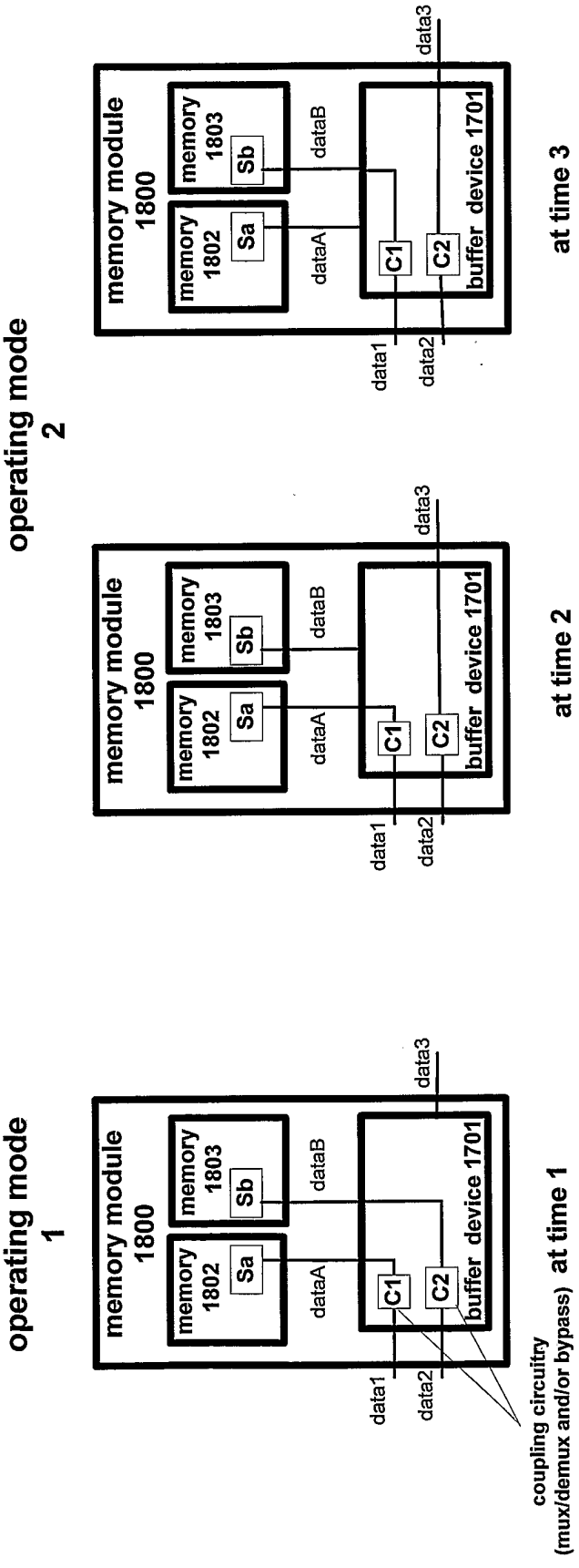

operating mode 1
memory module 1800
memory 1802
Sa
memory 1803
Sb
dataA
dataB
C1
C2
buffer device 1701
data1
data2
data3
coupling circuitry (mux/demux and/or bypass)
at time 1
operating mode 2
memory module 1800
memory 1802
Sa
memory 1803
Sb
dataA
dataB
C1
C2
buffer device 1701
data1
data2
data3
at time 2
memory module 1800
memory 1802
Sa
memory 1803
Sb
dataA
dataB
C1
C2
buffer device 1701
data1
data2
data3
at time 3

Fig. 18

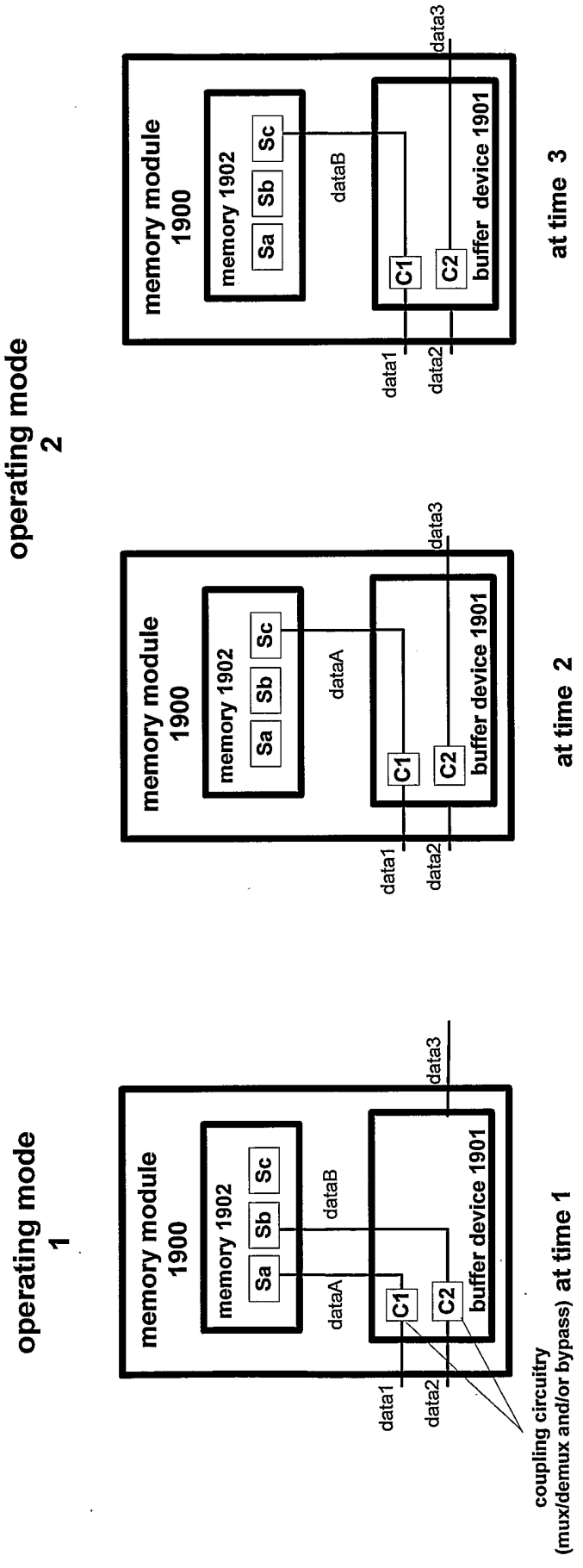

operating mode 1
memory module 1900
memory 1902
Sa
Sb
Sc
dataA
dataB
buffer device 1901
C1
C2
data1
data2
data3
coupling circuitry (mux/demux and/or bypass)
at time 1
operating mode 2
memory module 1900
memory 1902
Sa
Sb
Sc
dataA
buffer device 1901
C1
C2
data1
data2
data3
at time 2
memory module 1900
memory 1902
Sa
Sb
Sc
dataB
buffer device 1901
C1
C2
data1
data2
data3
at time 3

Fig. 19

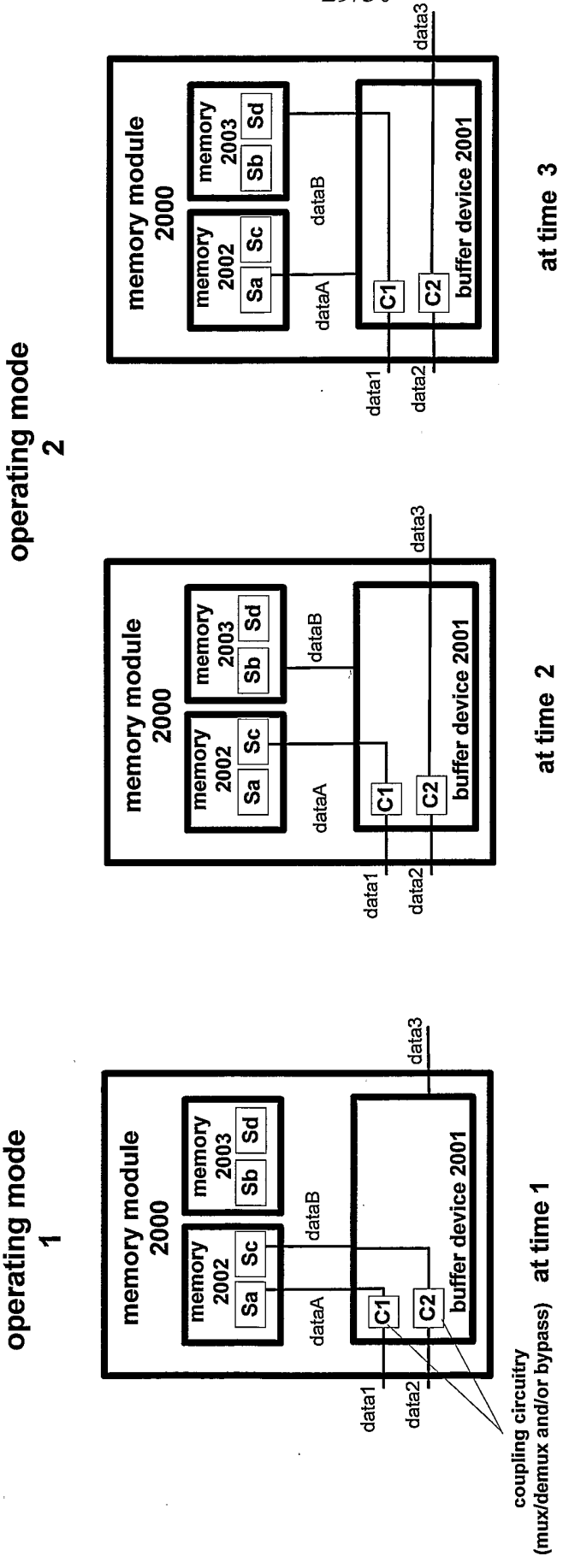
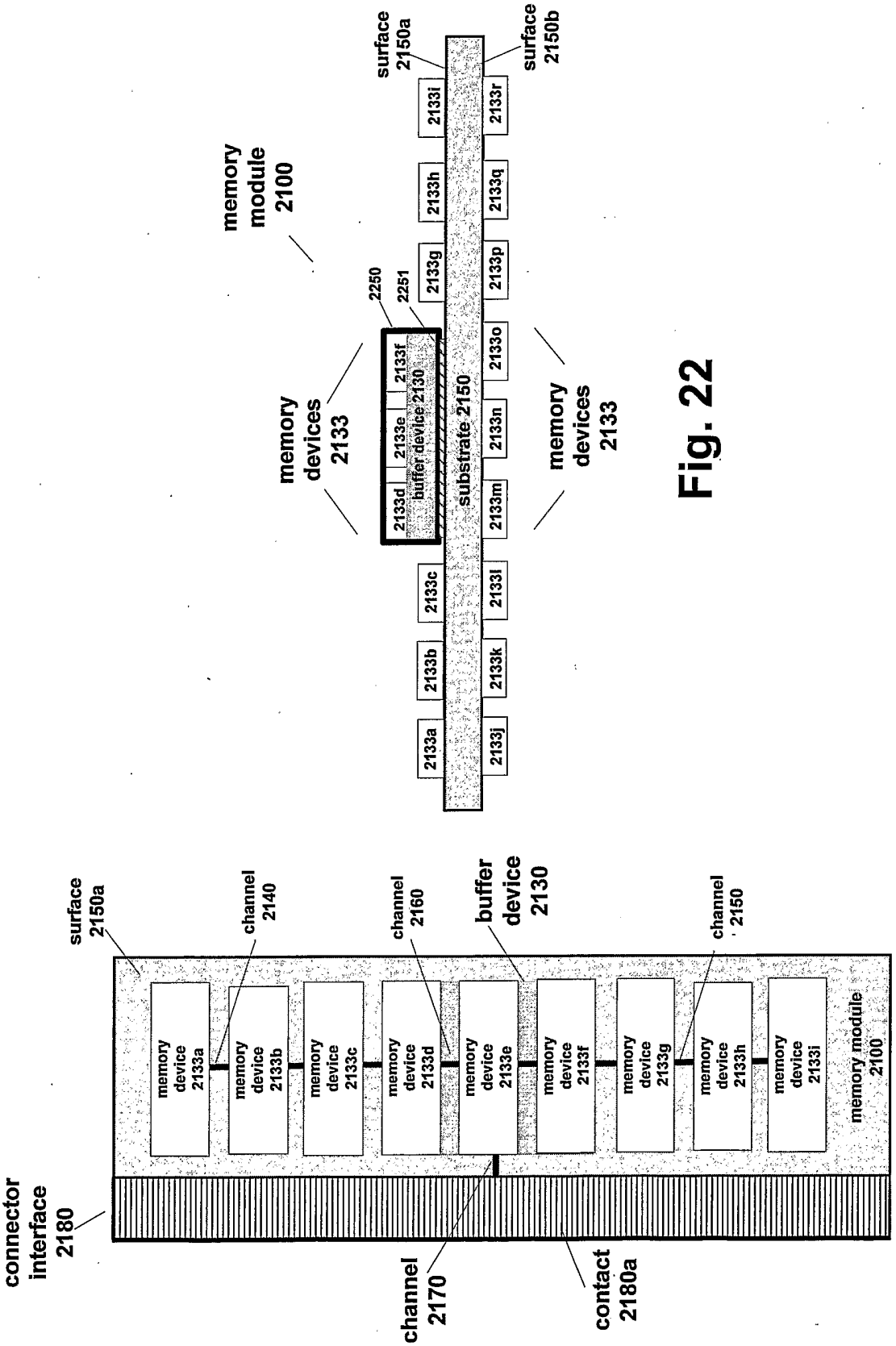

operating mode 1
memory module 2000
memory 2002
Sa
Sc
memory 2003
Sb
Sd
dataA
dataB
C1
C2
buffer device 2001
data1
data2
data3
coupling circuitry (mux/demux and/or bypass)
at time 1
operating mode 2
at time 2
at time 3

Fig. 20


memory module 2100
surface 2150a
surface 2150b
memory devices 2133
memory devices 2133
substrate 2150
buffer device 2130
2250
2251
2133a
2133b
2133c
2133d
2133e
2133f
2133g
2133h
2133i
2133j
2133k
2133l
2133m
2133n
2133o
2133p
2133q
2133r
Fig. 22
connector interface 2180
surface 2150a
channel 2140
channel 2160
buffer device 2130
channel 2150
channel 2170
contact 2180a
memory device 2133a
memory device 2133b
memory device 2133c
memory device 2133d
memory device 2133e
memory device 2133f
memory device 2133g
memory device 2133h
memory device 2133i
memory module 2100
Fig. 21

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US05/17066

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G06F 12/00
US CL : 711/5,104
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 711/5,104

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST - USPAT, PGPUB, EPO, JPO, IBM TDB, Derwent

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,513,135 (DELL et al) 30 April 1996 (30.04.1996), Fig. 1.	51-59, 62

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 October 2005 (18.10.2005)	02 NOV 2005
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Mano Padmanabhan Telephone No. 571-272-2100

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