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Khandros et al.

(54) **METHOD OF MAKING A SOCKET TO PERFORM TESTING ON INTEGRATED CIRCUITS AND SOCKET MADE**

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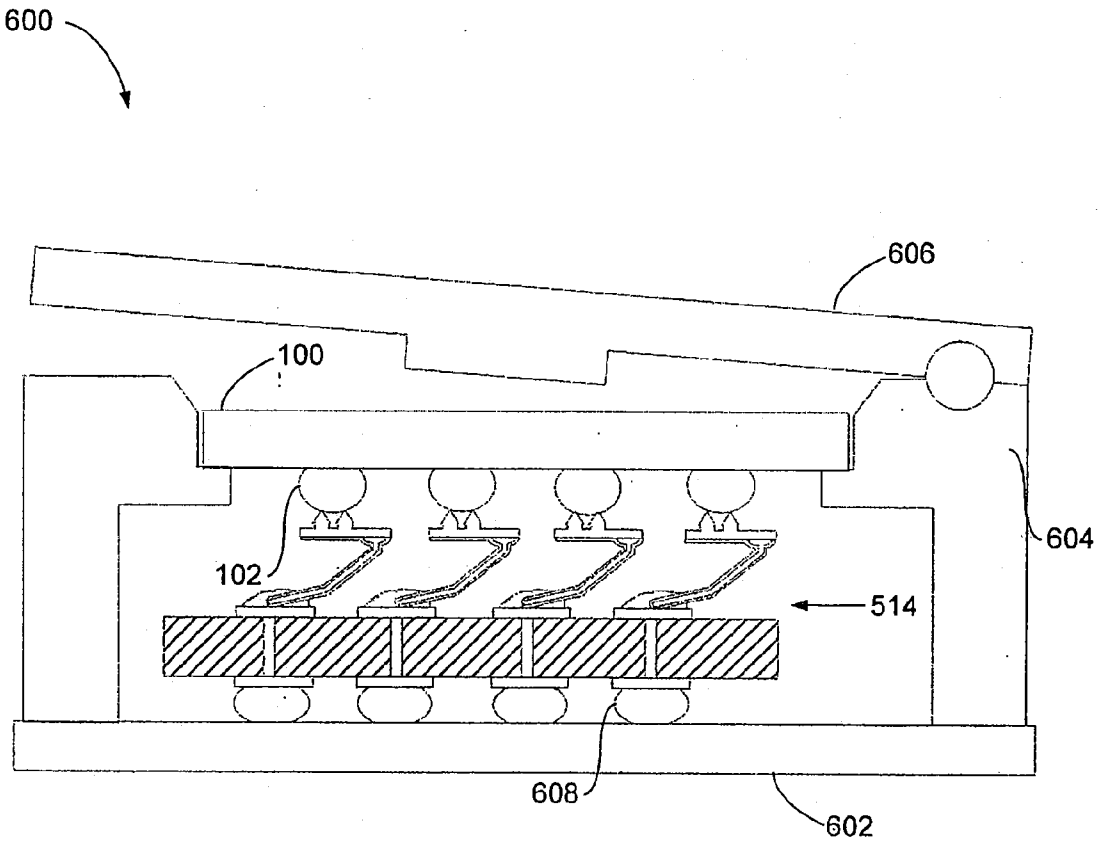
(57) **ABSTRACT**

A interconnect structure is inexpensively manufactured and easily insertable into a socket. The interconnect structure is manufactured by forming a sacrificial substrate with cavities that is covered by a masking material having openings corresponding to the cavities. A first plating process is performed by depositing conductive material, followed by coupling wires within the openings and performing another plating process by depositing more conductive material. The interconnect structure is completed by first removing the masking material and sacrificial substrate. Ends of the wires are coupled opposite now-formed contact structures to a board. To complete the socket, a support device is coupled to the board to hold a tested integrated circuit.



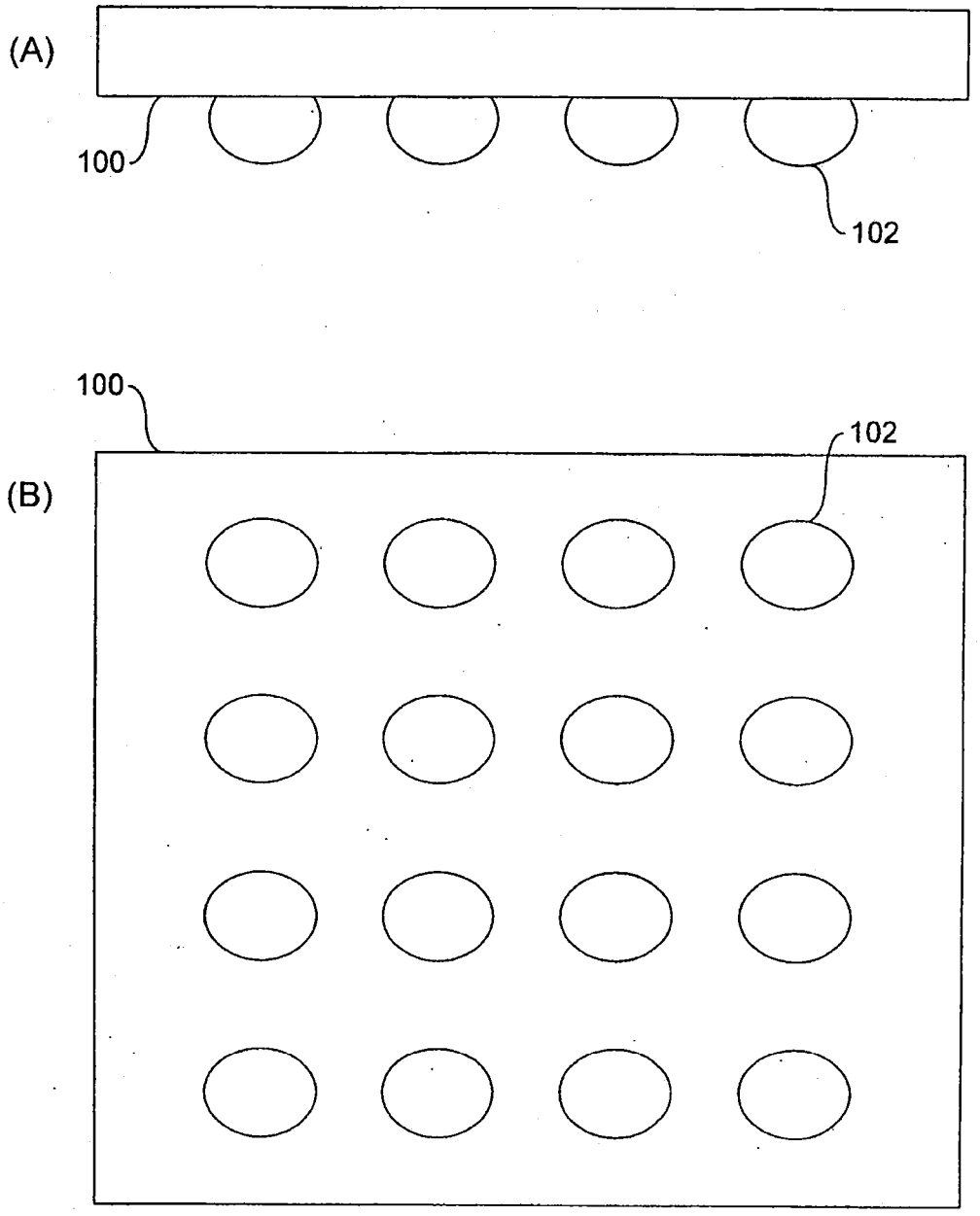


FIG. 1

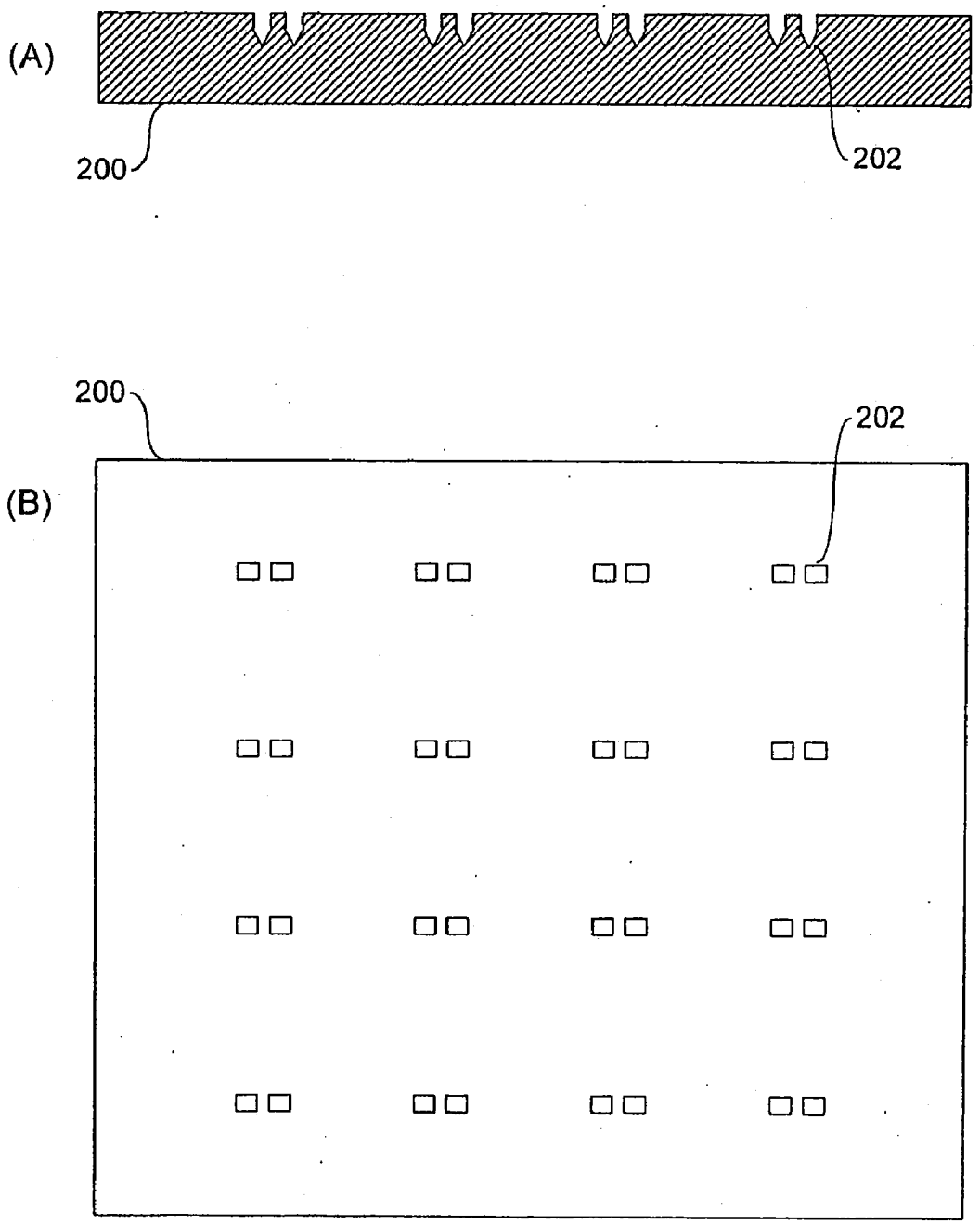


FIG. 2

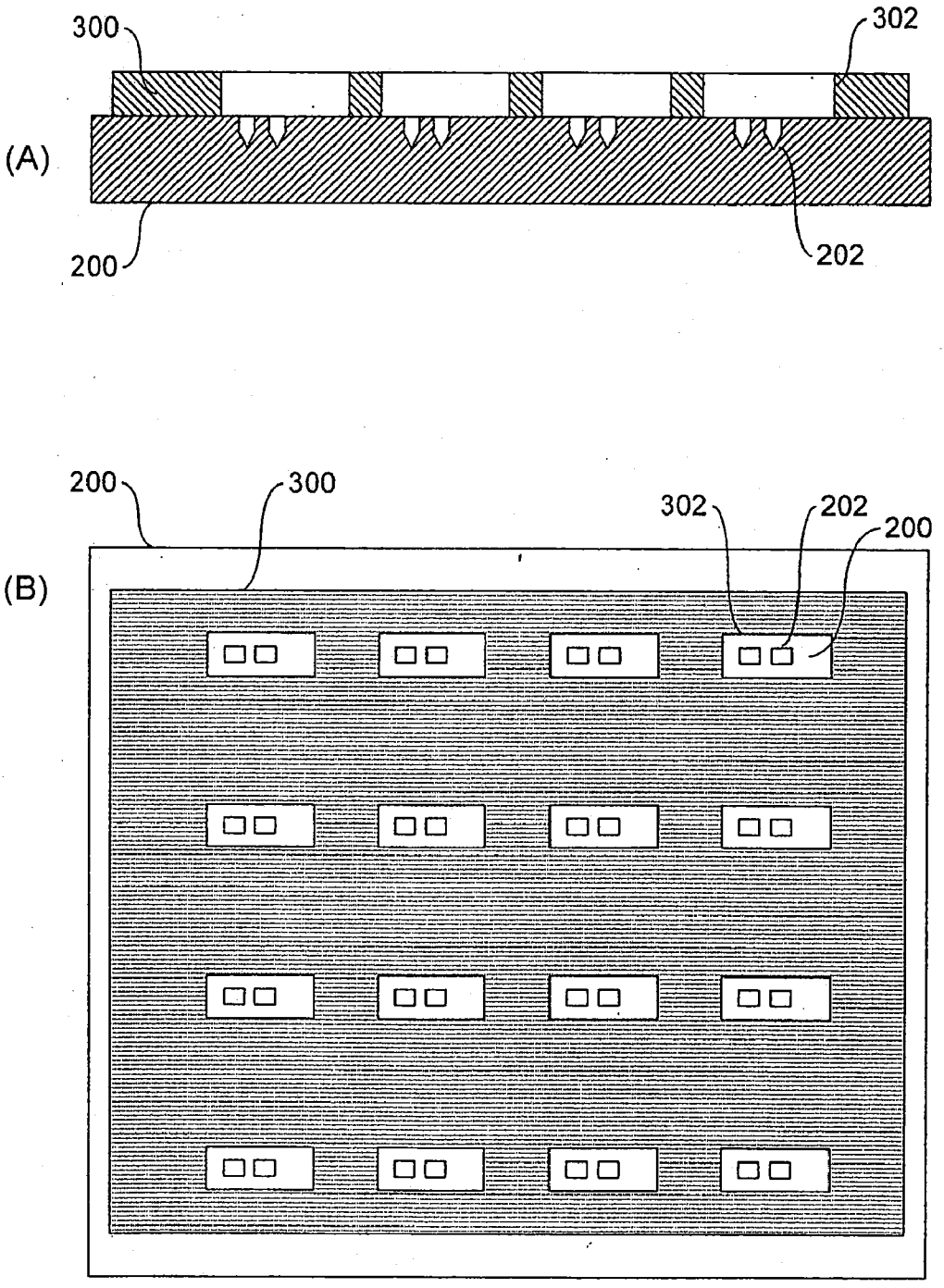


FIG. 3

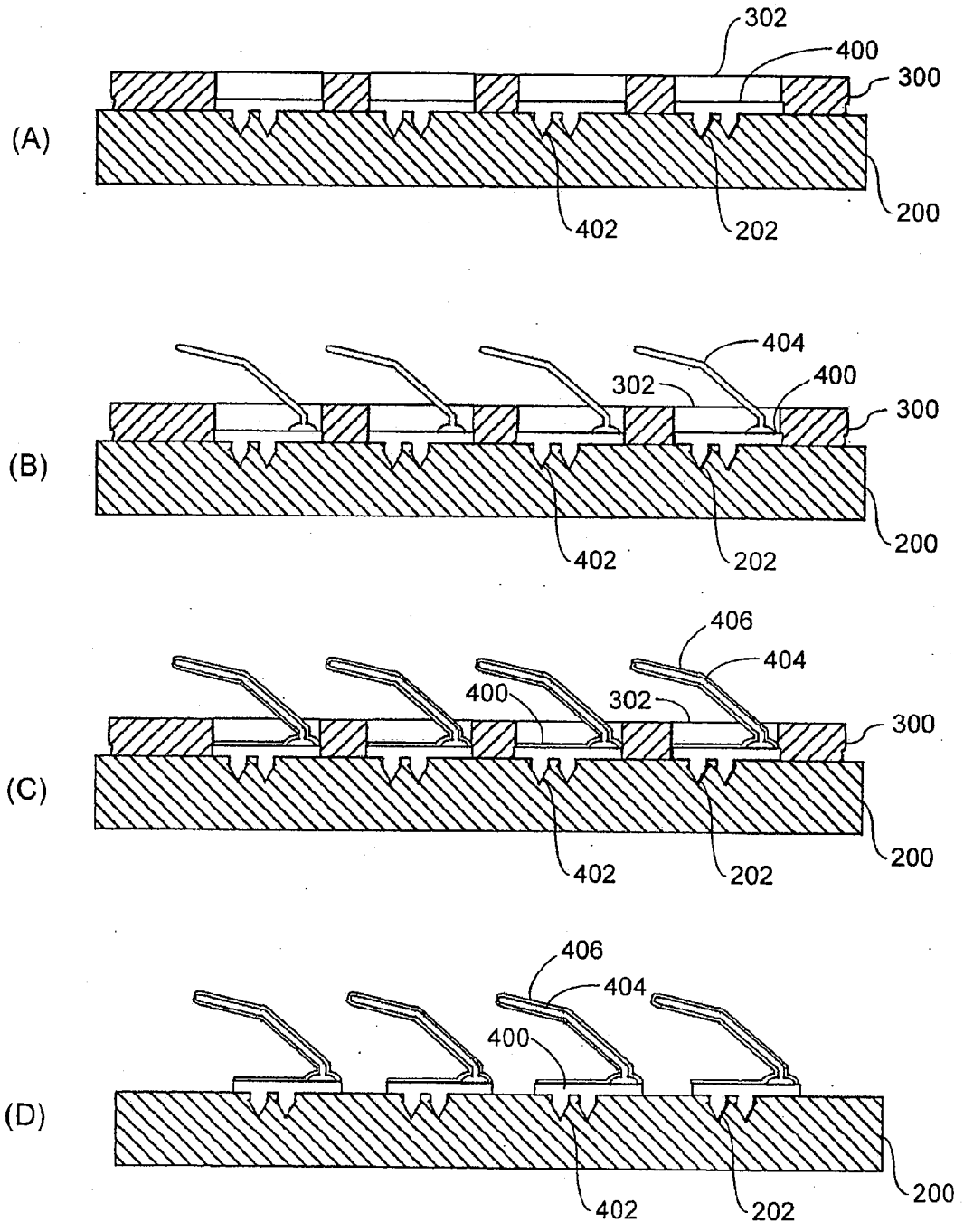

(A)
302
400
300
200
402
202
(B)
404
302
400
300
200
402
202
(C)
406
404
400
302
300
200
402
202
(D)
406
404
400
200
402
202

FIG. 4

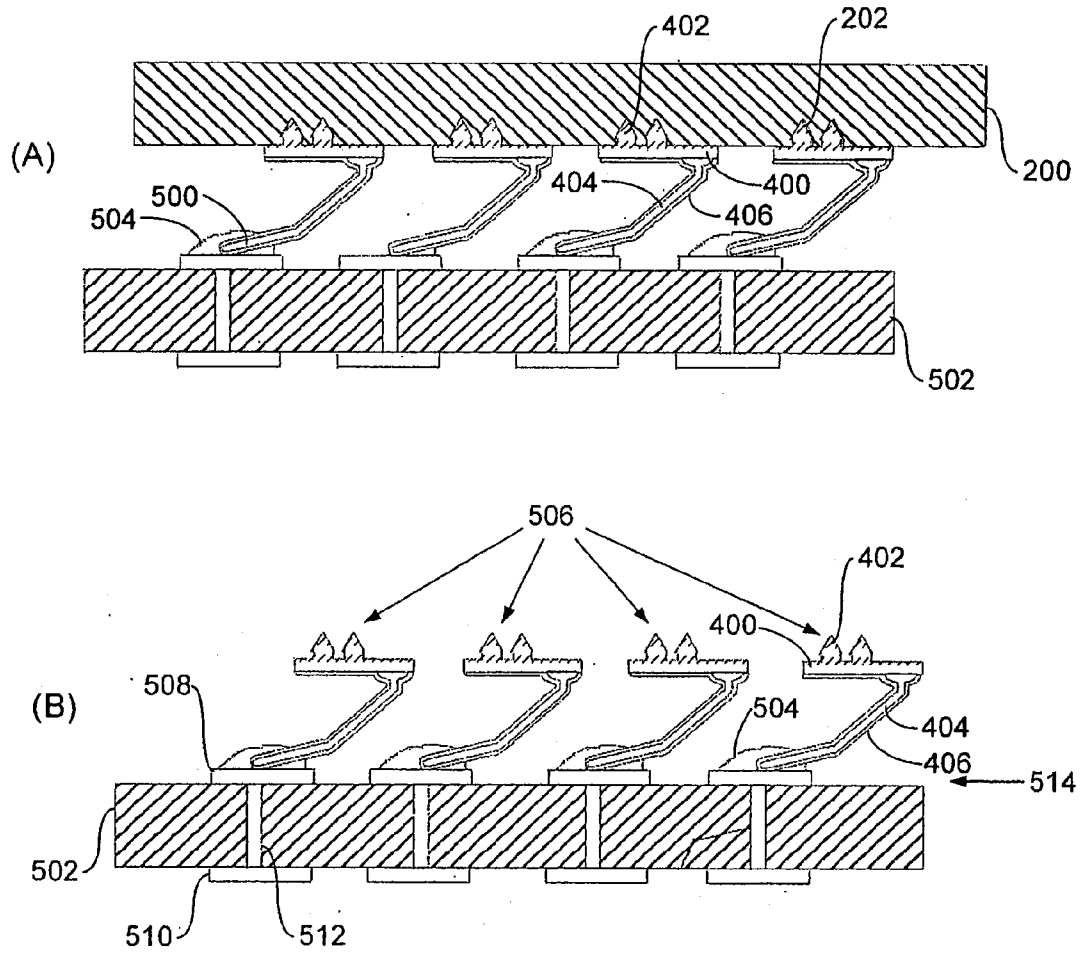

(A)
402
202
200
500
504
404
400
406
502
(B)
506
402
400
508
504
404
406
514
502
510
512

FIG. 5

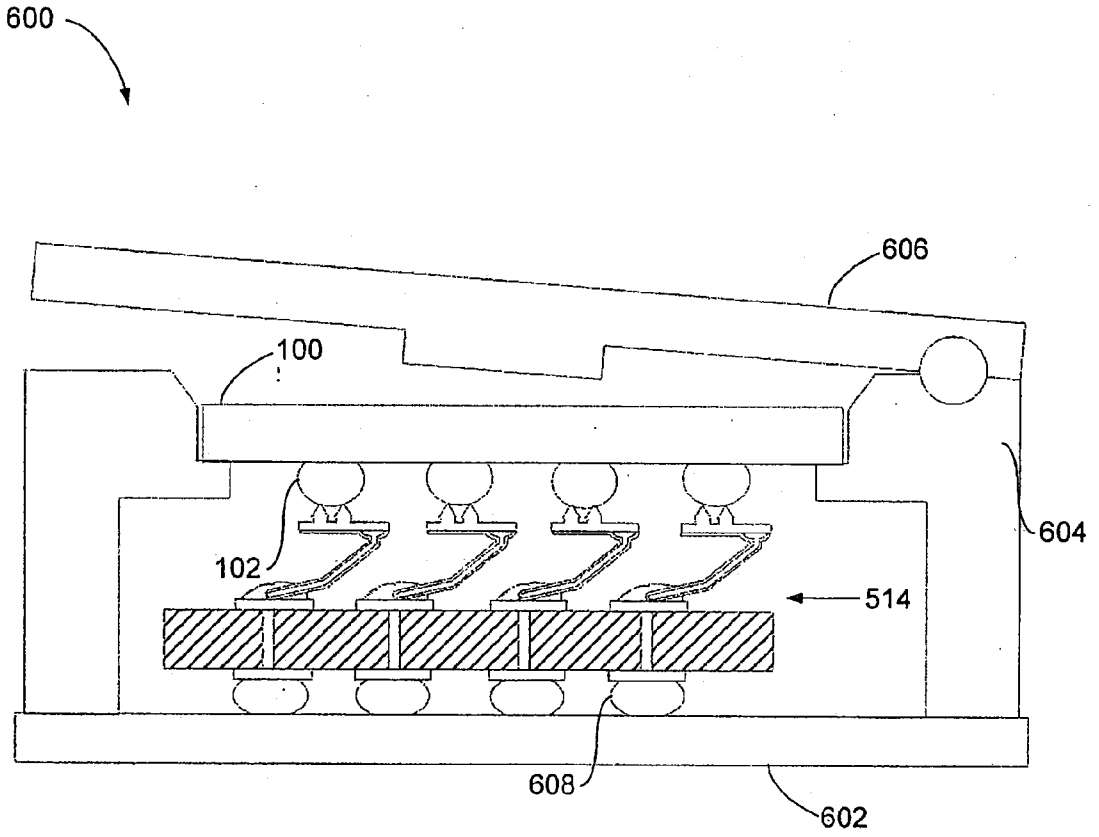


FIG. 6

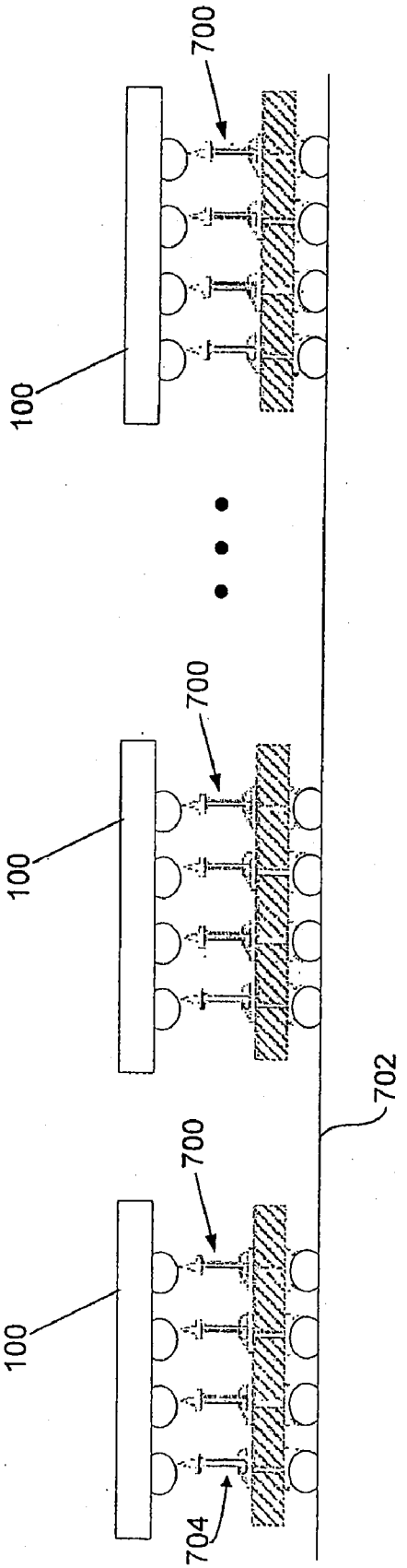


FIG. 7

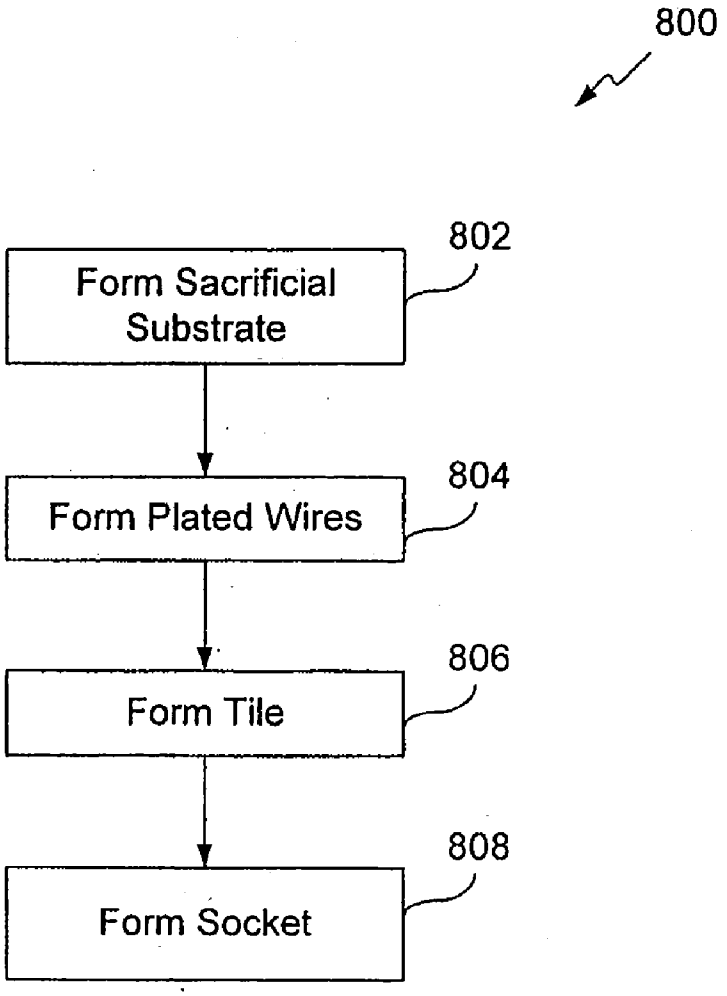

800
802
Form Sacrificial Substrate
804
Form Plated Wires
806
Form Tile
808
Form Socket

FIG. 8

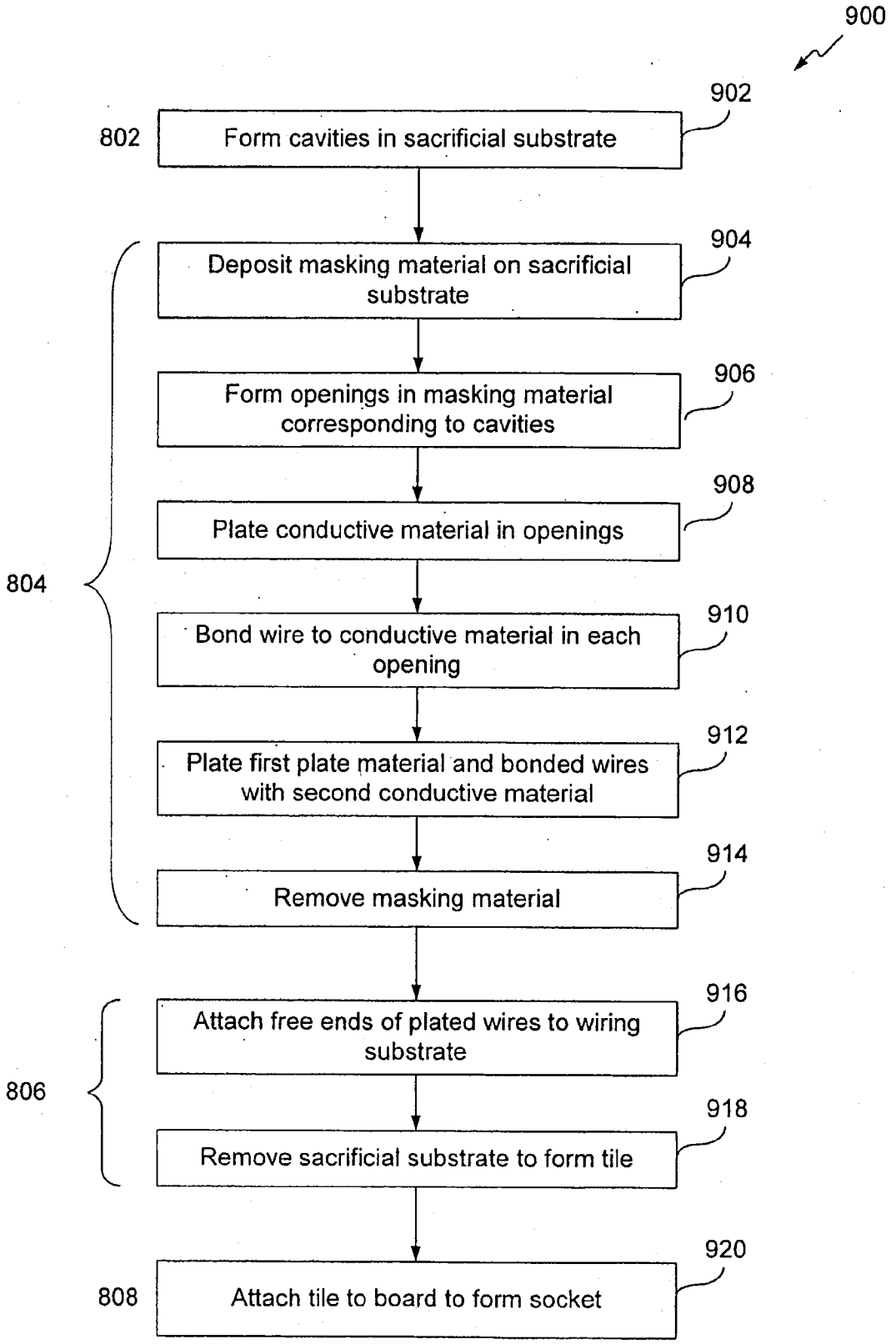

900
902
802
Form cavities in sacrificial substrate
904
Deposit masking material on sacrificial substrate
906
Form openings in masking material corresponding to cavities
908
Plate conductive material in openings
804
910
Bond wire to conductive material in each opening
912
Plate first plate material and bonded wires with second conductive material
914
Remove masking material
916
Attach free ends of plated wires to wiring substrate
806
918
Remove sacrificial substrate to form tile
920
808
Attach tile to board to form socket

FIG. 9

METHOD OF MAKING A SOCKET TO PERFORM TESTING ON INTEGRATED CIRCUITS AND SOCKET MADE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] This invention is directed to a socket for an integrated circuit. More particularly, the socket is a test or burn-in socket for connecting an integrated circuit to a tester for final testing or a burn-in board for burn-in.

[0003] 2. Background Art

[0004] Testing of semiconductor chips is an important operation in semiconductor manufacturing. Different types of tests are performed at different stages of a semiconductor chip manufacturing process. For example, initial tests can be performed on a wafer scale when semiconductor chips have been fabricated on a wafer, but have not yet been diced and packaged. These initial tests may help to identify defective chips prior to performing more expensive and time consuming packaging steps. After the initial testing, a wafer is diced and individual semiconductor chips are packaged. More exacting tests and burn-in operations are then performed on a chip scale to evaluate individual semiconductor chips or groups of multiple chips.

[0005] One technique for performing testing and burn-in operation is to cast individual chips in sockets. Unfortunately, limitations exists in conventional sockets. Conventional sockets maybe expensive to manufacture and somewhat unreliable. Some conventional sockets have also used pogo pins as contact elements. Such pogo pins are unreliable and non-wiping. Pogo pins also limit the pitch of an interconnect structure in a socket. For example, a pitch of less than 40 mils with pogo pins becomes mechanically difficult and prohibitively expensive.

[0006] Therefore, what is needed is a burn-in socket testing device with an easily insertable interconnect structure that is coupled via drop-in, plug-in, or the like connections. The interconnect structure also needs to be manufactured through an inexpensive manufacturing process.

BRIEF SUMMARY OF THE INVENTION

[0007] Embodiments of the present invention provide a method including the steps of fabricating elements (e.g., cavities) in a sacrificial substrate, fabricating a contact structure utilizing the elements in the sacrificial substrate, fabricating an interconnect structure utilizing the contact structure, and fabricating a testing board utilizing the interconnect structure. Other embodiments of the present invention provide a burn-in socket manufactured by this method.

[0008] Still other embodiments of the present invention provide a system for testing an integrated circuit board. The system includes a socket. The socket includes a board, an interconnect structure manufactured to be insertable into the socket, the interconnect structure being coupled to the board. The interconnect structure includes a substrate and first and second pads coupled to the substrate and coupled to each other through vias running through the substrate, the second pads coupling the interconnect structure to the board. The interconnect structure also includes resilient contacts coupled to the first pads, the resilient contacts interacting with the integrated circuit during the testing. The socket also includes a support structure coupled to the board that secures contact between the integrated circuit board and the resilient contacts during the testing.

[0009] Further embodiments, features, and advantages of the present inventions, as well as the structure and operation of the various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0010] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate exemplary embodiments of the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

[0011] FIGS. **1**A and **1**B illustrate a side view and a bottom view, respectively, of a tested flip-chip semiconductor according to embodiments of the present invention.

[0012] FIGS. **2**A and **2**B illustrate a cross-sectional and bottom view, respectively, of a sacrificial substrate according to embodiments of the present invention.

[0013] FIGS. **3**A and **3**B illustrate a cross-sectional and bottom view, respectively, of the sacrificial substrate of FIGS. **2**A and **2**B with a masking material.

[0014] FIGS. **4**A, **4**B, **4**C, and **4**D show processing steps for forming a testing socket according to embodiments of the present invention.

[0015] FIGS. **5**A and **5**B show further processing steps for forming the testing socket according to embodiments of the present invention.

[0016] FIG. **6** shows a still further processing step for forming the testing socket according to embodiments of the present invention.

[0017] FIG. **7** shows a plurality of sockets used to test a plurality of devices on a wafer according to embodiments of the present invention.

[0018] FIG. **8** shows a flowchart depicting an overall method for making a socket according to embodiments of the present invention.

[0019] FIG. **9** shows a flowchart depicting more detailed method steps for the method of FIG. **8**.

[0020] Exemplary embodiments of the present invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number identifies the drawing in which the reference number first appears.

DETAILED DESCRIPTION OF EMBODIMENTS THE INVENTION

[0021] Embodiments of the invention provide an interconnect structure that is inexpensively manufactured and easily insertable into a socket. The interconnect structure is manufactured by forming a sacrificial substrate with cavities that is covered by a masking material having openings corresponding to the cavities. A first plating process is performed by depositing conductive material, followed by coupling wires within the openings and performing another plating process by depositing more conductive material. The interconnect structure is completed by first removing the masking material and sacrificial substrate. Ends of the wires are coupled opposite now-formed contact structures to a board. To complete the socket, a support device is coupled to the board to hold a tested integrated circuit.

Integrated Circuit Semiconductor

[0022] FIGS. **1**A-**1**B show side and bottom views, respectively, of a semiconductor chip **100** (e.g., an integrated circuit (IC)) that is to be tested according to embodiments of the present invention. Semiconductor chip **100** can be packaged

or unpackaged. Semiconductor chip **100** can be, but is not limited to, a flip-chip semiconductor with solder ball contacts **102** (e.g., "controlled collapse chip connection" (also known as "C4")). In general, any type of semiconductor chip and contacts can be used.

Interconnect structure Manufacturing Process

[0023] FIGS. **2-6** illustrate a process of making an interconnect structure (e.g., a tile) **514** (FIG. **5**) for a socket **600** (FIG. **6**) according to embodiments of the present invention.

[0024] FIGS. **2**A-**2**B show cross-sectional and bottom views, respectively, of a sacrificial substrate **200** according to embodiments of the present invention. Sacrificial substrate **200** can be any material into which elements (e.g., cavities) **202** can be formed. As its name implies, sacrificial substrate **200** can be dissolved, etched away, or otherwise removed from a final structure. In some embodiments, a copper or aluminum sheet or foil can be used for sacrificial substrate **200**. In other embodiments, silicon, ceramic, titanium-tungsten, and the like can be used for the sacrificial substrate **200**. As shown, cavities **202** are formed in the sacrificial substrate **200**. In various embodiments, cavities **200** can be formed by embossing, etching, or the like. As will be seen, cavities **200** correspond to contacts **102** on semiconductor chip **100**.

[0025] FIGS. **3**A-**3**B show cross-sectional and bottom views, respectively, of sacrificial substrate **200** with a masking material **300** applied, according to embodiments of the present invention. In some embodiments, masking material **300** can be a photoresist material. As shown, openings **302** are formed in masking material **300**. These openings **302** expose cavities **202** that were formed in FIG. **2**.

[0026] FIGS. **4**A-**4**D show additional processing steps according to embodiments of the present invention. In FIG. **4**A, a conductive material **400** is deposited or plated in openings **302**. In some embodiments, conductive material **400** can be a hard, metallic, and/or electrically conductive material. For example, conductive material **400** can be a rhodium material and a palladium cobalt alloy. As will be seen, conductive material **400** forms a contact tip **402** that is used to contact semiconductor chip **100** during testing. Although shown with two extensions, contact tip **402** can have one or more extensions as required by different specifications and embodiments. In other embodiments, contact tip **402** can be made of a plurality of layered materials, for example a soft gold layer, a nickel layer, and a hard gold layer. In other embodiments an non-exhaustive list of other materials can include: silver, palladium, platinum, rhodium, conductive nitrides, conductive carbides, tungsten, titanium, molybdenum, rhenium, indium, osmium, refractory metals, or the like. Throughout the rest of the specification the term conductive material **400** will be used, and this term is meant to include one or more materials, and if more than one material, layered materials. Conductive material **400** can be deposited in openings **302** using any suitable method. In various embodiments, the deposition method can be electroplating, physical or chemical vapor deposition, sputtering, or the like. The layers that form the contact tip **402** may be deposited in a like manner.

[0027] Although not shown, in various embodiments a release material can be deposited in openings **302** before depositing conductive material **400**. Use of a release material facilitates eventual removal of a contact structure **506** (FIG. **5**B) formed by conductive material **400** from sacrificial substrate **200**. In some embodiments, a release layer can be a layer of aluminum. In still other embodiments, although also not shown, a seed layer consisting of a conductive material can also be deposited in openings **302** before depositing conductive material **400**. In still other embodiments, the seed layer can be deposited as a blanket layer over the entire sacrificial substrate **200** prior to depositing masking material **300**. The seed layer can facilitate electroplating, if electroplating is used to deposit conductive material **400**.

[0028] FIG. **4**B shows a wire **404** being bonded in each opening **302** to conductive material **400** according to embodiments of the present invention. Wire **404** can be bonded using well known wire bonding techniques. One example of a wire bonding technique is found in U.S. Pat. No. 5,601,740 to Eldridge et al., which is incorporated by reference herein in its entirety. In some embodiments, wire **404** can be made of a relatively soft, readily shapeable material, while in other embodiments other types of materials can be used. Examples of materials that can be used for wire **404** include gold, aluminum, copper, platinum, lead, tin, indium, their alloys, or the like. In some embodiments, the diameter of wire **404** can be in the range 0.25 to 10 mils. It is to be appreciated, wire **404** can have other shaped cross-sections, such as rectangular or any other shape.

[0029] FIG. **4**C shows wires **404** and conductive material **400** being plated with a second conductive material **406**. In some embodiments, conductive material **406** is harder than a material making up wire **404** to strengthen the contact structure **506** (FIG. **5**B). Some examples of suitable materials include, nickel, copper, solder, iron, cobalt, tin, boron, phosphorous, chromium, tungsten, molybdenum, bismuth, indium, cesium, antimony, gold, lead, tin, silver, rhodium, palladium, platinum, ruthenium, their alloys, or the like. In some embodiments, conductive material **406** can be 0.2 to 10 mils thick. Conductive material **406** can be deposited on wire **404** using any suitable method. In various embodiments, deposition methods include electroplating, physical or chemical vapor deposition, sputtering, or the like. Example methods for wire bonding a wire and then over plating the wire are described in U.S. Pat. No. 5,476,211 to Khandros, U.S. Pat. No. 5,917,707 to Khandros et al., and U.S. Pat. No. 6,336,269 to Eldridge et al., which are all incorporated by reference herein in their entirety.

[0030] FIG. **4**D illustrates the process after masking material **300** has been removed.

[0031] FIGS. **5**A-**5**B show additional processing steps according to embodiments of the present invention. FIG. **5**A shows free ends **500** of wires **404** having conductive coating **406** being coupled to a wiring substrate **502** through use of coupling material **504**. In various embodiments, the coupling can be done by wiring, soldering, brazing, or the like. In embodiments that the step of coupling free end **500** of wires **404** having conductive coating **406** includes heating, wires **404** and contact structure **506** (FIG. **5**B) can also be heat treated. One example of this is found in U.S. Pat. No. 6,150,186 to Chen et al., which is incorporated herein by reference in its entirety, and which discloses methods for heat treating spring contact structures.

[0032] FIG. **5**B shows a configuration for wiring substrate **502** according to embodiments of the present invention. Wiring substrate **502** can be a ceramic substrate with pads **508** and **510** on opposite sides of wiring substrate **502**. The pads **508** and **510** can be coupled through the use of vias **512** that run through wiring substrate **502**. In other embodiments, wiring substrate **502** can be a printed circuit board or a printed wiring board. As also shown in FIG. **5**B, sacrificial substrate **200** is removed, which can be done by etching, dissolving, or the like, the material forming sacrificial substrate **200**. Another term for the wiring substrate **502** having contact elements **506**, the pads **508**, **510** and vias **512** is an interconnect structure **514**. In some embodiments, interconnect structure **514** can be used to make a test or burn-in socket **600** (FIG. **6**). In various embodiments interconnect structure **514** can be

a modular interconnect structure, a drop-in interconnect structure, a plug-in interconnect structure, or the like, that is easily inserted into the socket **600**, or any other socket.

[0033] Further advantages of the process of making interconnect structure **514** according to the present invention are that the process can be inexpensive and can be performed separately on a interconnect structure. In this way, defective interconnect structures can be identified and removed prior to formation of the socket. This process has further advantages in that a interconnect structure with contact elements arranged at a fine pitch of less than 40 mils, including about 10 mils or less, can be made inexpensively and mass produced. Accordingly, this process is a reliable and inexpensive technique for producing a fine pitch socket.

Socket Forming Process

[0034] FIG. **6** shows a socket **600** in which interconnect structure **514** is coupled and electrically wired to a board **602** (e.g., a test board or socket board) according to embodiments of the present invention. In some embodiments, board **602** can include a support structure **604** with a hinged closing device **606** for holding integrated circuit (IC) **100** during testing. In various embodiments, board **602** can be a test board or burn-in board. Interconnect structure **514** can electrically connected to board **602** in any suitable manner, such as by soldering **608**, pins (not shown), or any other type of contact. For example, the pins can form a friction fit with corresponding holes (not shown). In alternative embodiments, board **602** can be a socket board that is itself plugged into or otherwise attached to a larger test system (not shown).

[0035] FIG. **7** shows an embodiment with multiple interconnect structures **700** coupled to board **702** according to the present invention. Although shown with multiple IC's **100**, in other embodiments one IC **100** with many ball contacts **102** can be tested. In this embodiment, an array of spring contacts **704** for contacting IC **100** is built by coupling a plurality of interconnect structures **700** to board **702** in various configurations depending on the configuration of ball contacts **102**. As discussed above, in various embodiments board **702** can be a test board or burn in board, and a plurality of support structures similar to **604** (not shown in FIG. **7** for convenience) can be secured to board **702** around interconnect structures **700**.

Methodology to Manufacture the Interconnect Structure and Socket

[0036] FIG. **8** shows a method **800** for making sockets according to embodiments of the present invention. At step **802**, a sacrificial substrate is formed with any type or amount of elements formed in the substrate as desired. For example, cavities can be formed as depicted in FIG. **2**. At step **804**, plated wires are formed based on the sacrificial substrate. This can be done through the various methods as described with respect to FIGS. **3-4**. At step **806**, an interconnect structure is formed based on the plated wires. This can be done through the various methods described with respect to FIG. **5**. At step **808**, a socket is formed based on the interconnect structure. Thus can be done through the various methods described with respect to FIGS. **6** and **7**.

[0037] FIG. **9** shows a flowchart depicting a more detailed method **900** for making sockets according to embodiments of the present invention. At step **902**, cavities (e.g. elements or cavities **202**) are formed in a sacrificial substrate (e.g., substrate **200**). At step **904**, a masking material (e.g., masking material **300**) is deposited on the sacrificial substrate. At step **906**, openings (e.g., openings **302**) are formed in the masking material corresponding to the cavities. At step **908**, conductive material (e.g., conductive material **400**) is deposited or plated in the openings. At step **910**, wires (e.g., wires **404**) are coupled to the conductive material. At step **912**, a second conductive material (e.g., conducting material **406**) is deposited or plated on the wires and the first conductive material. At step **914**, the masking material is removed. At step **916**, a coupling material (e.g., coupling material **504**) is used to couple tips (e.g., tips **500**) of the wires having the conductive material to a wiring substrate (e.g., wiring substrate **502**). At step **918**, the sacrificial substrate is removed to form an interconnect structure (e.g., interconnect structure **514** or **700**). At step **920**, the interconnect structure is coupled to a board (e.g., board **602** or **702**) to form a socket (e.g., socket **600**).

CONCLUSION

[0038] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

1-46. (canceled)

47: A burn-in socket for testing an integrated circuit manufactured by the method of:

fabricating contact elements in a sacrificial substrate, the sacrificial substrate including cavities to form tips of the contact elements;

fabricating an interconnect structure by attaching the contact elements to a wiring substrate supporting electrical routing lines, by connecting the electrical routing lines to the contact elements opposite the tips, and by then removing the sacrificial substrate; and

fabricating a socket board configured to hold a semiconductor chip diced from a wafer for test purposes, wherein fabricating the socket board includes attaching said interconnect structure to the socket board.

48: A method comprising the steps of:

providing resilient spring contact elements on a substrate;

fabricating a socket configured to hold a device under test;

providing the substrate in the socket so that when the device under test is placed in the socket, electrical connectors of the device under test can contact the resilient spring contact elements; and

performing burn in testing of the device under test with the device under test supported in the socket.

49: The method of claim **47**, wherein the step of providing resilient spring contact elements includes forming tips for the contact elements in cavities within a sacrificial substrate.

50: The method of claim **49** further comprising the step of etching the sacrificial substrate to form the cavities.

51: The method of claim **49** further comprising the step of forming the sacrificial substrate from copper.

52: The method of claim **49** further comprising the step of forming the sacrificial substrate from aluminum.

53: The method of claim **49** further comprising the step of forming the sacrificial substrate from silicon.

54: The method of claim **49** further comprising the step of forming the sacrificial substrate from ceramic.

55: The method of claim **49**, further comprising the step of forming the sacrificial substrate from titanium-tungsten.

56: The method of claim **48**, wherein the step of providing resilient spring contact elements comprises the steps of:

depositing masking material on the substrate;

forming openings in the masking material corresponding to the elements;

depositing a first conductive material in the openings;

bonding a wire to said conductive material in each of the openings;

depositing a second conductive material over the wires;

removing the masking material.

57: The method of claim **56**, further comprising the step of using rhodium material as the first conductive material.

58: The method of claim **48**, further comprising the step of providing vias in the substrate for electrically connecting the resilient spring contact elements to a board in the socket.

* * * * *