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(54) **Title:** A SIMULATION SYSTEM AND METHOD FOR TESTING A SIMULATION OF A DEVICE AGAINST ONE OR MORE VIOLATION RULES

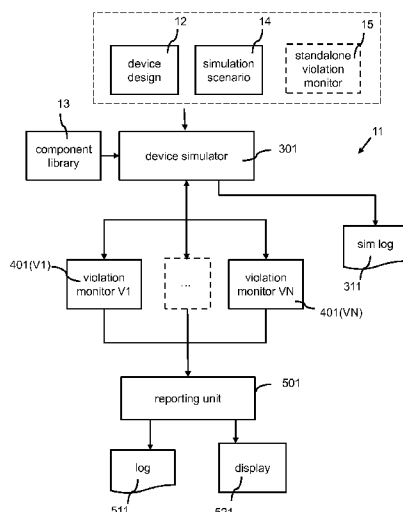


Fig. 2

(57) **Abstract:** A simulation system (11) for testing a simulation of a device against one or more violation rules is described. The simulation system comprises a device simulator (301) for executing the simulation of a device using a device design, a device model and a simulation scenario; and one or more violation monitors (401), one for each violation rule. Each violation monitor comprises a violation information detector (411) for detecting one or more violations of the respective violation rule during the executing of the simulation and, for each violation, determining information representing the respective violation; a violation score unit (421) for calculating, for each violation of the respective violation rule, a violation score in dependence on the information representing the violation and on a violation rule-specific scheme, and a rule score unit (431) for determining, for the respective violation rule, a rule score from the violation scores of the one or more violations during the simulation. The simulation system further comprises a reporting unit (501) for preparing a report of the rule scores associated with the one or more violation rules and for reporting the report to a user. A method (10) of testing a simulation of a device against one or more violation rules is described.

Title : A simulation system and method for testing a simulation of a device against one or more violation rules

Description

Field of the invention

This invention relates to a simulation system, a method and a computer program product for testing a simulation of a device against one or more violation rules.

Background of the invention

During the design process of a new electronic device, such as a new semiconductor device, a designer usually performs a simulation of the real-time performance of the device. Such simulations may e.g. be performed pre- or post-layout of the semiconductor device. During the simulation, the performance of the designed device is tested against one or more of test scenarios by reporting reliability warnings and errors during quasi-stationary (DC) or transient simulations. Such warnings and errors may, for example, be issued by tools for detecting safe operating area (SOA) warnings and errors, errors due to electromigration (EM), errors due to electrostatic discharge (ESD), etc. The reported warnings and errors may be written into a log file which can be checked by the designer by inspection of all entries in the log file. In inspecting the log file, the designer evaluates all reported warnings and errors, uses a statistical analysis of the reported errors and warning, and/or uses some graphical representation indicating the positions of errors and warnings on the device design. However, when designers find such reliability warnings during pre- or post-layout simulation, it may be difficult or even impossible to assess how critical the warnings and errors are, and where to focus attention in adapting the design to overcome the violations. Often, there are too many warnings and errors produced by reliability checks, making it difficult for the designer to review and address all warnings and errors and having a risk that the designer overlooks a critical one. Further, warnings and errors may be due to non-critical transients or may have been introduced as a simulation artefact by the simulator and hence may not be relevant for the actual device, while still requiring attention from the designer.

Summary of the invention

The present invention provides a simulation system and a method for testing a simulation of a device against one or more violation rules, and a computer program product and a violation monitor library component as described in the accompanying claims.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

Figure 1 schematically shows an example of an embodiment of a method;

Figure 2 schematically shows an example of an embodiment of a system;

Figure 3 schematically shows an example of an embodiment of a violation monitor;

Figure 4 schematically shows a simplified example of violations;

Figure 5 schematically shows a further simplified example of violations;

Figure 6 schematically shows an example of reported scores;

Figure 7 schematically shows an exemplary user interaction system;

Figure 8 shows a computer readable medium comprising a computer program product; and

Figure 9 shows another computer readable medium comprising another computer program product.

Detailed description of the preferred embodiments

Figure 1 schematically shows an example of an embodiment of a method 10 of testing a simulation of a device against one or more violation rules and Figure 2 schematically shows an example of an embodiment of a system 11 for testing a simulation of a device against one or more violation rules Vi. The system 11 of Figure 2 is arranged for executing the method 10 of Figure 1. The simulation system 11 comprises a device simulator 301 for executing the simulation of the device using a device design 12, a component library 13 comprising one or more device component models and a simulation scenario 14. The device model 12 may represent a design of the device in terms of at least one or more device components. The device component models in the component library may represent an electrical and/or thermal model of the device component. The simulation system 11 is arranged to build a device model from the device design 12 and the associated one or more device component models from the component library 13 at the start of the simulation, and uses the device model in the simulation. The device simulator 301 is thus arranged to execute the simulation of the device using the device design 12, the device model and the simulation scenario 14. The device simulator 301 is arranged to write simulation results to a simulation log file 311. The simulation is, in this example, an analogue device simulation, where an electrical state of a semiconductor device is simulated using the device design 12 representing a layout of the device components of the design of the semiconductor device, the simulation scenario 14 representing test stimuli and the device model built of device model components in component library 13 describing the behaviour of the device components. The simulation hereto simulates voltages and currents at nodes of the device design and determines voltage levels and current levels during the execution of the simulation. In further examples the simulation may also simulate current densities, rise and/or fall times of signals, temperature levels, occurrences of certain states, and/or other suitable parameters. The simulation system 11 further comprises a plurality of

violation monitors 401, one for each violation rule. Each violation monitor 401 is arranged to detect and score violations of one of the violation rules. Figure 2 shows a simulation system 11 having a plurality violation monitors, indicated as 401(V1), ..., 401(VN). Figure 3 shows a violation monitor, indicated as 401, in detail. In the following, reference may be made to a plurality of violation rules $V_i = V_1, V_2, \dots, V_N$, further referred to as V_i , and respective violation monitors 401(V1), 401(V2), ..., further referred to as 401(V_i). In the following, components associated with a violation rule V_i may be indicated with V_i in between brackets behind the name of the components. In the following non-limiting example, a first violation rule V1 relates to a first violation type and a second violation rule V2 relates to a second violation type. In the example, the first violation rule V1 relates to a violation of a current level threshold of an analogue current at a node of the device and a second violation rule V2 relates to a violation of a voltage level threshold of an analogue voltage at another node of the device. Current levels and voltage levels at certain nodes may, for example, relate to violations which impact reliability, such as electromigration issues, which may be identified with a large current density in excess of an allowed current density that may be a function of a width and/or length of an interconnect, and/or of operating or simulation temperature; electrostatic discharge (ESD) risks, hot carrier injection (HCI), negative bias temperature instability (NBTI) or positive bias temperature instability (PBTI), which may be identifiable with currents into, for example, the device substrate and/or voltages on certain nodes. HCI, NBTI, and PBTI violations may alternatively be identified from e.g. threshold voltage shift of the device or a device component. HCI, NBTI, and PBTI voltage and/or current limits may be a function of the operating or simulation voltage, temperature, and device geometry and type.

Each violation monitor 401(V_i) comprises a violation information detector 411(V_i) for detecting one or more violations of the respective violation rule V_i during the executing of the simulation and for, for each violation, determining information representing the respective violation. In this example, the information representing the respective violation comprises a peak level of the respective violation, a duration of the respective violation and a relaxation duration of the respective violation. Herein, the term "relaxation duration" relates to the time between the start of the violation and the end of the preceding violation of the respective violation rule.

Each violation monitor 401(V_i) further comprises a violation score unit 421(V_i) for calculating, for each violation of the respective violation rule, a violation score in dependence on the information representing the violation and on a violation rule-specific scheme. The violation rule-specific scheme may, for example, take into account the peak level, the duration and the relaxation duration of the violation. The violation rule-specific scheme may further comprise a violation rule-specific weight and/or a device-specific weight. Hereby, the violation scores of different violation types may be scaled to a level of severity. Such scaling may be referred to as normalizing, and the violation scores thus obtained may be referred to as normalized scores. This may facilitate relatively straightforward comparison and/or ranking of violations of different violation types, as the designer does can directly use the normalized scores. The information used for calculating the violation score of a respective violation rule may comprise at least a first violation parameter of a violation parameter group comprising a violation start time, a violation stop time, a violation

duration, a violation count, a violation peak amplitude and a violation relaxation duration relative to a preceding violation, and the violation score is calculated using a violation rule-specific function of at least the first violation parameter. The first violation parameters may for example be tested against a respective threshold value, e.g. the first violation rule relating to the current at a certain node exceeding a current threshold level.

The information used for calculating the violation score of a respective violation rule may further comprise at least a second violation parameter. An exemplary violation rule-specific scheme may, for example, be described as follows. Upon the detection of a next violation $n+1$ of the i -th violation rule V_i , the corresponding violation score unit 421(V_i) calculates a violation score ΔSc from the violation information using the violation rule-specific scheme defined by the following formula:

$$\Delta Sc(V_i(n+1)) = \frac{(P(V_i(n+1)) - Thr(V_i))}{Thr(V_i)} * No(V_i) * f(D(V_i(n+1)), R(V_i(n+1)), V_i) * Vt(DT, V_i)$$

with:

$\Delta Sc(V_i(n+1))$: violation score calculated for $(n+1)^{th}$ violation of violation rule V_i ,

$P(V_i(n+1))$: peak value of V_i , $(n+1)^{th}$ violation of violation rule V_i ,

$Thr(V_i)$: threshold for violation of violation rule V_i ,

$No(V_i)$: violation type-specific weight for type of violation rule V_i (relative weight of this violation type against other violation types),

$Vt(DT, V_i)$: device class-specific weight for this violation type for device component DT (correction factor to $No(V_i)$ for this device component class);

$D(V_i(n+1))$: duration of V_i $(n+1)^{th}$ violation of violation rule V_i ,

$R(V_i(n+1))$: relaxation duration between n^{th} and $(n+1)^{th}$ violation of violation rule V_i ,

and wherein function $f(.)$ is a function defining a raw score as a function of the duration, relaxation duration and violation type. The function $f(.)$ may, for example, be linear with the duration of the violation and inversely proportional with the relaxation duration for one type of violation, whereas it is only dependent on the duration and independent of relaxation duration for another type of violation. The function $f(.)$ may, as another example, be proportional to the duration if the violation and independent on relaxation duration for again another type.

The information may thus comprise at least a first violation parameter and a second violation parameter of a violation parameter group comprising a violation start time, a violation stop time, a violation duration, a violation count, a violation peak amplitude and a violation relaxation duration relative to a preceding violation, and each violation score is calculated using a violation rule-specific function of at least the first violation parameter and the second violation parameter. At least one of the first and second violation parameters are tested against a respective threshold value, e.g. the first violation rule may relating to the current at a certain node exceeding a current threshold level, an associated first and second violation parameter may be the peak amplitude of the current during the violation and the duration of the violation respectively, and the violation score may be calculated using the peak amplitude of the current during the violation, the current

threshold level, and the duration, wherein the calculation comprises calculating a difference between the peak amplitude and the current threshold level, and multiplying the difference with the duration.

Although violation scores are calculated using a violation rule-specific scheme, different violation rule-specific schemes may use a standardized formula, for example, the formula for ΔSc shown above, wherein only the coefficients are violation rule-specific (e.g., $Thr(V_i)$, $No(V_i)$, $Vt(DT, V_i)$). The coefficients may, for example, be defined by a user, such as a designer, to facilitate scoring according to user needs.

Each violation monitor 401(V_i) further comprises a rule score unit 431(V_i) for determining, for the respective violation rule, a rule score from the violation scores of the one or more violations during the simulation.

In this example, each rule score unit 431(V_i) calculates a respective rule score $Sc(V_i)$ by adding the violation score to the previous rule score:

$$Sc(V_i(n+1)) = Sc(V_i(n)) + \Delta Sc(V_i(n+1))$$

where the previous rule score is the rule score as determined until the detection of the (N+1)th violation of the violation rule V_i .

Thus, each violation rule V_i may be associated with a violation of a different violation type of a plurality of violation types and the calculating of the violation score using a weighting factor $No(V_i)$ dependent on the violation type. The violation type-specific weight $No(V_i)$ may allow to normalize errors of one violation type relative to errors of another violation type, whereby violations of different types may easily be compared, ranked and/or filtered.

Each violation rule V_i may be associated with a device class-specific weight $Vt(DT, V_i)$. The device class-specific weight may for example be selected according to the device design by the simulation system or method, or by a user. Using device class-specific weights $Vt(DT, V_i)$ may be seen as a correction to the violation type-specific weight $No(V_i)$, to effectively adjust the violation type-specific weight in dependence on the device class, to accommodate for different levels of criticality of the same violation type for different classes of devices.

The simulation system 11 in Fig. 2 further comprises a reporting unit 501 for preparing a report of the rule scores associated with the one or more violation rules and for reporting the report to a user. The reporting unit may hereto obtain the rule scores V_i from all violation monitors 401(V_i) and, for example, sort or filter them to report, for example, only the most critical violations. The sorting may relate to putting the rule scores in order of criticality. The filtering may relate to only reporting rule scores when a certain condition is met, for example, when a rule score exceeds a certain threshold, with the certain threshold, for example, being controlled by the designer.

The reporting unit 501 may report real-time while running the simulation, and/or at end of simulation. The reporting unit 501 may further report individual violation scores of the one or more detected violations and/or (at least part of) the information representing the detected violations. This may allow the designer to do a detailed inspection of individual violations of, for example, the

highest-ranked violation type and to adapt the design of the semiconductor device to make it robust against such violations.

The reporting unit 501 is arranged to write the selection of the rule scores to a log file 511. The rule scores of different type of violations may thus be gathered in the log file so that a user, for example, the designer, can inspect them offline. Subsequent log processing may sort violations by rule score, for example, in order of importance of the violating event, and/or filter violations by rule score, for example, with filtering dependent on the stage in the design and simulation process. The scoring may thus allow the designer to pay attention to the highest priority violation(s), while taking away the burden of investigating many individual warnings or errors of all kinds of violation types from the log file. Once the designer has fixed the highest priority violation, he may find that one or more other violations of other violation types have also been fixed. If not, he may continue to fix the next highest priority violation set.

Hereby, a way is provided for the designer to quantify the risk of not meeting reliability thresholds from a ranking by criticality of run time errors, combining any type of reliability issues (device degradation, line degradation, thermal effects). The violation monitors may comprise a plurality of different tools for checking different types of violations, such as, for example, an ESD checker, a Safe Operating Area checker, a thermal events checker, a stress migration or electromigration checker, a substrate currents checker. These different tools may provide warning and errors to a single reporting unit 501, for obtaining a single violation database with a normalized rule score for each violated rule.

The violation monitor 401 may be part of the device simulator unit 301. Alternatively, the violation monitor and the device simulator unit may be separate units.

The detection and scoring of violations may be built inside the device component model or as a standalone component. The reporting may occur during DC or transient simulation.

Figure 1 schematically shows a method 10 of testing a simulation of a device against one or more violation rules that may be performed by the simulation system 11. The method comprises providing 100 a device design, a component library and a simulation scenario; executing 300 a simulation of the device using the device design, the component library and the simulation scenario; detecting and scoring 400 one or more violations of the respective violation rule V_i during the executing of the simulation; preparing 500 a report of rule scores associated with the one or more violation rules and reporting 550 the report. The report is reported real-time, i.e., during the execution of the simulation, allowing a user to view 550 the report during the simulation.

The detecting and scoring 400 of the one or more violations of the respective violation rule V_i during the executing of the simulation comprises initializing 405 a plurality of rule scores at the start of the simulation; detecting 410, for each violation rule of the plurality of violation rules, one or more violations of the respective violation rule during the executing of the simulation and determining information representing the violation of the respective violation rule; calculating 420, for each violation of each violation rule of the plurality of violation rules, a violation score in dependence on the information representing the violation of the respective violation rule during the executing of the simulation; and determining 430, for each violation rule of the plurality of violation rules, a

respective rule score from the violation scores of the one or more violations during the simulation. The detecting 410 comprises detecting at least a first violation parameter and a second violation parameter of a violation parameter group comprising a violation start time, a violation stop time, a violation duration, a violation peak amplitude and a violation relaxation duration relative to a preceding violation, wherein the information comprises at least the first violation parameter and the second violation parameter as detected, and each violation score is calculated using a violation rule-specific function of at least the first violation parameter and the second violation parameter.

The device model comprises the violation monitor(s) for one or more violation rules in one example. The device design comprises the violation monitor(s) for one or more violation rules in another example. In another example, the method comprises, prior to executing the simulation 300 of the device, connecting 150 a stand-alone violation monitor 15 to the device design or to the device model. The stand-alone violation monitor 15 is arranged to, for one violation rule, perform the detecting 410 of the violations of the respective violation rule during the executing of the simulation and the determining of the information representing the violation of the respective violation rule; the calculating 420 of the violation score in dependence on the information for representing the violation of the respective violation rule during the executing of the simulation; and the determining 430 of the rule score from the violation scores during the simulation.

Figure 4 schematically shows a simplified example of violations of a first violation rule. In this example, the first violation rule V1 relates to a first violation type corresponding to a violation of a current level threshold TV1 of an analogue current at a node of the device. The reference to V1 in duration D(.), peak level P(.), relaxation duration R(.), and log time L(.) is suppressed in Figure 4 in order not to obscure the figure. The simulated current level, indicated with its signal amplitude S1 along the vertical axis, is indicated as a function of time, as indicated with t along the horizontal axis, with trace 1000.

Figure 4 shows an example wherein the simulated current violates the first violation rule 3 times over the shown period of time. A first violation occurs with a duration D(n) with peak level P(n) until time L(n). At time L(n), the violation score of the first violation is calculated from the violation-specific rule associated with the first violation rule, and the rule score of the first violation rule is updated with the violation score and reported. As an example, calculating the violation score ΔSc , may be done using the formula presented above with $f(.)$ being proportional to the violation duration by using $f(D(V_i(n)), R(V_i(n)), V_i) = 0.5 * D(n)$, whereby the violation score ΔSc corresponds to a triangular approximation of a measure of the area between the curve 1000 and the threshold TV1, as schematically indicated by triangle T(n). A second violation occurs after a relaxation duration R(n+1). The second violation has a duration D(n+1) with peak level P(n+1) until time L(n+1). At time L(n+1), the violation score of the second violation is calculated using triangular approximation via triangle T(n+1), and the rule score of the first violation rule is updated with the violation score and reported. At the end of a subsequent third violation at time L(n+2), the violation score of the third violation is calculated, and the rule score of the first violation rule is updated with the violation score and reported.

Figure 5 schematically shows a simplified example of violations of a second violation rule. In this example, the second violation rule V2 relates to a second violation type corresponding to a violation of a voltage level threshold TV2 of a voltage at another node of the device. The simulation starts with a rule score initialized at $Sc(V2) = 0$. The voltage corresponds to a drain-source voltage over a low-voltage transistor. The threshold voltage TV2 is 1.35 V. The reference to V2 in duration D(.), peak level P(.), relaxation duration R(.), and log time L(.) is suppressed in Figure 5 in order not to obscure the figure. The simulated voltage level, indicated with its signal amplitude S2 along the vertical axis, is indicated as a function of time, as indicated with t along the horizontal axis, with trace 1100. Figure 5 shows an example wherein the simulated voltage violates the second violation rule 3 times over the shown period of time. A first violation occurs from time 150 ns to 250 ns with a duration $D(n)=250-150=100$ ns and peak level $P(n)=1.9$ V, corresponding to a 40% voltage overshoot. At time $L(n)=250$ ns, the violation score of the first violation is calculated from the violation-specific rule associated with the second violation rule as $\Delta Sc(V2(n)) = 100 \text{ ns} \times 40\% = 40$, and the rule score of the second violation rule is updated with the violation score to $Sc(V2) = 0 + 40 = 40$ and reported. In this example, the second violation occurs after a relaxation duration $R(n+1)$. The second violation occurs from time 250 ns to 300 ns, i.e. a duration $D(n+1)=50$ ns, with peak level $P(n+1)$ corresponding to a 30% voltage overshoot. At time $L(n+1)$, the violation score of the second violation is calculated as $\Delta Sc(V2(n+1)) = 50 \text{ ns} \times 30\% = 15$, and the rule score of the first violation rule is updated with the violation score to $Sc(V2) = 40 + 15 = 55$ and reported. At the end of a subsequent third violation, from time 350 ns to 360 ns, at a peak level $P(n+2)$, corresponding to a 30% voltage overshoot, the violation score of the third violation is calculated as $\Delta Sc(V2(n+2)) = 10 \text{ ns} \times 30 = 3$, and the rule score of the second violation rule is updated with the violation score to $Sc(V2) = 55 + 3 = 58$ and reported.

In other embodiments, other methods of computing the score may be used, for example, but not limited to, a count of the violations of each type for each device of interest.

Figure 6 schematically shows an example of reporting scores on a display 521, as displayed to a designer. Figure 6 shows a window 540 with a header bar indicating a window title as VREP and symbols “_” and “X” for minimizing or closing the window. The window 540 displays a first list 542 of entries indicating the name of the violation rules, here schematically indicated as VIOL1, ..., VIOL6, for all non-zero rule scores associated with six violation rules V1, ..., V6. The entries are shown and sorted in order of decreasing rule score. The names of the violation rules may for example provide a textual description of the violation type by referring to the type of simulated parameter, such as “current violation”, “voltage violation”, “temperature violation”. The names of the violation rules may for example alternatively or additionally provide a textual description of the violation type by referring to the type of physical effect, such as “ESD risk”, “NBTI risk”. In this example, a fifth violation rule V5 named VIOL5 shows the highest rule score, $Sc(V5)=103$, a second violation rule V2 named VIOL2 has a second-highest rule score ($Sc(V2)=58$), while violation rule V4 is not shown as it has a score $Sc(V4)=0$. As indicated with the shading in the first list 542 in Figure 6, violation rule V5 is selected, and a second list 542 shows the individual violation scores ΔSc of the three violations of violation rule V5 together with the information,

representing start and stop time and peak value, of these individual scores. Another box 546 indicates that violation rule V5 is associated with a source voltage of a device component labelled "MOSFET32". The designer can thus easily recognize that violation rule V5 has the largest rule score and needs to be addressed with the highest priority. The designer can further recognize that, for this violation rule, violations have occurred with different violation scores, which may be of relevance for the designer in order to improve the device component "MOSFET32". A further window (not shown) may show the circuit layout of the semiconductor device, wherein device component "MOSFET32" is highlighted.

Figure 7 schematically shows an exemplary user interaction system 2000 having a programmable processor 2005. The user interaction system 2000 is shown to be a personal computer, but may be any type of suitable user interaction system 2000. The programmable processor may comprise one or more components of system 11. The user interaction system 2000 further comprises a storage unit 2007, a user input 2003 and a display 2006, which may be the same as display 521 in Fig. 2 or an additional display. The user input 2003 allows the user to input user data and user instructions 2004 to the processor 2005 by e.g. using a keyboard 2001 or a mouse 2002. Also, although not shown, the display 2006 may comprise a touch-sensitive surface for enabling the user to provide user data and user instructions to the user input 2003 by means of touching the display 2006. The processor 2005 is arranged to perform any one of the methods according to the invention, to receive user data and user instructions 2004, to present visual information on the display 2006 and to communicate with a data I/O device 2009, such as an optical disc drive or a solid state reader/writer. The processor 2005 is arranged to cooperate with the storage unit 2007, allowing storing and retrieving information on the storage unit 2007, such as the violation information of one or more violations, the violation scores and/or the rule scores determined during the execution of the simulation. The user interaction system 2000 may further comprise a communication channel 2008 allowing the processor 2005 to connect to an external cloud 2500 for communicating with other devices in the cloud. The external cloud may e.g. be the Internet. The user interaction system 2000 may allow generation, inspection and further processing of the violation information of one or more violations, the violation scores and/or the rule scores by a user. The processor 2005 may also be arranged to retrieve the violation information of one or more violations, the violation scores and/or the rule scores determined during further executions of the simulation from the storage unit 2007, or from another device in the cloud 2500, and generate a report by the processor 2005. The processor 2005 may be capable to read, using the data I/O device 2009, a computer readable medium comprising a program code. The processor 2005 may be capable to read, using the data I/O device 2007, a computer readable medium comprising a computer program product comprising instructions for causing the user interaction system 2000 to perform a method of testing a simulation of a device against new or more violation rules using a device design, a component library and a simulation scenario, the method comprising: executing the simulation of the device using the device design, the component library and the simulation scenario; detecting, for each violation rule of the plurality of violation rules, a violation of the respective violation rule during the executing of the simulation and determining information

representing the violation of the respective violation rule; calculating, for each violation rule of the plurality of violation rules, a violation score in dependence on the information representing the violation of the respective violation rule during the executing of the simulation; determining, for each violation rule of the plurality of violation rules, a respective rule score from the violation scores during the simulation; preparing a report of the rule scores associated with the one or more violation rules. The report may be reported to the user as visual information on the display and/or written to a log file and/or displayed on the display.

Figure 8 shows a computer readable medium 3000 comprising a computer program product 3100, the computer program product 3100 comprising instructions for causing a processor apparatus to perform a method of testing a simulation of a device against new or more violation rules using a device design, a component library and a simulation scenario, the method comprising: executing the simulation of the device using the device design, the component library and the simulation scenario; detecting, for each violation rule of the plurality of violation rules, a violation of the respective violation rule during the executing of the simulation and determining information representing the violation of the respective violation rule; calculating, for each violation rule of the plurality of violation rules, a violation score in dependence on the information representing the violation of the respective violation rule during the executing of the simulation; and determining, for each violation rule of the plurality of violation rules, a respective rule score from the violation scores during the simulation. The computer program product 3100 may further comprise instructions for causing the processor apparatus to perform preparing a report of the rule scores associated with the one or more violation rules. The computer program product 3100 may be embodied on the computer readable medium 3000 as physical marks or by means of magnetization of the computer readable medium 3000. However, any other suitable embodiment is conceivable as well. Furthermore, it will be appreciated that, although the computer readable medium 3000 is shown in Figure 8 as an optical disc, the computer readable medium 3000 may be any suitable computer readable medium, such as a hard disk, solid state memory, flash memory, etc., and may be non-recordable or recordable. .

Figure 9 shows another computer readable medium 4000 comprising another computer program product 4100, the computer program product 4100 comprising a violation monitor library component for use in a simulation of a performance of a device component on a processor system, the violation monitor library component comprising instructions for causing the processor system to perform detecting a violation of a violation rule during the executing of the simulation; determining information representing the violation of the violation rule during the executing of the simulation during the executing of the simulation; calculating a violation score in dependence on the information representing the violation of the violation rule during the executing of the simulation; determining an rule score from the violation score during the executing of the simulation; and providing the rule score to a program function executing the violation monitor library component. The computer program product 4100 may be embodied on the computer readable medium 4000 as physical marks or by means of magnetization of the computer readable medium 4000. However, any other suitable embodiment is conceivable as well. Furthermore, it will be appreciated that,

although the computer readable medium 4000 is shown in Figure 9 as an optical disc, the computer readable medium 4000 may be any suitable computer readable medium, such as a hard disk, solid state memory, flash memory, etc., and may be non-recordable or recordable. The computer program product 4100 thus comprises a violation monitor library component, which may be used in a device simulation. The violation monitor library component may be a standalone library component, or integrated in a device library component, representing a simulation of a performance of a device or a device component. Thus, in an embodiment, the violation monitor library component is part of a device library component arranged to simulate the device component. In another embodiment, the library component is arranged to cooperate with a device library component arranged to simulate the device component.

The invention may thus be implemented in a computer program for running on a computer system, at least including code portions for performing steps of a method according to the invention when run on a programmable apparatus, such as a computer system or enabling a programmable apparatus to perform functions of a device or system according to the invention. The computer program may for instance include one or more of: a subroutine, a function, a procedure, an object method, an object implementation, an executable application, an applet, a servlet, a source code, an object code, a shared library/dynamic load library and/or other sequence of instructions designed for execution on a computer system. The computer program may be provided on a data carrier, such as a CD-rom or diskette, stored with data loadable in a memory of a computer system, the data representing the computer program. The data carrier may further be a data connection, such as a telephone cable or a wireless connection.

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, other formulas may be used for the calculation of the violation score ΔSc and/or the calculation of the rule score Sc . For example, the connections may be any type of connection suitable to transfer signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise the connections may for example be direct connections or indirect connections.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

The term "program," as used herein, is defined as a sequence of instructions designed for execution on a computer system. A program, or computer program, may include a subroutine, a function, a procedure, an object method, an object implementation, an executable application, an applet, a servlet, a source code, an object code, a shared library/dynamic load library and/or other sequence of instructions designed for execution on a computer system.

Some of the above embodiments, as applicable, may be implemented using a variety of different information processing systems. For example, although Figure 7 and the discussion thereof describe an exemplary information processing architecture, this exemplary architecture is presented merely to provide a useful reference in discussing various aspects of the invention. Of course, the description of the architecture has been simplified for purposes of discussion, and it is just one of many different types of appropriate architectures that may be used in accordance with the invention. Those skilled in the art will recognize that the boundaries between logic blocks are merely illustrative and that alternative embodiments may merge logic blocks or circuit elements or impose an alternate decomposition of functionality upon various logic blocks or circuit elements.

Thus, it is to be understood that the architectures depicted herein are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality. In an abstract, but still definite sense, any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

Furthermore, those skilled in the art will recognize that boundaries between the functionality of the above described operations merely illustrative. The functionality of multiple operations may be combined into a single operation, and/or the functionality of a single operation may be distributed in additional operations. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments.

All or some of the software described herein may be received from elements of system 11, for example, from computer readable media such as memory 2007 or other media on other computer systems. Such computer readable media may be permanently, removably or remotely coupled to an information processing system such as system 11. The computer readable media may include, for example and without limitation, any number of the following: magnetic storage media including disk and tape storage media; optical storage media such as compact disk media (e.g., CD-ROM, CD-R, etc.) and digital video disk storage media; nonvolatile memory storage media including semiconductor-based memory units such as FLASH memory, EEPROM, EPROM, ROM; ferromagnetic digital memories; MRAM; volatile storage media including registers, buffers or caches, main memory, RAM, etc.; and data transmission media including computer networks, point-to-point telecommunication equipment, and carrier wave transmission media, just to name a few.

In one embodiment, system 11 is a computer system such as a personal computer system. Other embodiments may include different types of computer systems. Computer systems are information handling systems which can be designed to give independent computing power to one or more users. Computer systems may be found in many forms including but not limited to

mainframes, minicomputers, servers, workstations, personal computers, notepads, personal digital assistants, electronic games, automotive and other embedded systems, cell phones and various other wireless devices. A typical computer system includes at least one processing unit, associated memory and a number of input/output (I/O) devices.

A computer system processes information according to a program and produces resultant output information via I/O devices. A program is a list of instructions such as a particular application program and/or an operating system. A computer program is typically stored internally on computer readable storage medium or transmitted to the computer system via a computer readable transmission medium. A computer process typically includes an executing (running) program or portion of a program, current program values and state information, and the resources used by the operating system to manage the execution of the process. A parent process may spawn other, child processes to help perform the overall functionality of the parent process. Because the parent process specifically spawns the child processes to perform a portion of the overall functionality of the parent process, the functions performed by child processes (and grandchild processes, etc.) may sometimes be described as being performed by the parent process.

Also, the invention is not limited to physical devices or units implemented in non-programmable hardware but can also be applied in programmable devices or units able to perform the desired device functions by operating in accordance with suitable program code. Furthermore, the devices may be physically distributed over a number of apparatuses, while functionally operating as a single device. Also, devices functionally forming separate devices may be integrated in a single physical device.

However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps than those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

1. A simulation system (11) for testing a simulation of a device against one or more violation rules, the simulation system comprising:
 - a device simulator (301) for executing the simulation of a device using a device design, a device model and a simulation scenario; and
 - one or more violation monitors (401), one for each violation rule, each violation monitor comprising:
 - a violation information detector (411) for detecting one or more violations of the respective violation rule during the executing of the simulation and, for each violation, determining information representing the respective violation,
 - a violation score unit (421) for calculating, for each violation of the respective violation rule, a violation score in dependence on the information representing the violation and on a violation rule-specific scheme , and
 - a rule score unit (431) for determining, for the respective violation rule, a rule score from the violation scores of the one or more violations during the simulation.
2. A simulation system according to claim 1, further comprising a reporting unit (501) for preparing a report of the rule scores associated with the one or more violation rules.
3. A simulation system according to claim 2, the reporting unit (501) being arranged to perform a filtering and/or a sorting on the rule scores in preparing the report.
4. A simulation system according to claim 2 or 3, the reporting unit (501) being arranged to write the selection of the rule scores to a log file (511).
5. A simulation system according to any one of the preceding claims, the one or more violation monitors being part of the device simulator unit.
6. A simulation system according to any one of claims 1 – 4, the one or more violation monitors and the device simulator unit being separate units.
7. A simulation system according to any one of the preceding claims, each violation rule being associated with a violation of a different violation type of a plurality of violation types, the calculating of the violation score using a weighting factor dependent on the violation type.
8. A simulation system according to any one of the preceding claims, the information comprising at least a first violation parameter and a second violation parameter of a violation parameter group comprising a violation start time, a violation stop time, a violation duration, a violation count, a violation peak amplitude and a violation relaxation duration relative to a preceding violation,
 - each violation score being calculated using a violation rule-specific function of at least the first violation parameter and the second violation parameter.
9. A method (10) of testing a simulation of a device against one or more violation rules, the method comprising:
 - providing (100) a device design, a component library and a simulation scenario;
 - executing (300) the simulation of the device using the device design, the component library and the simulation scenario;

detecting (410), for each violation rule of the plurality of violation rules, one or more violations of the respective violation rule during the executing of the simulation and determining information representing the violation;

calculating (420), for each violation of each violation rule of the plurality of violation rules, a violation score in dependence on the information representing the violation of the respective violation rule during the executing of the simulation; and

determining (430), for each violation rule of the plurality of violation rules, a respective rule score from the violation scores of the one or more violations during the simulation.

10. A method according to claim 9, further comprising preparing (500) a report of the rule scores associated with the one or more violation rules.

11. A method according to claim 10, further comprising reporting (510) the report.

12. A method according to any one of claims 10 – 11, the preparing (500) the report comprising filtering and/or a sorting of the rule score.

13. A method according to any one of claims 10 – 12, further comprising writing the report into a log file and/or presenting the report on a display for presenting the report to a user.

14. A method according to any one of claims 9 – 13, each violation rule being associated with a violation of a different violation type of a plurality of violation types, the calculating of the violation score using a weighting factor dependent on the violation type.

15. A method according to any one of claims 9 – 14, the detecting (410) comprising detecting at least a first violation parameter and a second violation parameter of a violation parameter group comprising a violation start time, a violation stop time, a violation duration, a violation count, a violation peak amplitude and a violation relaxation duration relative to a preceding violation,

the information comprising at least the first violation parameter and the second violation parameter as detected, and

each violation score being calculated using a violation rule-specific function of at least the first violation parameter and the second violation parameter.

16. A method according to any one of claims 9 – 15 wherein:

the method comprises, prior to executing (300) the simulation of a device, connecting (150) at least one violation monitor to the device design or to the device model; and

each violation monitor (15) being arranged to provide for one violation rule of the one or more violation rules :

- the detecting (410) of the violations of the respective violation rule during the executing of the simulation and the determining of the information representing the violation of the respective violation rule,

- the calculating (420) of the violation score in dependence on the information for representing the violation of the respective violation rule during the executing of the simulation, and

- determining (430) the rule score from the violation scores during the simulation.

17. A computer program product (3100) comprising instructions for causing a processor system to perform a method of testing a simulation of a device against one or more violation rules using a device design, a component library and a simulation scenario, the method comprising:

executing the simulation of the device using the device design, the component library and the simulation scenario;

detecting, for each violation rule of the plurality of violation rules, a violation of the respective violation rule during the executing of the simulation and determining information representing the violation of the respective violation rule;

calculating, for each violation rule of the plurality of violation rules, a violation score in dependence on the information representing the violation of the respective violation rule during the executing of the simulation; and

determining, for each violation rule of the plurality of violation rules, a respective rule score from the violation scores during the simulation. .

18. A computer program product (4100) comprising a violation monitor library component for use in a simulation of a performance of a device component on a processor system, the violation monitor library component comprising instructions for causing the processor system to perform:

detecting a violation of a violation rule during the executing of the simulation;

determining information representing the violation of the violation rule during the executing of the simulation during the executing of the simulation;

calculating a violation score in dependence on the information representing the violation of the violation rule during the executing of the simulation;

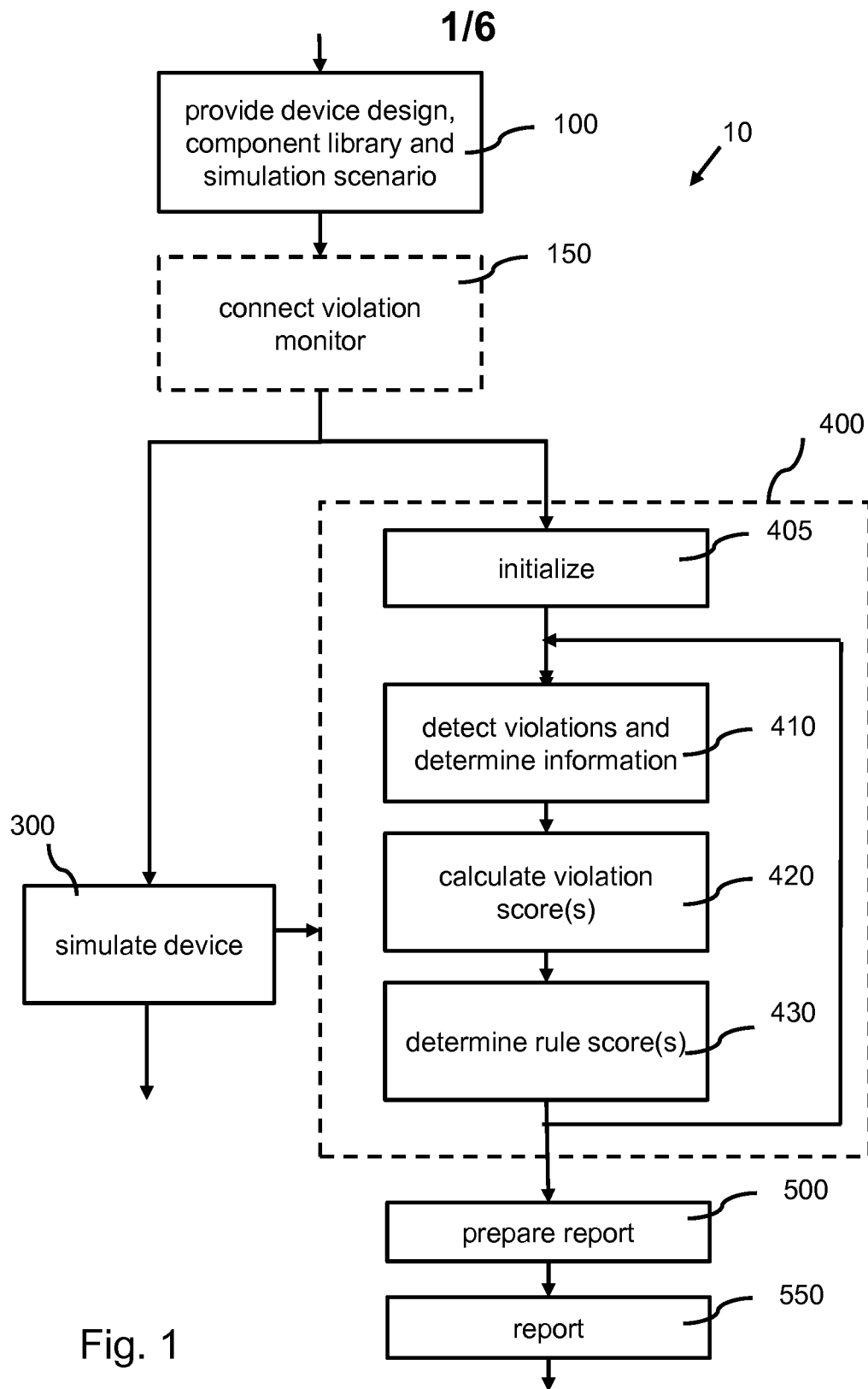
determining a rule score from the violation score during the executing of the simulation;

and

providing the rule score to a program function executing the violation monitor library component.

19. A computer program product (4100) according to claim 18, the violation monitor library component being part of a device library component arranged to simulate the device component.

20. A computer program product (4100) according to claim 18, the library component being arranged to cooperate with a device library component arranged to simulate the device component.



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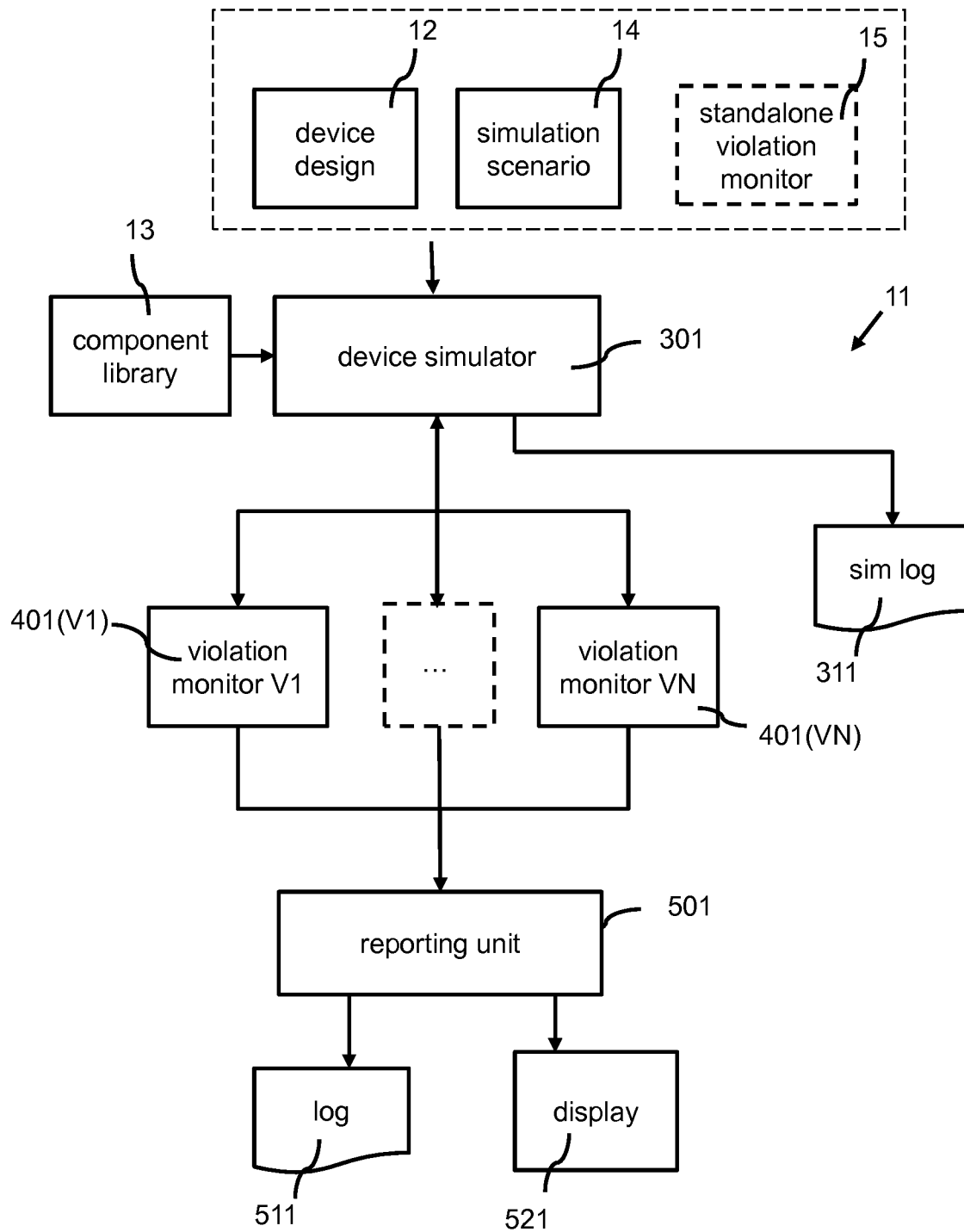


Fig. 2

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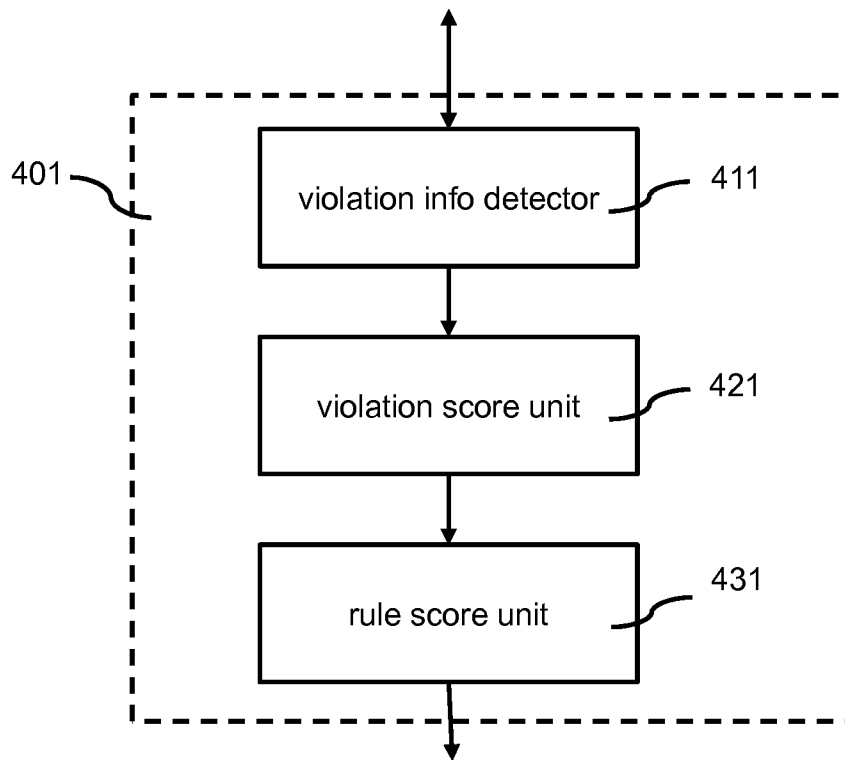


Fig. 3

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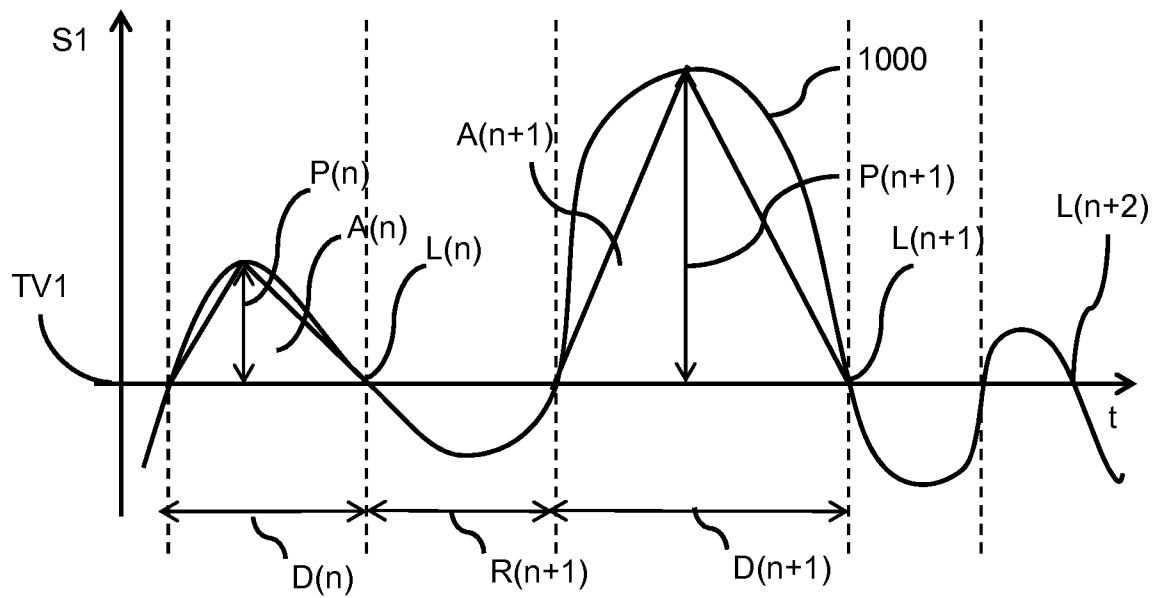


Fig. 4

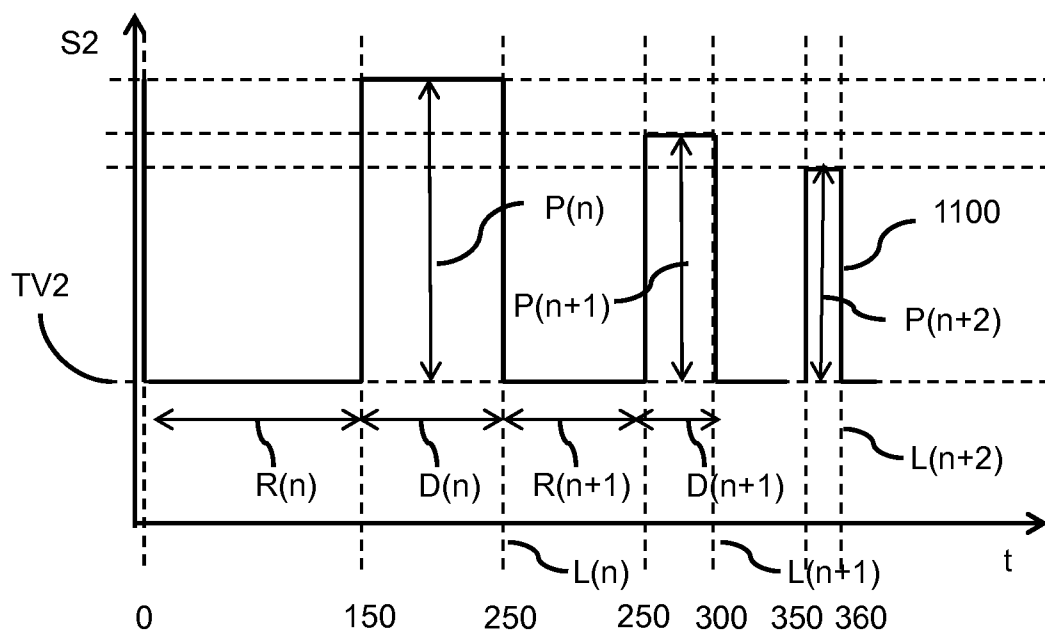


Fig. 5

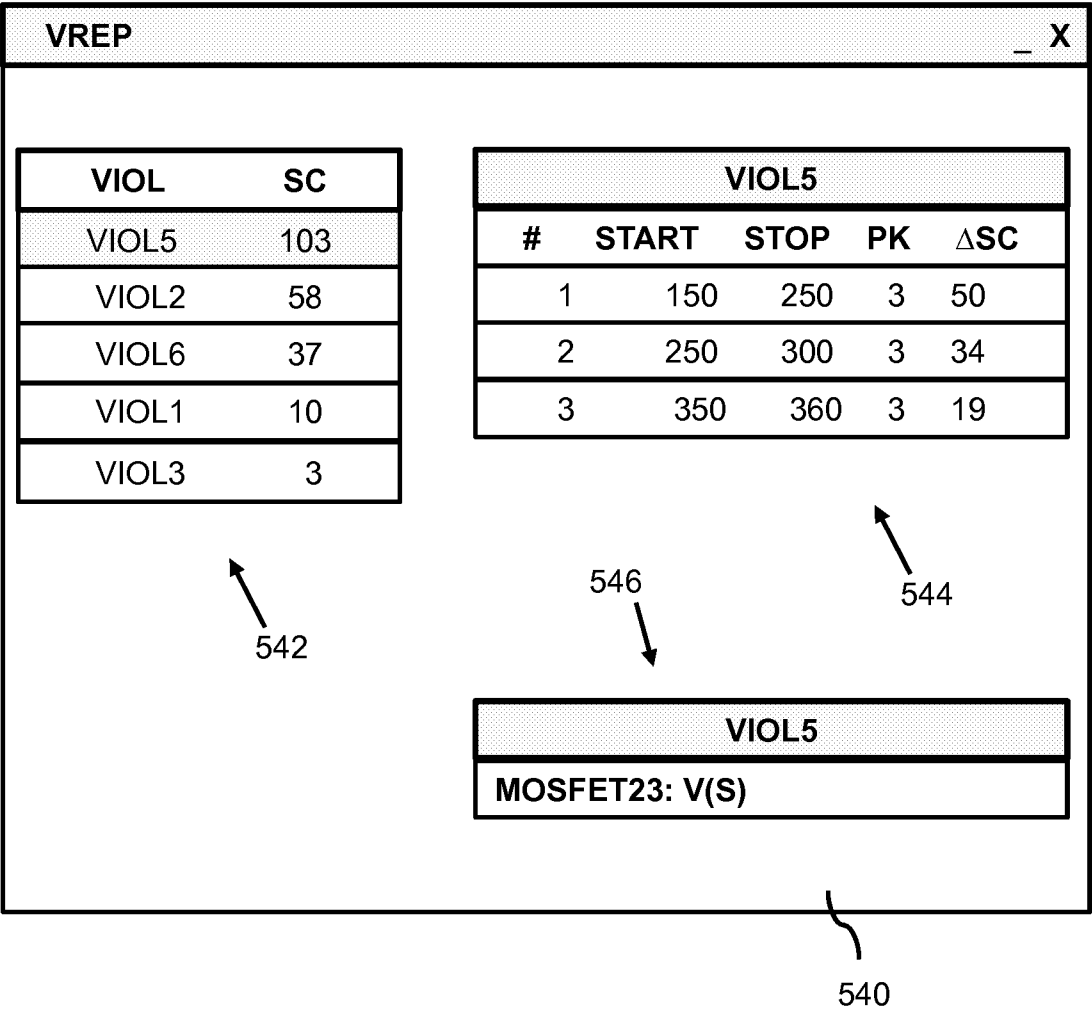


Fig. 6

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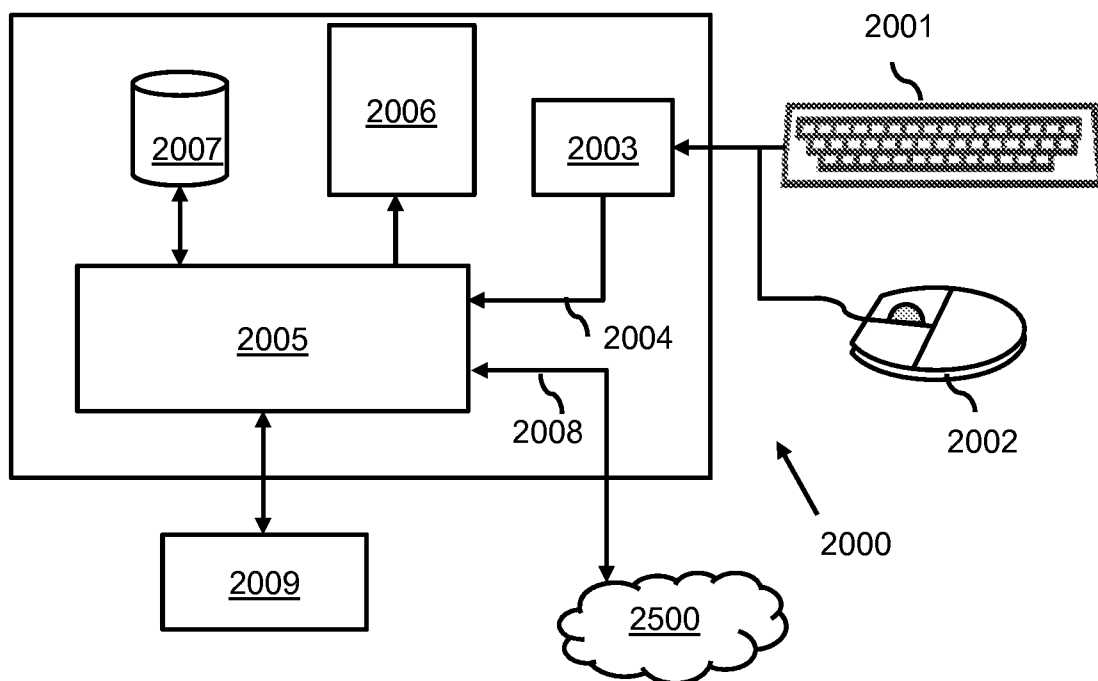


Fig. 7

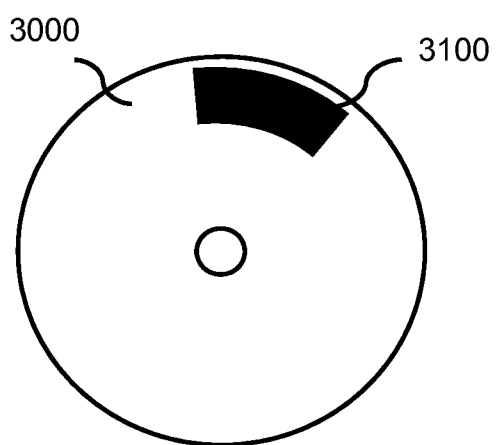


Fig. 8

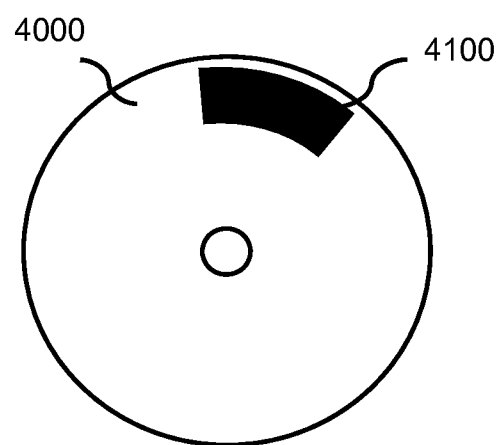


Fig. 9

A. CLASSIFICATION OF SUBJECT MATTER***G06F 11/28(2006.01)i, G06F 9/455(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

semiconductor device, design, simulation test, violation rule, score, calculate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0278663 A1 (DOUGLAS W. KEMERER et al.) 15 December 2005 See abstract; paragraphs 5, 15-16; claim 1; and figures 1-3.	1-20
A	US 2008-0163134 A1 (ERIC NEQUIST et al.) 03 July 2008 See abstract; paragraphs 36-43; and figure 4.	1-20
A	US 7689948 B1 (DAVID WHITE et al.) 30 March 2010 See abstract; column 5, line 46-column 6, line 36; and figure 5.	1-20
A	US 6588002 B1 (KOEN LAMPAERT et al.) 01 July 2003 See abstract; column 10, line 7-column 12, line 10; and figure 6.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 JANUARY 2013 (31.01.2013)

Date of mailing of the international search report

31 JANUARY 2013 (31.01.2013)

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Authorized officer

lee Jung Eun

Telephone No. 82-42-481-5391



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/IB2012/001195

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2005-0278663 A1	15.12.2005	US 7076749 B2	11.07.2006
US 2008-0163134 A1	03.07.2008	US 2008-0163150 A1	03.07.2008
		US 2011-0093826 A1	21.04.2011
		US 7698666 B2	13.04.2010
		US 7861203 B2	28.12.2010
		WO 2008-083307 A1	10.07.2008
US 7689948 B1	30.03.2010	None	
US 6588002 B1	01.07.2003	None	