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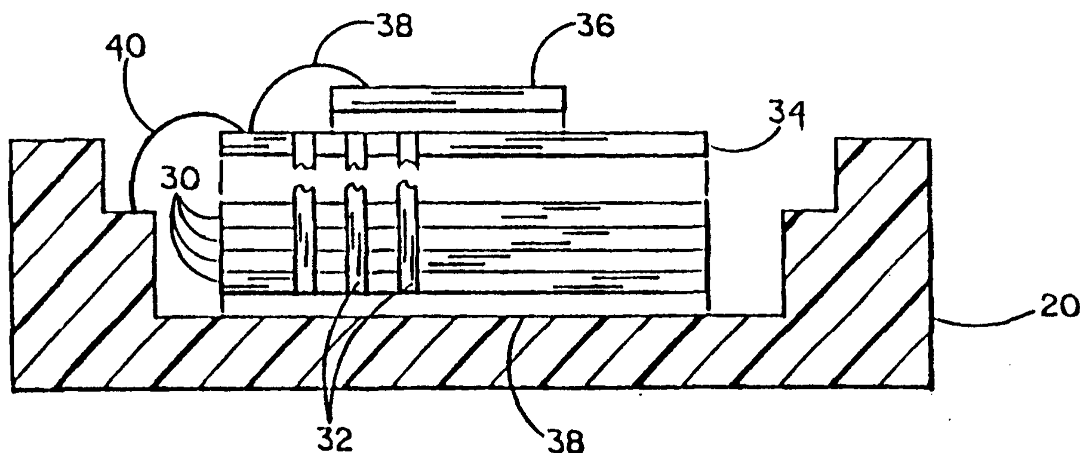

(57) Abstract

An electronic package (20) is disclosed in which a plurality of stack IC (30) is designed to substitute for a single higher capacity IC chip, and fit into a host computer system, in such a way that the system is "unaware" that the substition has been made. Memory packages are of primary interest. In order to "translate" signals between the host system and the stacked IC memory chips, it is necessary to include suitable interface circuitry (140) between the host system and the stacked chips (30). Specific examples are disclosed of a 4 MEG SRAM package containing 4 stacked IC chips each supplying a 1 MEG memory, and of 64 MEG DRAM packages containing 4 stacked IC chips each supplying a 16 MEG memory. The interface circuitry (140) can be provided by a single special purpose IC chip included in the stack, which chip provides both buffering and decoding circuitry.

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STACK OF IC CHIPS AS SUBSTITUTE FOR SINGLE IC CHIP

Background of the Invention

This invention relates to the use of stacks of IC chips in lieu of a next generation progression of single IC chip technology. The primary need for this technology is in the field of memory chips, but it can be adapted to other IC chips, such as those used in DSP (digital signal processing) systems and in communication systems.

The progression of memory chip technology from one generation to the next, e.g., from 4 Megabit (MEG) Dynamic Random Access Memory (DRAM) to 16 Megabit (MEG) DRAM, drives the design of successive generations of computer systems and processors. These generational jumps in memory technology grow progressively more and more expensive (now on the order of $1 billion per generation) for manufacturers of memory chips, because of the relatively fixed planar geometry of single memory chips and the resultant need for more and more geometrically precise semiconductor processing techniques to add features within this confined space.

The present invention is useful with all types of memory chips, including DRAM, SRAM (Static Random Access Memory), EEPROM (Electrically Erased Programmable Read Only Memory), and FLASH , a fast EEPROM. A high priority is the progression of DRAM memories, which are currently being redesigned to go from monolithic 16 MEG units to 64 MEG units. In the current redesign of SRAM memory units, the effort is to go from 1 MEG to 4 MEG units.

Summary of the Invention

This invention provides a generational progression in IC chip density by stacking IC chips in such a way that the package containing the stacked chips can be placed in the host system as though it were a new generation single IC chip. Both the function and the size of the stacked chip package can be identical in the host system to the new

generation IC chip. The term "Virtual Chip" has been coined to express the new concept.

In order to provide more feature space with less demanding chip-level processing technology, multiple memory chips of an earlier generation can be thinned and stacked into a package unit using the memory short stack technology developed by the assignee of this application, Irvine Sensors Corporation. This stacked unit can be made in a form which appears to the host system to be identical to a more advanced single chip. For example, four 16 MEG DRAMs can be stacked into a unit which appears functionally, electrically and dimensionally to be a 64 MEG single chip DRAM when installed.

The present invention provides in a short stack of IC chips the additional functions (i.e., "additional" to the functions of previous short stacks) needed to mimic the performance of a single new generation IC chip. Specifically the new short stack incorporates novel decoding and buffering circuitry. This novel circuitry may be conveniently provided by a separate chip included in the short stack.

The short stack which is substituted for a single IC chip also can, if desired, provide functional improvements over the single chip, which are not feasible in the latter because of the complexity of circuitry design in a single chip.

Several packaging options are available, based on industry standards. Examples are the SOJ (small outline J), LCC (leadless chip carrier), PGA (pin grid array), DIP (dual in-line package), etc. Generally, any new design can be fitted to any package. The industry standard referred to as JEDEC determines which size packages are appropriate for a given memory capability, e.g., 4 MEG, 16 MEG, 64 MEG. The number of leads used in a given package (established by the standard) has to be sufficient to provide the necessary address lines, data lines, and control lines.

Brief Description of the Drawings

Figures 1a-1d are exterior views of a JEDEC standard 32 lead SOJ package which is adapted to contain a 4 MEG SRAM chip. Figure 1a is an end view, Figure 1b a bottom view, Figure 1c a top view, and Figure 1d a side view;

Figure 2, 3 and 4 are exploded elevation views of three different versions of "pancake" stacks of chips, as they would be combined and supported in the lower portion of a plastic or ceramic enclosure;

Figure 5 is an elevation view of a "sliced bread" stack of chips supported by and bonded to an active substrate, which engages the supporting surface of the package enclosure;

Figure 6 shows the IC chips of Figure 2 mounted in the lower portion of a JEDEC package;

Figure 7 is a block diagram of the "VIC" chip circuitry and its connections with the four memory chips;

Figure 8 is a schematic showing details of the circuitry in Figure 7;

Figure 9 shows a diagram of a commercially available 16 MEG single chip DRAM;

Figure 10 shows a diagram of a 64 MEG DRAM package having a VIC which does not include an address decoder; and

Figure 12 shows a diagram of a 64 MEG DRAM package having a VIC which does include an address decoder.

Detailed Description of Specific Embodiment

Essentially the same principles apply to the application of JEDEC standards to any type of memory chip (e.g., DRAM, SRAM, etc.) and to any capacity of memory chip (e.g., 4 MEG, 16 MEG, 64 MEG, etc.).

Figures 1a to 1d show exterior views of a JEDEC standard SOJ container adapted to house a 4 MEG SRAM. The same general concepts apply to other types and capacities of memory chips, except for variations in the size of the container (package) and the number of leads attached to the package.

Figure 1a is drawn to a larger scale than the other three figures. The package exterior comprises a lower body portion 20, an upper body portion 22, and a seal 24 between the lower and upper body portions. Extending from the enclosed IC memory chip (not shown) are a plurality of J-shaped (in profile) leads 26, which connect the enclosed chip (or chips) to exterior electrical connections in the host system. From the bottom view, Figure 1b, it is apparent that 32 J-shaped leads are provided, 16 along each side of the package. Corresponding numerals are applied in Figures 1c and 1d.

The dimensions of the package shown in Figures 1a-1d are approximately 0.75 inch long x 0.4 inch wide x 0.1 inch high. A single 4 MEG SRAM chip would largely fill the length and width space inside the package. However, its thickness would generally be 20 mils or less, leaving a substantial amount of unused vertical space ("Z" dimension).

The present invention, in effect, replaces the single 4 MEG chip with a stack of chips. Assuming each chip in the stack provides a 1 MEG SRAM, four such chips will equal the memory capacity of the single 4 MEG chip. The thickness of each 1 MEG chip can be 4 mils or less.

It is not feasible to merely replace the 4 MEG single chip with a stack of four 1 MEG chips. In order to have the stack "mimic" the single chip, and operate within the

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host system as though it were a single chip, it is necessary to provide in the stack additional circuitry. Such additional circuitry must include two types of functions: (1) a decoding function, and (2) a driving/buffering function.

The circuitry for these functions can be included in a single IC chip which is added to the stack. Additionally, it is convenient to include in the stack a sixth layer, which is a terminal-carrying layer, such as the ceramic top layer disclosed in common assignee Application Serial No. 07/884,660, filed May 15, 1992. Various stacking concepts can be used.

Figure 2, 3 and 4 show three different chip-stacking concepts in which "pancake" stacks are used, i.e., stacks in which the layers are parallel to the supporting plane under the stack. In Figure 2, four silicon IC chips 30 are active chips containing IC memory capacity. Each of the chips 30 has a large number of parallel leads which are originally exposed at the access plane of the stack, i.e., the stack surface seen in the figure. Bus strips 32 and other terminals are applied to the access plane, in order to provide electrical connections to exterior circuitry.

Above the four silicon IC chips 30 is a ceramic cap layer 34. The cap layer 34 is the terminal-carrying layer in S/N 07/884,660. In Figure 2, the cap layer is next to the four memory chips 30. The extra (6th) layer, which is needed to "translate" signals moving between the memory stack and the host system, is shown in Figure 2 as a smaller IC chip 36 mounted on top of ceramic layer 34. All six of the chips are glued together and are glued to the surface 38 provided by the lower portion 20 of the enclosure (see Figure 1). The acronym "VIC" has been applied to the added IC chip, the letter V representing "virtual", to reflect its function in converting the stack of memory chips into the equivalent of a single memory chip.

As in S/N 07/884,660, the ceramic layer 34 has

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conducting traces on its lower surface which lead from T-connects on the access plane to interior locations where vias have been formed extending through the ceramic layer. Metallic conductors extend through the vias to connect with terminals formed on the upper surface of the ceramic layer 34. As shown in Figure 2, wire bonds 38 may be used to connect terminals on the VIC chip 36 to certain terminals on the ceramic layer 34. And other wire bonds 40 may be used to connect other terminals on the ceramic layer 34 to leads extending outside the sealed package (e.g., the J-shaped leads in Figure 1).

In Figure 3, a VIC chip 36a is located between four memory chips 30a and a ceramic cap layer 34a. The six layers are glued together and are supported on surface 38. Wire bonds 40a may be used to connect to leads extending outside the sealed package. Internal connections are used between the VIC chip 36a and the memory chips 30a.

In Figure 4, the VIC chip is in the form of an "active substrate" 36b, which both supports the chips 30b in the memory stack and contains integrated circuitry which provides interface connection between the memory stack and the host system. A ceramic layer 34b is at the top of the stack. Its terminals may be connected by wire bonds 38b to terminals on the active substrate 36b. And wire bonds 40b connect other terminals on substrate 36b to leads extending outside the sealed package.

In all structures which substitute multiple memory chips for a single, higher capacity memory chip, the VIC chip must be electronically interposed between the memory stack and the host system, for the purposes previously mentioned. The control (decoding) functions must be altered; and the means for driving and buffering the incoming and outgoing signals must be altered.

In Figures 2, 3 and 4, the number of memory chips shown is four. This number may be increased, if adequate vertical space is available, and if the total memory capacity matches that of the package for which it is being

substituted.

Figure 5 shows a somewhat more radical concept. The stack of memory chips is of the type referred to as a "sliced bread" stack. It permits a much larger number of memory chips to be included in the stack. Since the vertical dimension is greater than that of a "pancake" stack, the package cover would probably need to be shaped differently from the cover shown in Figure 1. The memory chips 30c in Figure 5 are supported on an active substrate 36c, to which they are bonded by flip chip bonds 42. No ceramic layer is included. Wire bonds 40c may connect terminals on the active substrate to leads extending outside the sealed package. The flip chip bonds 42 carry signals between the active substrate 36c and the memory chips 30c.

Common assignee Application Serial No. 08/052,475, filed April 23, 1993, describes in detail the use of an active substrate as a carrier of integrated circuitry capable of providing numerous valuable interface functions between a memory stack and exterior circuitry.

The next step in this description is to detail the circuitry on a VIC chip used in a specific package. The package described in the greatest detail is one which converts four 1 Megabit SRAM IC chips into the equivalent of a single 4 Megabit SRAM IC chip. Figure 6, which is similar to Figure 2, shows a VIC chip 44 secured to the top of a ceramic terminal layer 46, which in turn is secured to a stack 48 comprising, in this embodiment, four IC SRAM chips, each having 1 Megabit capacity. Wire bonds 50 are shown connecting terminals on VIC chip 44 to terminals on layer 46; and wire bonds 52 are shown connecting terminals on layer 46 to terminals which lead to external circuitry (i.e., the host system). Most of the electrical connections between the host system and the chip stack 48 pass through the VIC chip 44, because of the need to decode and/or alter the drive capability of the incoming or outgoing signals. However, the power supply to the

package, as represented by the symbols Vcc and Vss, is taken directly to the chips in the memory stack.

Figure 7 is a diagram of the circuitry in the stacked chip package, including the four IC memory chips, and the VIC chip 44, which is needed to provide appropriate connections between the host system and the four identical stacked SRAM chips 60. The Vcc/Vss power source 54 is diagrammed at the left side of the figure. As shown at the top of the figure, 17 address lines A0-A16 each connect directly via lines 56 to each of the four memory chips 60. Each memory chip is arranged as a 128K x 8 (bit) unit; and 217=131,072, which is referred to as 128K in computer parlance. A 128K x 8 memory chip is referred to as a 1 Megabit memory. Simple one-way buffers 62 are provided in address lines A0-A16, because address information is flowing only one way, i.e., into the memory. To the input from the host system, the 4-chip unit appears the same as a single chip unit.

The four chip stack provides a 512K x 8 bit memory capacity. In order to address this four stack memory, two additional address lines A17 and A18 and a decoder 64 are required (shown at the bottom of the figure). The 512K represents 219 (524,288) bits. The 512K x 8 memory of the stacked chips is referred to as a 4 Megabit memory. Decoder 64 has three inputs: address lines A17, A18, and enable line CE. The decoder provides four options, by means of which one of the four chips 60 is enabled, while the other three are not enabled. The four options from the decoder 64 represent (a) both lines high, (b) both lines low, (c) the first line high and the second line low, and (d) the first line low and the second line high. The CE port 66 of each chip 60 receives the enable/not enable signal from decoder 64, via one of the lines 68. The CE2 port 70 of each chip 60 is present on the chip, but is not used in the VIC circuitry. Therefore, the ports 70 are grounded by lines 72.

Recapitulating the use of the VIC chip to cause the

four chip stack to be addressed as if there were a single higher capacity chip, there are 19 address lines available at the package. A17 and A18 are decoded in the VIC chip to select one of the four chips in the stack. The remaining address lines, A0-A16, feed into all four memory chips. Thus A17 and A18 select the stack layer and A0-A16 select the memory location. From the outside (i.e., the host system) it appears that lines A0-A18 are selecting the memory location just as it would appear if a single 4 Megabit chip were being addressed. The layer is selected by decoding A17 and A18 and using the result to drive the appropriate chip enable.

The other portion of the memory interface problem deals with data transmission, which can flow in both directions, i.e., from the host system into the stacked chip package, or out of the package into the host system. As stated above, the data in this system travels along 8 parallel lines, which are labelled, in Figure 7, DQ1-DQ8. The data lines in the VIC chip are buffered by "tri-state" buffers. The term "tri-state" refers to three possible conditions: (a) coming in, (b) going out, or (c) off. In Figure 7, the data buffers are represented by a block 74. Another block 76 represents a decoder, which controls the data flow. Three control lines are connected to the data buffer decoder 76: chip enable line CE, write enable line WE, and output (read) enable line OE. The data buffers 74 are connected to each of the four chips by lines 78. The write enable signal, in addition to its decoder line 80, is connected directly to each of the chips 60 by lines 82. The output (read) enable signal, in addition to its decoder line 84, is connected directly to each of the chips 60 by lines 86. The chip enable signal is connected to decoder 76 by line 88. The data buffers 74 on the VIC chip cause the 4 chip stack to appear to the host system as a single chip. Instead of driving the input capacitance of four memories in parallel, the host system is only driving the input capacitance of the VIC, which in turn drives the

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parallel capacitance of the four memory chips.

The data control logic determines the direction of flow of the data. The address lines control the location on each chip to or from which the data travels.

5 Figure 8 shows the integrated circuitry of VIC chip 44 in greater detail, and also shows its interconnection to the memory chips. The dashed line rectangle 90 surrounds the integrated circuitry on the VIC chip. The dashed line 92 surrounds the circuitry on the four memory chips.
10 "Layer A" represents one of the four chips, and "Layer B, C, D" represents each of the other three chips. The circuitry of each of the four memory chips is identical.

Beginning at the bottom of Figure 8, lines 94 are shown connecting each of address lines A0-A16, whose
15 signals have passed through buffers 62, to the memory chip designated Layer A. Blocks 96 on Layer A represent the address circuitry on the chip. Lines 98 are shown connecting each of the address lines A0-A16 to Layers B, C and D, representing each of the other three memory chips.

20 The next segment of circuitry above the address lines A0-A16 in Figure 8 is the logic in decoder 64, which uses address lines A17, A18 and CE to select which of the four chips is enabled. Buffers 62 are provided on lines A17 and A18 ahead of decoder 64. Line 100, which is also
25 designated CEM4, leads from the decoder to the fourth memory chip in the stack (Layer D). Line 102, which is also designated CEM3, leads from the decoder to the third memory chip in the stack (Layer C). Line 104, which is also designated CEM2, leads from the decoder to the second
30 memory chip in the stack (Layer B). Line 106, which is also designated CEM1, leads from the decoder to the gates 108 and 110, which are part of the control system on the first memory chip in the stack (Layer A). The same circuitry is present on each of the four memory chips. The
35 chart enclosed by dashed line 112 shows the logic that determines which of the four chips is enabled.

As seen in Figure 8, each memory chip 60 (Layers A, B,

C and D) incorporates data buffering circuitry in the data read and write lines DQ1A,B,C&D-DQ8A,B,C&D. Each data line has an output (read) amplifier/buffer 113, and an input (write) amplifier/buffer 114. In other words, the on-chip data buffers are tri-state buffers. This buffering circuitry is, in effect, redundant with the special buffering and driving circuitry on the VIC chip, described below. Lines 116 symbolize the presence of on-chip buffering on each of Layers B, C and D.

Data buffers 74 and data lines DQ1-DQ8 are shown at the top of the VIC schematic in Figure 8. They are under control of logic circuitry included in decoder 76 of Figure 7, which responds to the interactions of three input lines: (1) WE line 120, which is a "write" enable signal (i.e., bringing data into the memory); (2) OE line 122, which is a "read" enable signal (i.e., outputting data from the memory); and (3) CE line 124, which is the same chip enable signal used in selecting the appropriate chip in the address portion of the control logic. In addition to controlling the logic which enables the buffers on the VIC chip, the WE and OE lines 120 and 122 lead to each of the four memory chips to enable the buffers 113 and 114 on each chip.

Each of the data lines DQ1-DQ8 on the VIC chip has a tri-state buffer/amplifier. Each output (read) buffer/amplifier 130, which is generally referred to as a driver, is relatively powerful, because it is sending signals off the memory chips toward the computer in the host system. Each input (write) buffer/amplifier 132 needs less power than the output driver because the computer drivers which send signals into the memory are quite powerful.

The function of each tri-state buffer on the VIC chip is to translate signals designed for use by a monolithic chip (one large memory chip) into signals involving a stack of four memory chips, without disturbing the host system. In other words, the VIC chip causes the four-chip stack to

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mimic a single chip having the same memory capacity by making four loads appear to be a single load. The capacitance of four gates in parallel should appear to be the capacitance of a single gate.

A significant feature of the circuitry on the VIC chip is its power supply capacitance, shown in the dashed line rectangle 136. A high capacitance is desired, in order to transfer signals quickly, both incoming and outgoing. One large capacitor, or a plurality of capacitors 138, may be used. The large capacitance on the VIC chip can cause the necessary current flow as voltages change. By stabilizing the voltage levels, noise is reduced, and transitions between high and low occur faster. The need to provide signal transfer is important for both outgoing and incoming signals. One of the reasons for the high capacitance on the VIC chip is the fact that each of the four memory chips in the stack was designed to function as a single chip. Some advantages could be obtained by designing stacked chips with the intention of substituting the package for a single next generation memory chip.

The foregoing explanation re a SRAM package substituting stacked memory chips for a single memory chip is also generally applicable to EEPROM and FLASH memories. In addition to 4 chip stacks, larger stacks are feasible, e.g., 8 or 16 chip stacks.

The following description focuses on using the present invention in conjunction with DRAM memories. The basic concepts are the same, but the difference of DRAMS from SRAMs dictates a somewhat different electronic configuration for the VIC, in order to cause the stack of DRAM chips to mimic a single larger capacity DRAM chip. Two general types of configurations are available by which the present invention can replace a single high capacity chip with a plurality of stacked lower capacity chips. In one type, the VIC chip has no address decoding; in the other type, the VIC chip has address decoding but not data decoding.

Figure 9 shows the functional block diagram of a state of the art 16 MEG DRAM chip designed by Micron Semiconductor, Inc. By packaging four 16 MEG DRAM chips, e.g., the Micron chip shown in Figure 9, the present invention will provide a 64 MEG DRAM package, which will fit into a host system as if it were a single 64 MEG DRAM chip.

The memory array of the chip in Figure 9 is arranged as 4096 x 1024 x 4, which provides a 16 MEG (16, 777,216 bits) chip. Data lines DQ1-DQ4 are connected to a data-in buffer and a date-out buffer. Twelve address lines A0-A11 are fed to 12 row address buffers and to 10 column address buffers. In the column address, A10-A11 are "don't care" bits. The column address buffers are bused to a column decoder which selects 1 of the 1024 columns. The row address buffers are bused to a row decoder, which selects 1 of the 4096 rows. Read and write cycles are selected with the WE input. The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE and OE.

Figures 10 and 11 each show a 64 MEG DRAM package in which four 16 MEG chips are stacked. Such chips might be the same as the chip diagrammed in Figure 9, or they might be other types of 16 MEG chips. Figure 10 shows a configuration in which the VIC chip provides only buffering and no decoding of the address. Figure 11 shows a configuration in which the VIC chip provides address decoding.

Figure 10 shows a diagram of a 64 MEG DRAM package having a VIC chip 140 and four stacked 16 MEG DRAM chips 142, 144, 146 and 148, each 4 MEG x 4. The VIC chip 140 feeds the address lines A0-A11 to each of the four IC chips in the stack, after buffering at 150. Line 152 feeds the 12 address lines to chip 142, line 154 feeds the 12 address lines to chip 144, line 156 feeds the 12 address lines to chip 146, and line 158 feeds the 12 address lines to chip 148. When an address comes in from the host system, it is

decoded by each of the four IC chips in the stack in parallel. Each IC chip in the stack first decodes the row, using all 12 address bits (212 = 4096). Then 10 bits of the address are used to decode the column (210 = 1024). The memory array in each IC chip in the stack is arranged as 4096 x 1024 x 4. Each IC chip in the stack receives the same address. However, each IC chip only has a data width of 4 bits.

In this configuration , VIC chip 140 and the stack of four chips can handle data widths of 16 bits. When the host system supplies a 16-bit wide data word, DQ1-DQ16, the first 4 bits DQ1-DQ4 are sent to chip 142 via line 160, the next 4 bits DQ5-DQ8 are sent to chip 144 via line 162, the next four bits DQ9-DQ12 are sent to chip 146 via line 164, and the last four bits DQ13-DQ16 are sent to chip 148 via line 166. All four ICs in the stack are operating in parallel. Thus, decoding of 16 bit wide data takes place by routing the input of VIC buffers 168 to the appropriate IC chip in the stack. Address decoding takes place in each of the stacked IC chips. Decoding is not required to determine which IC chip 142, 144, 146 or 148 is enabled. The RAS (row address strobe), CAS (column address strobe), WE (write enable) and OE (output enable) lines are each sent in parallel to each of the four chips in the stack. In sum, the package diagrammed in Figure 10 is a 64 MEG DRAM organized as a 4 MEG x 16 package from 4 layers of 4 MEG x 4 monolithic IC chips.

Figure 11 shows a diagram of a 64 MEG DRAM organized as a 16 MEG x 4 package from 4 layers of 4 MEG x 4 monolithic IC chips. In this configuration decoding is required in the VIC. The figure has a VIC chip 170 and four stacked 16 MEG DRAM IC chips 172, 174, 176 and 178, each 4 MEG x 4. In this configuration, the VIC chip provides address decoding. Data lines DQ1-DQ4, after passing through tri-state buffers 180, are connected to each of the four IC chips. Address lines A0-A11 also are connected to each of the four IC chips, after passing

through buffers 182. As in Figure 10, this provides 12 address lines at each chip.

Decode and buffer circuitry 184 is provided in the VIC chip, because the 12 address lines only address 4096 rows x 1024 columns. Each of these amounts needs to be doubled to obtain a 64 MEG DRAM capacity in the package. The configuration in Figure 11 may be thought of as 8192 x 2048 (16 MEG) with a data width of 4 bits. The VIC chip 170 contains an extra address line A12. This line is decoded on the VIC chip, utilizing the RAS and CAS inputs, just as the individual IC memory chips decode the address to provide the necessary address width. The VIC chip in essence decodes to determine which of the 4 IC chips in the stack will be enabled, utilizing the A12 line and the RAS and CAS lines. In this configuration only one IC chip at a time is enabled. Chip 172 is shown enabled by VIC chip outputs RAS-0 and CAS-0; chip 174 is shown enabled by VIC chip outputs RAS-1 and CAS-0; chip 176 is shown enabled by VIC chip outputs RAS-0 and CAS-1; and chip 178 is shown enabled by VIC chip outputs RAS-1 and CAS-1.

Packaging of the stacked chips in the DRAM memories of Figures 10 and 11 is comparable to that of the SRAM chips detailed earlier. The stacked chips are arranged to fit in a standard package enclosure designated for a single 64 MEG chip.

From the foregoing description, it will be apparent that the devices disclosed in this application will provide the significant functional benefits summarized in the introductory portion of the specification.

The following claims are intended not only to cover the specific embodiments disclosed, but also to cover the inventive concepts explained herein with the maximum breadth and comprehensiveness permitted by the prior art.

What Is Claimed Is:

1. A memory package adapted to be substituted for a single IC memory chip in a host computer system, comprising:
5 a plurality of stacked IC memory chips having a total memory capacity equal to that of the single chip for which the stack is being substituted; and
an additional interface IC chip included in the stack which is electronically interposed between the stacked
10 chips and the host system in such a way that the latter interfaces with the stack as it would with a single chip.

2. The memory package of claim 1 in which each of the stacked IC memory chips has been configured as a chip capable of functioning independently where a lower capacity memory is desired.

3. The memory package of claim 1 in which the interface IC chip includes:
circuitry adapted to buffer and transmit a plurality of parallel address signals from the host system to the
5 stacked IC memory chips.

4. The memory package of claim 1 in which the interface IC chip includes:
circuitry adapted to transmit data signals in both directions between the host system and the stacked IC
5 memory chips.

5. The memory package of claim 1 in which the interface IC chip includes:
circuitry adapted to transmit data signals in both directions between the host system and the stacked IC
5 memory chips, and to buffer such signals in both directions.

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6. The memory package of claim 1 in which the interface IC chip includes circuitry which decodes one or more address signals from the host system to enable one of the stacked IC memory chips at a time.

7. The memory package of claim 4 in which the interface IC chip also includes circuitry which causes the data signals to communicate with only one at a time of the stacked IC memory chips.

8. The memory package of claim 2 in which the interface IC chip includes:

circuitry adapted to buffer and transmit a plurality of parallel address signals from the host system to the
5 stacked IC memory chips.

9. The memory package of claim 2 in which the interface IC chip includes:

circuitry adapted to transmit data signals in both directions between the host system and the stacked IC
5 memory chips.

10. The memory package of claim 2 in which the interface IC chip includes:

circuitry adapted to transmit data signals in both directions between the host system and the stacked IC
5 memory chips, and to buffer such signals in both directions.

11. The memory package of claim 2 in which the interface IC chip includes circuitry which decodes one or more address signals from the host system to enable one of the stacked IC memory chips at a time.

12. The memory package of claim 9 in which the interface IC chip also includes circuitry which causes the data signals to communicate with only one at a time of the

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stacked IC memory chips.

13. For use in a host computer system which provides multiple separate address signals and multiple separate data signals, a memory package adapted to be substituted for a single memory chip, comprising:

5 a plurality of stacked IC memory chips having a total memory capacity equal to that of the single chip for which the stack is being substituted;

circuitry in the package which receives incoming address signals from the host system, buffers each of the

10 address signals, and selects the appropriate address on one of the memory chips; and

circuitry in the package which receives both incoming and outgoing data signals, buffers each of the separate data signals in both directions, and interconnects the

15 separate data signals between the host system and the stacked memory chips in both directions.

14. The memory package of claim 13 which also includes:

decoding circuitry which causes only one of the chips in the stack to be enabled at a time.

15. The memory package of claim 14 in which the decoding circuitry is controlled by one or more of the incoming address signals.

16. The memory package of claim 13 in which each of the memory chips connects to a different group of data signals in order to provide a data bit word having the width provided by all memory chips in the stack.

17. For use in a host computer system which provides multiple separate address signals and multiple separate data signals, a memory package adapted to be substituted for a single memory chip, comprising:

5 a plurality of stacked IC memory chips having a total

memory capacity equal to that of the single chip for which the stack is being substituted;

an additional interface IC chip included in the stack which is electronically interposed between the stacked chips and the host system in such a way that the latter interfaces with the stack as it would with a single chip, said interface IC chips including:

circuitry which receives incoming address signals from the host system, buffers each of the address signals, and selects the appropriate address on one of the memory chips; and

circuitry which receives both incoming and outgoing data signals, buffers each of the separate data signals in both directions, and interconnects the separate data signals between the host system and the stacked memory chips in both directions.

18. The memory package of claim 17 in which:

the interface IC chip includes decoding circuitry which causes only one of the chips in the stack to be enabled at a time.

19. The memory package of claim 18 in which the decoding circuitry is controlled by one or more of the incoming address signals.

20. The memory package of claim 17 in which:

the interface IC chip includes circuitry which connects each of the memory chips to a different group of data signals in order to provide a data bit word having the width provided by all memory chips in the stack.

21. The memory package of claim 17 in which the IC interface chip also includes:

circuitry providing sufficient capacitance to compensate for the use of a plurality of stacked memory chips in place of a single memory chip.

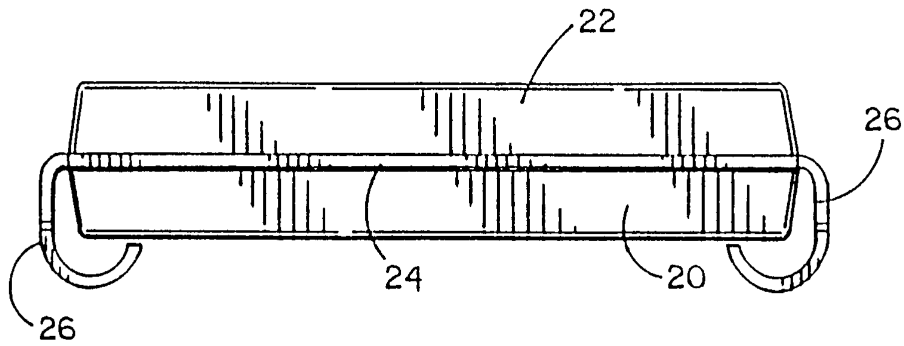

FIG. 1a

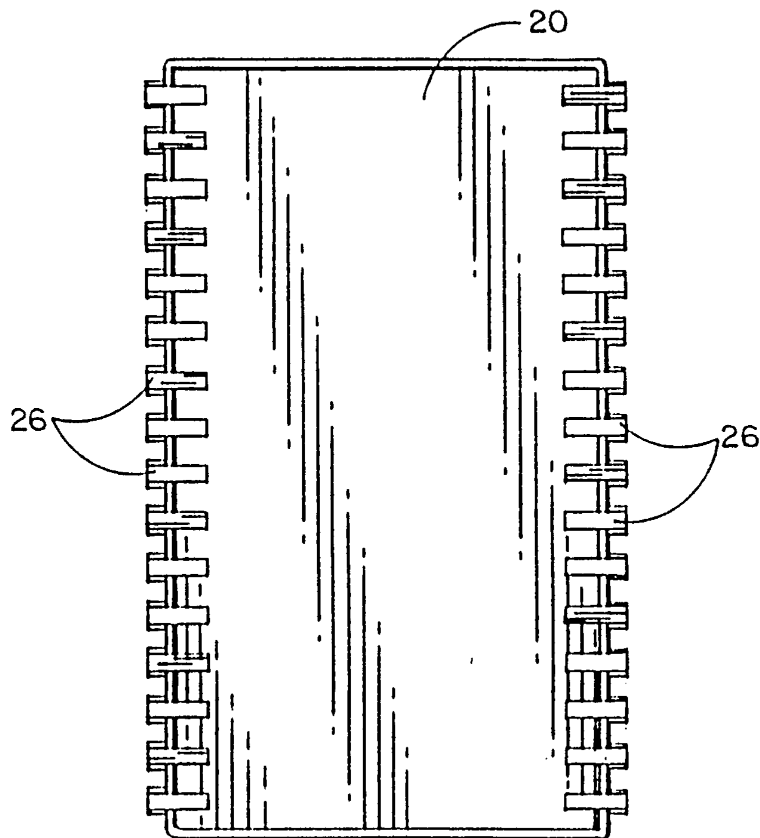

FIG. 1b

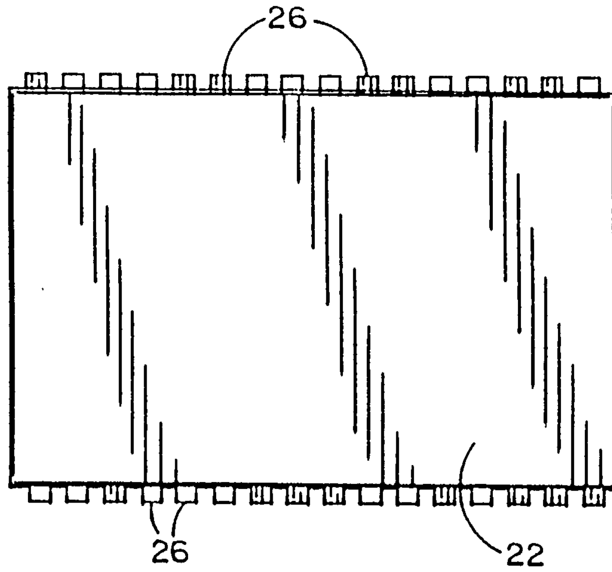

FIG. 1c

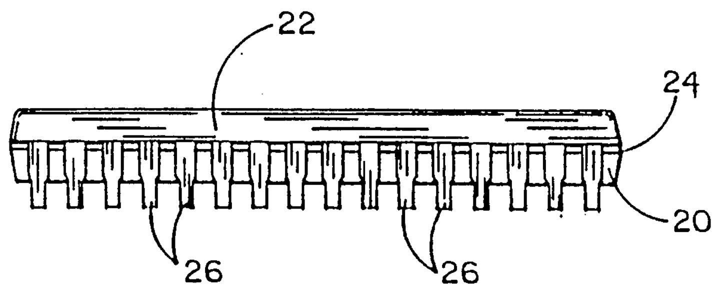

FIG. 1d

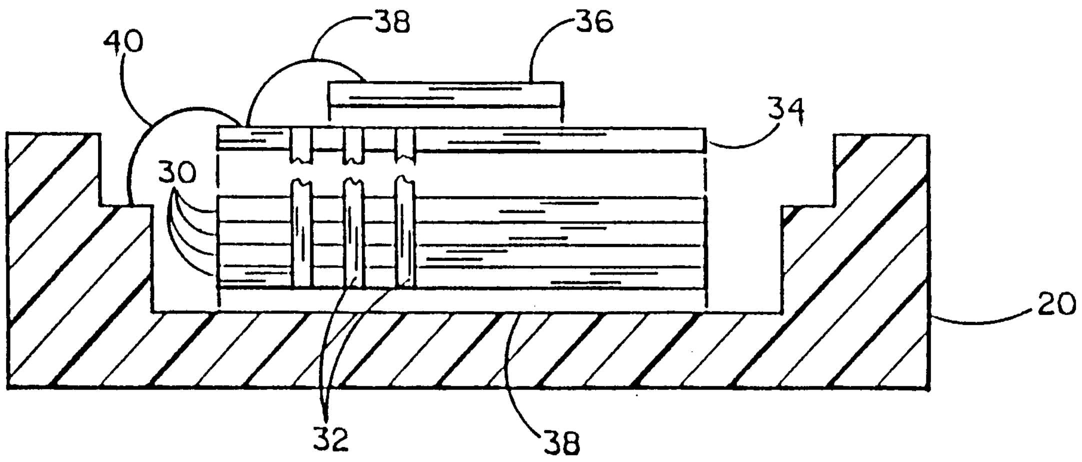

FIG. 2

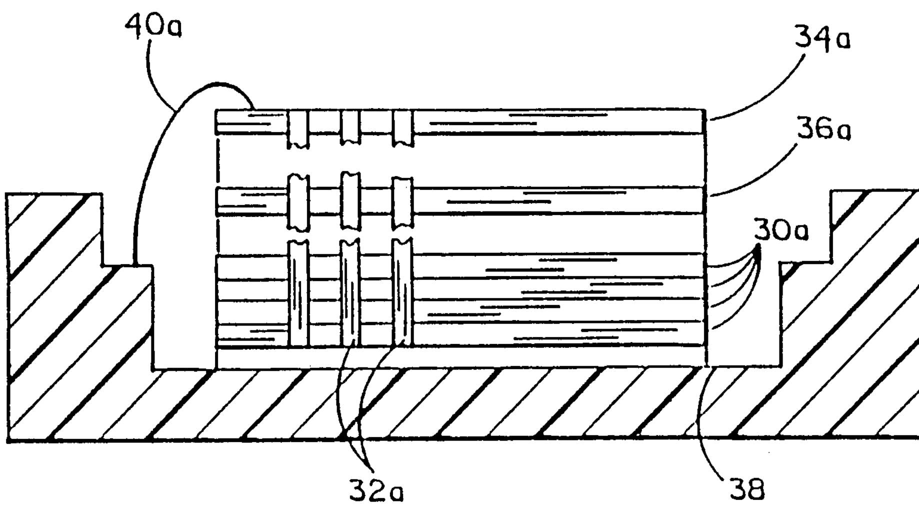

FIG. 3

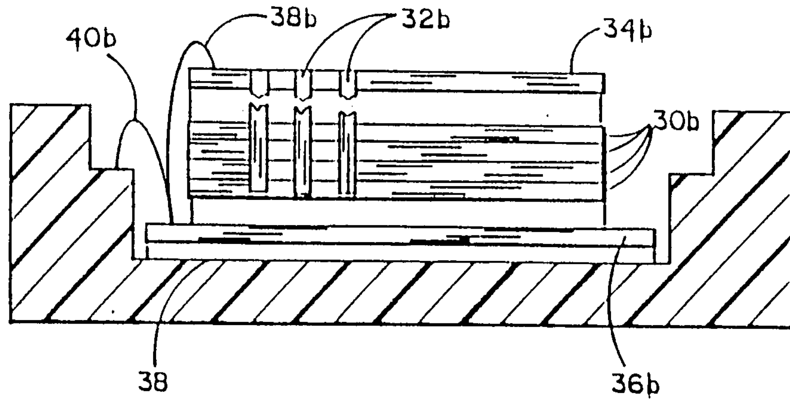

FIG. 4

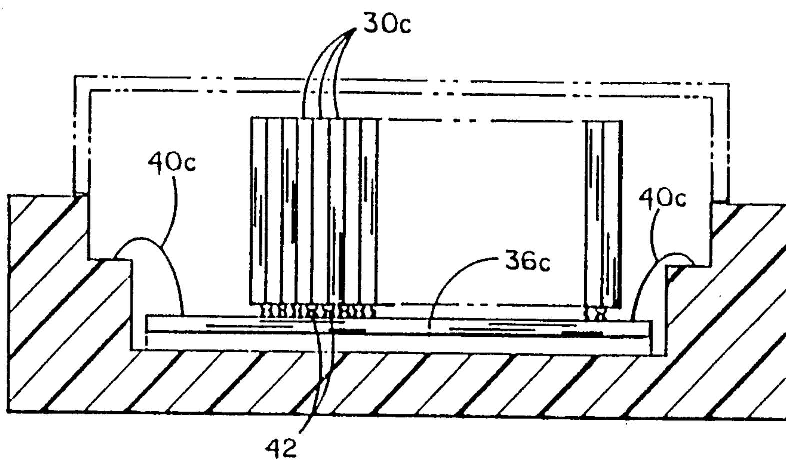

FIG. 5

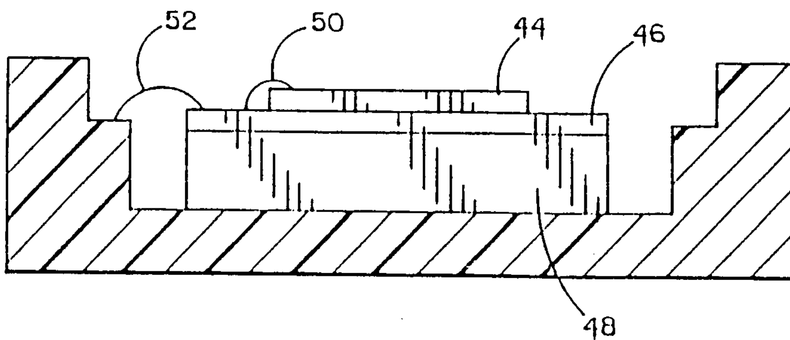

FIG. 6

FIG. 7

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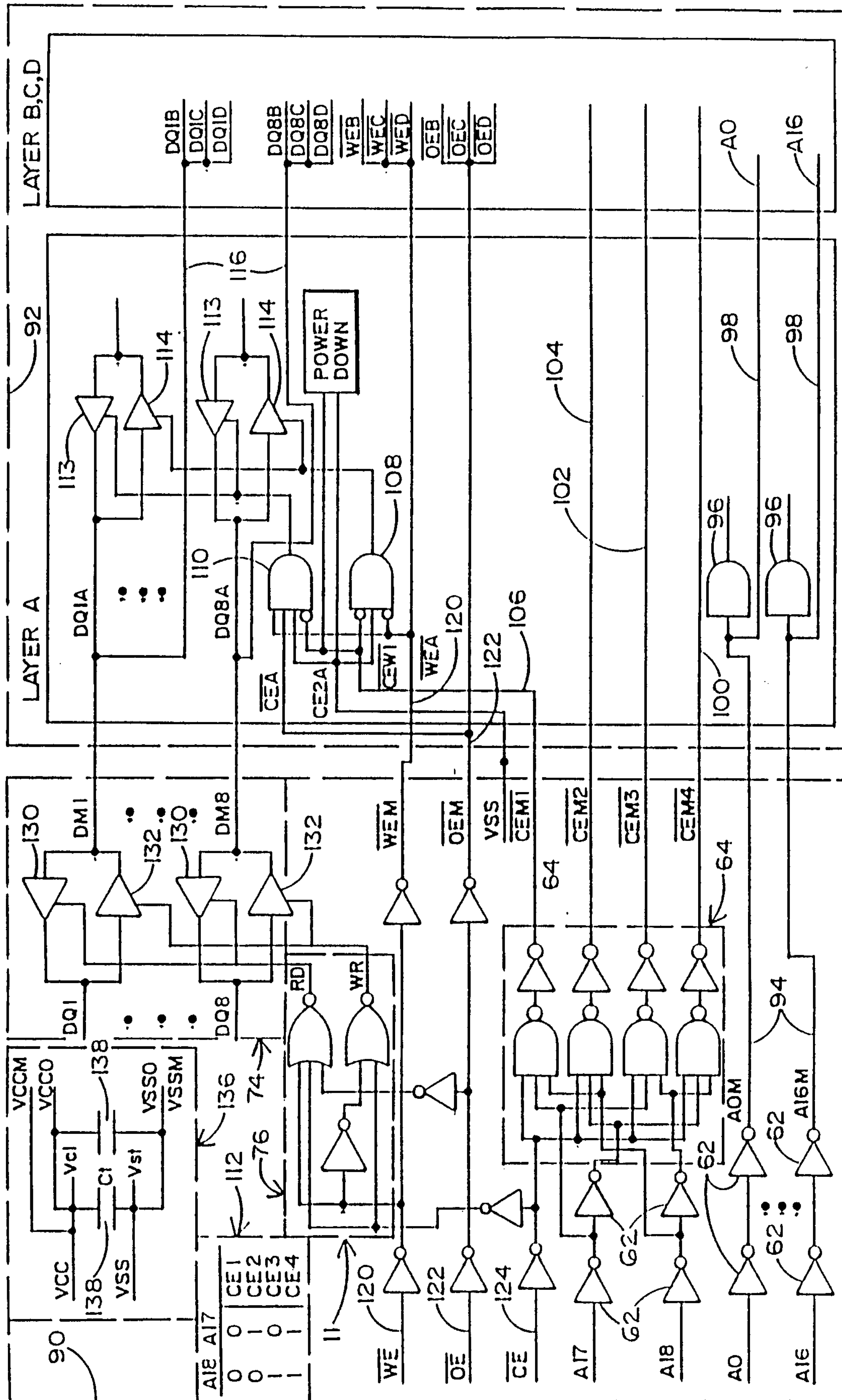

FIG. 8

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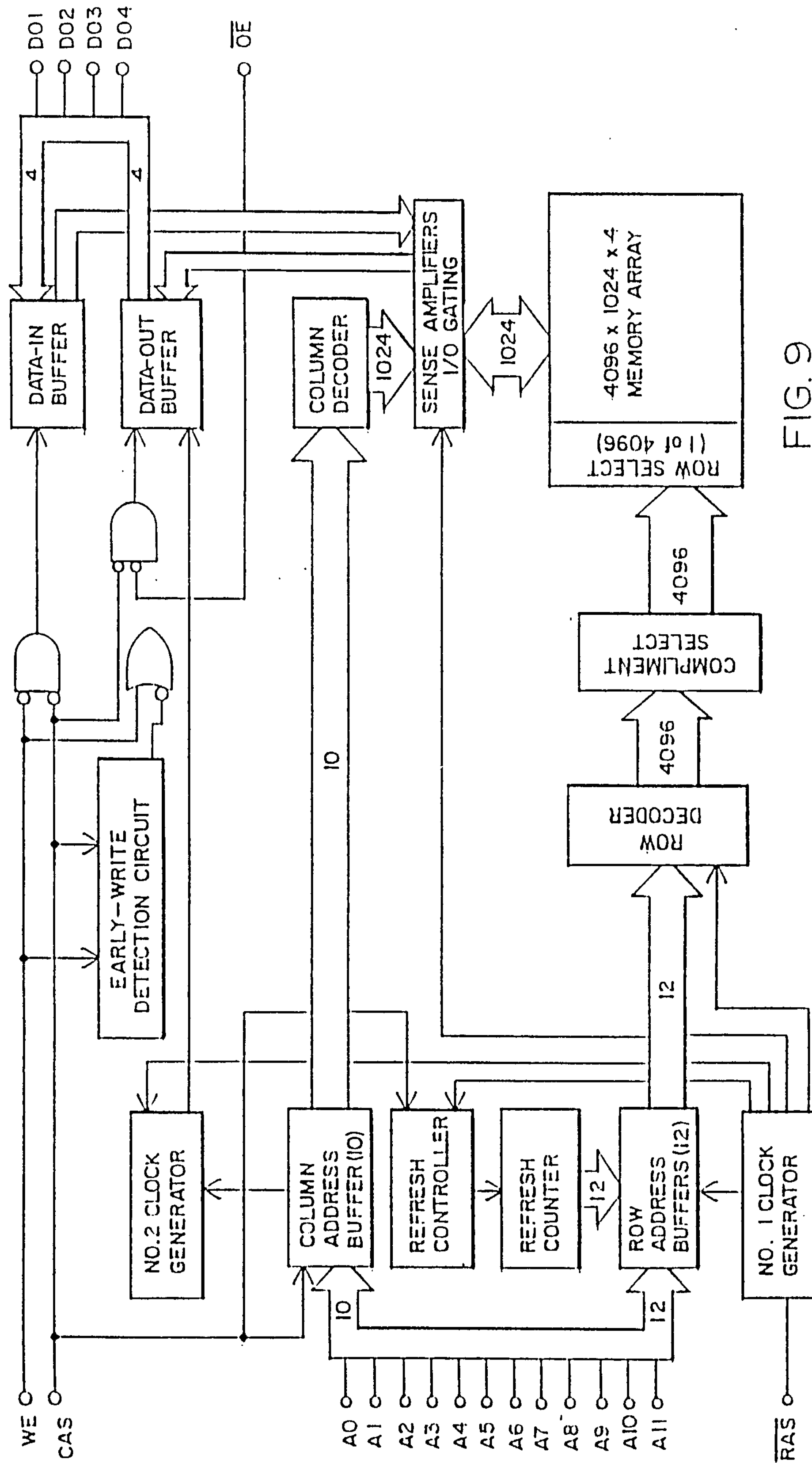

FIG. 9

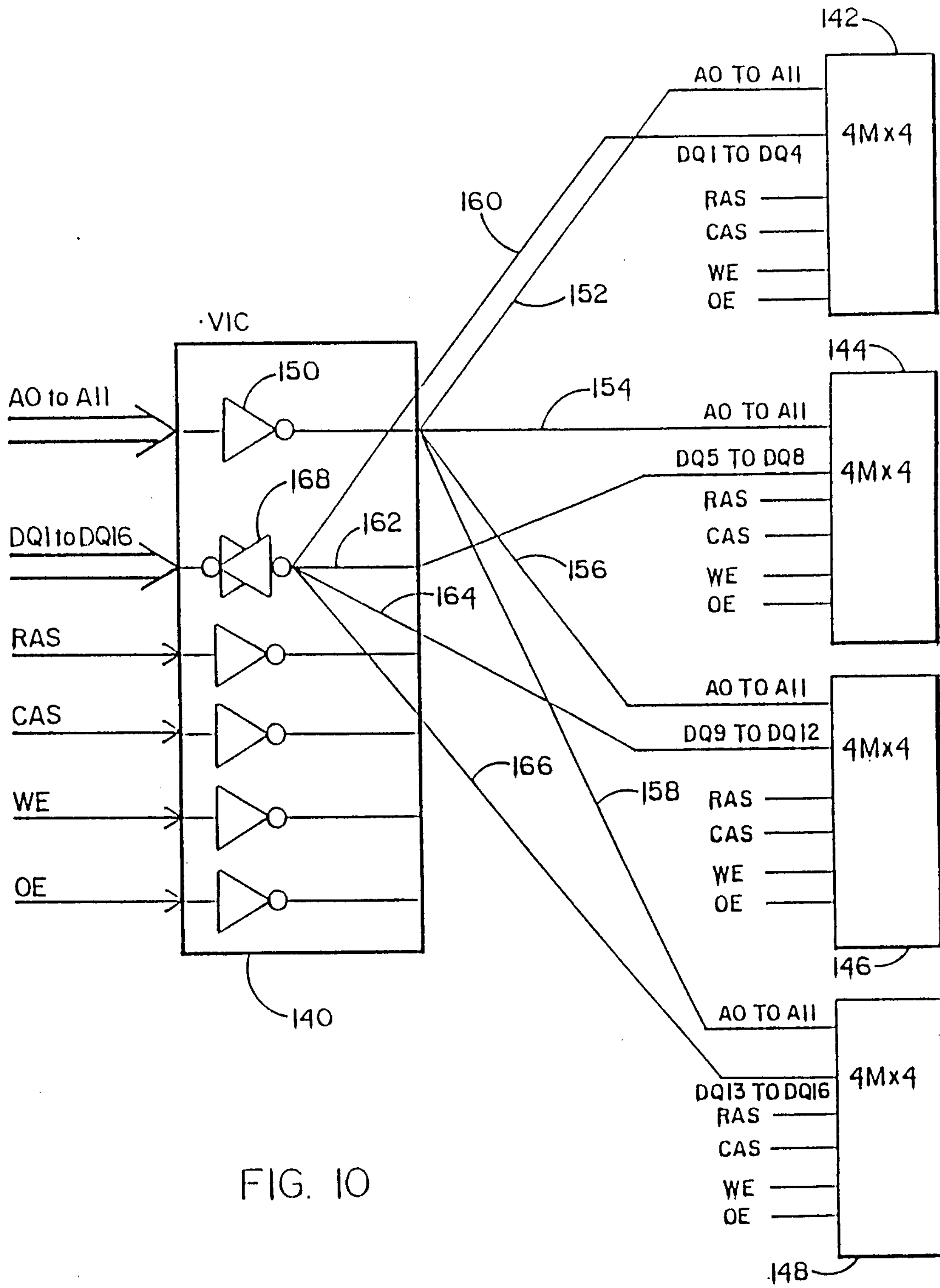

FIG. 10

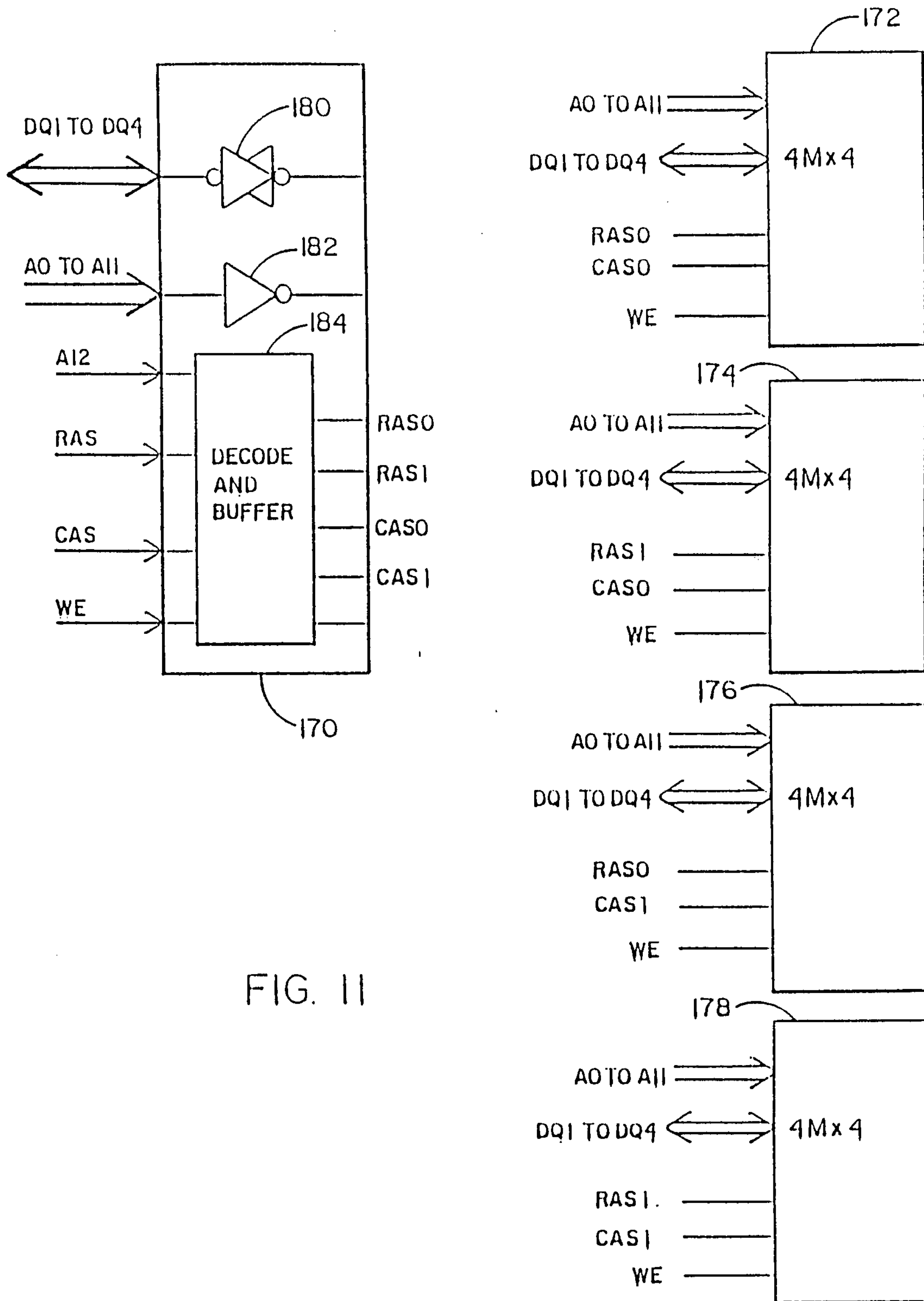

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/09186

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 25/00, 27/00
US CL :365/52, 63; 257/686, 777
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/52, 63; 257/686, 777

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, E	US, A, 5,345,412 (Shiratsuchi) 06 September 1994, col. 6, line 46 to col. 7, line 25.	1-21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 NOVEMBER 1994	28 NOV 1994

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