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H01L 27/108

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(58) Field of search
UK CL (Edition K) **H1K KFL KGAM**
INT CL^5 **H01L**

(54) Capacitors for DRAM cells

(57) The DRAM cell includes a trench capacitor which is made by doping impurities in the surface of a trench 10 formed in a semi conductor substrate 100. The impurity doped layer 13, which comprises an electrode of the capacitor, enables a large capacitance to be formed. The doping is done by impurity diffusion or ion implantation. A dielectric film 14 is deposited on the layer 13 which is connected to the source region 3 of a F.E.T. 2-4.

FIG. 2

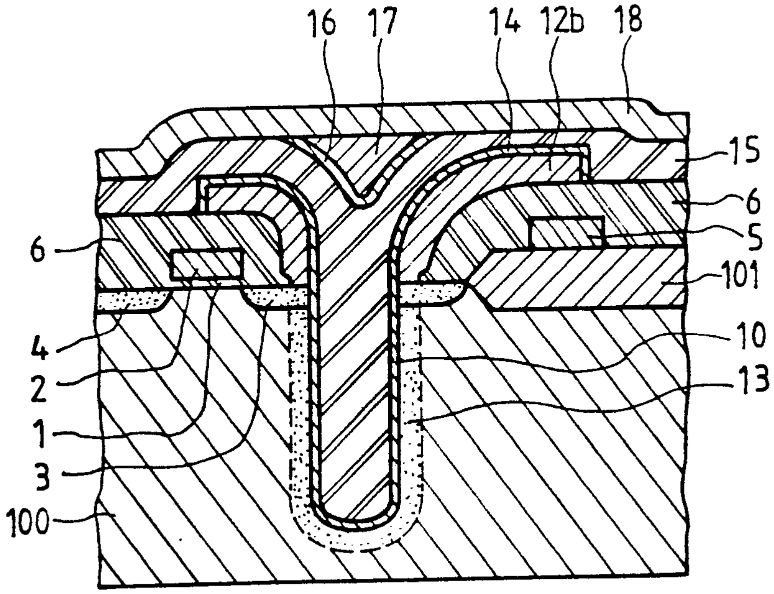

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FIG. 1 (Prior Art)

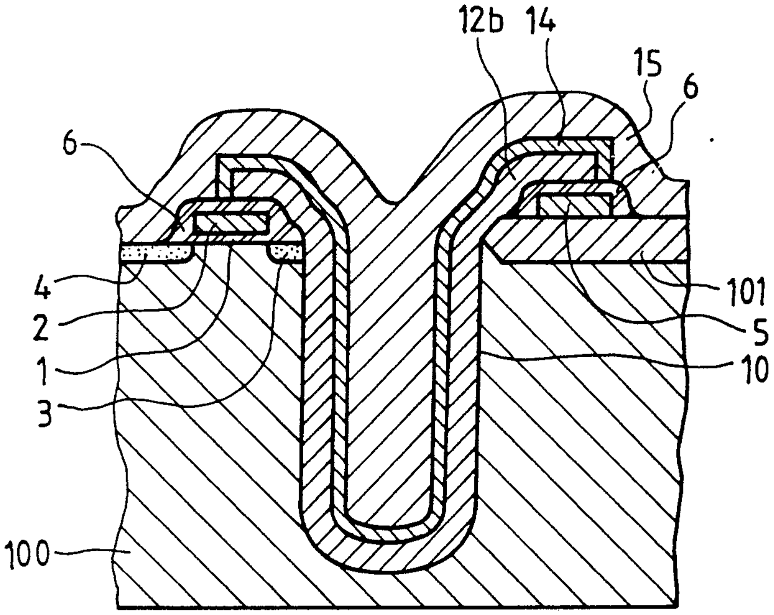


FIG. 2

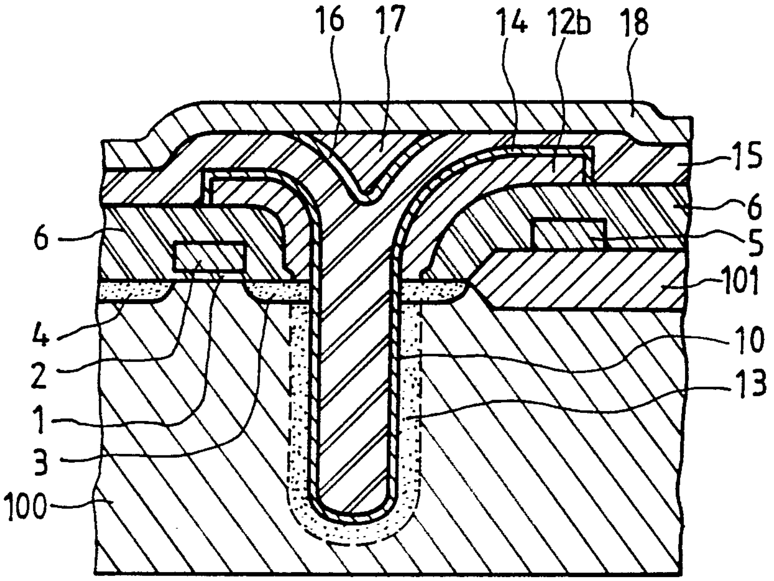


FIG. 3A

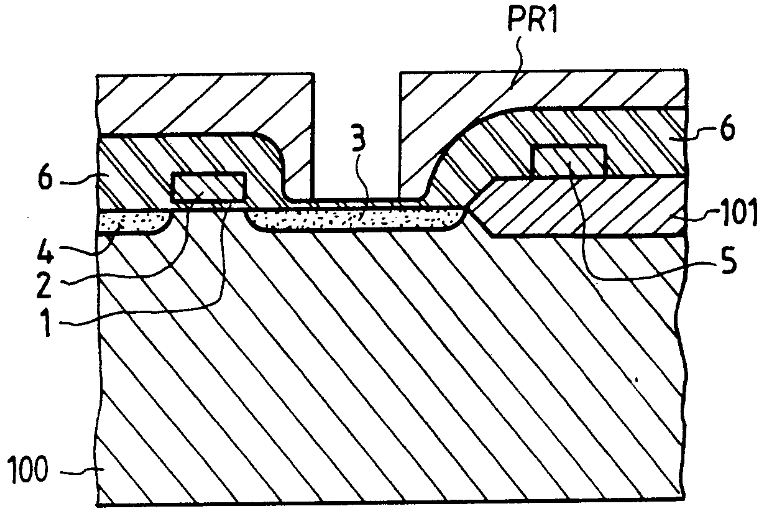


FIG. 3B

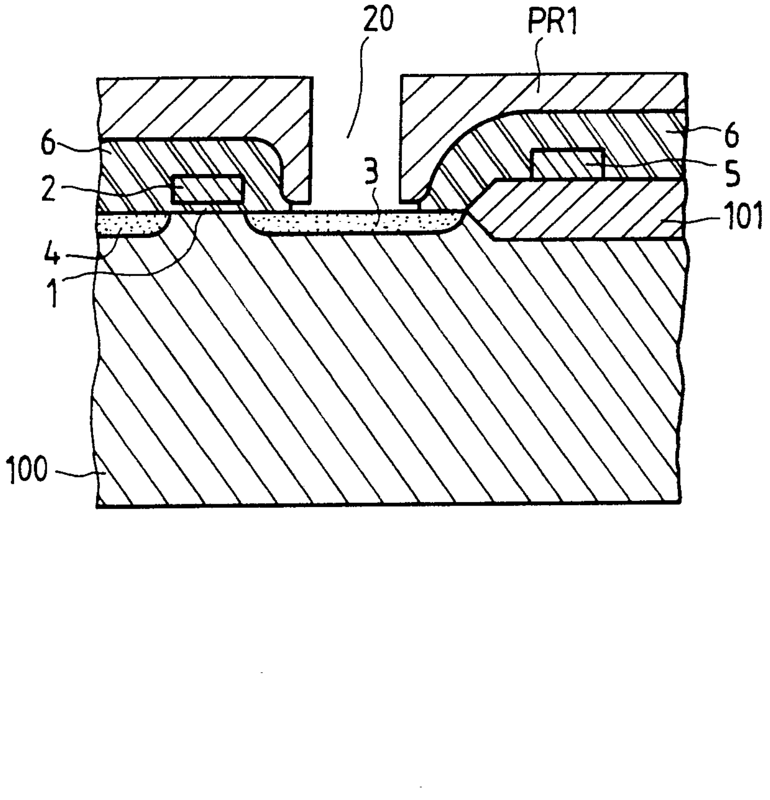


FIG. 3C

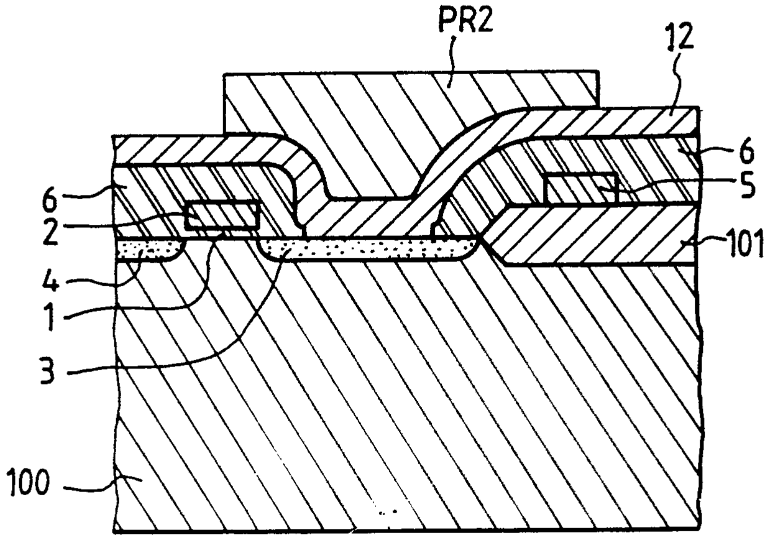


FIG. 3D

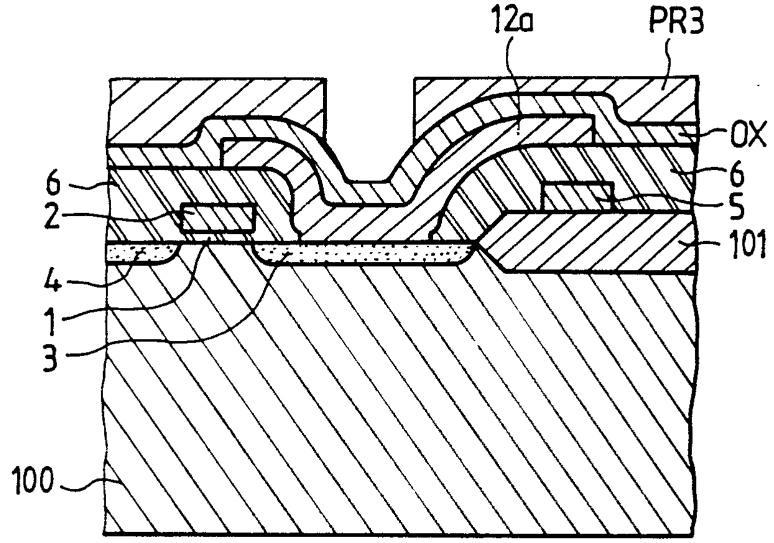


FIG. 3E

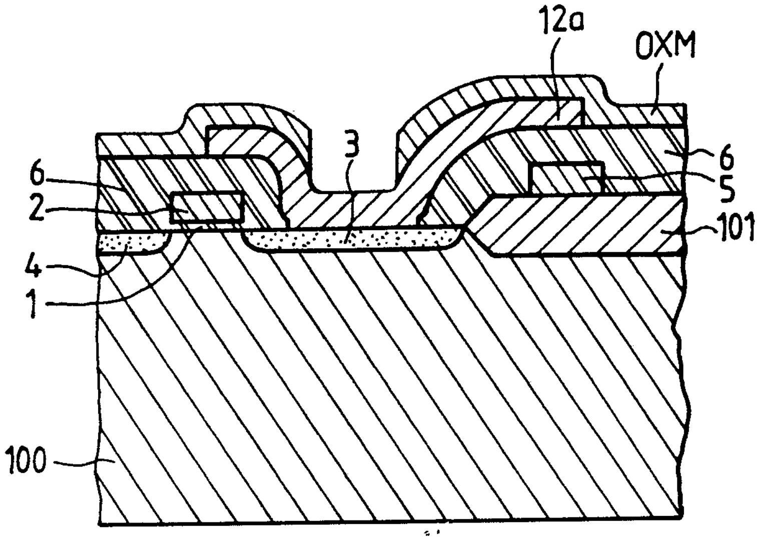


FIG. 3F

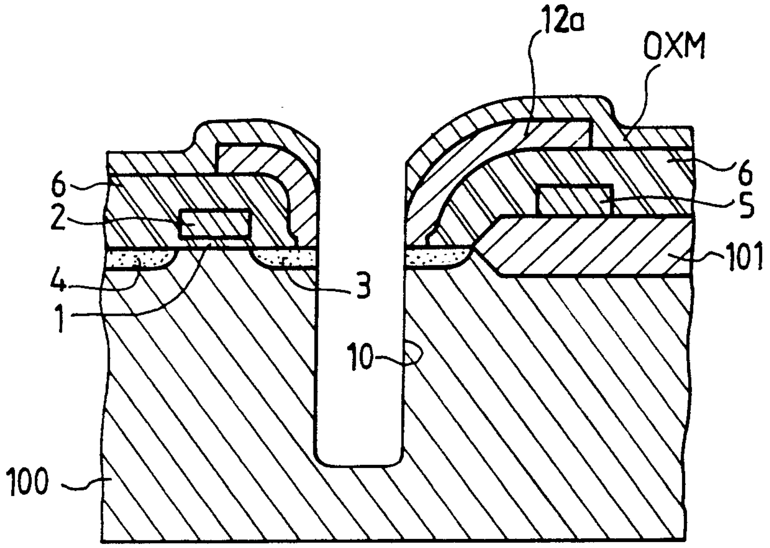


FIG. 3G

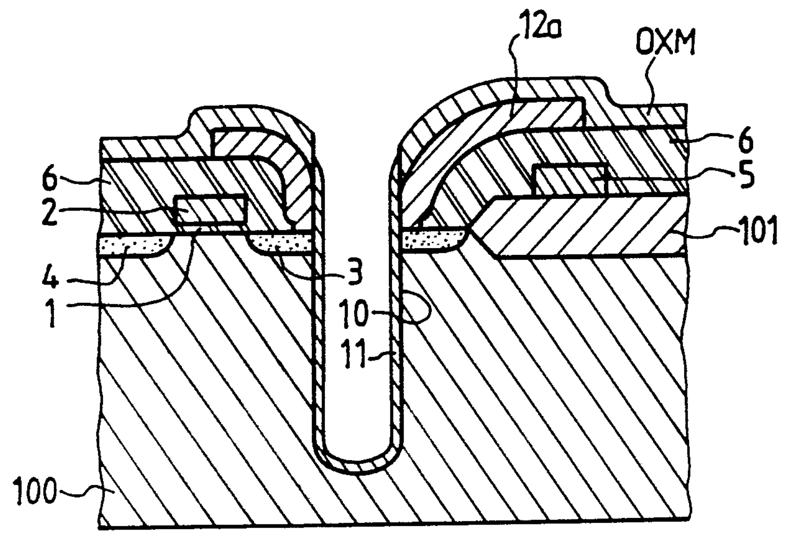


FIG. 3H

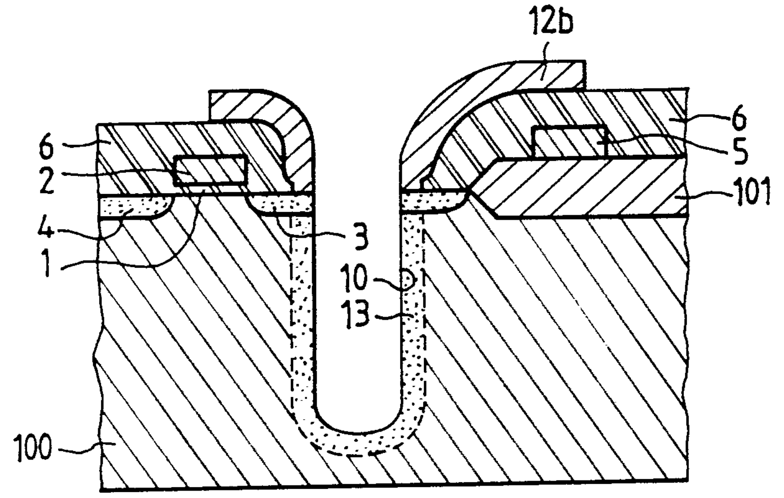


FIG. 3I

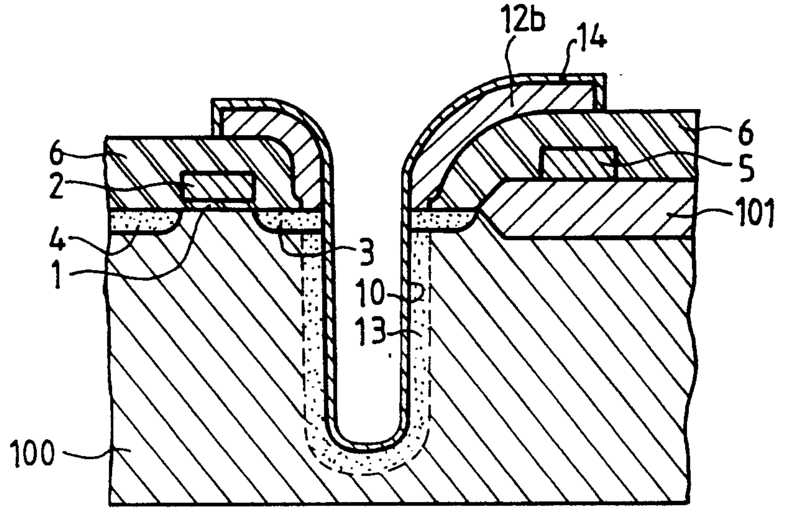
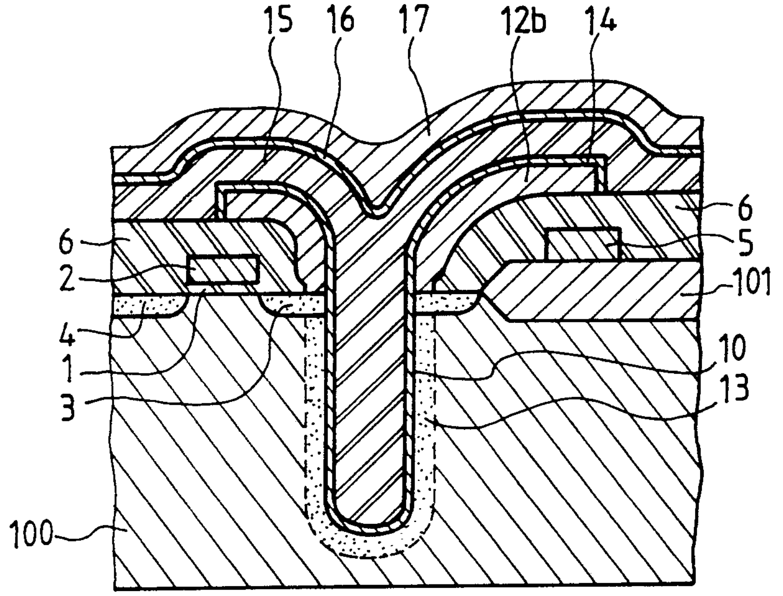
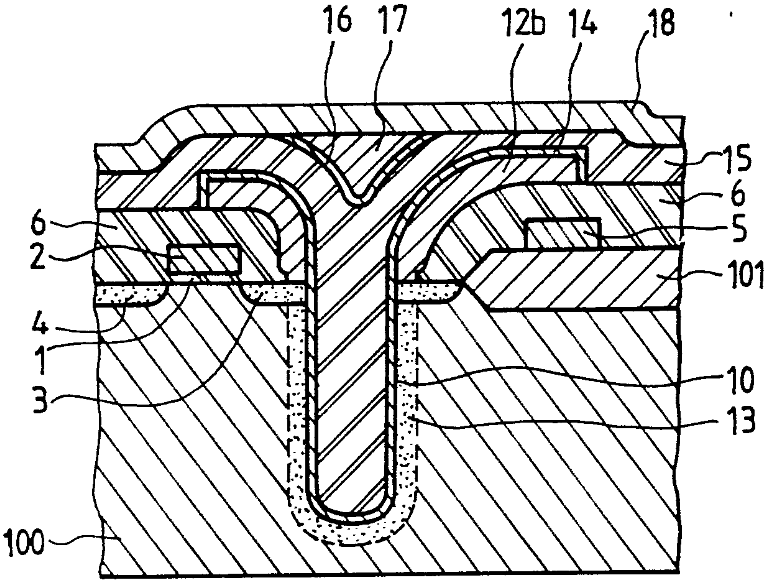

12b
14
6
2
4
1
3
10
13
100
6
5
101

FIG. 3J


15
16
17
12b
14
6
2
4
1
3
100
6
5
101
10
13

8/8

FIG. 3K



SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

The present invention relates to a semiconductor device and a manufacturing method thereof, and particularly to a semiconductor device and a manufacturing method thereof, in which the capacitance of a memory device can be maximised.

Recently, with the progress of semiconductor manufacturing techniques and with the expansion of the application of semiconductor, memory devices of large capacities are developed and promoted. Particularly, DRAM(Dynamic Random Access Memory) having the advantage of very-large-scale integration(VLSI) by constituting one memory cell into one capacitor and one transistor has been considerably developed.

This DRAM applies to the 4M DRAM by contriving the three dimensional structure having a stack type capacitor cell and a trench type capacitor cell instead of a prior planar type capacitor cell in memory cell structure, but it has a difficulty in applying to the 16M DRAM. Also in the above stack type capacitor cell, step coverage problem occurs owing to the capacitor structure stacked on transitor, and in the trench type capacitor cell, leakage current problem between trenches occurs during the process of scaling down work. As the result, above mentioned DRAM is difficult to apply to the 64M DRAM.

Therefore, to solve the problem of this large capacity DRAM, stack-trench combined type capacitor as a new three dimensional structure is proposed, which is shown in Figure 1.

Referring to the Figure 1, an active region is defined by growing a field oxide layer 101 on the semiconductor substrate 100 and a first conductive layer such as an impurity-doped first polycrystalline silicon layer, namely, gate electrode 2 is formed on the active region by interpositing the gate oxide layer 1, and then, a first conductive layer 5, e.g., an impurity-doped first polycrystalline silicon layer is formed on the field oxide layer 101 in such a manner that the first conductive layer is connected with a gate electrode of an adjacent memory cell, thereafter a source region 3 and a drain region 4 are formed on the semiconductor substrate surface of both sides of the gate electrode 2, and a first insulating layer 6 is formed on the entire surface of the structure as above mentioned. Then, through the application of the mask on the first insulating layer 6 and between the field oxide layer 101 and the gate electrode 2, a trench is formed in the semiconductor substrate 100, and then, a first electrode pattern which is formed by a second conductive layer 12b, e.g., an impurity-doped second polycrystalline silicon layer is formed on both the inside of the trench 10 and the first insulating layer 6. Here, the second conductive layer 12b is used as a first electrode of the capacitor. Then, a dielectric film 14 covering the surface of the first electrode pattern is formed, and then, a third conductive layer 15, e.g., an impurity-doped third polycrystalline silicon layer is formed on the entire surface of the above mentioned structure, so that the third conductive layer 15 is used as a second electrode of the capacitor, thereby forming the stack-trench combined type capacitor. Since the prior stack-trench combined type capacitor above mentioned in detail as shown in Figure 1 directly forms the second conductive layer used as the first electrode of the capacitor on the inside of the trench, the surface area of the trench gets small. When the capacitor is formed by forming the dielectric film and the third conductive layer on the small surface, i.e. the surface of the trench in turn, the problem of lossing capacitance brings about.

It is an object of the present invention to provide a stack-trench combined type capacitor for increasing the capacitance by using the surface of the trench formed in the semiconductor substrate as the first electrode of the capacitor.

It is another object of the present invention to provide a manufacturing method which is suitable for manufacturing the stack-trench combined type capacitor having the above mentioned structure in an effective manner.

To accomplish the above object, a stack-trench combined type capacitor according to the present invention is characterized by comprising a field oxide layer which is selectively formed to define an active region on the semiconductor substrate of a first conductivity type, a gate electrode of the first conductive layer electrically insulated on the active region, a source and a drain regions of a second conductivity type formed at the both sides of the gate electrode and on the semiconductor substrate surface, a trench formed in the semiconductor substrate and within the source region, an impurity-doped region of the second conductivity type formed at the surface of the trench for connecting to the source region, a first insulating layer for insulating the first conductive layer, a second conductive layer formed for connecting to the impurity-doped region through a part of the source region on the first insulating layer, a dielectric film formed on both the second conductive layer and the inside of the trench including the impurity-doped region, a third conductive layer having an etch blocking layer and a fourth conductive layer and formed on the dielectric film, and a fifth conductive layer formed to cover the third conductive layer and the fourth conductive layer.

The method suitable for manufacturing the above described structure of capacitor is characterized by providing the first process in order to define an active region by growing a field oxide layer on the semiconductor substrate of the first conductivity type, the second process forming a gate electrode of a first conductive layer, a source and a drain regions of a second conductivity type on the active region and forming a first insulating layer on the above obtained sample, the third process forming an opening to expose a portion of the source region, the fourth process forming a first electrode pattern by depositing a second polycrystalline silicon layer on both the first insulating layer and the entire surface of the substrate exposed, the fifth process forming the mask by depositing a second insulating layer on the first electrode pattern, the sixth process forming a trench in the semiconductor substrate and within the source region by applying the mask, the seventh process doping an impurity of the second conductivity type at both the first electrode pattern and the semiconductor substrate of the inside of the trench, the eighth process forming a dielectric film on both an impurity-doped first electrode pattern and the inside of the trench including the impurity-doped region, the ninth process depositing a third conductive layer, an etch blocking layer and a fourth conductive layer on the dielectric film in turn, and the tenth process depositing the fifth conductive layer after planarizing the sample obtained by the above processes.

The above objects and other advantages of the present invention will become more apparently by describing in detail the preferred embodiment of the present invention with reference to the attached drawing in which:

Figure 1 is a cross-sectional view of the conventional stack-trench combined type capacitor;

Figure 2 is a cross-sectional view of the stack-trench combined type capacitor according to the present invention.

Figures 3A to 3K show the manufacturing processes of one embodiment for the stack-trench combined type capacitor according to the present invention.

The stack-trench combined type capacitor according to the present invention as shown in Figure 2 is manufactured in such a manner that a field oxide layer 101 is selectively formed in order to define an active region on the semiconductor substrate 100 of a first conductivity type, and then, a gate electrode 2 is formed on the above active region by interpositing the gate oxide layer 1. Thereafter a source and a drain regions of a second conductivity type is formed on the semiconductor substrate surface and at the both sides of the gate electrode 2, and then, a first conductive layer 5 is formed on any predetermined portion of the field oxide layer 101 in such a manner that the first conductive layer is connected with a gate electrode of an adjacent memory cell. Thereafter, a trench 10 is formed in the semiconductor substrate and within the source region 3, and then, an impurity-doped region of a second conductivity type is formed at the surface of the trench 10 in order to connect the source region. Thereafter, a first insulating layer 6 is formed on both the gate electrode 2 and the first conductive layer 5, and then, a second polycrystalline silicon layer 12b doped by impurity of the second conductivity type is formed on the first insulating layer 6 of the upper part of the gate electrode 2 and the first conductive layer 5 in order to connect the impurity-doped region 13 through a part of the source region. Thereafter a dielectric film 14 is formed on both the second polycrystalline silicon layer 12b and the inside of the trench formed the impurity-doped region 13, and then, a planarized third conductive layer 15 having an etch blocking layer 16 and a fourth conductive layer 17 is formed on the dielectric film 14, and a fifth conductive layer 18 is formed on the entire surface of the above-described structure, thereby completing the manufacturing of the stack-trench combined type capacitor according to the present invention.

Figures 3A to 3K are sectional views showing sequentially one embodiment of the manufacturing method for the stack-trench combined type capacitor according to the present invention.

Figure 3A illustrates the formation process of a transistor and a first photoresist pattern PR1 on the semiconductor substrate 100. In the process of Figure 3A, first of all, a field oxide layer is grown to define an active region by the selective oxidation process on the first conductivity type, e.g., P-type semiconductor substrate 100. Thereafter a gate oxide layer 1 having a thickness of approximately 100Å ~ 200Å is formed on the active region, and then, a first conductive layer which becomes the gate electrode 2 of the transistor such as an impurity-doped first polycrystalline silicon layer is formed on the gate oxide layer 1, and simultaneously, a first conductive layer 5 is formed on any predetermined portion of the field oxide layer 101 in such a manner that the first conductive layer is connected with a gate electrode of an adjacent memory cell. And then, a source region 3 and a drain region 4 are formed through the ion implantation of N^+ impurities of a second conductivity type on the surface of the semiconductor substrate and at the both sides of the gate electrode 2, and then, a first insulating layer 6 is formed on the entire surface of the above-described structure. Thereafter a first photoresist pattern PR1 is formed in order to expose a part of the source region through the processes such as photoresist coating, mask exposure, development, etc on the first insulating layer 6.

Figure 3B illustrates the formation process of an opening 20 through an etching process. In the process of Figure 3B, with the application of the first photoresist pattern PR1, the first insulating layer 6 on the source region is etched through a wet etching process or a wet-dry combined etching process, and therefore, a portion of the source region 3 is exposed. Owing to occurrence of a horizontal etching during the above etching process, the first insulating layer 6 is overetched to the inside in comparison with the actual dimension of the first photoresist pattern PR1, and therefore, an opening 20 is formed as shown in Figure 3B.

Figure 3C illustrates the formation process of a second polycrystalline silicon layer used as a first electrode of the capacitor and a second photoresist pattern PR2. In the process of Figure 3C, after removing the first photoresist pattern, the second polycrystalline silicon layer 12 is deposited on both the first insulating layer 6 and the entire surface of the exposed substrate. Thereafter, through the processes such as photoresist coating, mask exposure, development, etc on the second polycrystalline silicon layer 12, a second photoresist pattern PR2 is formed in order to overlap a part of the gate electrode 2 and the first conductive layer 5.

Figure 3D illustrates the formation process of a first electrode pattern 12a, a second insulating layer OX and a third photoresist pattern PR3. In the process of Figure 3D, with the application of the second photoresist pattern, a first electrode pattern 12a of the capacitor is formed through the etching of the second polycrystalline silicon layer, and then, a second insulating layer OX such as an LTO (Low Temperature Oxide) layer or an HTO (High Temperature Oxide) layer is deposited in order to cover the first electrode pattern 12a. Thereafter, through the processes such as photoresist coating, mask exposure, development, etc on the second insulating layer ox, a third photoresist pattern PR3 is formed in order to expose the second insulating layer OX on the source region. Here, the dimension of the third photoresist pattern PR3 is manufactured to be same as or smaller than the critical dimension of the first photoresist pattern.

Figure 3E illustrates the formation process of a mask OXM for the purpose of forming the trench. In the process of Figure 3E, the second insulating layer is etched by applying the third photoresist pattern, and the mask OXM used to form the trench is manufactured by removing the third photoresist pattern.

Figure 3F illustrates the formation process of a trench. In the process of Figure 3F, a trench 10 is formed in the semiconductor substrate within source region by applying the mask OXM of the second insulating layer.

Figure 3G illustrates the formation process of a sacrificial oxide layer 11. In the process of Figure 3G, a sacrificial oxide layer 11 having the thickness of approximately 100Å ~ 300Å is formed through thermal oxidation on both the side of the first electrode pattern 12a and the inside of the trench 10 by using the second insulating layer used as the mask OXM in the process of forming the trench in order to round the sharp corner region of the trench. Here, the second insulating layer is utilized as the seed in order to form the sacrificial oxide layer 11. Also, Owing to the formation of the sacrificial oxide layer 11, the surface damage of the semiconductor substrate can be removed which is produced in the process of forming the trench 10.

Figure 3H illustrates the formation process of an impurity-doping. In the process of Figure 3H, after removing the above mask and the sacrificial oxide layer by means of the BOE (Buffered Oxide Etchant), N^+ type impurity of the second conductivity type such as $POCl_3$, or P, or As, etc, is doped into both the second polycrystalline silicon layer of the first electrode pattern and the semiconductor substrate of the inside of the trench by means of an impurity-diffusion or an ion implantation. Owing to directly connecting the impurity-doped second polycrystalline silicon layer 12b with the impurity-doped region formed at the surface of the trench 10 through a part of the N^+ type source region which is formed by overetching the first insulating layer of the Figure 3B, the above impurity-doped second polycrystalline silicon layer 12b and the above impurity-doped region 13 are used as the first electrode of the capacitor.

Figure 3I illustrates the formation process of a dielectric film 14. In the process of Figure 3I, a first oxide layer having the thickness of approximately 10Å ~ 60Å such as an HTO layer or an LTO layer is deposited on both the impurity-doped second polycrystalline silicon layer 12b and the inside of the trench 10 including the impurity-doped region 13. Thereafter, a nitride layer having the thickness of approximately 50Å ~ 150Å is formed on the first oxide layer during the flowing of NH_3 gas by means of the LPCVD (Low Pressure Chemical Vapor Deposition) technigue, and then, the dielectric film 14 of the ONO structure, i.e., Oxide layer/ Nitride layer/ Oxide layer structure is formed by growing a second oxide layer having the thickness of approximately 10Å ~ 60Å on the nitride layer. Here, as an HTO layer or an LTO layer is used as the lower oxide layer of the dielectric film having ONO structure, uniform oxide layer can be obtained which is not affected by the doped level and kind of the substrate on which the oxide layer is formed. In other words, uniform oxide layer can be obtained on both the impurity-doped second polycrystalline silicon layer 12b and the inside of the trench 10 including the impurity-doped region 13 by simultaneously depositing the oxide layer such as an HTO layer or an LTO layer. Also, the characteristic of the dielectric film can be improved by manufacturing the nitride layer having a multi-layer structure among the dielectric film of the ONO structure.

Figure 3J illustrates the formation process of a third conductive layer 15, an etch blocking layer 16 and a fourth conductive layer 17. In the process of Figure 3J, the interior of the trench is filled with a third conductive layer used as the first layer of the second electrode of the capacitor, e.g., an impurity-doped third polycrystalline silicon layer on the dielectric film 14. Thereafter, after thinly depositing an etch blocking layer 16 of an LTO layer or an HTO layer on the third conductive layer 15 in order to remove the defects which produce the voids in the interior of the trench during the filling-up, the voids producing in the interior of the trench are removed by continuing to form the fourth conductive layer 17, e.g., an impurity-doped fourth polycrystalline silicon layer.

Figure 3K illustrates the formation process of a fifth conductive layer 18 after planarizing the surface of the sample obtained by the above described processes. In the process of Figure 3K, in order to planarizing the surface after forming the fourth conductive layer 17, etchback process is carried out until the etch blocking layer 16 is exposed, and the etch blocking layer 16 exposed from the etching process is romoved by BOE. Thereafter, the stack-trench combined type capacitor is accomplished by depositing a fifth conductive layer 18 used as the second layer of the second electrode of the capacitor such as the fifth polycrystalline silicon layer doped by impurity.

According to the present invention as described above, as both the impurity-doped polycrystalline silicon layer of the upper portion of the transistor and the inside of the trench including the impurity-doped region are simultaneously used as the first electrode of the capacitor, the surface area of the capacitor electrode can be made larger than that of the capacitor electrode which was made by using the conductive layer formed in the inside of the trench as the first electrode of the capacitor in prior art, therefore the capacitor having large capacitance can be obtained.

Also, the break-down phenomina of the dielectric film due to the local electric field at the boundary of the polycrystalline silicon and the single crystalline silicon and the non-uniformity of the dielectric film by each differently growing thickness of the oxide layer on the polycrystalline silicon and the single crystalline silicon can be prevented by using an HTO layer or an LTO layer as the lower oxide layer of the dielectric film having ONO structure.

Also, by forming in turn the etch blocking layer and the fourth conductive layer on the third conductive layer used as the first layer of the second electrode of the capacitor, the voids produced in the interior of the trench during the formation of the third conductive layer can be removed. Therefore, the reliability and the electrical characteristics of capacitor can be improved.

CLAIMS:

1. A semiconductor device comprising:

a field oxide layer selectively formed in order to define an active region on a semiconductor substrate of a first conductivity type;

a gate electrode of the first conductive layer electrically insulated on said active region;

a source region and a drain region of a second conductivity type formed on the surface of said semiconductor substrate and at the both sides of said gate electrode;

a trench formed in said semiconductor substrate within said source region;

an impurity-doped region of said second conductivity type formed at the surface of said trench in order to be connected to said source region;

a first insulating layer for insulating said first conductive layer;

a second conductive layer formed in order to be connected to said impurity-doped region through a part of said source region on said first insulating layer;

a dielectric film formed on both said second conductive layer and the inside of said trench including said impurity-doped region;

a third conductive layer having an etch blocking layer and a fourth conductive layer in order to planarize the main center formed on said dielectric film; and

a fifth conductive layer formed in order to cover said third conductive layer and said fourth conductive layer.

2. The semiconductor device as claimed in claim 1, wherein, said first, second, third, fourth and fifth conductive layers are an impurity-doped polycrystalline silicon layer, respectively.

3. The semiconductor device as claimed in claim 1, wherein, impurites of said second conductive layer and said impurity-doped region are $POCl_3$, or P, or As.

4. The semiconductor device as claimed in claim 1, wherein, said dielectric film constituts the structure of oxide layer/nitride layer/oxide layer (ONO structure).

5. The semiconductor device as claimed in claim 4, wherein, a lower oxide layer of said dielectric film having ONO structure is made of an HTO layer or an LTO layer.

6. The semiconductor device as claimed in claim 5, wherein, said lower oxid layer has the thickness of 10Å ~ 60Å.

7. The semiconductor device as claimed in claim 1, wherein, said etch blocking layer is made of an HTO layer or an LTO layer.

8. A manufacturing method for a semiconductor device comprising :

first process of growing a field oxide layer on a semiconductor substrate of a first conductivity type in order to define an active region;

second process of forming a first insulating layer on the sample obtained after forming a gate electrode of a first conductive layer, a source region and a drain region on said active region;

third process of forming an opening in order to expose a part of said source region;

fourth process of forming a first electrode pattern by depositing a second polycrystalline silicon layer on said first insulating layer and the entire surface of the exposed substrate;

fifth process of forming a mask by depositing a second insulating layer on said first electrode pattern;

sixth process of forming a trench in said semiconductor substrate within said source region by applying to said mask;

seventh process of doping impurities on both said first electrode pattern and said semiconductor substrate of the inside of said trench;

eighth process of forming a dielectric film on both said impurity-doped first electrode pattern and said inside of said trench including said impurity-doped region;

ninth process of depositing a third conductive layer, an etch blocking layer and a fourth conductive layer on said dielectric film in turn; and

tenth process of depositing a fifth conductive layer after planarizing the sample obtained in said processes.

9. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, said opening of said third process is formed by etching said first insulating layer through a wet etching or a wet-dry combined etching.

10. The manufacturing method for a semiconductor device as claimed in claim 9, wherein, said first insulating layer is overetched larger than the dimension of the photoresist pattern used in forming said opening.

11. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, said second insulating layer of said fifth process is made of an LTO layer or an HTO layer.

12. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, a dimension of said mask of said fifth process is same as or smaller than the critical dimension of said photoresist pattern used in forming said opening of said third process.

13. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, after forming said trench of said sixth process, said mask of said fifth process is used as a seed of growing sacrificial oxide layer

in order to round the sharp conner region of said trench.

14. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, an impurity-doping technique of said seventh process is a diffusion technique or an ion implantation.

15. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, said dielectric film of said eighth process include the process of forming a first oxide layer on both said second conductive layer and said inside of said trench including said impurity-doped region, the process of forming a nitirde oxide layer on said first oxide layer, and the process of forming a second oxide layer on said nitride layer.

16. The manufacturing method for a semiconductor device as claimed in claim 15, wherein, said first oxide layer is made of an HTO layer or an LTO layer.

17. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, said etch blocking layer of said ninth process is made of an LTO layer or an HTO layer.

18. The manufacturing method for a semiconductor device as claimed in claim 8, wherein, said planarization of said tenth process is formed by etchback techinque.

19. The manufacturing method for a semiconductor device as claimed in claim 18, wherein, said etch blocking

layer exposed through the process of said planarization is removed by BOE.

20. A semiconductor device having a memory cell including a trench capacitor, said capacitor comprising a recess extending into the depth of a semiconductor substrate and a conductor/dielectric/ conductor sandwich structure formed in the trench, the outermost conductor layer comprising an impurity-doped surface region formed in the wall of the trench.

21. A semiconductor device substantially as hereinbefore described with reference to Figure 2 of the accompanying drawings.

22. A method of manufacturing a semiconductor device, substantially as hereinbefore described with reference to Figures 3A to 3K of the accompanying drawings.

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