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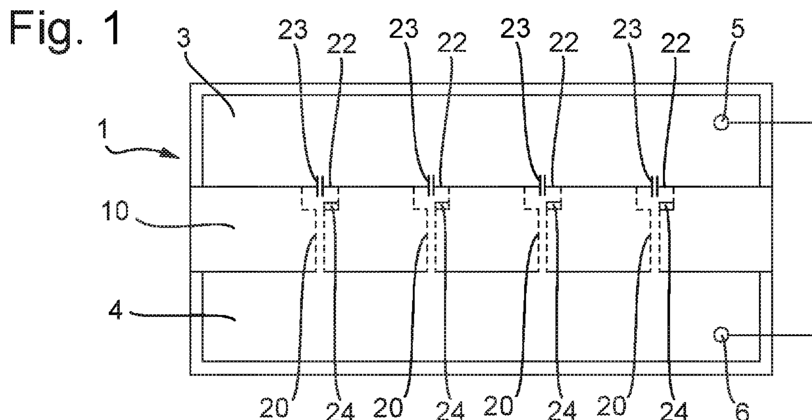
(54) **Title:** NANOPORE SENSING DEVICE



(57) **Abstract:** A nanopore sensing device comprises a planar structure provided with plural fluidic passages extending between the first and second chambers. The planar structure supports nanopores in membranes across respective passages and sensor electrodes are arranged to sense a fluidic electrical potential in respective passages between the nanopores and the second chamber. The passages comprise planar fluidic resistor portions between the sensor electrode and the second chamber, the planar fluidic resistor portions extending in a planar direction of the planar structure and being configured to form a fluidic resistor.

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Nanopore Sensing Device

The present invention relates to a nanopore sensing device.

Nanopore sensing devices have been developed for sensing a wide range of species, including single molecules such as polymer molecules. A known nanopore sensing device is a MinION^{TM}, manufactured and sold by Oxford Nanopore Technologies Ltd. The nanopore- based sensing therein employs the measurement of ionic current flow through a biological nanopore located in a highly resistive amphiphilic membrane. The MinION^{TM} has an array of nanopore sensors. As a molecule, such as a polymer analyte e.g. DNA, is caused to translocatea nanopore, measurement of the fluctuations in ionic current may be used to determine the sequence of the DNA strand. Nanopore devices for detection of analytes other than polynucleotides such as proteins are also known from WO2013/123379.

Many nanopore sensing devices, such as MinION^{TM}, use biological nanopores, but an alternative is to use solid state nanopores. An example of a nanopore sensing device using solidstate nanopores is disclosed in WO2016/127007, hereby incorporated by reference in its entirety. The performance of solid-state nanopore sensors is limited by the sensing components,manufacturing techniques and their tolerances, which can occur as a result of variation in the formation of the nanopore or the assembly of the sensor. These and other factors detriment thebandwidth, sensitivity and ability to control such nanopore sensors.

The present invention is concerned with the overcoming problems associated with implementing a nanopore sensor device having a plurality of nanopore sensors.

According to an aspect of the invention, there is provided a nanopore sensing device comprising: first and second chambers; a planar structure provided with plural fluidic passagesextending between the first and second chambers, the planar structure being configured to support nanopores in membranes across respective passages; sensor electrodes arranged to sense a fluidic electrical potential in respective passages between the nanopores and the second chamber, wherein the passages comprise planar fluidic resistor portions between the sensor electrode and the second chamber, the planar fluidic resistor portions extending in a planar direction of the planar structure and being configured to form a fluidic resistor.

By providing the planar fluidic resistor portion a voltage divider is formed across the sensor electrode including the resistance of the nanopore in one leg and including the

resistanceof the planar fluidic resistor portion in the other leg. As a result, the fluidic electrical potentials sensed in the passages by the sensor electrodes allow sensing of the current flowing through thepassage and hence the nanopores. This allows for nanopore sensing.

5 Furthermore, the formation of the planar fluidic resistor portion extending in a planar direction of the planar structure improves the ease of manufacture compared to a fluidic resistor portion formed by an access hole extending through the thickness of the planar structure. This is because typical resistances of nanopores mean that the fluidic resistor portion needs to be provided with a relatively high resistance to perform the voltage divider 10 with the nanopore. Thus, fluidic resistor portions formed by access holes extending through the thickness of the planar structure need to be relatively long and to have a relatively high aspect ratio which is difficult to manufacture. In contrast, a planar fluidic resistor portion extending in a planar direction of the planar structure is in principle more easy to form. However, their configuration and formation remains a technical issue, and some of 15 the following aspects of the present invention are concerned with improving the ease of manufacture.

The fluidic resistor portion can be linear in shape. The fluidic resistor portion can have a continuous linear shape, with no bends or turns. The fluidic resistor portion can be linear in shape and extend in a direction normal to the planar structure. The fluidic 20 resistance of the fluidic resistor portion can be less than the resistance of the nanopore. The fluidic resistance ofthe fluidic resistor portion can be between less than 50% and about 1% of the resistance of the nanopore. The fluidic resistance of the fluidic resistor portion can be about 10% of the resistance of the nanopore. In one aspect, the planar structure comprises: a nanopore support layer that is configured to support the nanopores in the membranes 25 extending across the passages; and a further layer in which the planar fluidic resistor portions are formed.

By forming the planar fluidic resistor portions in a different layer from the nanopore support layer supports the nanopores in the membranes, the nanopore support layer may be designed and manufactured with suitable properties for the nanopore support, while 30 allowing the planar the planar fluidic resistor portions to be formed in a further layer having different material properties.

In some types of embodiment, the nanopore support layer is provided with wells

openinginto the first chamber, the wells forming part of the passages and being configured to support said nanopores in said membranes extending across the wells.

The further layer may be a dielectric layer. This facilitates manufacture of the planar fluidic resistor portions by permitting use various techniques suitable for processing dielectric materials, for example deposition and removal process.

The first and second chambers may be on opposite sides of the planar structure so that the passages extend through the planar structure. In that case, the substrate may be provided with access holes which extend therethrough and form part of the passages.

In another aspect which may be combined with a separate nanopore support layer but isnot dependent thereon, the first and second chambers are on opposite sides of the planar structureso that the passages extending through the planar structure. In that case, the planar structure maycomprise a substrate; and a further layer that is supported by the substrate, with the planar fluidic resistor portions being formed in the further layer, and the substrate being provided with accessholes extending therethrough to form part of the passages.

This facilitates manufacture of the planar fluidic resistor portions by allowing the furtherlayer to be processed on the substrate. For example, the further layer may be a dielectric layer which, as mentioned above, facilitates manufacture of the planar fluidic resistor portions by permitting use of various techniques suitable for processing dielectric materials, for example deposition and removal process.

In some embodiments, the further layer is between the first chamber and the substrate. Advantageously, this locates the further layer in which the planar fluidic resistor portions are formed closer to the nanopore within the passages.

Advantageously, each access hole may be shared by plural passages by being fluidicallyconnected in common to plural planar fluidic resistor portions. This permits the area density ofthe passages and nanopores across the area of the planar structure to be increased.

The substrate may be a semiconductor wafer. This permits the planar fluidic resistor portions to be formed in the further layer using conventional semiconductor processing techniques.

In addition, the planar structure may further comprise a circuit layer supported by the semiconductor wafer, the circuit layer comprising circuit components connected to the sensor electrode. This allows the semiconductor wafer both to provide a substrate

supporting both thecircuit layer and the further layer in which the planar fluidic resistor portions are formed.

In this case, advantageously, the circuit layer is formed on the semiconductor wafer andthe dielectric layer is formed on the circuit layer. This order simplifies the manufacture to provide the circuit layer and the further layer in which the planar fluidic resistor portions areformed.

In other embodiments, the planar structure further comprises a semiconductor waferhaving a circuit layer supported thereby, the circuit layer comprising circuit components connected to the sensor electrode, the semiconductor wafer and the circuit layer is provided withaccess holes which extend therethrough and form part of the passages, and the substrate isbonded to the semiconductor wafer between the semiconductor wafer and the second chamber.

In other embodiments, the planar structure comprises: a substrate; a circuit layer supported by the semiconductor wafer, the circuit layer comprising circuit components connected to the sensor electrode; and a nanopore support layer that is configured to support thenanopores in the membranes extending across the passages, the planar fluidic resistor portions being formed in the nanopore support layer. This facilitates manufacture of the planar fluidic resistor portions by permitting various techniques suitable for processing the nanopore supportlayer.

In this case, the nanopore support layer may be provided with wells opening into the first chamber, the wells forming part of the passages and being configured to support said nanopores in said membranes extending across the wells.

The first and second chambers may be on opposite sides of the planar structure, in whichcase the passages extend through the planar structure. The substrate can be provided with access holes, forming part of the passages, which extend therethrough.

An access hole may be shared by plural passages by being fluidically connected in common to plural planar fluidic resistor portions. When an access hole is shared between two or more passages the resistance of the access hole is configured to inhibit crosstalk between passages. The resistance of a common access hole can be negligible within the passage.

The substrate may be a semiconductor wafer.

In any of the embodiments, advantageously, the planar fluidic resistor portion may

extend along a tortuous path. This facilitates packaging of a planar fluidic resistor portion withsufficient length to provide a desired resistance within a discrete area on the planar structure, thereby assisting with increasing the area density of the nanopore sensors.

In any of the embodiments, advantageously, the planar fluidic resistor portion may comprise sections each extending in the planar direction of the planar structure but at different depths within the planar structure. This facilitates packaging of a planar fluidic portion with sufficient length to provide a desired resistance within a discrete area on the planar structure, thereby assisting with increasing the area density of the nanopore sensors. The sections at different depths may overlap.

To allow better understanding, embodiments of the present invention will now be described by way of non-limitative example with reference to the accompanying drawings, in which:

Fig. 1 is a cross-sectional view of a nanopore sensing device;

Fig. 2 is a cross-sectional view of a planar structure of the nanopore sensing device;

Fig. 3 is a plan view of the planar structure;

Fig. 4 is a diagram of a circuit of the nanopore sensing device;

Fig. 5 is a plan view of a planar fluidic resistor portion that can be formed in a dielectriclayer of the planar structure;

Figs. 6a – 6j are a series of cross-sectional views of layers being processed during manufacture of the planar structure;

Fig. 7 is a cross-sectional view of the planar structure with a first modified construction;

Figs. 8a and 8b are cross-sectional views of the planar structure with second and thirdmodified constructions;

Fig. 9 is a plan view of an alternative configuration of the planar fluidic resistor portion formed in a dielectric layer of the planar structure;

Figs. 10a - 10m are a series of cross-sectional views of layers being processed during manufacture of the planar structure in which the planar fluidic resistor portion has the alternativeconfiguration of Fig. 9;

Figs. 11a - 11d are a series of cross-sectional views of layers being processed during manufacture of the base layer of the planar structure with a fourth modified construction in which the planar fluidic resistor portion is formed on a substrate that is

bonded to semiconductorwafer; and

Figs. 12a – 12f are a series of cross-sectional views of layers being processed during manufacture of the planar structure with a fifth modified construction in which the planar fluidic resistor portion is formed in the nanopore support layer.

5 Fig. 1 shows a nanopore sensing device 1 that is arranged as follows.

The nanopore sensing device 1 comprises a first chamber 3 and a second chamber 4 with a planar structure 10 between the first and second chambers 3, 4. The first and second chambers3, 4 are filled with fluid, such as an ionic solution or ionic liquid, in use. The first and second chambers 3, 4 are shown schematically in Fig. 1 but may be arranged with any 10 suitable structure.

The first and second chambers 3, 4 may be closed or may arranged as part of flow cells permitting flow of solution therethough.

The planar structure 10 is provided with plural fluidic passages 20 that extend between the first and second chambers 3, 4. Thus, the fluidic passages 20 are filled with 15 fluid, in use, andis fluidically connect the first and second chambers 3, 4. Each of the fluidic passages 20 is connected to the first and second chambers 3, 4, so the nanopores 22 lies in parallel paths of fluidic communication. The plural fluidic passages 20 may be arranged in an array in two dimensions across the planar structure 10.

In Fig. 1, the construction of the planar structure 10 is not shown Fig. 1 and so the 20 fluidicpassages 20 are shown schematically. The configuration of the planar structure 10 and the fluidic passages 20 is described in detail below.

In this example, as the first and second chambers 3, 4 are on opposite sides of the planarstructure 10, the passages 20 extend through the planar structure 10. However, as an alternative,the first and second chambers 3, 4 could be arranged in different locations on 25 the same side of the planar structure 10.

In this example, drive electrodes 5, 6 are provided in the first and second chambers 3, 4.In use, an electrical potential difference may be applied across the drive electrodes 5, 6 and therefore across each fluidic passage 20 to induce an analyte to flow between the first and secondchambers 3, 4. The drive electrodes 5, 6 may be configured to apply substantially 30 the same potential difference across all the fluidic passages 20. Additionally, or alternatively, the nanopore sensing device 1 can be configured to induce an analyte flow through the fluidic passages 20 using other techniques.

The first chamber 3 may function as a cis chamber and hold an analyte to be analysed by the nanopore sensing device 1. The second chamber 4 may function as a trans chamber and receive the analyte from the first chamber 3.

As described in more detail below, the planar structure 10 supports nanopores 23 in membranes 22 that extend across respective passages 20. Examples of suitable membranes 22 and nanopores 23 are described below.

The fluidic passages 20 are each provided with a sensor electrode 24 arranged to sense a fluidic electrical potential in the respective passage 20 between the nanopores 23 and the second chamber 4. As an analyte passes through a nanopore 22, the fluctuation in electrical potential caused by changes in ion current flow is detected by the sensor electrode 24. Thus, the passage 20 and the sensor electrode 24 formed therein act as respective sensors in the nanopore sensor device 1.

Fig. 2 illustrates the construction of the planar structure 10, showing a single one of theplural fluidic passages 20 for clarity, as follows.

The planar structure 10 comprises a nanopore support layer 30 and a base layer 100 which are fixed together.

The nanopore support layer 30 is configured to support the nanopores 23 in the membranes 22 extending across the passages 20. In particular, the nanopore support layer 30 isprovided with wells 31 opening into the first chamber 3. The wells 31 form part of the passages 20. The wells 31 are configured to support the membranes 22 extending across the passages 20,specifically extending across the openings of the wells 31, and thereby to support the nanopores 22. The nanopore support layer 30 includes a wall layer 32 comprising walls 33 that define thewells 31.

The nanopore support layer 30 may be made of any suitable material, for example: ceramics such as silicon dioxide or silicon nitride; photoresist such as SU-8 or TMMF/TMMR;plastic such as acrylic (PMMA); or epoxy resin.

Fig. 3 shows an example in which the plural wells 31 are arranged in a plane in a regularplanar array having a repeating structure in plan view (from above in Fig. 2). Fig. 3 shows onlynine wells 4 for simplicity, but in general the nanopore support layer 30 may have any number of wells 31, typically being much larger than nine, for example of the order of 1000 or more, practically in the order of 100,000, and feasibly up to 5,000,000 or more. Each of the wells 31 and the corresponding passages 20 is arranged within a

respective footprint 35.

The base layer 100 is between the nanopore support layer 30 and the second chamber 4and includes the following layers. The base layer 100 includes a semiconductor wafer 101 which forms a substrate in this example and supports a circuit layer 110 and a dielectric layer 120. Thecircuit layer 110 comprises circuit components connected to the sensor electrodes 24. The circuit components in respect of each passage 20 are arranged within the same footprint 35 as the passage 20.

The semiconductor wafer 101 is typically made of silicon, but can in principle be any semiconductor material which is suitable as a support for a circuit layer 110, such as silicon dioxide, quartz, glass, amorphous aluminium oxide or sapphire.

The dielectric layer 120 provides a planar fluidic resistor portion 150 that forms part ofthe passage 20, so forms the further layer in this example. In this manner, the fluidic passage 20provides a fluidic resistor between the sensor electrode 24 and the second chamber 4. More specifically, the fluidic passage 20 through the base layer 100 includes the following portions that are fluidically connected in series:

- the well 31, or access thereto, as described above;
- a dielectric access hole 121 that extends from the well 31 through the dielectric layer;
- the planar fluidic resistor portion 150 formed in the dielectric layer and fluidically connected to the dielectric access hole 121;
- a circuit layer access hole 111 extending through the circuit layer 110 and fluidically connected to the planar fluidic resistor portion 150; and
- a wafer access hole 102 extending through the semiconductor wafer 101 and fluidicallyconnected to the circuit layer access hole 111.

The sensor electrode 24 is formed in the dielectric access hole 121.

The planar fluidic resistor portion 150 is configured to form a fluidic resistor. In this manner, the fluidic passages 20 are configured to provide fluidic resistors between the sensor electrode 24 and the second chamber 4 as will now be described with reference to Fig. 4 whichis a diagram of a circuit of the nanopore sensing device 1.

As a result, the passage 20 forms a voltage divider 50 with the nanopore 23 such that the sensor electrode 24 is positioned between two legs 51 and 52 of the voltage divider 50. The firstleg 51 of the voltage divider 50 is formed between the first drive electrode 5 and the sensor electrode 24, and the second leg 52 of the voltage divider 50 is formed between the

sensor electrode 24 and the second drive electrode 6.

The resistance of the nanopore 23 with any additional solution resistance between first drive electrode 5 and the sensor electrode 24 is present in a first leg 51 of the voltage divider 50. The well 31 and dielectric access hole 121 may be designed to have a minimal fluidic resistance compared to the nanopore 23.

The fluidic resistance of the planar fluidic resistor portion 150 is present in the second leg 52 of the voltage divider 50. The circuit layer access hole 111 and the wafer access hole 102 may be designed to provide a fluidic resistance that is negligible compared to the fluidic resistance of the planar fluidic resistor portion 150, but this is not essential and they may be designed to provide additional fluidic resistance.

The first and second chambers 51, 52 also have a negligible fluidic resistance compared to the passage 20 due to the relatively narrow cross-sectional area of the passage 20.

A sensor circuit 55 is configured to sense the electrical potential of the fluid at the sensorelectrode 24 in the passage 20. As a result of the voltage divider 50, the fluidic electrical potentials sensed in the passage 20 by the sensor electrode 24 permits sensing of the current flowing through the passage 20 and hence the through the nanopore 23. The sensor electrode 24can detect fluctuations in voltage as matter, such as a molecule on a strand of DNA, translocates through the nanopore 23. This provides nanopore sensing.

The sensor electrode 24 lies between the nanopore 23 and the planar fluidic resistor portion 150. Although the configuration in Fig. 2 is an example, the sensor electrode 24 can belocated elsewhere in the passage 20, for example in the well 31.

In some embodiments, the sensor electrode 126 can function as a terminal (e.g. base or gate) of a transistor device for measuring electrical potential of the fluid at the location of the sensor electrode 24.

Some or all of the components of the sensor circuit 55 are formed in the circuit layer. 110. Such components may include, for example, any one or more of: a transistor device of which the sensor electrode 24 functions as a terminal (e.g. base or gate), amplifiers, gate circuits and so on. Where only some of the components of the sensor circuit 55 are formed in the circuitlayer 110, the remainder of the sensor circuit 55 may be formed in a separate integrated circuitchip connected to the circuit layer 150.

Considerations in the design of the planar fluidic resistor portion 150 and the overall

passage 20 are as follows.

The passage, and in particular the planar fluidic resistor portion 150, can be configuredsuch that the resistance of the first and second legs 51, 52 of the voltage divider 50 are substantially matched when the passage 22 is filled by fluid, and relatively high relative to the resistance of fluid in the first and second chambers 3, 4 such that the resistance of the first and second chambers 3, 4 does not appreciably influence the measurements.

The signal-to-noise ratio may be optimised by selecting the fluidic resistances of the first and second legs 51, 52 of the voltage divider 50 to be equal. However, this is not essential and the fluidic resistance of the planar fluidic resistor portion 150 may be varied to take account ofother factors, while still obtaining an acceptable signal-to-noise ratio. An acceptable signal-to- noise ratio may be achieved with the fluidic resistance of the second leg 52 of the voltage divider50 being significantly less than the resistance of first leg of the voltage divider, for example with the fluidic resistance of the second leg 52 of the voltage divider 50 being 10% or less of the resistance of first leg 51 of the voltage divider 50, for example 2% thereof. In some embodiments, a lower limit on the fluidic resistance of the second leg 52 of the voltage divider50 may be set by the desired signal to noise ratio.

Other factors that may be considered in the selection of the fluidic resistance of the second leg 52 of the voltage divider 50, and specifically the planar fluidic resistor portion 150,are as follows.

As the fluidic resistance of the second leg 52 increases, the diffusion of ions decreases,causing an increased depletion of ions near the pore, and thereby causing a decay of the signal over the timescale of a typical event over which a signal is obtained. In order to increase the limit on read length caused by this effect, the fluidic resistance of the planar fluidic resistor portion 150 may be reduced. In many embodiments, this factor may place an upper limit on thefluidic resistance of the planar fluidic resistor portion 150.As the fluidic resistance of the planarfluidic resistor portion 150 increases, the variation in the voltage across the nanopore 23 increases, which can complicate signal processing. In order to limit this effect, the fluidic resistance of the planar fluidic resistor portion 150 may be reduced. Reducing the fluidic resistance of the planar fluidic resistor portion 150 may increase bandwidth or provide leeway for additional capacitance in the passage 20 or the membrane 22.

Taking into account these factors, the fluidic resistance of the second leg of the voltage divider may be less than the resistance of the nanopore 23, typically at most 50%, or at most 25% of the resistance of the nanopore 23. In some embodiments, the optimal fluidic resistance of the second leg 52 of the voltage divider 50 may be around 10% of 5 the resistance of the nanopore 23.

When reducing the ratio of the fluidic resistance of the second leg 52 of the voltage divider 50 to the resistance of the first leg 51 of the voltage divider 50, the signal to noise ratiodoes not scale linearly with that resistance ratio. For example, in some embodiments when the fluidic resistance of the second leg 52 of the voltage divider 50 is around 10% of 10 the resistanceof the nanopore 23, then the signal to noise ratio is around 30% of its optimal value.

Fig. 5 illustrates an example of the planar fluidic resistor portion 150 which is arranged as follows.

The planar fluidic resistor portion 150 extends in a planar direction of the planar 15 structure 10 along a tortuous path between the dielectric access hole 121 and the circuit layer access hole 111. By providing the planar fluidic resistor portion 150 with such a planar configuration it is can be manufactured in the dielectric layer 120. By providing the planar fluidic resistor portion150 with a tortuous path, the planar fluidic resistor portion 150 may be provided with sufficientlength while being packaged within a discrete area on the 20 planar structure 10, that being an approximately square area in this example within the footprint 35.

In this example, the tortuous path of the fluidic resistor portion 150 is rectilinear and comprises plural straight legs extending back and forth. More generally, the planar fluidic resistor portion 150 could be provided with any suitable tortuous path, being any path that is 25 nota straight line between its ends, ranging including paths that are much simpler or much more complex to that shown in Fig. 5. For example, a simple variation is for the tortuous path could comprise plural legs extending back and forth in a similar manner, but being a curved configuration, rather than being rectilinear. In other examples, the tortuous path could have some other curved shape, including a spiral shape.

30 The geometry of the planar fluidic resistor portion 150, in particular its path length and cross-sectional area are designed to provide the desired fluidic resistance, in conjunction with the fluid with which it is to be filled. That is, the fluidic resistance of the

planar fluidic resistorportion 150 can be varied by varying its length, cross-sectional area and the ionic concentrationsof the fluids therein. For example, to increase the fluidic resistance, the planar fluidic resistor portion 150 can be configured with an increased ratio of length to cross-sectional area and/or a lower ionic concentration. The passage may be provided with a lower ionic concentration thanthe first and/or second chambers 3, 4, because maintenance of a relatively high ionic concentration in the first and second chambers 3, 4 improves the signal to noise ratio.

In embodiments, the planar fluidic resistor portion 150 may have a length of at least 1μm, at least 10μm, at least 100μm, or at least 1000μm.

In embodiments, the planar fluidic resistor portion 150 may have cross-section having a characteristic dimension (for example the square root of the area) that is at most 100μm, at most10μm, at most 1μm, or at most 10nm.

In general, any length and cross-section may be chosen together.

In very general terms, the passage 20 could have any geometry that provides a measurable signal at the sensor electrode 24. The measurable signal will depend on the measurement circuit, bandwidth, noise etc, but may typically be at least 1μV, at least 10μV, at least 100μV, or at least 1mV.

Some methods for forming the planar structure 10 are as follows.

In some of these methods, the planar fluidic resistor portions 150 are formed in the dielectric layer 120. This permits use of various techniques suitable for processing dielectric materials, for example deposition and removal processes, thereby facilitating manufacture of the planar fluidic resistor portions 150.

Also, in some of these methods, the circuit layer 110 is formed on the semiconductor wafer 101 and the dielectric layer 120 is formed on the circuit layer 110, and is therefore betweenthe first chamber 3 and the semiconductor wafer 101. This again simplifies the manufacture because the circuit layer 110 may be formed using conventional semiconductor processing techniques and then the planar fluidic resistor portions 150 is formed in the dielectric layer 120 on top. This facilitates the construction of the entire base layer 100 using similar techniques, typically as part of a common process in a semiconductor fabrication facility. It also avoids theneed for a separate bonding process as would be needed the planar fluidic resistor portions 150 are formed on a substrate separate from the semiconductor wafer 101 on which the circuit layer110 is formed.

Figs. 6a – 6j show a series of views of layers being processed during a method of manufacture which is performed as follows. The base layer 100 is fabricated from a semiconductor wafer 101, for example a single complementary metal-oxide semiconductor (CMOS) silicon wafer.

5 Fig. 6a shows the semiconductor wafer 101 prior to the fabrication of the structure of the base layer, with deep trench isolation (DTI) and a connection in the circuit layer 110 for the sensor electrode 24.

In Fig. 6b, the metal sensor electrode 24 has been deposited. In this example, the sensorelectrode 24 is a platinum electrode approximately 100nm thick, which is deposited
10 by sputtering, evaporation, or plating as Pt is not a standard metal in a typical CMOS foundry. Passivation of the surface and open electrode has been performed. The passivation can be plasma-enhanced chemical vapor deposition (PECVD) low stress nitride or oxynitride. A thickness of 500 nm - 1 μm is sufficient for passivation, since further passivation layers will deposited later in the process. A circuit layer access hole 111 is
15 formed through the circuit layer110, specifically through the region of the DTI, although generally the circuit layer access hole 111 may be formed in other regions of the circuit layer 110. Typically, the circuit layer access hole111 through the DTI is approximately 6 μm in diameter and 20 μm deep.

Fig. 6c shows that a sacrificial polymer coating has been deposited via a lithography
20 process. The sacrificial polymer can be polyimide or any other compatible polymer. The sacrificial polymer coating is formed in the shape of the channels of the planar fluidic resistor 15 portion 150 and also fills the circuit layer access hole 111. The thickness of the sacrificial polymer defines the thickness of the planar fluidic resistor portion 150, which in this example is approximately 300 nm. The width in the plane of the channels making up
25 the tortuous path of the planar fluidic resistor portion 150 will be chosen by the micro-electromechanical system(MEMS) foundry. In this example, the width is approximately 1 μm. For larger structures, for example where the width in the plane of the channels is larger, supporting pillars along the tortuous path might be necessary. These can be formed by creating additional holes in the sacrificial polymer layer (not shown in Fig. 6).

30 In Fig. 6d, a thin passivation layer is deposited that forms the lower portion of the dielectric layer 120. The thin passivation layer can be the same PECVD low stress nitride or oxynitride as used previously in the process. The thin passivation layer needs to be of a

minimum thickness to hold structural integrity during later stages of the manufacturing process,but also need to be thin enough to permit the fabrication and later filling in of vias. For the aboveexample of a 1μm width in the plane of the channels, a thickness of 1-2 μm for the thin passivation layer is appropriate.

5 In the step shown in Fig. 6e, open vias 154 are formed through the thin passivation layerto provide access to the sacrificial polymer (as shown in Fig. 5). The vias 154 expose the sides of the sacrificial polymer for the etching, dissolving or plasma ashing process to remove the sacrificial polymer. For a high aspect ratio channel such as used in the tortuous path of the planar fluidic resistor portion 150, multiple locations along the tortuous path 10 need to be exposedto reduce the etch aspect ratio. This can be promoted by the design of the tortuous path of the planar fluidic resistor portion 150. Fig. 6f shows the state following plasma ashing or etching of the sacrificial polymer.

In Fig. 6g, a thick passivation layer is deposited to fill in the vias 154 that were used to provide access to the sacrificial polymer. The thick passivation layer (also referred to as 15 a fill-in layer) should be much thicker than the earlier thin passivation layer, but can be formed from the same PECVD low stress nitride or oxynitride material. In this example, a thickness ofapproximately 5 μm is used. This allows the thick passivation layer to hold the structureintegrity of the planar fluidic resistor portion 150. Following this, in Fig. 6h, the thickpassivation layer is opened above the sensor electrode 24 to form the 20 dielectric access hole 121.

In Fig. 6i, the semiconductor wafer 101 is ground down from below to thin it. In this example, the semiconductor wafer 101 is thinned to approximately 200-400 μm. Additionally,or alternatively, the semiconductor wafer 101 can be ground down at the beginning or middle of the process. This reduces the aspect ratio for the deep reactive ion 25 etching (DRIE) process used to form the wafer access hole 102. During the thinning process, the front side of the semiconductor wafer, which now holds the structures deposited in earlier steps, is protected. The wafer access hole 102 is formed by DRIE, which is stopped at the DTI that holds the circuitlayer access hole 111. Since the wafer access hole 102 is not part of the planar fluidic resistorportion 150, its diameter can be 30 larger than the width of the tortuous path, e.g. approximately20 μm, and without thick dielectric. This is a relatively easy process for a 40-50 μm pitch chip.

Following this step, the complete base layer 100 is formed. Following this, the

rear (lower) side of the semiconductor wafer 101 is supported, and the protection/support removed from the front/upper side. The nanopore support layer 30 is then formed by further laminationand lithography on the front/upper side of the base layer 100 to create the completed planar structure 10, shown in Fig. 6j. Final dicing can then be performed to
5 divide the semiconductorwafer 101 as appropriate.

This invention has the advantage that the base layer 100 can be manufactured using a single conventional semiconductor wafer (such as bulk CMOS). This includes fabrication of the planar fluidic resistor portion 150 with sacrificial polymer channels deposited directly on top of the semiconductor wafer. The method further uses DTI to separate the
10 circuit layer 110 from the wafer access hole 102, and the wafer access holes 102 do not provide significant fluidicresistance, such that the planar fluidic resistor portion 150 can be the main determiner of the fluidic resistance in the second leg 52 of the voltage divider.

The nanopore sensing device 1 shown in Fig. 2 and described above is merely an example, and various alternatives are possible. Some non-limitative examples of such
15 alternatives will now be described.

As in the example shown in Figs. 6a – 6j, the planar fluidic resistor portion 150 is formed in the dielectric layer 120 at the interface with the circuit layer 110, for example as shown in Fig. 6c. Alternatively, the planar fluidic resistor portion 150 may be formed at any other depth in the dielectric layer 120. As a first example of such an alternative, the
20 planar fluidic resistor portion 150 may be formed in the dielectric layer 120 at a position separated from the interface with the circuit layer 110 and separated from the outer surface of the dielectric layer 120 which forms an interface with the nanopore support layer 30. Fig. 2 schematically illustrates this example. As a second example of such an alternative, the planar fluidic resistor portion 150 maybe formed in the dielectric layer 120 at the outer
25 surface of the dielectric layer 120 which forms an interface with the nanopore support layer 30.

In the examples shown in Fig. 2 and Figs. 6a – 6j, the circuit layer 110 is formed on the semiconductor wafer 101 and the dielectric layer 120 is formed on the circuit layer 110, whichprovides the advantages described above. However, as an alternative, the dielectric
30 layer 120 may be disposed between the circuit layer 110 and the semiconductor wafer 101. This alternativemay be manufactured using similar techniques to those described above with respect to Figs. 6a – 6j, except that the dielectric layer 120 is formed on the semiconductor

wafer 101 before the circuit layer 110.

A silicon-on-insulator (SOI) CMOS wafer can be used in this manufacturing method with very minimal modification to the methods described above. By way of example, Fig. 7 shows a base layer 100 manufactured using an SOI semiconductor wafer 101, which
5 includes an insulator layer 160 (often a buried oxide) that can help to reduce parasitic resistance in the semiconductor wafer. The only requirement of the SOI wafer is that the insulator layer 160 should be thick enough to provide a reliable DRIE etch stop. A suitable example is a 1 µm buried oxide (BOX) layer. Such materials are commonly available in semiconductor manufacturing, and so these improvements can be applied
10 directly to existing SOI CMOS wafers using existing equipment already used for prior art devices, so that the new designs caneasily be implemented.

Considerations about the area density of the respective sensors formed by the passages 20 and associated in the nanopore sensor device 30 will now be described.

In some embodiments, the area density of the sensors may be relatively low, for
15 exampleof 100 per mm^2 (corresponding to a square footprint 35 of side 100µm). In such a case, the circuit layer access hole 111 and the wafer access hole 102 may be designed to provide a fluidic resistance that is negligible compared to the fluidic resistance of the planar fluidic resistor portion 150.

However a range of densities are possible. By way of example, in one embodiment,
20 thearea density of the sensors may be 400 per mm^2 (corresponding to a square footprint 35 of side50µm), in which case the length of the planar fluidic resistor portion 150 may be 250µm and the cross-sectional area of the planar fluidic resistor portion 150 may be 0.3μm^2 (e.g. 0.3µm by 1µm). In another embodiment, the area density of the sensors may be 2500 per mm^2 (corresponding to a square footprint 35 of side 20µm), in which case the length of
25 the planar fluidic resistor portion 150 may be 75µm and the cross-sectional area of the planar fluidic resistor portion 150 may be 0.09μm^2 (e.g. 0.3µm by 0.3µm).

As the area density of the sensors increases and the area of the footprint 35 decreases, itmay be become difficult to achieve or provide the fluidic resistance of the planar fluidic resistorportion 150 with sufficient resistance because of spatial constraints, although this
30 depends on other factors such as the resistance of the nanopore 23, in which case the fluidic resistance of the circuit layer access hole 111 and the wafer access hole 102 become significant in the second leg 52 of the voltage divider 50.

With the dimensions of the examples discussed herein, this may start to occur once the area density of the sensors reaches 625 per mm^2 (corresponding to a square footprint 35 of side40μm).

Typically, when the area density of the sensors approaches 10,000 per mm^2 or more (corresponding to a square footprint 35 of side 10μm or less), then at least one of the circuitlayer access hole 111 and the wafer access hole 102 may provide a fluidic resistance in addition to the fluidic resistance of the planar fluidic resistor portion 150. The size of the layer access hole 111 and/or the wafer access hole 102 can be adjusted to provide the required fluidic resistance - if an access hole is shared between two or more sensors then the resistance is configured to be negligible.

It is desirable to increase the area density of fluidic passages 20 on the semiconductor wafer. In general, there are three main limiting factors on how densely the fluidic passages can be packed:

- The configuration of the circuit components associated with each fluidic passage 20 in the circuit layer 110, which must be packaged within the footprint 35.
- The configuration of the planar fluidic resistor portion 150, which must also be packaged within the footprint 35. This problem can be mitigated by reducing the cross-sectional of the planar fluidic resistor portion 150 along its the tortuous path, thereby reducing the required length thereof. It is also possible to use a multi-layer planar fluidic resistor portions 150, as will be discussed further below.
- How densely the wafer access holes 102 can be packed without affecting the mechanical integrity of the semiconductor wafer.

Once the footprint of the circuit components is reduced, the limiting factor on the area density of fluidic passage 20 will shift from the circuit components to the packing of wafer access hole 102. With the dimensions of the examples discussed herein, this will start to occuronce the pitch of the circuit components in the circuit layer 110 reduces significantly below 40 μm. It is also difficult to reduce the diameter of the wafer access holes 102 while still maintaining a reliable manufacturing method with a sufficiently thick wafer (e.g. 300 μm). However, the layout of the circuit components and fluidic passage 20 can be re-designed to bundle multiple fluidic passage 20 to one shared access hole. Either or both of the wafer accesshole 102 and circuit layer access hole 111 may be shared. This design not only allows a further increase in the area density of fluidic passages 20 (e.g.

beyond a 40 μm pitch in the examples herein), but also provides a chance to reduce the wafer access hole 102 aspect ratio requirement.Reducing the aspect ratio is advantageous when the wafer access holes 102 are manufactured using DRIE.

Figs. 8a and 8b show two examples of base layers 100 where each access hole is shared by plural passages by being fluidically connected in common to plural planar fluidic resistor portions 150. Fig. 8a shows an example in which a single wafer access hole 102 is shared between two fluidic passages 20. Fig. 8b shows an example in which two neighbouring fluidicpassages 20 share both a wafer access hole 102, and a circuit layer access hole 111. Although Figs. 8a and 8b show two fluidic passages 20 sharing the circuit layer access hole 111 and/or the wafer access hole 102, in other embodiments more than two fluidic passages 20 may share access hole, for example three or four fluidic passages. This design can also be incorporated into the example of Fig. 7 using an SOI CMOS wafer. When a common wafer access hole 102and/or a common circuit layer access hole 111 are implemented, their resistance can be negligible compared to the total resistance of a passage 20 to inhibit cross talk between nanopores 23 sharing a part of the passage 20 in common. The common part of the passage preferably has negligible resistance.

The cross-section of a common wafer access hole 102 can have a dimension (for example the square root of the area) that is greater than the maximum dimension (for example the square root of the area) of the sensor footprint.

In these examples, the dielectric layer 120 is between the first chamber 3 and the substrate. As an alternative the dielectric layer 120 could be between the semiconductor wafer 101 and the second chamber 4. For example, the dielectric layer 120 could be on the opposite side of the semiconductor wafer 101 from the circuit layer 110. Alternatively, the circuit layer110 could be also formed on opposite side of the semiconductor wafer 101 to the first chamber 3, with the dielectric layer 120 formed thereon. Although this is possible, it is not preferred because it includes the capacitance of the access holes into the voltage divider thus lowered thebandwidth.

The area density of fluidic passages 20 may be further increased by using a multi-layer planar fluidic resistor portion 150. Fig. 9 shows a top-down view of such a multi-layer planar fluidic resistor portion 150. In this example, the planar fluidic resistor portion 150 comprises sections 151, 152 each extending in the planar direction of the planar structure

10 but at differentdepths within the planar structure 10. The dielectric access hole 121 is connected to the first section 152 of the planar fluidic resistor portion 150, on top of the sensor electrode 24. In this example, the first section 152 is on top of the second section 151 (i.e. between the second section and the first chamber 3). However this is not essential, and the first section 152 could instead be below the second section 151 (i.e. between the second section 151 and the semiconductor wafer 101). The second section 151 is connected to the circuit layer access hole 111 and therebyto the wafer access hole 102. The first and second sections 152, 151 are connected together with a via 153. Vias 154 are provided adjacent parts of the passage 20 and are used for the plasma ashing process that is used to etch away the sacrificial polymer during manufacture. These vias 154 are optional, they are used to reduce the aspect ratio the ashing process has to reach inside the fluidic channel. These vias 154 are filled by the thick passivation layer followingremoval of the sacrificial polymer.

Figs. 10a – 10m shows a series of views of layers being processed during a method of manufacture to form a multi-layer planar fluidic resistor portion 150, which is performed as follows. Figs. 10a – 10d show the same steps as performed in Figs. 6a – 6d. Following these steps, sacrificial polymer has been deposited in the shape of the second section 151 of the planarfluidic resistor portion 150, and a thin passivation layer deposited on top.

In Fig. 10e, the via 153 is formed in the thin passivation layer, along with a further partof the dielectric access hole 121. In Fig. 10f, further sacrificial polymer is deposited in the form of the first section 152 of the planar fluidic resistor portion 150 and the dielectric access hole 121.

In Fig. 10h, a further thin passivation layer is deposited, and in Fig. 10i, vias are formedthrough the further thin passivation layer and through both passivation layers to expose the sacrificial polymer in both the first and second section 152, 151 of the planar fluidic resistor portion 150, and the dielectric access hole 121. The vias expose the sides of the sacrificial polymer for the etching or plasma ashing process to remove the sacrificial polymer. Fig. 10j shows the state following the etching or plasma ashing of the sacrificial polymer.

The steps shown in Figs. 10k to 10m are the same as those shown in Figs. 6h to 6j, namely depositing the thick passivation layer, opening the thick passivation layer above the sensor electrode 24, and forming the wafer access hole 102.

In the examples above, the substrate which supports the dielectric layer 120 in which theplanar fluidic resistor portion 150 is formed is the semiconductor wafer 101, and the planar structure 10 is formed by depositing layers directly onto the semiconductor wafer 101. However, in some embodiments, the substrate which supports a dielectric layer in
5 which the planar fluidic resistor portion 150 is formed may be a different component from the semiconductor wafer 101 on which the circuit layer 110 is formed. In this case, the substrate which supports the planar fluidic resistor portion 150 and the semiconductor wafer 101 may bemanufactured separately and then bonded together.

An example of a method of making a base layer 100 of a planar structure 10 of this
10 typeis shown in Figs. 11a – 11e and performed as follows. In this example, the substrate on which the planar fluidic resistor portion 150 is formed is a MEMS (micro-electromechanical system) wafer 170. The MEMS wafer 170 and has the advantage of being able to withstand a high temperature thermal oxide process used for forming the planar fluidic resistor portion 150 and allows conventional MEMS processes to be used.
15 The MEMS wafer 170 may be made of any suitable material, for example quartz, silicon oxide, glass, aluminium oxide or sapphire. In10 principle, the MEMS wafer 170 could be replaced by a substrate made from any other material suitable for supporting the dielectric layer 172 described below, for example being a semiconductor wafer.

As shown in Fig. 11a, the MEMS wafer 170 is provided and a MEMS wafer access
20 hole171 is formed extending therethrough by DRIE.

Fig. 11b shows the formation of a dielectric layer 172 on the surface of the MEMS wafer170 by thermal oxidation. Typically, the dielectric layer 172 may have thickness of order 2μm or more. Thus, in this example, the dielectric layer 172 is an oxide of the material of the MEMSwafer 170.

25 Fig. 11c shows the formation of the planar fluidic resistor portion 150 in the dielectric layer 172 by etching using a lithographic process. The planar fluidic resistor portion 150 may have a form as described above.

In Fig. 11d, the base layer 100 is formed by bonding the MEMS wafer 170 shown in Fig. 11c to a semiconductor wafer 101 supporting a circuit layer 110. The semiconductor
30 wafer101 has the same construction as described above except that the dielectric layer 120 is not provided and the semiconductor wafer 101 is upside down in Fig. 11d compared to the previousfigures. As described above, the circuit layer 110 comprises circuit

components connected to the sensor electrode 24. The semiconductor wafer 101 and the circuit layer 110 are provided with access holes 102, 111 which extend therethrough and form part of the passages 20. In thisexample, the semiconductor wafer 101 is an SOI CMOS wafer including an insulator layer 170, similar to that shown in Fig. 7, and the handle layer
5 is removed after bonding.

Similarly, the semiconductor wafer 101 and circuit layer 101 may be manufactured using the same processes as described above.

The MEMS wafer 170 shown in Fig. 11c is bonded to the semiconductor wafer 101 by bonding the outer surface of the dielectric layer 172 in which the planar fluidic resistor
10 portion150 is formed to the outer surface of the circuit layer 110. As a result, the MEMS wafer 170, which forms the substrate in this example, is bonded to the semiconductor wafer 101 between the semiconductor wafer 101 and the second chamber 4.

As in the above examples, the nanopore support layer 30 is fixed to the base layer 100 shown in Fig. 11d, for example by forming the nanopore support layer 30 separately
15 and bonding it to the base layer 100, or forming the nanopore support layer 30 directly on the base layer 100.

This bonded two wafer route for fabrication, with separate wafers used to form the planarfluidic resistor portion 150 and the circuit components has the advantage that the processing forforming each structure can be optimised more easily when performed
20 separately. For example,the semiconductor wafer 101 can be thinned down prior to forming the wafer access holes 102 more easily without the layers forming the planar fluidic resistor portion 150 thereon. This mayadvantageous in some situations. However, the two-wafer process adds considerable complexity, since two entirely separate fabrication processes must be carried out, and an additional joining step performed. The processes used
25 to process the SOI CMOS also creates limitations on circuit design and foundry choices. This is likely to increase the cost of manufacture compared to forming all of the planar structure 10 in a single, albeit longer, process.Therefore, the single wafer method is likely to be preferred in many situations.

Although various methods for manufacturing the planar structure have been
30 discussed above, the planar structure is not limited to these methods, and may be formed by any other suitable method.

In the examples above, the planar fluidic resistor portion 150 is formed in a dielectric

layer, for example the dielectric layer 120 supported by the semiconductor wafer 101 in Fig. 2 or the dielectric layer 172 supported by the MEMS wafer 170 in Figs. 11a – 11d. As an alternative, the planar fluidic resistor portion 150 may be formed in the nanopore support layer 30. This provides the advantage that the planar fluidic resistor portion 150 may be manufactured using the same processes used to manufacture the structure of nanopore support layer 30. In thefollowing method, the planar fluidic resistor portion 150 follows a tortuous path that may be the same as that shown in Fig. 5, albeit that it is formed in the nanopore support layer 30.

An example of a method of making a planar structure 10 of this type is shown in Figs. 12a – 12f and performed as follows.

Fig. 12a and 12b are in general terms the same as the steps described above with respect to Figs. 6a and 6b.

After these steps, the semiconductor wafer 101 (which forms the substrate of the planarstructure 10) and circuit layer 110 are present, with the sensor electrode 24 deposited. A passivation layer has been deposited, and the circuit layer access hole 111 opened through the passivation layer and circuit layer 110. Fig. 12c shows the formation of the wafer access hole 102 prior to formation of the planar fluidic resistor portion 150. This is in contrast to the methodof Fig. 6, where the wafer access hole 102 is only formed in the penultimate step after the formation of the planar fluidic resistor portion 150. Alternatively, the wafer access hole 102 can be formed after the nanopore support layer 30 has been formed.

Fig. 12d shows a sacrificial polymer layer 180 deposited in the shape of the planar fluidic resistor portion 150 on top of the dielectric layer 110. This is similar to the step shown in Fig. 6c. The sacrificial polymer layer 180 may comprise photoresist, which can be deposited by spincoating and/or lamination, and subsequently patterned into the shape of the planar fluidic resistor portion 150. The patterning of the photoresist may, for example, comprise exposure using a mask and subsequent development.

As shown in Fig. 12e, a photoresist layer 181 is then deposited onto the base layer 100,covering the sacrificial polymer layer 180. The photoresist layer 181 is used to form the nanopore support structure 30. The photoresist layer 181 is exposed to light and developed so as to form the wall layer 32 comprising walls 33 that define the wells 31.

As shown in Fig. 12f, the photoresist layer 181 is then developed, and the

sacrificial polymer layer 180 is also removed to form the planar fluidic resistor portion 150.

Following these steps, and similarly to the embodiments described above, the planar structure comprises the substrate, which in this example comprises a semiconductor wafer 101,the circuit layer 110 supported by the semiconductor wafer 101, the circuit layer comprising circuit components connected to the sensor electrode, and the nanopore support layer 30 that is 30 configured to support the nanopores 23 in the membranes 22 extending across the passages 20. However, in contrast to the embodiments above, the planar fluidic resistor portions 150 are formed in the nanopore support layer 30.

As shown in Fig. 12f, the nanopore support layer 30 is provided with wells 31. When the planar structure 10 is integrated into the nanopore sensing device 1, the wells 31 open into the first chamber 3. The wells 31 form part of the passages 20 and are configured to support the nanopores 23 in the membranes 22 extending across the wells 31.

In the nanopore sensing device 1, the first and second chambers 3, 4 are on opposite sides of the planar structure 10. The passages 20 extend through the planar structure 10 and thesubstrate (in this case the semiconductor wafer 101) is provided with access holes 102 which extend therethrough and form part of the passages 20.

As illustrated in Fig. 8, in some embodiments, each access hole 102 is shared by plural passages 20 by being fluidically connected in common to plural planar fluidic resistor portions150. In the case of the planar structure of Fig. 12, where the planar fluidic resistor portions 150are formed in the nanopore support layer 30, the plural passages 20 may be connected to one another within the nanopore support layer 30, or alternatively may be connected by sharing only of the wafer access hole 102 and/or the circuit layer access hole 111 in the base layer 100.

Table 1 sets out some non-limitative examples of area densities of the sensors in the nanopore sensing device 1 which may be applied to any of the configurations described above.Table 1 also sets out the corresponding sizes and areas of the footprints 35 in the case that the footprints 35 are square, although the footprints 35 could have any other shape.

Table 1:

Area density (no. per mm^2)	Size of footprint 35 (μm)	Area of footprint 35 (μm^2)

100	100	10000
400	50	2500
625	40	1600
2500	20	400
10000	10	100
40000	5	25
62500	4	16
250000	2	4
1000000	1	1

Table 2 sets out some non-limitative examples of distribution of fluidic resistance between the nanopore 23 and different parts of the passage 20 for different area densities of sensor that may be applied to the nanopore sensing device 1 in the configurations described above.

In Table 2:

- the column labelled "23" indicates the % of the fluidic resistance provided by the nanopore 23;
- the column labelled "30" indicates the % of the fluidic resistance provided by a planar fluidic resistor portion 150 formed in the nanopore support layer 30, for example as shown in Fig. 12;
- the column labelled "120-above" indicates the % of the fluidic resistance provided by aplanar fluidic resistor portion 150 formed in a dielectric layer 120 disposed above the circuit layer 110, for example as shown in Fig. 2;
- the column labelled "120-below" indicates the % of the fluidic resistance provided by a planar fluidic resistor portion 150 formed in a dielectric layer 120 disposed between thecircuit layer 110 and the semiconductor wafer 101, in accordance with the alternative described above;
- the column labelled "111" indicates the % of the fluidic resistance provided by the dielectric access hole 111;
- the column labelled "102" indicates the % of the fluidic resistance provided by the waferaccess hole 102 (and/or the circuit layer access hole 111) in the case that each passage 20 has a respective wafer access hole 102, for example as shown in Fig. 2; and

- the column labelled "102-common" indicates the % of the fluidic resistance provided by the wafer access hole 102 (and/or the circuit layer access hole 111) in the case that plural passages 20 share a wafer access hole 102 (and/or the circuit layer access hole 111), forexample as shown in Fig. 8a and 8b. NB: when a common wafer access hole 102
5 and/ora common circuit layer access hole 111 are implemented, their resistance can be negligible compared to the total resistance to inhibit cross talk between nanopores 23 sharing a part of the passage 20 in common. Common parts of the passages 20 preferably have negligible resistance.

Table 2:
10

Area density (no. per mm^2)	23	30	120-above	120-below	111	102	102-common
100	50%	50%					
100	50%		50%				
100	50%			50%			
100	50%				50%		
100	50%					50%	
100	90%				10%		
100	90%			10%			
100	90%		10%				
100	90%	10%					
10000	50%	25%	25%				0%
10000	50%	25%		25%			0%
10000	50%			25%		25%	
10000	50%	25%				25%	
10000	90%	5%	5%				0%
10000	90%	5%		5%			0%
10000	90%			5%		5%	
10000	90%	5%				5%	
25000	50%	20%	20%		10%		0%
25000	90%	4%	3%		3%		0%

25000	90%	4%		4%	2%		0%
25000	80%	20%		5%	5%		0%
25000	70%	30%		10%	10%		0%

Some general points are as follows.

The ratio of the percentage “%” in the column labelled “23”, which indicate the % of the fluidic resistance provided by the nanopore 23, to the total resistance in all other columns canbe 1:1. This ratio can range from 1:1 up to around 99:1. The upper range of the ratio can be for example 3:2, 7:3, 4:1 or 19:1. An exemplary ratio is 9:1. In other words, the nanopore resistance can be ~50% when the ratio is 1:1 and can be >50% as the resistance of the nanoporedominates the total resistance in the passage. The nanopore resistance can be >60%, >70% … >90%... etc.

The present inventors have found that whilst a nanopore resistance of around 1:1 provides an optimal signal : noise ratio, it results in an increased voltage drop across the nanopore leading to increased ion depletion during translocation and measurement of a speciessuch as DNA through a nanopore. This results in a change in the fluidic and nanopore resistance,eventually leading to a reduction of the voltage signal. Thus a nanopore resistance of greater than 50% of the total resistance is preferred. A nanopore resistance of ~90% will cause ~20mVvoltage drop, which is considered an acceptable upper bound for the voltage drop while allowingthe generation of enough voltage signal on the sensing electrode.

As the density area density of the array increased beyond a certain number of sensors per mm^2, such as densities above 10000 per mm^2 and at densities of 25000 per mm^2 and above the resistance of the fluidic passage is distributed between planar fluidic resistance portions andaccess hole portions, along its length. It is to be noted that at high densities the wafer access hole can be common to two or more sensors, and when this occurs the resistance of a common access hole is preferably negligible to inhibit detectable cross talk between nanopore sensors that share the same wafer access hole.

The nanopore sensing device 1 shown in Figs. 1 and 2 is filled with fluid and the membranes 22 are shown extending across the respective passages 20 and the nanopores 23 inserted in the membranes 22, but some types of nanopore sensing device 1 may be

provided without the membranes 22 and nanopores 23. In that case, the end user of the nanopore sensingdevice 1 carries out the steps to form the membranes 22 and cause the nanopores 23 to insert therein.

WO 2020/183172 discloses various nanopore sensing devices, and the structures and methods disclosed in WO 2020/183172 may be also applied to the present disclosure. WO 2020/183172 is incorporated herein by reference in its entirety.

Examples of the membranes 22 and the nanopores 23 are as follows.

In one type of nanopore sensing device 1, the nanopores 23 are biological nanopores andthe membranes 22 are capable of having the biological nanopores 23 inserted therein. In anothertype of nanopore sensing device 1, the membranes 22 are solid state layers and the nanopores 23 are formed therein either as apertures or as biological nanopores.

The membrane 22 may be an amphiphilic layer, that is a layer formed from amphiphilic molecules, such as phospholipids, which have both hydrophilic and lipophilic properties. The amphiphilic molecules may be synthetic or naturally occurring. Non-naturally occurringamphiphiles and amphiphiles which form a monolayer are known in the art and include, for example, block copolymers (Gonzalez-Perez et al., Langmuir, 2009, 25, 10447-10450). The membrane 22 may be a triblock or diblock copolymer membrane.

Membranes 22 formed from block copolymers hold several advantages over biologicallipid membranes. Because the triblock copolymer is synthesized, the exact construction can becarefully controlled to provide the correct chain lengths and properties required to formmembranes and to interact with pores and other proteins.

The membrane 22 can be one of the membranes disclosed in WO2014/064443 or WO2014/064444, hereby incorporated by reference in their entirety. These documents also disclose suitable polymers.

The amphiphilic molecules may be chemically modified or functionalized to facilitate coupling of the polynucleotide.

The amphiphilic layer may be a monolayer or a bilayer.

The membrane 22 may be a lipid bilayer. Suitable lipid bilayers are disclosed in WO2008/102121, WO2009/077734 and WO2006/100484, hereby incorporated by reference intheir entirety. Methods for forming lipid bilayers are known in the art. Lipid bilayers are commonly formed by the method of Montal and Mueller (Proc. Natl. Acad. Sci. USA., 1972; 69: 3561-3566).

The membrane 22 may be a solid-state layer. Suitable state layers can be formed from both organic and inorganic materials including, but not limited to, microelectronic materials, insulating materials such as Si_3N_4, $A1_2O_3$, and SiO, organic and inorganic polymers such as polyamide, plastics such as Teflon® or elastomers such as two-component addition-cure silicone rubber, and glasses. The solid-state layer may be formed from graphene. Suitable graphene layers are disclosed in WO2009/035647, hereby incorporated by reference in its entirety. Yusko et al., Nature Nanotechnology, 2011; 6: 253-260 and US Patent Application No.2013/0048499 , hereby incorporated by reference in their entirety, describe the delivery of proteins to transmembrane pores in solid state layers without the use of microparticles.

The nanopore 23 may be any transmembrane pore. The nanopore 23 may be biologicalor artificial. Suitable nanopores 23 include, but are not limited to, protein pores, polynucleotide pores and solid-state pores. The nanopore 23 may be a DNA origami pore (Langecker *et al.*, Science, 2012; 338: 932-936).

The transmembrane protein pore may comprise a barrel or channel through which the ions may flow. The barrel or channel of the transmembrane protein pore typically comprises amino acids that facilitate interaction with nucleotides, polynucleotides or nucleic acids.

Transmembrane protein pores for use in accordance with the invention can be derived from β-barrel pores or α-helix bundle pores. The transmembrane pore may be derived from orbased on, for example, Msp, α-hemolysin (α-HL), lysenin, CsgG, ClyA, Sp1 and hemolytic protein fragaceatoxin C (FraC). The transmembrane protein pore can be derived from CsgG.Suitable pores derived from CsgG are disclosed in WO 2016/034591. The transmembrane poremay be derived from lysenin. Suitable pores derived from lysenin are disclosed in WO 2013/153359.

The analytes (including, *e.g.*, proteins, peptides, small molecules, polypeptide, polynucleotides) may be present in an analyte. The analyte may be any suitable sample. The analyte may be a biological sample. Any embodiment of the methods described herein may be carried out *in vitro* on an analyte obtained from or extracted from any organism or microorganism. The organism or microorganism is typically archaean, prokaryotic or eukaryotic and typically belongs to one of the five kingdoms: plantae, animalia, fungi, monera and protista. In some embodiments, the methods of various

aspects described herein may be carried out *in vitro* on an analyte obtained from or extracted from any virus.

The analyte can be a fluid sample. The analyte can comprise a body fluid. The body fluid may be obtained from a human or animal. The human or animal may have, be suspected of having or be at risk of a disease. The analyte may be urine, lymph, saliva, mucus, seminal fluid or amniotic fluid, but can be whole blood, plasma or serum. Typically, the analyte is human in origin, but alternatively it may be from another mammal such as from commercially farmed animals such as horses, cattle, sheep or pigs or may alternatively be pets such as cats ordogs. Alternatively, an analyte can be of plant origin.

The analyte may be a non-biological sample. The non-biological sample can be a fluidsample. An ionic salt such as potassium chloride may be added to the sample to effect ion flow through the nanopore.

The polynucleotide may be single stranded or double stranded. At least a portion of thepolynucleotide may be double stranded.

The polynucleotide can be a nucleic acid, such as deoxyribonucleic acid (DNA) or ribonucleic acid (RNA). The polynucleotide can comprise one strand of RNA hybridised to one strand of DNA. The polynucleotide may be any synthetic nucleic acid known in the art.The polynucleotide can be naturally occurring or artificial.

The method may involve measuring two, three, four or five or more characteristics of apolynucleotide. The one or more characteristics can be selected from (i) the length of the polynucleotide, (ii) the identity of the polynucleotide, (iii) the sequence of the polynucleotide, (iv) the secondary structure of the polynucleotide and (v) whether or not the polynucleotide is modified.

For (iii), the sequence of the polynucleotide can be determined as described previously.Suitable sequencing methods, particularly those using electrical measurements, are described inStoddart D et al., Proc Natl Acad Sci, 12;106(19):7702-7, Lieberman KR et al, J Am Chem Soc. 15 2010;132(50):17961-72, and International Application WO 2000/28312.

The secondary structure may be measured in a variety of ways. For instance, if the method involves an electrical measurement, the secondary structure may be measured using a change in dwell time or a change in ion current flowing through the pore. This

allows regions of single-stranded and double-stranded polynucleotide to be distinguished.

The presence or absence of any modification may be measured. The method can comprises determining whether or not the polynucleotide is modified by methylation, by oxidation, by damage, with one or more proteins or with one or more labels, tags or spacers. Specific modifications will result in specific interactions with the pore which can be measured using the methods described below.

In some embodiments of various aspects described herein, the method may involve further characterizing the target polynucleotide. As the target polynucleotide is contacted withthe pore, one or more measurements which are indicative of one or more characteristics of the target polynucleotide are taken as the polynucleotide moves with respect to the pore.

The method may involve determining whether or not the polynucleotide is modified. The presence or absence of any modification may be measured. The method can comprisesdetermining whether or not the polynucleotide is modified by methylation, by oxidation, by damage, with one or more proteins or with one or more labels, tags or spacers.

Also provided is an apparatus for characterising a target analyte, such as a target polynucleotide. The apparatus comprises a plurality of the pores as disclosed herein and a plurality of membranes. The plurality of pores can be present in the plurality of membranes. The number of pores and membranes can be equal. A single pore can be present in each membrane.

The apparatus for characterising target analytes, may comprise or an array of pores as disclosed herein, in a plurality of membranes.

The apparatus can further comprise instructions for carrying out the method. The apparatus may be any conventional apparatus for analyte analysis, such as an array or a chip. Any of the embodiments discussed above with reference to the methods are equally applicableto the apparatus of the invention.

The apparatus can be set up to carry out a method as disclosed herein.

The apparatus can comprise: a nanopore sensor device 1 that is capable of supporting the plurality of pores and membranes and being operable to perform analyte characterisation using the pores and membranes; and at least one port for delivery of the material for performingthe characterisation.

Alternatively, the apparatus can comprise: a nanopore sensor device 1 that is capable ofsupporting the plurality of pores and membranes being operable to perform analyte characterisation using the pores and membranes; and at least one reservoir for holding material for performing the characterisation.

5 The apparatus can comprise: a sensor device that is capable of supporting the membraneand plurality of pores and membranes and being operable to perform analyte characterising using the pores and membranes; at least one reservoir for holding material for performing the characterising; a fluidics system configured to controllably supply material from the at least onereservoir to the sensor device; and one or more containers for 10 receiving respective samples, thefluidics system being configured to supply the analytes selectively from one or more containersto the sensor device.

The apparatus may be any of those described in WO 2009/077734, WO 2010/122293, WO 2011/067559 or WO 00/28312, modified to include the nanopore sensing device 1disclosed herein.

15 Control of the movement of an analyte with respect to the nanopore e.g. speed of translocation, rejection of the analyte etc, can be managed by the systems and methods disclosedin WO2016/059427. Rejection of an analyte by the nanopore sensor can comprise ejection of the analyte from the nanopore.

The features in description above and drawings are interchangeable and compatible in 20 light of the teaching herein. The present invention has been described above purely by way of example, and modifications can be made within the spirit and scope of the invention, which extends to equivalents of the features described and combinations of one or more features described herein. The invention also consists in any individual features described or implicit herein.

Claims

1. A nanopore sensing device comprising:

first and second chambers;

5 a planar structure provided with plural fluidic passages extending between the first and second chambers, the planar structure being configured to support nanopores in membranes across respective passages; and

sensor electrodes arranged to sense a fluidic electrical potential in respective passages between the nanopores and the second chamber,

10 wherein the passages comprise planar fluidic resistor portions between the sensor electrode and the second chamber, the planar fluidic resistor portions extending in a planar direction of the planar structure and being configured to form a fluidic resistor.

2. A nanopore sensing device according to claim 1, wherein the planar structure comprises:

15 a nanopore support layer that is configured to support the nanopores in the membranesextending across the passages; and

a further layer, the planar fluidic resistor portions being formed in the further layer.

3. A nanopore sensing device according to claim 2, wherein the nanopore support 20 layer is provided with wells opening into the first chamber, the wells forming part of the passages andbeing configured to support said nanopores in said membranes extending across the wells.

4. A nanopore sensing device according to claim 2 or 3, wherein the further layer 25 is adielectric layer.

5. A nanopore sensing device according to any one of claims 2 to 4, wherein the planarstructure further comprises a substrate, the further layer being supported by the substrate.

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6. A nanopore sensing device according to claim 5, wherein the first and second chambers are on opposite sides of the planar structure, the passages extend through the

planar structureand the substrate is provided with access holes which extend therethrough and form part of the passages.

7. A nanopore sensing device according to claim 1, wherein

5 the first and second chambers are on opposite sides of the planar structure, the passages extending through the planar structure, and

the planar structure comprises:

a substrate; and

a further layer, the further layer being supported by the substrate,

10 wherein the planar fluidic resistor portions are formed in the further layer, and the substrate is provided with access holes extending therethrough, the access holes forming part of the passages.

8. A nanopore sensing device according to claim 7, wherein the planar structure

15 furthercomprises a nanopore support layer that is configured to support the nanopores in the membranes extending across the passages.

9. A nanopore sensing device according to claim 8, wherein the nanopore support layer isprovided with wells opening into the first chamber, the wells forming part of the

20 passages and being configured to support the nanopores in the membranes extending across the wells.

10. A nanopore sensing device according to any one of claims 7 to 9, wherein the furtherlayer is a dielectric layer.

25

11. A nanopore sensing device according to any one of claims 6 to 10, wherein the further layer is between the first chamber and the substrate.

12. A nanopore sensing device according to any one of claims 6 to 11, wherein each

30 accesshole is shared by plural passages by being fluidically connected in common to plural planar fluidic resistor portions.

13. A nanopore sensing device according to any one of claims 5 to 12, wherein the substrate is a semiconductor wafer.

14. A nanopore sensing device according to claim 13, wherein the planar structure furthercomprises a circuit layer supported by the semiconductor wafer, the circuit layer comprising circuit components connected to the sensor electrode.

15. A nanopore sensing device according to claim 14, wherein the circuit layer is formed onthe semiconductor wafer and the dielectric layer is formed on the circuit layer.

16. A nanopore sensing device according to any one of claims 6 to 12, wherein

the planar structure further comprises a semiconductor wafer having a circuit layer supported thereby, the circuit layer comprising circuit components connected to the sensor electrode, the semiconductor wafer and the circuit layer is provided with access holes which extend therethrough and form part of the passages, and

the substrate is bonded to the semiconductor wafer between the semiconductor wafer and the second chamber.

17. A nanopore sensing device according to claim 1, wherein the planar structure comprises:

a substrate;

a circuit layer supported by the substrate, the circuit layer comprising circuit componentsconnected to the sensor electrode; and

a nanopore support layer that is configured to support the nanopores in the membranes extending across the passages, the planar fluidic resistor portions being formed in the nanoporesupport layer.

18. A nanopore sensing device according to claim 17, wherein the nanopore support layer isprovided with wells opening into the first chamber, the wells forming part of the passages and being configured to support said nanopores in said membranes extending across the wells.

19. A nanopore sensing device according to claim 17 or 18, wherein the first and second chambers are on opposite sides of the planar structure, the passages extend through the planar structure and the substrate is provided with access holes which extend therethrough and formpart of the passages.

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20. A nanopore sensing device according to claim 19, wherein each access hole is shared by plural passages by being fluidically connected in common to plural planar fluidic resistorportions.

10 21. A nanopore sensing device according to any one of claims 17 to 20, wherein the substrateis a semiconductor wafer.

22. A nanopore sensing device according to any one of the preceding claims, wherein theplanar fluidic resistor portion extends along a tortuous path.

15

23. A nanopore sensing device according to any one of the preceding claims, wherein the nanopores are biological nanopores and the membranes are capable of having the biologicalnanopores inserted therein.

20 24. A nanopore sensing device according to claim 23, wherein the planar structure furthercomprises the membranes extending across the respective passages and optionally also the biological nanopores inserted in the membranes.

25. A nanopore sensing device according to any one of claims 1 to 22,
25 wherein themembranes are solid state membranes, the planar structure further comprises the solid-state membranes and the nanopores are formed therein.

26. A nanopore sensing device according to any one of the preceding claims, wherein the planar fluidic resistor portion comprises sections each extending in the planar
30 direction of the planar structure but at different depths within the planar structure.

27. A nanopore sensing device according to any one of the preceding claims,

wherein the passages comprise wells opening into the first chamber, the planar structure being configured to support the nanopores in membranes extending across the wells.

28. A nanopore sensing device according to any one of the preceding claims,
5 wherein thefirst and second chambers are on opposite sides of the planar structure and the passages extend through the planar structure.

29. A nanopore sensing device according to any one of the preceding claims, furthercomprising drive electrodes in the first and second chambers.
10

30. A nanopore sensing device according to any one of the preceding claims, wherein theresistance of the nanopore is greater than 50% of the total resistance of the passage.

15 31. A nanopore sensing device according to claim 30, wherein the resistance of thenanopore is 90% of the total resistance of the passage.

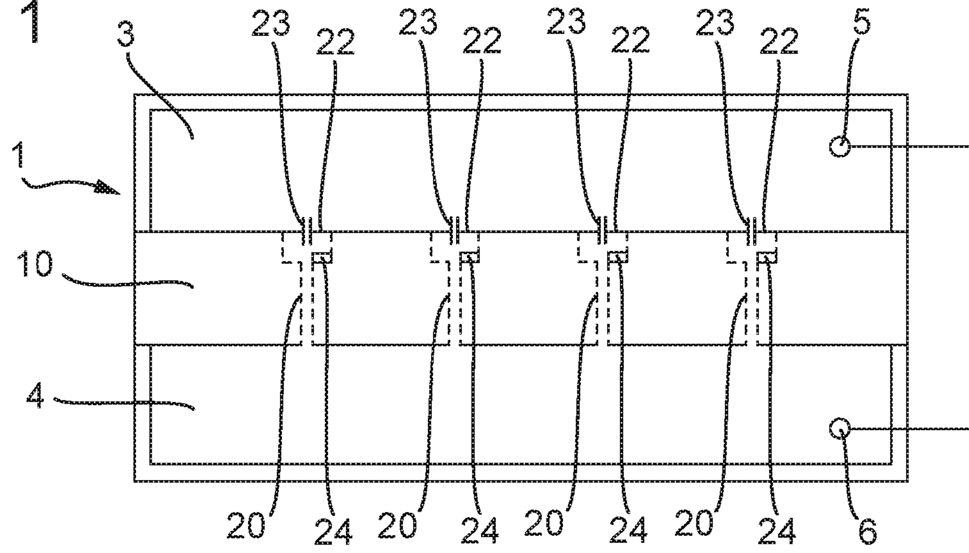
Fig. 1
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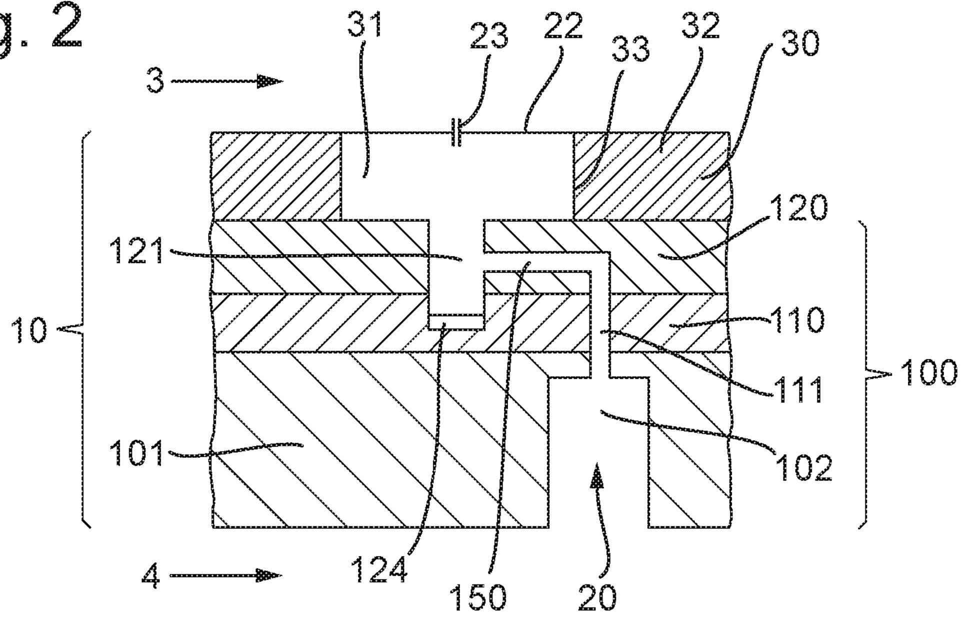
Fig. 2
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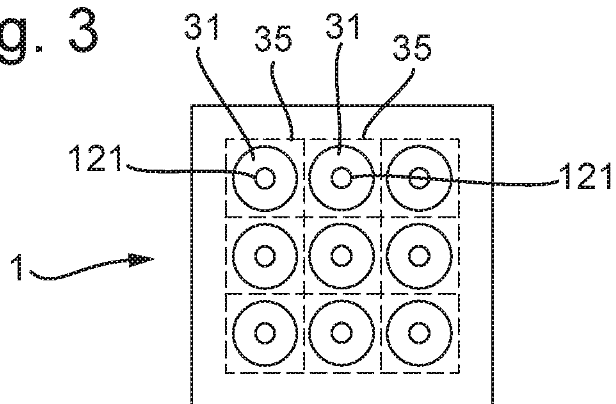
Fig. 3
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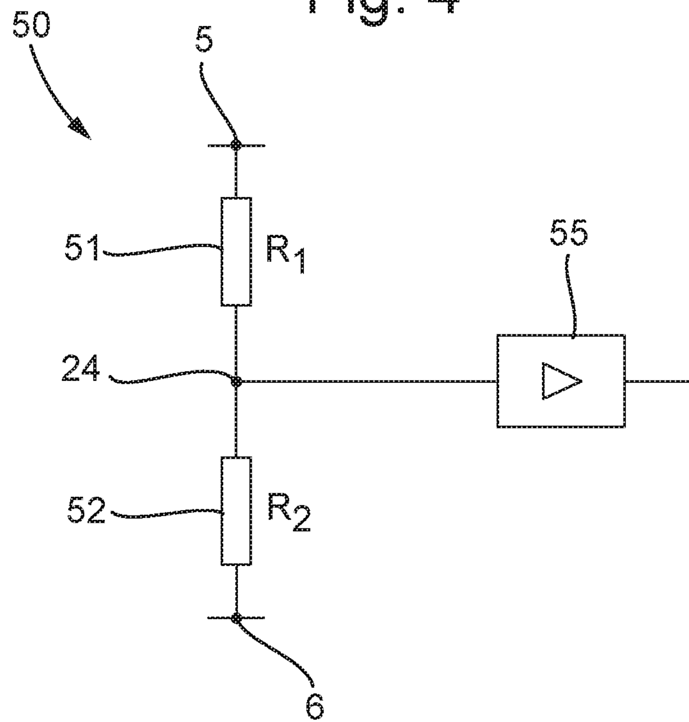

Fig. 4
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R1
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R2
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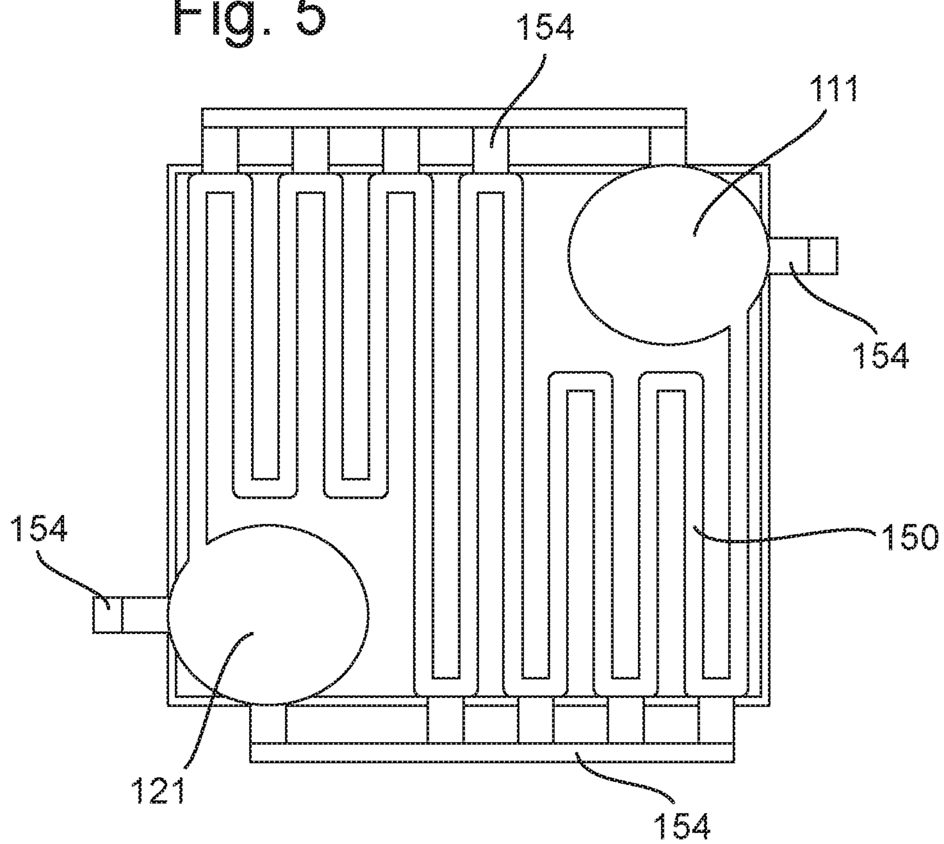

Fig. 5
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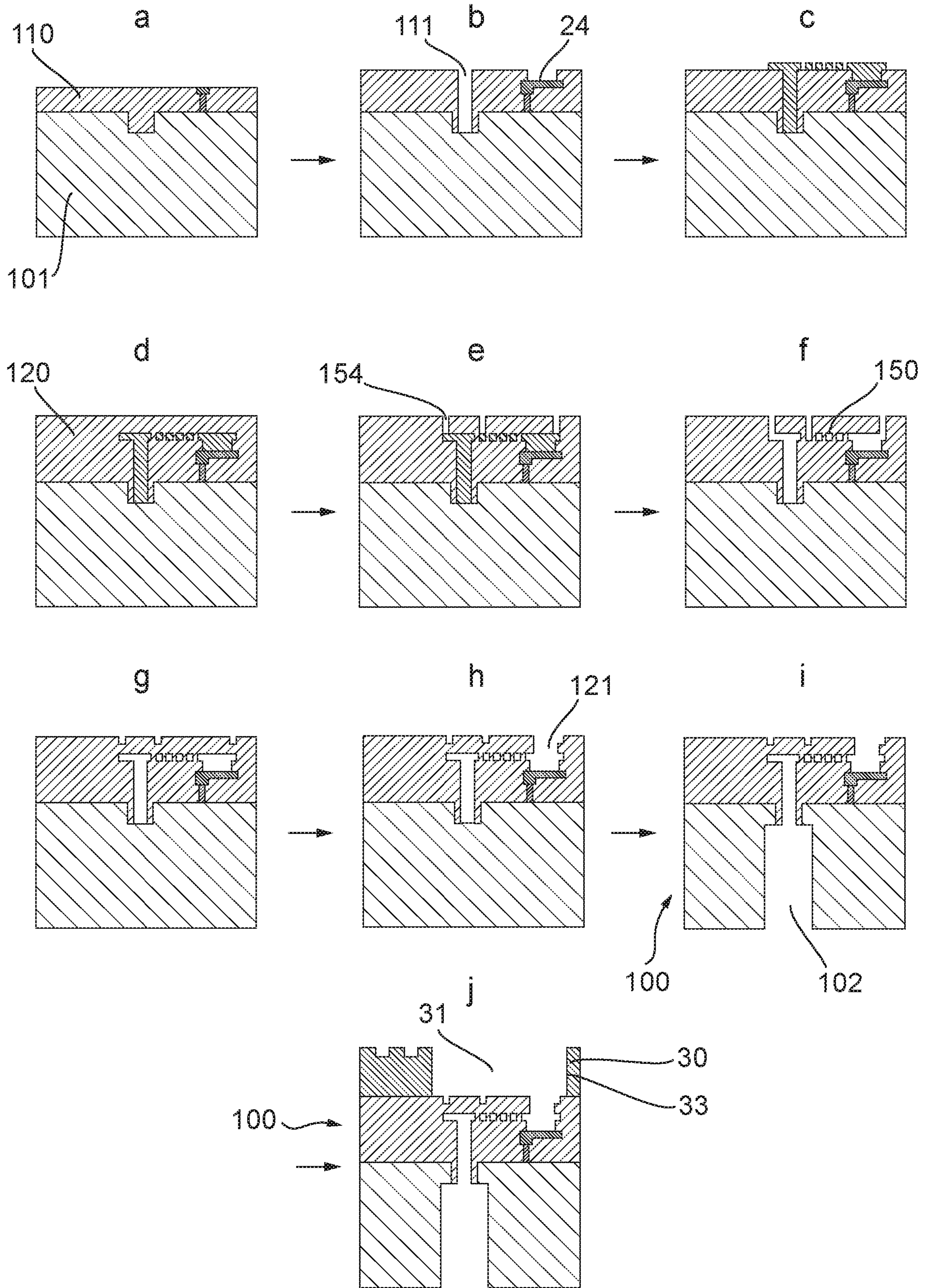
Fig. 6
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Fig. 7

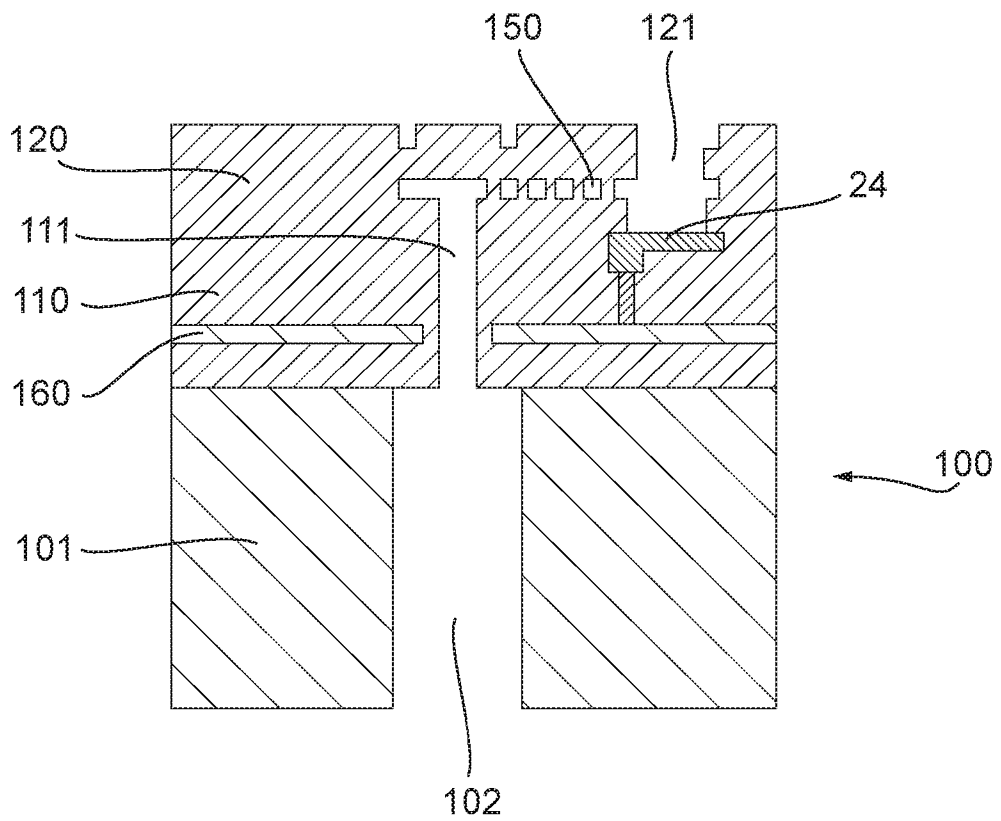
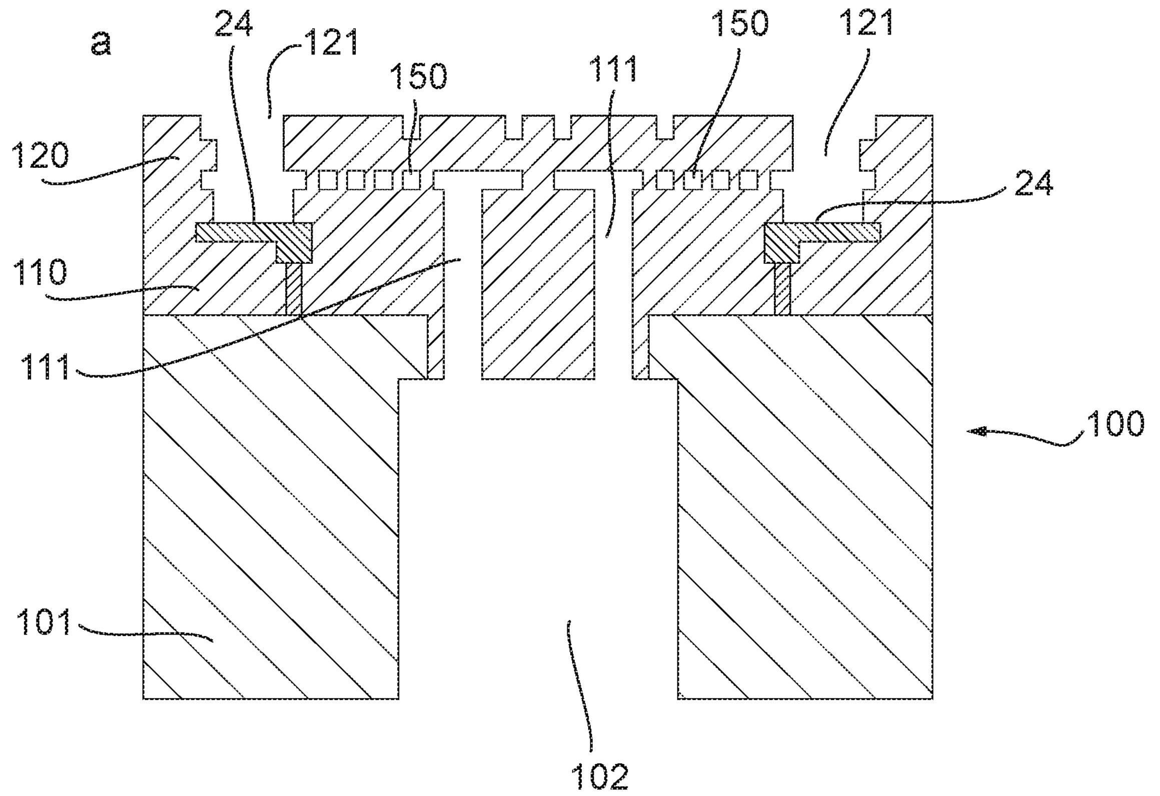


Fig. 8



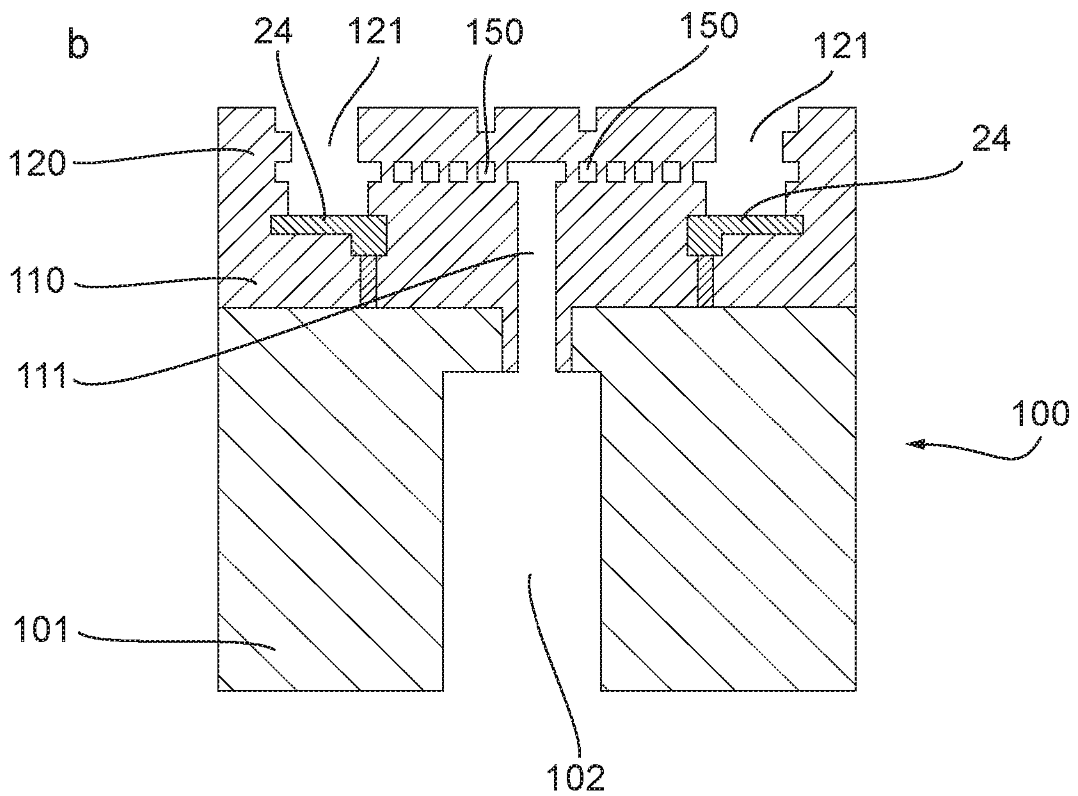
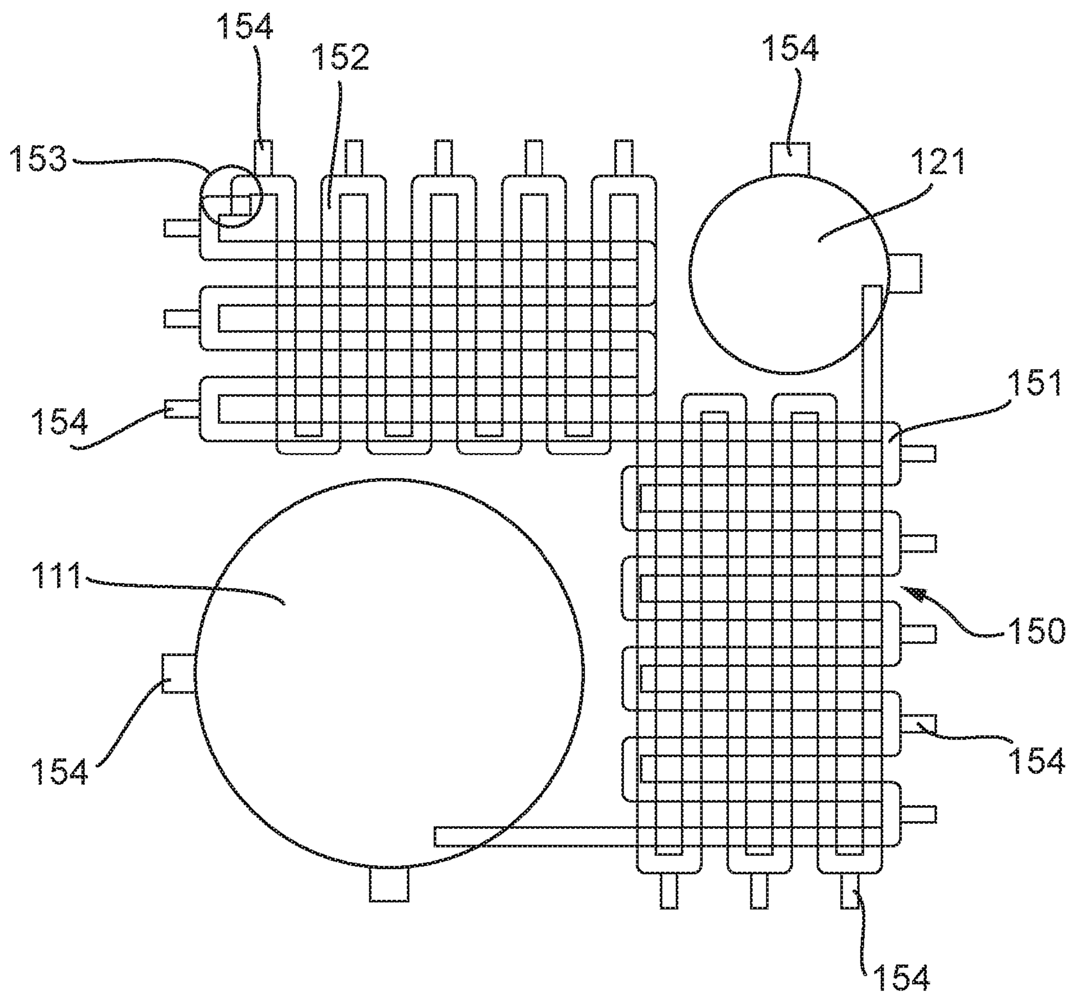


Fig. 9



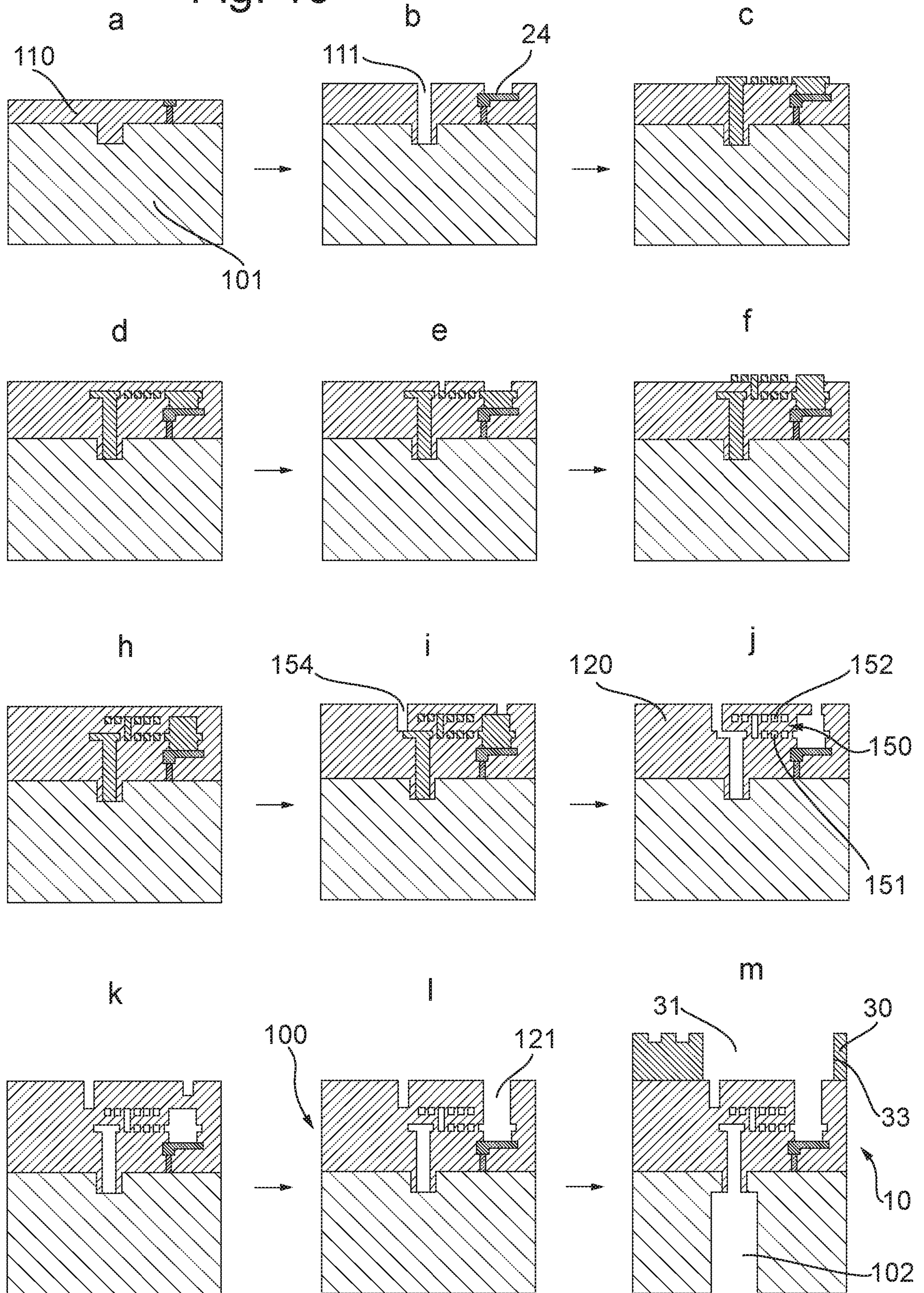


Fig. 10
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k
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m
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102

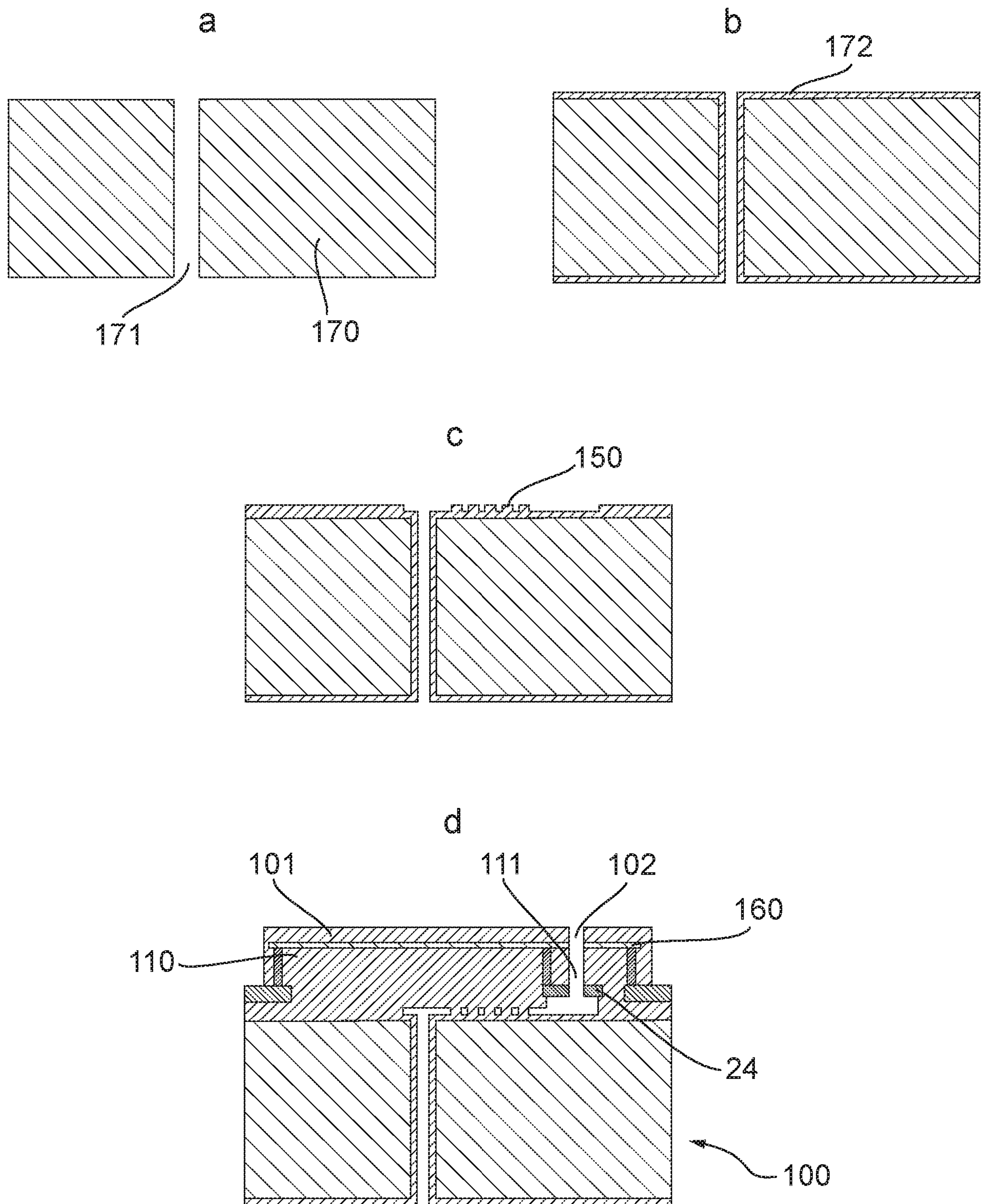
Fig. 11
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171
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c
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111
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160
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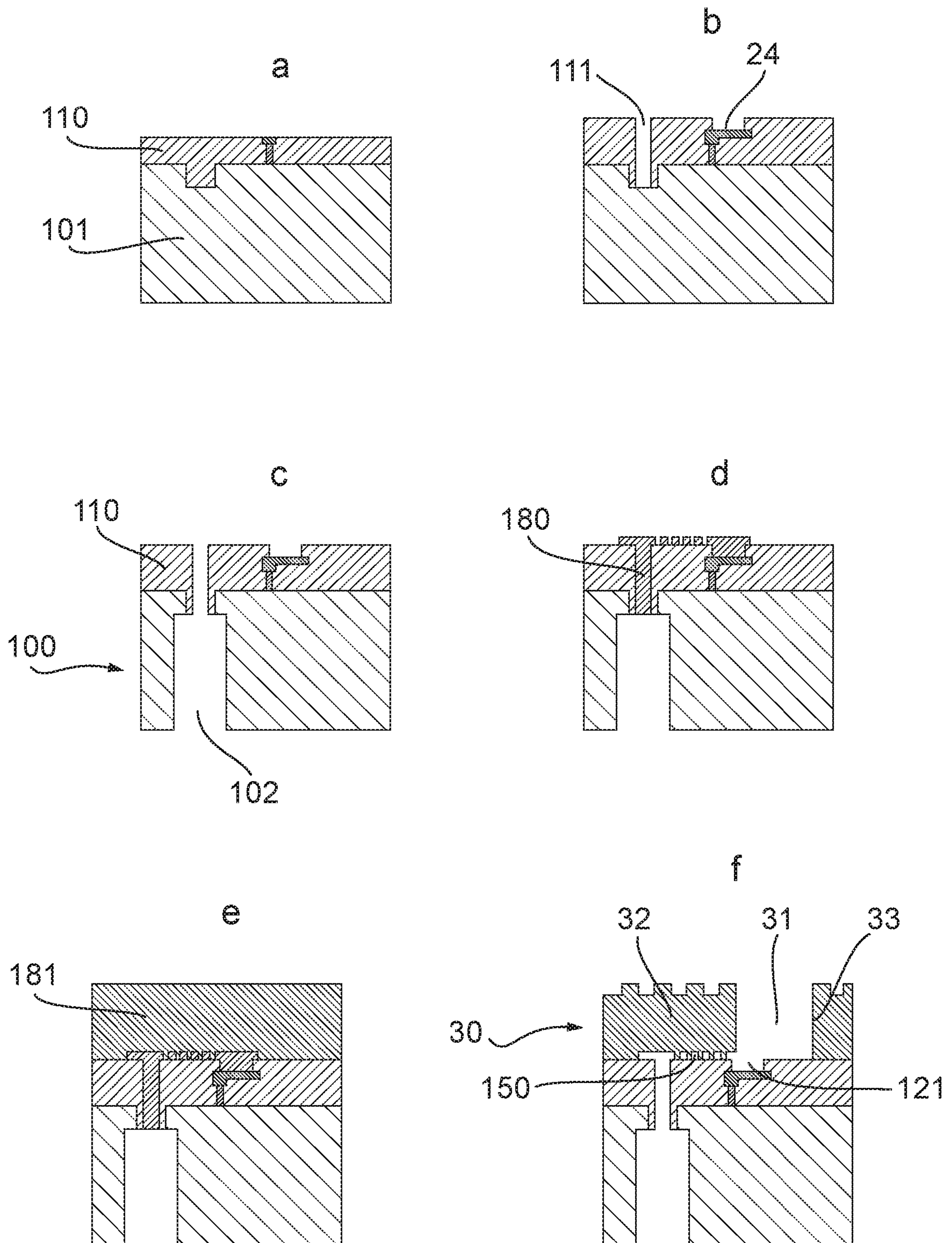
Fig. 12
a
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101
b
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c
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INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2021/051806

A. CLASSIFICATION OF SUBJECT MATTER
INV. G01N33/487 G01N15/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01N C12Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2016/231307 A1 (XIE P) 11 August 2016 (2016-08-11) paragraph [0073] - paragraph [0139]; figures 5, 6, 11-21B paragraph [0178] - paragraph [0182] -----	1-31
X	WO 2019/160925 A1 (ILLUMINA INC [US]) 22 August 2019 (2019-08-22) paragraph [0035] - paragraph [0119]; figures 1A-8M paragraph [0178] - paragraph [0182] -----	1-31
X	US 2018/372713 A1 (STAMM RETO [US] ET AL) 27 December 2018 (2018-12-27) paragraph [0011] - paragraph [0037]; figures 1-5 -----	1-31

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 September 2021	28/09/2021

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Stavroulakis, E

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
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