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(54) Titre : MEMOIRE COMPOSITE DOTEE D'UN DISPOSITIF DE PONTAGE POUR CONNECTER DES DISPOSITIFS DE MEMOIRE DISTINCTS A UN SYSTEME

(54) Title: A COMPOSITE MEMORY HAVING A BRIDGING DEVICE FOR CONNECTING DISCRETE MEMORY DEVICES TO A SYSTEM

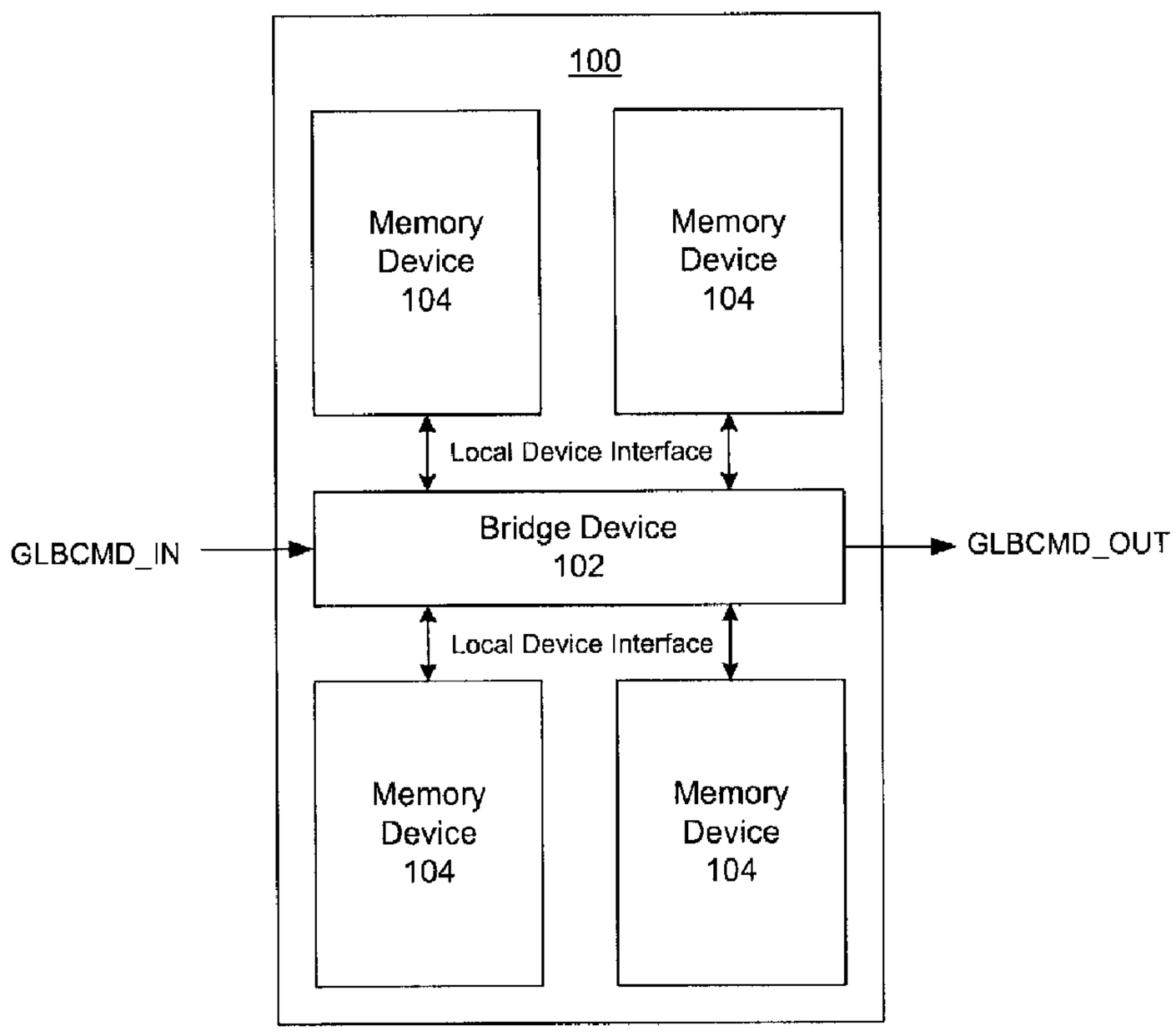

FIG. 3A

(57) Abrégé/Abstract:
A composite memory device including discrete memory devices and a bridge device for controlling the discrete memory devices in response to global memory control signals having a format or protocol that is incompatible with the memory devices. The discrete

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(57) Abrégé(suite)/Abstract(continued):
memory devices can be commercial off-the-shelf memory devices or custom memory devices which respond to native, or local memory control signals. The global and local memory control signals include commands and command signals each having different formats. The composite memory device includes a system in package including the semiconductor dies of the discrete memory devices and the bridge device, or can include a printed circuit board having packaged discrete memory devices and a packaged bridge device mounted thereto.

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(54) Title: A COMPOSITE MEMORY HAVING A BRIDGING DEVICE FOR CONNECTING DISCRETE MEMORY DEVICES TO A SYSTEM

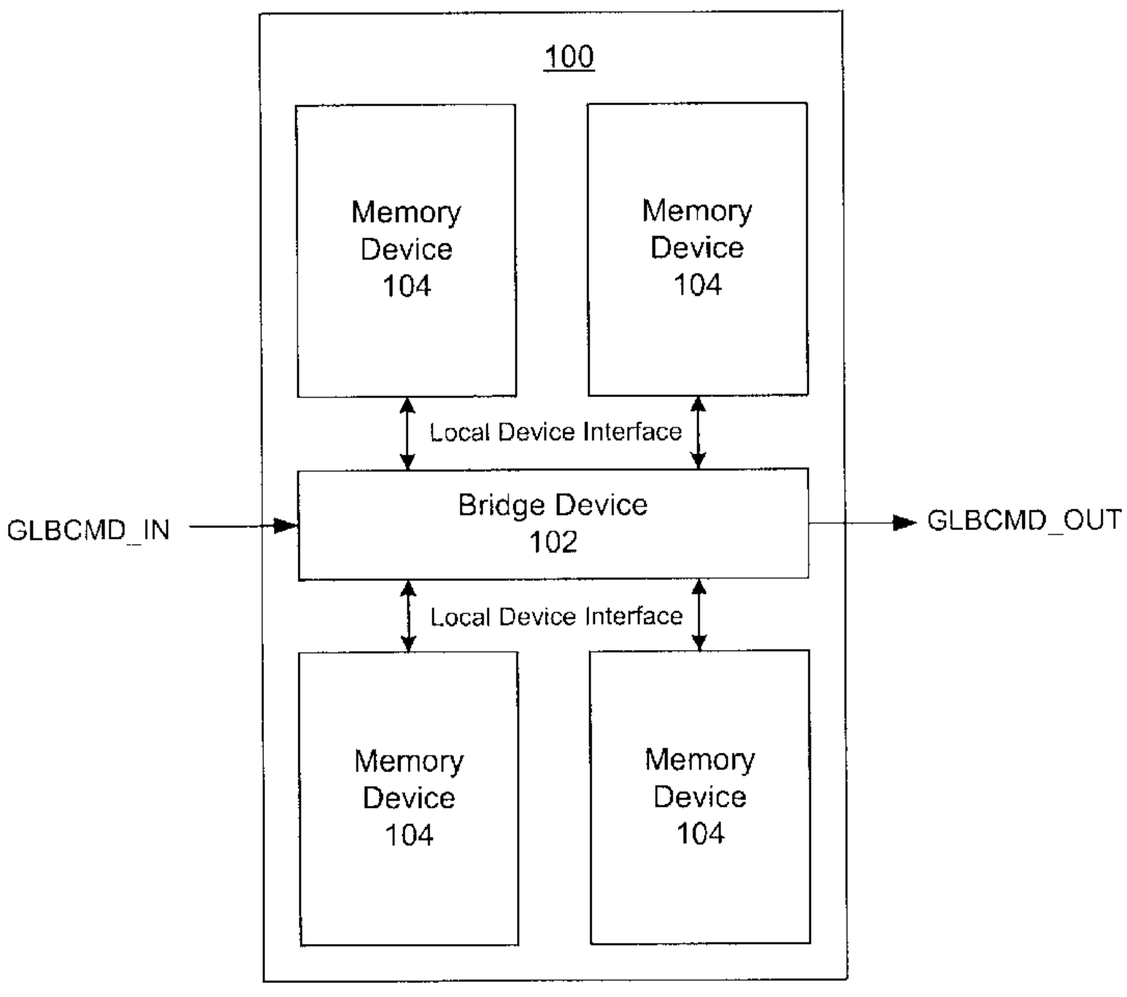

FIG. 3A

(57) Abstract: A composite memory device including discrete memory devices and a bridge device for controlling the discrete memory devices in response to global memory control signals having a format or protocol that is incompatible with the memory devices. The discrete memory devices can be commercial off-the-shelf memory devices or custom memory devices which respond to native, or local memory control signals. The global and local memory control signals include commands and command signals each having different formats. The composite memory device includes a system in package including the semiconductor dies of the discrete memory devices and the bridge device, or can include a printed circuit board having packaged discrete memory devices and a packaged bridge device mounted thereto.

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A COMPOSITE MEMORY HAVING A BRIDGING DEVICE FOR CONNECTING DISCRETE MEMORY DEVICES TO A SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of priority from U.S. Provisional Patent Application No. 61/105,061 filed October 14, 2008, from U.S. Provisional Patent Application No. 61/111,013 filed November 4, 2008, and from U.S. Patent Application Serial No. 12/401,963 filed on March 11, 2009, the disclosures of which are expressly incorporated herein by reference in their entirety.

BACKGROUND

[0002] Semiconductor memory devices are important components in presently available industrial and consumer electronics products. For example, computers, mobile phones, and other portable electronics all rely on some form of memory for storing data. While many memory devices are typically available as commodity, or discrete memory devices, the need for higher levels of integration and higher input/output (I/O) bandwidth has led to the development of embedded memory, which can be integrated with systems, such as microcontrollers and other processing circuits.

[0003] Most consumer electronics employ, non-volatile devices, such as flash memory devices, for storage of data. Demand for flash memory devices has continued to grow significantly because these devices are well suited in various applications that require large amounts of non-volatile storage, while occupying a small physical area. For example, flash is widely found in various consumer devices, such as digital cameras, cell phones, universal serial bus (USB) flash drives and portable music players, to store data used by these devices. Also, flash devices are used as solid state drives (SSDs) for hard disk drive (HDD) replacement. Such portable devices are preferably minimized in form factor size and weight. Unfortunately, multimedia and SSD applications require large amounts of memory which can increase the form factor size and weight of their products. Therefore, consumer product manufacturers compromise by limiting the amount of physical memory included in the product to keep its size and weight acceptable to consumers. Furthermore, while flash

memory has a higher density per unit area than DRAM or SRAM, its performance is limited due to its relatively low I/O bandwidth that negatively impacts its read and write throughput.

[0004] In order to meet the ever-increasing demand for and ubiquitous nature of applications of memory devices, it is desirable to have high-performance memory devices, i.e., devices having higher I/O bandwidth, higher read & write throughput, and increased flexibility of operations.

SUMMARY

[0005] A composite memory device including a bridge device and discrete memory devices is disclosed. The devices are, for example, memory devices, such as flash memories, dynamic random access memories (DRAMs), and static random access memories (SRAMs), DiNOR Flash EEPROM device(s), Serial Flash EEPROM device(s), Ferro RAM device(s), Magneto RAM device(s), Phase Change RAM device(s), or any suitable combination of these and/or other devices.

[0006] In an aspect, there is provided a composite memory device comprising at least one discrete memory device and a bridge device. The at least one discrete memory device executes memory operations in response to local memory control signals having a first format. The bridge device receives global memory control signals having a second format and converts the global memory control signals into the local memory control signals.

[0007] In an embodiment, the bridge device can include a local input/output port connected to the at least one discrete memory device, a global input port for receiving the global memory control signals, and a global output port for providing one of the global memory control signals and read data from the at least one discrete memory device.

[0008] The at least one discrete memory device and the bridge device can be encapsulated in a package. The global input port and the global output port can be electrically coupled to leads of the package. Electrical conductors can be used couple the local input/output port to the at least one discrete memory device. Alternatively, the local input/output port can be wirelessly coupled to the at least one discrete memory device.

[0009] In another embodiment, the at least one discrete memory device can be a packaged memory device and the bridge device can be a packaged bridge device. The packaged

memory device and the packaged bridge device can be mounted onto a printed circuit board. The local input/output port, the global input port and the global output port can be electrically coupled to leads of the packaged bridge device. The packaged memory device can have memory leads electrically connected to the local input/output port of the packaged bridge device.

[0010] In an embodiment, the global memory control signals, in the composite memory device, can be received in a global command. The global command can further include an address header. The address header can include a global device address corresponding to a selected composite memory device and a local device address corresponding to a selected discrete memory device of the at least one discrete memory device in the selected composite memory device.

[0011] In an embodiment of the composite memory device, the first format can include a serial data interface format or an ONFi specification interface format and the second format can include an asynchronous flash memory format.

[0012] In another aspect, there is provided a memory system comprising a memory controller and n composite memory devices connected serially with each other and the memory controller in a ring topology configuration. The memory controller provides a global command corresponding to a memory operation. Each of the n composite memory devices has m discrete memory devices and a bridge device. The bridge device of a selected composite memory device of the n composite memory devices receives the global command and provides local memory control signals corresponding to the memory operation to a selected discrete memory device of the m discrete memory devices, where n and m are integer values greater than 0.

[0013] In an embodiment, each of the n composite memory devices can be a system in package (SIP) or a printed circuit board (PCB). The m discrete memory devices and the bridge device can be packaged devices having package leads connected to conductive tracks in the PCB.

[0014] In another embodiment, the bridge device can include a bridge device input/output interface, a format conversion circuit and a memory device interface. The bridge device input/output interface has an input port for receiving the global command and an output port for providing the global command. The bridge device compares the global device address to

a predetermined address stored in a global device address register and when the global device address matches the predetermined address, the format conversion circuit converts the global memory control signals of the global command from a first format to the local memory control signals having a second format. The memory device interface then provides the local memory control signals to the selected discrete memory device in response to the local device address.

[0015] In an embodiment, the format conversion circuit comprises a command format converter and a data format converter. The command format converter converts the global memory control signals in the first format to the local memory control signals having the second format. The data format converter converts read data from the selected discrete memory device from the second format to the first format. In a write operation, the data format converter converts write data from the first format to the second format.

[0016] In yet another embodiment, a composite memory device in the memory system can have different types of discrete memory devices. In such cases, the bridge device can include a number of format conversion circuits corresponding to each type of the different types of discrete memory devices.

[0017] According to another aspect, there is provided a composite memory device package. The composite memory device package includes at least one discrete memory device and a bridge device. The at least one discrete memory device executes memory operations in response to local memory control signals having a first format. The bridge device receives global memory control signals having a second format and converts the global memory control signals into the local memory control signals. The bridge device and the at least one discrete memory device are positioned in a stacked manner in relation to each other.

[0018] In yet another aspect, there is provided memory module. The memory module includes at least one packaged discrete memory device and a packaged bridge device. The at least one packaged discrete memory device has memory device leads bonded to conductive tracks of a printed circuit board. The at least one packaged memory device executes memory operations in response to local memory control signals having a first format. The packaged bridge device has bridge device leads bonded to the conductive tracks of the printed circuit board. The at least one packaged bridge device receives global memory

control signals having a second format and for converting the global memory control signals into the local memory control signals.

[0019] In a further aspect, there is provided a bridge device to access a discrete memory device in response to global signals having a global format. The bridge device includes a bridge device input/output interface and a bridge device memory device interface. The bridge device input/output interface communicates the global signals having the global format to and from the bridge device. The bridge device memory device interface communicates local signals having a local format between the bridge device and the discrete memory device. The local signals correspond in function to the global signals and have a local format different from the global format.

[0020] In another aspect, there is provided a memory system having a memory controller and n composite memory devices. The memory controller provides a global command corresponding to a memory operation. The n composite memory devices are connected in parallel with each other and the memory controller, where each of the n composite memory devices has m discrete memory devices and a bridge device. The bridge device of a selected composite memory device of the n composite memory devices receives the global command for providing local memory control signals corresponding to the memory operation to a selected discrete memory device of the m discrete memory devices, where n and m are integer values greater than 0.

[0021] Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] Embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Fig. 1A is a block diagram of an example non-volatile memory system;

Fig. 1B is a diagram of a discrete flash memory device used in the example memory system of Figure 1A;

Fig. 2A is a block diagram of an example serial memory system;

Fig. 2B is a diagram of a discrete serial interface flash memory device used in the example memory system of Figure 2A;

Fig. 3A is a block diagram of a composite memory device having four discrete memory devices and a bridge device in accordance with an embodiment;

Fig. 3B is an illustration of a global command, according to a present embodiment;

Fig. 4 is a block diagram of a bridge device in accordance with an embodiment;

Fig. 5A is a cross-section of a composite memory device in a package in accordance with another embodiment;

Fig. 5B is a cross-section of an alternate composite memory device in a package in accordance with another embodiment;

Fig. 6 is a block diagram of a memory system having a number of discrete memory devices connected to a bridge device in a module in accordance with another embodiment;

Fig. 7 is a block diagram of a memory system having a number of composite memory devices connected to a controller in a serial interconnected memory system in accordance with an embodiment

Fig. 8 is a block diagram showing memory mapping of the bridge device of Figure 3A to NAND flash memory devices, according to a present embodiment;

Figs. 9A, 9B and 9C illustrate an example read operation from one NAND flash memory device using the bridge device of Figure 3A;

Figs. 10A, 10B, 10C and 10D illustrate example virtual page configurations for each memory bank of the bridge device of Figure 3A

Fig. 11 is a flow chart illustrating a method for reading data from a composite memory device, according to a present embodiment; and

Fig. 12 is a flow chart illustrating a method for writing data to a composite memory device, according to a present embodiment.

DETAILED DESCRIPTION

[0023] Generally, the embodiments of the present invention are directed to a composite memory device including discrete memory devices and a bridge device for controlling the discrete memory devices in response to global memory control signals having a format or protocol that is incompatible with the memory devices. The discrete memory devices can be commercial off-the-shelf memory devices or custom memory devices, which respond to native, or local memory control signals. The global and local memory control signals include commands and command signals each having different formats.

[0024] In accordance with an embodiment, the bridge device, or chip, includes a bridge device input/output interface; a format conversion circuit; and, a memory device interface. The bridge device input/output interface communicates with a memory controller or another composite memory device in a global format. The format conversion circuit converts global memory control signals from the global format to a corresponding local format compatible with discrete memory devices connected to it. The global format is followed only by the global memory control signals received by the bridge devices, while the local format is followed only by the local memory control signals used by the discrete memory devices. Thus the memory device interface communicates with each discrete memory device connected to the bridge device in the local format.

[0025] The system and device in accordance with the techniques described herein are applicable to a memory system having a plurality of devices connected in series. The devices are, for example, memory devices, such as dynamic random access memories (DRAMs), static random access memories (SRAMs), flash memories, DiNOR Flash EEPROM memories, Serial Flash EEPROM memories, Ferro RAM memories, Magneto RAM memories, Phase Change RAM memories, and any other suitable type of memory.

[0026] Following are descriptions of two different memory devices and systems to facilitate a better understanding of the later described composite memory device and bridge device embodiments.

[0027] Figure 1A is a block diagram of a non-volatile memory system **10** integrated with a host system **12**. The system **10** includes a memory controller **14** in communication with host system **12**, and a plurality of non-volatile memory devices **16-1, 16-2, 16-3** and **16-4**. For example the non-volatile memory devices **16-1 – 16-4** can be discrete asynchronous

flash memory devices. The host system **12** includes a processing device such as a microcontroller, microprocessor, or a computer system. The system **10** of Figure 1A is organized to include one channel **18**, with the memory devices **16-1 – 16-4** being connected in parallel to channel **18**. Those skilled in the art should understand that the system **10** can have more or fewer than four memory devices connected to it. In the presently shown example, the memory devices **16-1 – 16-4** are asynchronous and connected in parallel with each other.

[0028] Channel **18** includes a set of common buses, which include data and control lines that are connected to all of its corresponding memory devices. Each memory device is enabled or disabled with respective chip select (enable) signals CE1#, CE2#, CE3# and CE4#, provided by memory controller **14**. In this and following examples, the "#" indicates that the signal is an active low logic level signal. In this scheme, one of the chip select signals is typically selected at one time to enable a corresponding one of the non-volatile memory devices **16-1 – 16-4**. The memory controller **14** is responsible for issuing commands and data, via the channel **18**, to a selected memory device in response to the operation of the host system **12**. Read data output from the memory devices is transferred via the channel **18** back to the memory controller **14** and host system **12**. The system **10** is generally said to include a multi-drop bus, in which the memory devices **16-1 – 16-4** are connected in parallel with respect to channel **18**.

[0029] Figure 1B is a diagram of one of the discrete flash memory devices **16-1 – 16-4** which can be used in the memory system of Figure 1A. This flash memory device includes several input and output ports, which include for example power supply, control ports and data ports. The term "ports" refers to a generic input or output terminals into the memory device, which includes package pins, package solder bumps, chip bond pads, and wireless transmitters and receivers for example. The power supply ports include VCC and VSS for supplying power to all the circuits of the flash memory device. Additional power supply ports can be provided for supplying only the input and output buffers, as is well known in the art. Table 1 below provides a listing of the control and data ports, their corresponding descriptions, definitions, and example logic states. It is noted that that package pins and ball grid arrays are physical examples of a port, which is used for interconnecting signals or voltages of a packaged device to a board. The ports can include other types of connections,

such as for example, terminals and contacts for embedded and system-in-package (SIP) systems.

[0030] Table 1

Port	Description
R/B#	Ready/Busy: the R/B# is open drain port and the output signal is used to indicate the operating condition of the device. The R/B# signal is in Busy state (R/B# = LOW) during the Program, Erase and Read operations and will return to Ready state (R/B# = HIGH) after completion of the operation.
CE#	Chip Enable: the device goes into a low-power Standby mode when CE# goes HIGH during the device is in Ready state. The CE# signal is ignored when device is in Busy state (R/B# = LOW), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the CE# input goes HIGH
CLE	Command Latch Enable: the CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the WE# signal while CLE is HIGH.
ALE	Address Latch Enable (ALE): the ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of the WE# signal while ALE is HIGH.
WE#	Write Enable: the WE# signal is used to control the acquisition of data from the I/O port.
RE#	Read Enable: the RE signal controls serial data output. Data is available after the falling edge of RE#.
WP#	Write Protect: the WP# signal is used to protect the device from accidental programming or erasing. The internal voltage regulator (high voltage generator) is reset when WP# is LOW. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.

I/O[n]	I/O Port: are used as a port for transferring address, command and input/output data to and from the device. Variable n can be any non-zero integer value.

[0031] All the signals noted in Table 1 are generally referred to as the memory control signals for operation of the example flash memory device illustrated in Figure 1B. It is noted that the last port I/O[n] is considered a memory control signal as it can receive commands which instruct the flash memory device to execute specific operations. Because a command asserted on port I/O[n] is a combination of logic states applied to each individual line making up I/O[n], the logic state of each signal of I/O[n] functions in the same manner as one of the other memory control signals, such as WP# for example. The main difference being that it is a specific combination of I/O[n] logic states controls the flash memory device to perform a function. The commands are received via its I/O ports and the command signals include the remaining control ports. Those skilled in the art understand that operational codes (op codes) are provided in the command for executing specific memory operations. With the exception of the chip enable CE#, all the other ports are coupled to respective global lines that make up channel **18**. Individual chip enable signals are provided to each flash memory device by the memory controller **14**. All the ports are controlled in a predetermined manner for executing memory operations. This includes signal timing and sequencing of specific control signals while address, command and I/O data is provided on the I/O ports. Therefore, the memory control signals for controlling the asynchronous flash memory device of Figure 1B has a specific format, or protocol.

[0032] Each of the non-volatile memory devices of Figure 1A has one specific data interface for receiving and providing data. In the example of Figure 1A, this is a parallel data interface commonly used in asynchronous flash memory devices. Standard parallel data interfaces providing multiple bits of data in parallel are known to suffer from well known communication degrading effects such as cross-talk, signal skew and signal attenuation, for example, which degrades signal quality, when operated beyond their rated operating frequency.

[0033] In order to increase data throughput, a memory device having a serial data interface has been disclosed in commonly owned U.S. Patent Publication No. 20070153576 entitled “Memory with Output Control”, and commonly owned U.S. Patent Publication No.

20070076502 entitled “Daisy Chain Cascading Devices” which receives and provides data serially at a frequency, for example, 200 MHz. This is referred to as a serial data interface format. As shown in these commonly owned patent publications, the described memory device can be used in a system of memory devices that are serially connected to each other.

[0034] Figure 2A is a block diagram illustrating the conceptual nature of a serial memory system. In Figure 2A, the serial ring-topology memory system **20** includes a memory controller **22** having a set of output ports Sout and a set of input ports Sin, and memory devices **24**, **26**, **28** and **30** that are connected in series. The memory devices can be serial interface flash memory devices for example. While not shown in Figure 2A, each memory device has a set of input ports Sin and a set of output ports Sout. These sets of input and output ports includes one or more individual input/output ports, such as physical pins or connections, interfacing the memory device to the system it is a part of. In one example, the memory devices can be flash memory devices. Alternately, the memory devices can be DRAM, SRAM, DiNOR Flash EEPROM, Serial Flash EEPROM, Ferro RAM, Magneto RAM, Phase Change RAM, or any other suitable type of memory device that has an input/output interface compatible with a specific command structure, for executing commands or for passing commands and data through to the next memory device. The current example of Figure 2A includes four memory devices, but alternate configurations can include a single memory device, or any suitable number of memory devices. Accordingly, if memory device **24** is the first device of the system **20** as it is connected to Sout, then memory device **30** is the Nth or last device as it is connected to Sin, where N is an integer number greater than zero. Memory devices **26** to **28** are then intervening serially connected memory devices between the first and last memory devices. In the example of Figure 2A, the memory devices **24** to **30** are synchronous and connected in series with each other and the memory controller **22**.

[0035] Figure 2B is a diagram of the serial interface flash memory device (**24** to **30** for example) which can be used in the memory system of Figure 2A. This example serial interface flash memory device includes power supply ports, control ports and data ports. The power supply ports include VCC and VSS for supplying power to all the circuits of the flash memory device. Additional power supply ports can be provided for supplying only the input and output buffers, as is well known in the art. Table 2 below provides a listing of the control and data ports, their corresponding descriptions, and example logic states.

[0036] Table 2

Port	Description
CK / CK#	Clock: CK is the system clock input. CK and CK# are differential clock inputs. All commands, addresses, input data and output data are referenced to the crossing edges of CK and CK# in both directions.
CE#	Chip Enable: When CE# is LOW, the device is enabled. Once the device starts a Program or Erase operation, the Chip Enable port can be de-asserted. In addition, CE# LOW activates and CE# HIGH deactivates the internal clock signals.
RST#	Chip Reset: RST# provides a reset for the device. When RST# is HIGH, the device is on the normal operating mode. When RST# is LOW, the device will enter the Reset mode.
D[n]	Data Input: (n=1,2,3,4,5,6,7 or 8) receives command, address and input data. If the device is configured in '1-bit Link mode (=default)', D1 is the only valid signal and receives one byte of packet in 8 crossings of CK/CK#. If the device is configured in '2-bit Link mode', D1 & D2 are only valid signals and receive one byte of packet in 4 crossings of CK/CK#. Unused input ports are grounded.
Q[n]	Data Output: (n=1,2,3,4,5,6,7 or 8) transmits output data during read operation. If device is configured in '1-bit Link mode (=default)', Q1 is the only valid signal and transmits one byte of packet in 8 crossings of CK/CK#. If the device is configured in '2-bit Link mode', Q1 & Q2 are the only valid signals and transmit one byte of packet in 4 crossings of CK/CK#. Unused output ports are DNC (= Do Not Connect).
CSI	Command Strobe Input: When CSI is HIGH, command, address and input data through D[n] are latched on the crossing of CK and CK#. When CSI is LOW, the device ignores input signals from D[n].
CSO	Command Strobe Output: The echo signal CSO is a re-transmitted version of the source signal CSI.
DSI	Data Strobe Input: Enables the Q[n] buffer when HIGH. When DSI is LOW, the Q[n] buffer holds the previous data accessed.

DSO	Data Strobe Output: The echo signal DSO is a re-transmitted version of the source signal DSI.

[0037] With the exception of signals CSO, DSO and Q[n], all the signals noted in Table 2 are the memory control signals for operation of the example flash memory device illustrated in Figure 2B. CSO and DSO are retransmitted versions of CSI and DSI, and Q[n] is an output for providing commands and data. The commands are received via its D[n] ports and the command signals include the control ports RST#, CE#, CK, CK#, CSI and DSI. In the example configuration shown in Figure 2A, all signals are passed serially from the memory controller **22** to each memory device in series, with the exception of CE# and RST#, which are provided to all the memory devices in parallel. The serial interface flash memory device of Figure 2B thus receives memory control signals having its own format or protocol, for executing memory operations therein.

[0038] Further details of the serially connected memory system of Figure 2 are disclosed in commonly owned U.S. Patent Publication No. 20090039927 entitled "Clock Mode Determination in a Memory System" filed on February 15, 2008, which describes a serial memory system in which each memory device receives a parallel clock signal, and a serial memory system in which each memory device receives a source synchronous clock signal.

[0039] Having both the commonly available asynchronous flash memory devices of Figure 1B and the serial interface flash memory devices of Figure 2B allows a memory system manufacturer to provide both types of memory systems. However, this will likely introduce higher cost to the memory system manufacturer since two different types of memory devices must be sourced and purchased. Those skilled in the art understand that the price per memory device decreases when large quantities are purchased, hence large quantities are purchased to minimize the cost of the memory system. Therefore, while a manufacturer can provide both types of memory systems, it bears the risk of having one type of memory device fall out of market demand due the high market demand of the other. This may leave them with purchased supplies of a memory device that cannot be used.

[0040] As shown in Figure 1B and Figure 2B, the functional port assignments or definitions of the asynchronous and serial interface flash memory devices are substantially different

from each other, and are accordingly, incompatible with each other. The functional port definitions and sequence, or timing, of sets of signals used for controlling the discrete memory devices is referred to as a protocol or format. Therefore the asynchronous and serial flash memory devices operate in response to different memory control signal formats. This means that the serial interface flash memory device of Figure 2B cannot be used in a multi-drop memory system, and correspondingly, the asynchronous flash memory device of Figure 1B cannot be used in a serial connected ring topology memory system.

[0041] Although serial interface flash memory devices as shown in Figure 2A and Figure 2B are desirable for their improved performance over the asynchronous flash memory devices of Figures 1A and 1B, memory system manufacturers may not wish to dispose of their supplies of asynchronous flash memory devices. Furthermore, due to their ubiquitous use in the industry, asynchronous flash memory devices are inexpensive to purchase relative to lesser known alternative flash memory devices such as the serial interface flash memory device of Figure 2A. Presently, memory system manufacturers do not have a solution for taking advantage of the performance benefits of serially interconnected devices with minimal cost overhead.

[0042] At least some example embodiments provide a high performance composite memory device with a high-speed interface chip or a bridge device in conjunction with discrete memory devices, in a multi-chip package (MCP) or system in package (SIP). The bridge device provides an I/O interface with the system it is integrated within, and receives global memory control signals following a global format, and converts the commands into local memory control signals following a native or local format compatible with the discrete memory devices. The bridge device thereby allows for re-use of discrete memory devices, such as NAND flash devices, while providing the performance benefits afforded by the I/O interface of the bridge device. The bridge device can be embodied as a discrete logic die integrated with the discrete memory device dies in the package.

[0043] In the present examples, the global format is a serial data format compatible with the serial flash memory device of Figures 2A and 2B, and the local format is a parallel data format compatible with the asynchronous flash memory device of Figures 1A and 2B. However, the embodiments of the present invention are not limited to the above example formats, as any pair of memory control signal formats can be used, depending the type of discrete memory devices used in the composite memory device and the type of memory

system the composite memory device is used within. For example, the global format of the memory system can follow the Open NAND Flash Interface (ONFi) standard, and the local format can follow the asynchronous flash memory device memory control signal format. For example, one specific ONFi standard is the ONFi 2.0 Specification. Alternatively, the global format can follow the asynchronous flash memory device memory control signal format and the local format can follow the ONFi 2.0 Specification format. In general, the ONFi specification is a multi-drop synchronous protocol where data and commands are provided to the compliant memory device via its data input/output ports synchronously with a clock. In otherwords, an ONFi compliant memory device can have some similarities to an asynchronous NAND flash memory device having parallel bi-directional input/output ports with one important difference being that the ONFi compliant device receives a clock signal.

[0044] Figure 3A is a block diagram of a composite memory device, according to a present embodiment. As shown in Figure 3A, composite memory device **100** includes a bridge device **102** connected to four discrete memory devices **104**. Each of the discrete memory devices **104** can be asynchronous flash memory devices having a memory capacity of 8Gb, for example, but any capacity discrete flash memory device can be used instead of 8Gb devices. Furthermore, composite memory device **100** is not limited to having four discrete memory devices. Any suitable number of discrete memory devices can be included, when bridge device **102** is designed to accommodate the maximum number of discrete memory devices in the composite memory device **100**.

[0045] Composite memory device **100** has an input port GLBCMD_IN for receiving a global command, and an output port GLBCMD_OUT for passing the received global command and read data. Figure 3B is a schematic illustrating the hierarchy of a global command, according to a present embodiment. The global command **110** includes global memory control signals (GMCS) **112** having a specific format, and an address header (AH) **114**. These global memory control signals **112** provide a memory command and command signals, such as the memory control signals for the serial interface flash memory device of Figure 2B. The address header **114** includes addressing information used at the system level and the composite memory device level. This additional addressing information includes a global device address (GDA) **116** for selecting a composite memory device to execute an op code in the memory command, and a local device address (LDA) **118** for selecting a particular discrete device within the selected composite memory device to execute the op code. In

summary, the global command includes all the memory control signals corresponding to one format, and further addressing information which may be required for selecting or controlling the composite memory device or the discrete memory devices therein.

[0046] It is noted that bridge device **102** does not execute the op code or access any memory location with the row and address information. The bridge device **102** uses the global device address **116** to determine if it is selected to convert the received global memory control signals **112**. If selected, bridge device **102** then uses the local device address **118** to determine which of the discrete memory devices the converted global memory control signals **112** is sent to. In order to communicate with all four discrete memory devices **104**, bridge device **102** includes four sets of local I/O ports (not shown), each connected to a corresponding discrete memory device, as will be discussed later. Each set of local I/O ports includes all the signals that the discrete memory device requires for proper operation, and thereby functions as a local device interface.

[0047] Read data is provided by any one of a flash memory device **104** from composite memory device **100**, or from a previous composite memory device. In particular, the bridge device **102** can be connected to a memory controller of a memory system, or to another bridge device of another composite memory device in a system of serially interconnected devices. The input port GLBCMD_IN and output port GLBCMD_OUT can be package pins, other physical conductors, or any other circuits for transmitting/receiving the global command signals and read data to and from the composite memory device **100**, and in particular, to and from bridge device **102**. The bridge device **102** therefore has corresponding connections to the input port GLBCMD_IN and the output port GLBCMD_OUT to enable communication with an external controller, such as memory controller **22** of Figure 2A, or with the bridge devices from other composite memory devices in the system. As will be shown in the example embodiment of Figure 7, many composite memory devices can be connected serially to each other.

[0048] Figure 4 is a block diagram of a bridge device **200** in accordance with an embodiment, which corresponds to the bridge device **102** shown in Figure 3A. The bridge device **200** has a bridge device input/output interface **202**, a memory device interface **204**, and a format converter **206**. The format converter **206** includes a command format converter **208** for converting global memory control signals, which include global commands and global command signals in a first format to a second format, and a data format converter **210** for

converting data between the first format and the second format. The command format converter **208** further includes a state machine (not shown) for controlling the discrete memory devices, such as discrete memory devices 104 of Figure 3A in accordance with the second format in response to the global memory control signals in the first format.

[0049] The bridge device input/output interface **202** communicates with external devices, such as for example, with a memory controller or another composite memory device. The bridge device input/output interface **202** receives global commands from a memory controller or another composite memory device in the global format, such as for example in a serial command format. With further reference to Figure 3B, logic in the input/output interface **202** processes the global device address **116** of the global command **110** to determine if the global command **110** is addressed to the corresponding composite memory device, and processes the local device address **118** in the global command **110** to determine which of the discrete memory devices of the corresponding composite memory device is to receive the converted command, which includes an op code and optional row and column addresses and optional write data. If the global command is addressed to a discrete memory device connected to bridge device **200**, the command format converter **208** in the format converter **206** converts the global memory control signals **112**, which provides the op code and command signals and any row and address information from the global format to the local format, and forwards it to the memory device interface **204**. This converted local command has local signals corresponding in function to the global signals of the global format. In some cases, multiple local commands may be issued in response to a single global command since the multiple local commands may be required for completing the operation of the global command. If write data is provided to bridge device input/output interface **202** in a serial data format for example, then bridge device input/output interface **202** includes serial-to-parallel conversion circuitry for providing bits of data in parallel format. For read operations, bridge device input/output interface **202** includes parallel-to-serial conversion circuitry for providing bits of data in serial format for output through the GLBCMD_OUT output port.

[0050] It is assumed that the global format and the local format are known, hence logic in command format converter **208** is specifically designed to execute the logical conversion of the signals to be compatible with the discrete memory devices **104**. It is noted that command format converter **208** can include control logic at least substantially similar to that of a

memory controller of a memory system, which is used for controlling the discrete memory devices with memory control signals having a native format. For example, command format converter **208** may include effectively the same control logic of memory controller **14** of Figure 1A if the discrete memory devices are asynchronous memory devices, such as memory devices **16-1** to **16-4**. This means that the control logic in command format converter **208** provides the timing and sequencing of the memory control signals in the local format native to the discrete memory devices.

[0051] If the global command corresponds to a data write operation, the data format converter **210** in the format converter **206** converts the data from the global format to the local format, and forwards it to the memory device interface **204**. The bits of read or write data do not require logical conversion, hence data format converter **210** ensures proper mapping of the bit positions of the data between the first data format and the second data format. Format converter **206** functions as a data buffer for storing read data from the discrete memory devices or write data received from the bridge device input/output interface **202**. Therefore, data width mismatches between the global format and the local format can be accommodated. Furthermore, different data transmission rates between the discrete memory devices and the bridge device **200**, and the bridge device **200** and other composite memory devices are accommodated due to the buffering functionality of data format converter **210**.

[0052] The memory device interface **204** then forwards or communicates the converted command in the local command format to the discrete memory device selected by the local device address **118** in the global command **110** of Figure 3B. In the present embodiment, the converted command is provided via a command path **212**. In an embodiment, command path **212** includes i sets of dedicated local I/O ports LCCMD-i, or channels, connected between each discrete memory device in the composite memory device and the memory device interface **204**. The variable i is an integer number corresponding to the number of discrete memory devices in the composite memory device. For example, each LCCMD-i channel includes all the ports shown in Figure 1B and Table 1. In an alternate embodiment for example, an LCCMD-i channel includes all the ports of an ONFi compliant device, including a clock signal that can be generated in a clock circuit of the command format converter **208**. Clock generation circuits and techniques are well known in the art, and in the

present embodiment clock dividers or multipliers can be included to generate clock signals having a desired frequency from a single "master" clock signal.

[0053] Following is a description of example operations of bridge device **200**, with further reference to the composite memory device **100** of Figure 3A. For a read operation, a global command, such as a global read command arriving at the bridge device input/output interface **202** through input port GLBCMD_IN. This global read command includes the global memory control signals that provide an op code and row and column information in the global format, for data to be read out from a discrete memory device **104** connected to the bridge device **200**. Once the bridge device input/output interface **202** determines that it has been selected for the global read command by comparing the global device address **116** to a predetermined address of the composite memory device **100**, the command format converter **208** converts the global read command into the local format compatible with the discrete memory device **104** on which the read data command is to be executed. As will be described later, the composite memory device can have an assigned address. The local device address **118** of the global read command is forwarded to the memory device interface **204**, and the converted read data command is provided to the discrete memory device addressed by the local device address via a corresponding set of local I/O ports of the command path **212**.

[0054] Data referred to as read data, is read from the selected discrete memory device **104** and provided to the data format converter **210** via the same local I/O ports of memory device interface **204** in the local format. The data format converter **210** then converts the read data from the local format to the global format and provides the read data from the selected discrete memory device **104** to the memory controller through output port GLBCMD_OUT of bridge device interface **202**. Bridge device interface **202** includes internal switching circuitry for coupling either the read data from data format converter **210** or the input port GLBCMD_IN to the output port GLBCMD_OUT.

[0055] Figure 3A described above is a functional representation of a composite memory device, according to one embodiment. Figure 5 shows a composite memory device manufactured as a system in package (SIP), which corresponds to the composite memory device shown in Figure 3A, according to another embodiment. Figure 5 shows a cross-section of a composite memory device stacked in a package. The package **300** includes

bridge device **302** corresponding to bridge device **102** of Figure 3A, and four discrete memory devices **304** corresponding respectively to discrete memory devices **104** also from Figure 3A. In the present embodiment, these devices are fabricated semiconductor chips, or dies. The bridge device **302** communicates with memory devices **304** via memory device interface **306** in a local format such as the parallel asynchronous NAND format for example. The bridge device **302** communicates with a memory controller (not shown) or with another composite memory devices' bridge device via the bridge device input/output interface **308** in a global format, such as for example, the previously described serial data format. The format converter **310** includes the previously mentioned command format converter **208** and data format converter **210** of Figure 3A, for providing uni-directional command format conversion and bi-directional data format conversion between itself and the discrete memory devices **304**.

[0056] In the presently shown example, the composite memory device package **300** is referred to as an SIP system, or a multi-chip package (MCP) system. The package encapsulates bridge device **302** and all four discrete memory devices **304**. Local communication terminals, represented by wires **312**, connect the I/O ports of each discrete memory device **304** to the memory device interface **306** of bridge device **302**. Each wire **312** represents one channel LCCMD-i carrying all the signals corresponding to the local format. One example local format is the asynchronous flash memory format including the signals shown in Table 1. Global communication terminals, represented by wires **314** and **316** connect input port GLBCMD_IN and output port GLBCMD_OUT respectively, to package leads **318** via optional package substrate **320**. The physical arrangement of bridge device **302** and discrete memory devices **304** relative to each other depends on the position of the bond pads of discrete memory devices **304** and the position of the bond pads of the bridge device **302**.

[0057] In the embodiment of Figure 5A, each discrete memory device **304** has its data bond pads connected directly to the bond pads of the bridge device **302**. The data bond pads of each discrete memory device **304** forms a channel, which can be connected to dedicated corresponding data bond pads of the bridge device **302**. In the alternative embodiment shown in Figure 5B, each discrete memory device **304** is connected to the bridge device **302** through conductive tracks formed in the package substrate **320**. More specifically, the bond wires **312** are electrically connected to bond wires **314** through such conductive tracks

formed in the substrate **320**. In one embodiment, each discrete memory device **304** is electrically connected to corresponding data bond pads of the bridge device **302** via a respective channel such as in the embodiment of Figure 5A. Alternately, the bridge device **302** includes only one set of data bond pads that are connected in parallel to the data bond pads of each discrete memory device **304**. Therefore, there is one channel shared between all the discrete memory devices **304**. In this alternate embodiment, the conductive tracks formed in the substrate **320** can be coupled in parallel to the bridge device **302** and the discrete memory devices **304**, which is referred to as a multi-drop configuration.

[0058] In the presently shown example in Figure 5A, the discrete memory devices **304** are placed with their bond pads facing in the upwards direction and stacked upon each other in a staggered step pattern for exposure so as not to obstruct the bond pads of the devices which are located proximate to an edge of the chip. Bridge device **302** is placed with its bond pads facing in the upwards direction, and is stacked on the upper-most discrete memory device **304** of the stack. Other configurations are possible, depending on the placement of the discrete memory device bond pads, and different communication terminals can be used instead of bond wires. For example, wireless communication via inductive coupling technology can be used, or through silicon via (TSV) interconnection can be used instead of bond wires. Commonly owned U.S. Patent Publication No. 20090020855 entitled "Method for Stacking Serially-Connected Integrated Circuits and Multi-Chip Device Made from Same" shows a technique for stacking chips together. Also, bridge device **302** does not contribute significantly to the size of the stack in the package **300**. Accordingly, it should be clear persons skilled in the art that composite memory device **300** occupies minimal area in a larger system, while providing high storage capacity.

[0059] Figure 6 shows another embodiment of the composite memory device of Figure 3A, formed as a module or on a printed circuit board (PCB). As shown in Figure 6, composite memory device **400** includes a bridge device **402** and four discrete memory devices **404**. The bridge device **402** and the discrete memory devices **404** are packaged devices, meaning that each encapsulates a semiconductor die and has package leads bonded to preformed conductive tracks in the PCB. The bridge device **402** is connected to individual discrete memory devices **404** via the conductive tracks organized as dedicated local I/O ports or channels LCCMD-i for each memory device **404**. The module or the PCB including the bridge device includes an input port GLBCMD_IN, for receiving global commands, and an

output port GLBCMD_OUT for providing read data and global commands received at the input port. These input and output ports can be connected to a controller (not shown) or to other composite memory devices. As described for the embodiments of Figures 5A and 5B, the individual discrete memory devices **404** can be each connected directly to bridge device **402**, or alternately the individual memory devices **404** can be connected in parallel to bridge device **402** in the multi-drop configuration.

[0060] The composite memory device embodiments of Figures 5A, 5B and Figure 6 can be used in a memory system, such as the serial memory system of Figure 2A, according to another embodiment. Hence, the memory system **500** of Figure 7 is similar to the serial memory system **20** of Figure 2A. Memory system **500** includes a memory controller **502** and composite memory devices **504-1** to **504-j**, where j is an integer number. The individual composite memory devices **504-1 – 504-j** are serially interconnected with the memory controller **502**. Similar to system **20** of Figure 2A, composite memory device **504-1** is the first composite memory device of memory system **500** as it is connected to an ouput port Sout of memory controller **410**, and memory device **504-n** is the last device as it is connected to an input port Sin of memory controller **410**. Composite memory devices **504-2** to **504-7** are then intervening serially connected memory devices connected between the first and last composite memory devices. The Sout port provides a global command in a global format. The Sin port receives read data in the global format, and the global command as it propagates through all the composite memory devices.

[0061] Each of the composite memory devices shown in Figure 7 is similar to the composite memory device **100** shown in Figure 3A. Each of the composite memory devices has a bridge device **102** and four discrete memory devices **104**. As was previously described, each bridge device **102** in each of the composite memory device is connected to respective discrete memory devices **104**, and to either the memory controller **502** and/or a previous or subsequent composite memory device in the serial-ring topology or serial interconnection configuration. The function of each composite memory device **504-1** to **504-j** is the same as previously described for the embodiments of Figure 3A and Figure 4.

[0062] In memory system **500**, each composite memory device is assigned a unique global device address. This unique global device address can be stored in a device address register of the bridge device **102**, and more specifically in a register of the input/output interface **202**

of the bridge device block diagram shown in Figure 4. This address can be assigned automatically during a power up phase of memory system **500** using a device address assignment scheme, as described in commonly owned U.S. Patent Publication No. 20080192649 entitled "Apparatus and Method for Producing Identifiers Regardless of Mixed Device Type in a Serial Interconnection". Furthermore, each composite memory device **504** can include a discrete device register for storing information about the number of discrete memory devices in each composite memory device **504**. Thus during the same power up phase of operation, the memory controller can query each discrete device register and record the number of discrete memory devices within each composite memory device. Hence the memory controller can selectively address individual discrete memory devices **104** in each composite memory device **504** of memory system **500**.

[0063] A description of the operation of memory system **500** follows, using an example where composite memory device **504-3** is to be selected for executing a memory operation. In the present example, memory system **500** is a serially connected memory system similar to the system shown in Figure 2, and each of the discrete memory devices **104** are assumed to be asynchronous NAND flash memory devices. Therefore the bridge devices **102** in each of the composite memory devices **504-1** to **504-j** are designed for receiving global commands in a global format issued by memory controller **502**, and converting them into a local format compatible with the NAND flash memory devices. It is further assumed that memory system has powered up and addresses for each composite memory device have been assigned.

[0064] The memory controller **502** issues a global command from its Sout port, which includes a global device address **116** corresponding to composite memory device **504**-3. The first composite memory device **504-1** receives the global command, and its bridge device **102** compares its assigned global device address to that in the global command. Because the global device addresses mismatch, bridge device **102** for composite memory device ignores the global command and passes the global command to the input port of composite memory device **504-2**. The same action occurs in composite memory device **504-2** since its assigned global device address mismatches the one in the global command. Accordingly, the global command is passed to composite memory device **504-3**.

[0065] The bridge device **102** of composite memory device **504-3** determines a match between its assigned global device address and the one in the global command. Therefore,

bridge device **102** of composite memory device **504-3** proceeds to convert the global memory control signals into the local format compatible with the NAND flash memory devices. The bridge device then sends the converted command to the NAND flash memory device selected by the local device address **118**, which is included in the global command. The selected NAND flash device then executes the operation corresponding to the local memory control signals it has received.

[0066] While bridge device **102** of composite memory device **504-3** is converting the global command, it passes the global command to the next composite memory device. The remaining composite memory devices ignore the global command, which is eventually received at the Sin port of memory controller **502**. If the global command corresponds to a read operation, the selected NAND flash memory device of composite memory device **504-3** provides read data to its corresponding bridge device **102** in the local format. Bridge device **102** then converts the read data into the global format, and passes it through its output port to the next composite memory device. The bridge devices **102** of all the remaining composite memory devices pass the read data to the Sin port of memory controller **502**. Those skilled in the art should understand that other global commands may be issued for executing the read operation, all of which are converted by the bridge device **102** of selected composite memory device **102**.

[0067] In the present embodiment, the global command is propagated to all the composite memory devices in memory system **500**. According to an alternate embodiment, the bridge devices **102** include additional logic for inhibiting the global command from propagating to further composite memory devices in the memory system **500**. More specifically, once the selected composite memory device determines that the global device is addressed to it, its corresponding bridge device **102** drives its output ports to a null value, such as a fixed voltage level of VSS or VDD for example. Therefore, the remaining unselected composite memory devices conserve switching power since they would not execute the global command. Details of such a power saving scheme for a serially connected memory system are described in commonly owned U.S. Patent Publication No. 20080201588 entitled "Apparatus and Method for Producing Identifiers Regardless of Mixed Device Type in a Serial Interconnection", the contents of which are incorporated by reference in their entirety.

[0068] The previously described embodiment of Figure 7 illustrates a memory system where each composite memory device **504-1** to **504-N** having the same type of discrete memory

devices therein, such as for example asynchronous NAND flash memory devices. This is referred to as a homogeneous memory system because all the composite memory devices are the same. In alternate embodiments, a heterogeneous memory system is possible, where different composite memory devices have different types of discrete memory devices. For example, some composite memory devices include asynchronous NAND flash memory devices while others can include NOR flash memory devices. In such an alternate embodiment, all the composite memory devices follow the same global format, but internally, each composite memory device has its bridge device **200** designed to convert the global format memory control signals to the local format memory control signals corresponding to the NOR flash memory devices or NAND flash memory devices.

[0069] In yet other embodiments, a single composite memory device could have different types of discrete memory devices. For example, a single composite memory device could include two asynchronous NAND flash memory devices and two NOR flash memory devices. This "mixed" or "heterogeneous" composite memory device can follow the same global format described earlier, but internally, its bridge device can be designed to convert the global format memory control signals to the local format memory control signals corresponding to the NAND flash memory devices and the NOR flash memory devices.

[0070] Such a bridge device can include one dedicated format converter for each of the NAND flash memory device and the NOR flash memory device, which can be selected by previously described address information provided in the global command. As described with respect to Figure 3B, the address header **114** includes addressing information used at the system level and the composite memory device level. This additional addressing information includes a global device address (GDA) **116** for selecting a composite memory device to execute an op code in the memory command, and a local device address (LDA) **118** for selecting a particular discrete device within the selected composite memory device to execute the op code. The bridge device can have a selector that uses LDA **118** to determine which of the two format converters the global command should be routed to.

[0071] In an alternate embodiment of memory system **500**, composite memory devices can be used in a multi-drop configured memory system, such as the multi-drop memory system shown in Figure 1A. In this embodiment, each composite memory device is connected in parallel to each other and the memory controller via a single channel, such as channel **18** of Figure 1A. Accordingly, the bridge device of each composite memory device is configured to

receive commands and data through data input/output ports, such as data input/output ports I/O[n] of Figure 1B, while providing read data through the same data input/output ports. In one example, the bridge device of each composite memory device is configured to receive asynchronous control signals or synchronous control signals. For the synchronous control signals, the memory controller provides a source synchronous clock signal that is received by the bridge devices of each composite memory device. In an example of the present embodiment, the bridge devices are configured to receive ONFi standard commands, which can be converted by the bridge devices into a format compatible with the discrete memory devices.

[0072] To improve overall read and write performance of the composite memory device relative to the discrete memory devices, the bridge device is configured to receive write data and to provide read data at a frequency greater than the maximum rated frequency of the discrete memory devices. However, depending on the discrete memory devices selected for use within the composite memory device, they may not be able to provide its read data fast enough to the bridge device in real time so that the bridge device can output the read data at its higher data rate. Similarly, while write data can be provided to the bridge device at high speed, the discrete memory devices may have write speeds that are too slow. Therefore to compensate for this mismatch in speed, the bridge device includes virtual page buffers to temporarily store at least a portion of a page of data read from the page buffer of a discrete memory device, or to be written to the page buffer of a discrete memory device. According to the present embodiments, these virtual page buffers include memory for storing either read data from the discrete memory devices or write data to be written to the discrete memory devices. In the embodiment of Figure 4 for example, data format converter **210** includes such memory, which can be a known memory such as SRAM or DRAM memory for example. Further details of the virtual page buffer are described with reference to the embodiment shown in Figure 8.

[0073] Figure 8 is a block diagram of a composite memory device **600** illustrating the relationship between page buffers of four NAND flash memory devices and the memory of a bridge device. Composite memory device **600** is similar to composite memory device **100** shown in Figure 3A, and includes four NAND flash memory devices **602** in the example embodiment of Figure 8, and a bridge device **604**. The bridge device **604** is shown as a simplified version of bridge device **400** of Figure 4, where only the memory **606** is shown.

The other components of bridge device **400** are omitted from Figure 8, but should be understood to be present in order to ensure proper operation of bridge device **600**. As will be discussed later, memory **606** is logically organized into groups that correspond with the page buffer of each of the four NAND flash memory device **602**.

[0074] Each NAND flash memory device **602** has a memory array organized as two planes **608** and **610**, labeled “Plane 0” and “Plane 1” respectively. While not shown, row circuits drive wordlines that extend horizontally through each of planes **608** and **610**, and page buffers **612** and **614** which may include column access and sense circuits, are connected to bitlines that extend vertically through each of planes **608** and **610**. The purpose and function of these circuits are well known to those skilled in the art. For any read or write operation, one logical wordline is driven across both planes **608** and **610**, meaning that one row address drives the same physical wordline in both planes **608** and **610**. In a read operation, the data stored in the memory cells connected to the selected logical wordline are sensed and stored in page buffers **612** and **614**. Similarly, write data is stored in page buffers **612** and **614** for programming to the memory cells connected to the selected logical wordline.

[0075] Memory **606** of bridge device **604** is divided into logical or physical sub-memories **616** each having at least the same storage capacity of a page buffer **612** or **614**. A logical sub-memory can be an allocated address space in a physical block of memory while a physical sub-memory is a distinctly formed memory having a fixed address space. The sub-memories **616** are grouped into memory banks **618**, labeled Bank0 to Bank3, where the sub-memories **616** of a memory bank **618** are associated with only the page buffers of one NAND flash memory device **602**. In otherwords, sub-memories **616** of a memory bank **618** are dedicated to respective page buffers **612** and **614** of one NAND flash memory device **602**. During a read operation, read data in page buffers **612** and **614** are transferred to sub-memories **616** of the corresponding memory bank **618**. During a program operation, write data stored in sub-memories **616** of a memory bank **618** is transferred to the page buffers **612** and **614** of a corresponding NAND flash memory device **602**. It is noted that NAND flash memory device **602** can have a single plane, or more than two planes, each with corresponding page buffers. Therefore, memory **606** would be correspondingly organized to have sub-memories dedicated to each page buffer.

[0076] The present example of Figure 8 has NAND flash devices **602** with at total of 8KB of page buffer space, organized as two separate 4KB page buffers. Each separate 4KB page

buffer is coupled to the bitlines of a respective plane, such as plane **608** or plane **610** for example. Those skilled in the art understand that page buffer sizes have gradually increased as the overall capacity of NAND flash memory devices has increased, thus future NAND flash devices may have even larger page buffers. The larger page buffers allow for faster overall read and program operations because the core read and program times of the NAND flash memory device is substantially constant, and independent of the page buffer size which is well known to persons skilled in the art. When compared to a page buffer of half the size, a larger page buffer enables a relatively constant burst read of twice as much read data before another core read operation is needed to access another page of data stored in a different row of the memory array. Similarly, twice as much write data can be programmed to the memory array at the same time before another page of write data needs to be loaded into the page buffer. Therefore, larger page buffers are suited for multimedia applications where music or video data can be several pages in size.

[0077] In the composite memory device **600** of Figure 8, the total core read time includes the NAND flash memory device core read time, earlier referred to as Tr, plus a transfer time Ttr. The transfer time Ttr is the time required for the NAND flash memory device to output, or read out, the contents of the page buffers **612** and **614** so that they can be written to corresponding sub-memories **616** of one memory bank **618**. The total core program time includes a program transfer time Ttp plus the NAND flash memory device core program time earlier referred to as Tpgm. The program transfer time Ttp is the time required for the bridge device **608** to output, or read out, the contents of sub-memories **616** of one memory bank **618** so that they can be loaded into corresponding page buffers **612** and **614** of a NAND flash memory device **602** prior to a programming operation. For multimedia applications, the data can be stored across different NAND flash memory devices and concurrently operated to mask core operations of one NAND flash memory device while data corresponding to another NAND flash memory device **602** is being output by bridge device **604**. For example, during burst read out of data from one memory bank **618**, a core read operation may already be in progress for loading the sub-memories **616** of another memory bank **618** with data from another NAND flash memory device **602**.

[0078] There may be applications where the file sizes are smaller than a full page size of a NAND flash memory device page buffer. Such files include text files and other similar types of data files that are commonly used in personal computer desktop applications. Users

typically copy such files to Universal Serial Bus (USB) non-volatile storage drives which commonly use NAND flash memory. Another emerging application are solid state drives (SSD) which can replace magnetic hard disk drives (HDD), but use NAND flash memory or other non-volatile memory to store data. The composite memory device read and program sequence is the same as previously described, with the following differences. This example assumes that the desired data is less than a full page size, and is stored in a page with other data. For a read operation, after all the page buffer data has been transferred from page buffers **612** and **614** of a selected NAND flash memory device **602** to corresponding sub-memories **616**, a column address is used to define the locations of the first and last bit positions of the desired data stored in sub-memories **616** of the memory bank **618**. Then only the first, last and the intervening bits of data are read out from sub-memories **616** of bridge device **604**.

[0079] The transfer time Ttr in such scenarios may not be acceptable for certain applications due to its significant contribution to the total core read time of the composite memory device. Such applications include SSD where read operations should be performed as fast as possible. While the core read time Tr for NAND flash memory devices remains constant for any page buffer size, the transfer time Ttr for transferring the entire contents to the sub-memories **616** is directly dependent on the page buffer size.

[0080] According to a present embodiment, the transfer time Ttr of the composite memory device can be minimized by configuring the sub-memories **616** of a memory bank **618** to have a virtual maximum page size, referred to as a virtual page size, that is less than the maximum physical size of the page buffer of a NAND flash memory device within the composite memory device. Based on the virtual page size configuration for a particular memory bank **618**, the bridge device **604** issues read commands where only a segment of data corresponding to the virtual page size stored in the page buffer is transferred to the corresponding sub-memories **616**. This segment of the page buffer is referred to as a page segment.

[0081] Figures 9A to 9C illustrates how data corresponding to a set virtual page size is read from a discrete memory device, such as a flash memory device, is read out of a composite memory device, according to a present embodiment. Figures 9A to 9C shows a composite memory device **700** having one fully shown first NAND flash memory device **702**, a portion of a second NAND flash memory device **704**, and a portion of bridge device **706**. The NAND

flash memory devices of this example have a single plane **708** having bitlines connected to a single page buffer **710**. The shown portion of bridge device **706** includes a first sub-memory **712**, a second sub-memory **714**, and a bridge device input/output interface **716**. First sub-memory **712** corresponds to a first bank, which is associated with first NAND flash memory device **702** while second sub-memory **714** corresponds to a second bank, which is associated with second NAND flash memory device **704**. For the purpose of explaining a read operation in the present example, it is assumed that data from first NAND flash memory device **702** is to be accessed, and the virtual page size of the first bank (first sub-memory **712**) has been configured to be smaller than the maximum physical size of page buffer **710**.

[0082] Starting in Figure 9A, it is assumed that bridge device **706** has received global memory control signals representing a read operation to access data stored in first NAND flash memory device **702**, and has encoded and provided the appropriate local memory control signals to first NAND flash memory device **702**. In response to the local memory control signals corresponding to a read command, first NAND flash memory device **702** activates a row or wordline **718** selected by address information in the local memory control signals. Proceeding to Figure 9B, when the wordline **718** is activated, or driven to a voltage level effective for accessing the stored data of the memory cells connected to it, a current or voltage generated on the bitlines connected to each accessed memory cell is sensed by sense circuitry within page buffer **710**. Thus the data states of the accessed memory cells are stored in page buffer **710**. In Figure 9C, NAND flash memory device **702** outputs data stored within a specific range of bit positions of page buffer **710** to bridge device **706**, and in particular to first sub-memory **712**. This data output process is executed at up to the maximum rated speed or data rate for NAND flash memory device **702**.

[0083] In this example NAND flash memory device **702**, a burst read command including column addresses corresponding to this specific range of bit positions is provided by bridge device **706** automatically once NAND flash memory device **702** reports or signals to bridge device **706** that the read data from the selected row **718** is stored in page buffer **710**, usually by way of a ready/busy signal. The column addresses are determined based on the configured virtual page size for first sub-memory **712**. The data stored in first sub-memory **712** is then output through output data ports of composite memory device **700** via bridge device input/output interface **716** at the higher speed or data rate. In the present

embodiments, an output data port includes pins or leads corresponding to the Q[n] data output port previously shown in Table 2.

[0084] Therefore it can be seen that by setting a virtual page size for first sub-memory **712** to be less than the maximum physical size of page buffer **710**, only a correspondingly sized page segment of data from page buffer **710** is output to first sub-memory **712**. This page segment includes the specific range of bit positions, each of which are addressable by a column address. As will be discussed later, the page segment is addressable. Accordingly the transfer time Ttr for the NAND flash memory device **702** to output this page segment of data from page buffer **710** can be significantly reduced relative to the situation where all the data of page buffer **710** is transferred to first sub-memory **712**.

[0085] The above mentioned example illustrates how the transfer time Ttr can be minimized. Setting the virtual page size to be less than the maximum physical size of page buffer **710** provides the same performance advantage during write operations. In a write operation, the sequence shown in Figures 9A to 9C is effectively reversed. For example, write data is received by bridge device input/output interface **716** and written to a sub-memory such as first sub-memory **712**. This write data has a size matching the preset virtual page size, which is then transferred to page buffer **710**. The time required for transferring this write data from the bridge device **706** to the page buffer **710** is the transfer time Ttr, which depends on the size of the write data and the operating frequency of the NAND flash device **702**. The write data is stored within specific bit positions of page buffer **710**, called a page segment, and the core programming operation of NAND flash device **702** is initiated through activation of a selected row **718** and the application of the required programming voltages to the bitlines in response to the write data stored in page buffer **710**. Therefore, by shortening the transfer time Ttr during a write operation, the overall write time of the memory system is reduced.

[0086] According to the present embodiments, first sub-memory **712** of the bridge device **706** can be configured via a recognized command to have any one of preset virtual page sizes. Once the virtual page size of first sub-memory **712** is configured, then the page buffer **710** of the corresponding NAND flash memory device is logically subdivided into equal sized page segments corresponding to the configured virtual page size. Figures 10A to 10D are schematic representations of a NAND flash memory device page buffer **750** with differently sized page segments based on a configured virtual page size. It is noted that the page segments represent a virtual address space in page buffer **750**. In the present examples of

Figures 10A to 10D, the NAND flash page buffer, and the sub-memory of the bridge device, both have a maximum 4K physical size. In Figure 10A, the virtual page size (VPS) is set to the maximum, or full 4K size such that there is only one page segment **752**. In Figure 10B, the VPS is set to 2K, resulting in two 2K page segments **754**. In Figure 10C, the VPS is set to 1K, resulting in four 1K page segments **756**. In Figure 10D, the VPS is set to 612 bytes (B), resulting in eight page segments **758** that are 612B in size. Those skilled in the art will understand that even smaller sized VPS and corresponding page segments are possible, and that the total number of page segments depends on the maximum size of the NAND flash memory device page buffer **750**.

[0087] As previously discussed for the present embodiments, after the page buffer **750** of the NAND flash memory device has been loaded with data for a read operation, only page segment of the page buffer **750** is output to the bridge device. The desired data may be stored in one particular page segment of page buffer **750**. Therefore each page segment is addressable by a virtual page address provided in the global command to the bridge device. For example, two address bits are used to select one of four page segments **756** in Figure 10C. Once selected, the desired data may not occupy all bit positions in the selected page segment of page buffer **750**. Thus a virtual column address is used to select the first bit position within the selected page segment where read data is to be read out, typically in a burst read operation. Table 3 below summarizes example addressing schemes based on the example page segments shown in Figures 10A to 10D.

[0088] Table 3

Virtual Page Size Configuration	# of Page Segments	Bits for addressing Page Segments (VPA)	Bits for addressing bit position in each Page Segment (VCA)
4096B	1	N/A	12
2048B	2	1	11
1024B	4	2	10
612B	8	3	9

[0089] Example addressing schemes are shown in Table 3 by example, but those skilled in the art should understand that different addressing schemes can be used depending on the size of the page buffer of the NAND flash memory device. As shown in Table 3, each addressing scheme includes a first number of bits for addressing two or more page segments, and a second number of bits for addressing a column in the selected page segment. The first number of bits is referred to as a virtual page address (VPA) and the second number of bits is referred to as a virtual column address (VCA). The virtual page address and the virtual column address are collectively referred to simply as a virtual address. In the present embodiments, the VPS configuration of each sub-memory or bank of sub-memories is known to the memory controller or other host system that requests read data and provides write data to the composite memory device. Therefore a virtual address for reading a page segment from the page buffer of the NAND flash memory device is provided in the global command to the composite memory device with a corresponding addressing scheme for accessing a particular NAND flash memory device therein. The possible addressing schemes, including those shown in Table 3, address a virtual or logical address space of the page buffer. While this logical address space has been described as bit positions of page segments in page buffers **750** of Figures 10A to 10D, the actual page buffers are addressed with real physical addresses. The mapping of logical addresses to physical addresses is well known in the art.

[0090] Following is a discussion of the methods for reading data from a discrete memory device, and to write data to a discrete memory device, according to embodiments of the present invention. Figure 11 is a flow chart outlining a method for reading data from a composite memory device according to a present embodiment, while Figure 12 is a flow chart outlining a method for writing data to a composite memory device.

[0091] In the presently described method of Figure 11, it is assumed that one particular discrete memory device of the composite memory device is selected for reading data therefrom. It is further assumed that the selected discrete memory device has been configured to have a specific virtual page size configuration. The method starts at step **800** where the bridge device receives a global page read command to read data from a specific virtual page (VP) from a physical page (PP) of the selected discrete memory device. In the present example, the PP=A and the VP=X, where A represents a physical address of a page of memory and X represents a specific virtual page all the virtual pages that make up the

physical page. The bridge device converts the global read command into a local read command, and issues it to the selected discrete memory device. The discrete memory device receives the local page read command at PP=A, and initiates the internal core read operation. At step **802**, if the current read operation is directed to a new PP then the method proceeds to step **804**. At step **804**, the bridge device clears its virtual page buffers, which can include setting all their states to the logic "1" or "0" levels. At step **806** the bridge device then waits for the internal core read time Tr specified for the discrete memory device to load its page buffers with the data at PP=A. Proceeding to step **808** once the core read time Tr has passed, the bridge device issues a local burst data read command to the discrete memory device. In response, the discrete memory device outputs the data stored in a column address range corresponding to VP=X to the bridge device at step **808**, which stores this data into its virtual page buffers. In step **808** the bridge device sets a READY flag to indicate to the host system or memory controller that the data stored in the virtual page buffers can now be read out.

[0092] Returning to step **802**, if the current read operation is directed to the same PP of the previous read operation, ie. PP=A, then the method skips to step **808** where the bridge device issues a burst data read command to the discrete memory device. In response the discrete memory device outputs VP=Y. For example, if this subsequent read operation is for PP=A and VP=Y, where Y represents a specific virtual page different from X, then no discrete memory device core read operation is required since its page buffers already store the entire data contents of P=A, which includes the data corresponding to both VP=X and VP=Y. In this situation, the discrete memory device only needs to output the data stored in a column address range corresponding to VP=Y, which is received and stored in the virtual page buffers of by the bridge device at step **808**. In response to the set READY flag, the memory controller can issue a global burst data read command to output the data stored in the virtual page buffers.

[0093] In the read method embodiment described above, the reading of VP=X and VP=Y from PP=A can occur in sequence. In particular, steps **800** to **810** are executed for reading out VP=X from the composite memory device, followed by another read operation involving only steps **800**, **802**, **808** and **810** for reading VP=Y. According to an alternate embodiment of the read method shown in Figure 11, the second page read command to VP=Y can be issued before the first burst data read command. In this way the transfer of the data

corresponding to VP=Y between the discrete memory device and the bridge chip can occur at the same time as data corresponding to VP=X is outputted from the bridge device.

[0094] The method for writing data to a composite memory device according to a present embodiment is now described. In the method of Figure 12, it is assumed that one particular discrete memory device of the composite memory device is selected for writing data thereto. It is further assumed that the discrete memory device has been configured to have a specific virtual page size configuration. The programming method starts at step **900** where a global page program command is received by the bridge device. In this example the data is to be written to PP=A, and the data corresponds to VP=X. Upon receipt of the page program command at step 900, the virtual page buffers of the bridge device are loaded with the data to be programmed (VP=X). At step **902** the bridge device issues a burst data load start command to the discrete memory device and then transfers VP=X to the discrete memory device. Following at step **904**, if data corresponding to another virtual page of PP=A is to be written, then the method proceeds to step **906** where the bridge device issues another burst data load command to the discrete memory device. This command transfers data corresponding to another virtual page, such as VP=Y, to the discrete memory device. From step **906**, the method loops back to step **904**.

[0095] If there are no further virtual pages in PP=A to be programmed, then the method proceeds to step **908** where the bridge device issues a program command to the discrete memory device. This initiates core programming operations within the discrete memory device, to program the data such as VP=X and/or VP=Y to PP=A of the discrete memory device. Following at step 910, the bridge device waits for the core programming time Tprog to pass, and then sets the READY flag, which indicates to the memory controller that the program operation for VP=X and VP=Y to PP=A is complete.

[0096] The previously described embodiments of the composite memory device show how discrete memory devices responsive to memory control signals of one format can be controlled using global memory control signals having a second and different format. According to an alternate embodiment, the bridge device **200** can be designed to receive global memory control signals having one format, for providing local memory control signals having the same format to the discrete memory devices. In other words, such a composite memory device is configured to receive memory control signals that are used to control the discrete memory devices. Such a configuration allows multiple discrete memory devices to

each function as a memory bank operating independently of the other discrete memory device in the composite memory device. Therefore, each discrete memory device can receive its commands from the bridge device **200**, and proceed to execute operations substantially in parallel with each other. This is also referred to as concurrent operations. The design of bridge device **200** is therefore simplified, as no command conversion circuitry is required.

[0097] The previously described embodiments illustrate how discrete memory devices in a composite memory device can respond to a foreign command format. This is achieved through the bridge device that converts the received global command into a native command format compatible with the discrete memory devices. By example, a serial command format can be converted into an asynchronous NAND flash format. The embodiments are not limited to these two formats, as any pair of command formats can be converted from one to the other.

[0098] In the preceding description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the embodiments of the invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the invention. In other instances, well-known electrical structures and circuits are shown in block diagram form in order not to obscure the invention.

[0099] It will be understood that when an element is herein referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is herein referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (i.e., "between" versus "directly between", "adjacent" versus "directly adjacent", etc.).

[00100] Figures in this application are not necessarily to scale. For example, in Figure 5 the relative sizes of the bridge device **302** and discrete memory devices **304** are not to scale, and a fabricated bridge device is orders of magnitude smaller in area than the discrete memory devices **304**.

[00101] Certain adaptations and modifications of the described embodiments can be made. Therefore, the above-discussed embodiments are considered to be illustrative and not restrictive.

What is claimed is:

1. A composite memory device comprising:

at least one discrete memory device for executing memory operations in response to local memory control signals having a first format, and

a bridge device for receiving global memory control signals having a second format and for converting the global memory control signals into the local memory control signals.

2. The composite memory device of claim 1, wherein the bridge device includes

a local input/output port connected to the at least one discrete memory device,

a global input port for receiving the global memory control signals, and

a global output port for providing one of the global memory control signals and read data from the at least one discrete memory device.

3. The composite memory device of claim 2, wherein the at least one discrete memory device and the bridge device are encapsulated in a package.

4. The composite memory device of claim 3, wherein the global input port and the global output port are electrically coupled to leads of the package.

5. The composite memory device of claim 4, wherein electrical conductors couple the local input/output port to the at least one discrete memory device.

6. The composite memory device of claim 4, wherein the local input/output port is wirelessly coupled to the at least one discrete memory device.

7. The composite memory device of claim 2, wherein the at least one discrete memory device is a packaged memory device and the bridge device is a packaged bridge device.

8. The composite memory device of claim 7, wherein the packaged memory device and the packaged bridge device are mounted onto a printed circuit board.

9. The composite memory device of claim 8, wherein the local input/output port, the global input port and the global output port are electrically coupled to leads of the packaged bridge device.

10. The composite memory device of claim 8, wherein the packaged memory device has memory leads electrically connected to the local input/output port of the packaged bridge device.

11. The composite memory device of claim 1, wherein the global memory control signals are received in a global command, the global command further including an address header.

12. The composite memory device of claim 11, wherein the address header includes a global device address corresponding to a selected composite memory device and a local device address corresponding to a selected discrete memory device of the at least one discrete memory device in the selected composite memory device.

13. The composite memory device of claim 1, wherein the first format includes a serial data interface format and the second format includes an asynchronous flash memory format.

14. The composite memory device of claim 1, wherein the first format includes an ONFi specification interface format and the second format includes an asynchronous flash memory format.

15. A memory system comprising:

a memory controller for providing a global command corresponding to a memory operation; and

n composite memory devices connected serially with each other and the memory controller in a ring topology configuration, each of the n composite memory devices having m discrete memory devices and a bridge device, the bridge device of a selected composite

memory device of the n composite memory devices receiving the global command for providing local memory control signals corresponding to the memory operation to a selected discrete memory device of the m discrete memory devices, where n and m are integer values greater than 0.

16. The memory system of claim 15, wherein each of the n composite memory devices is a system in package (SIP)

17. The memory system of claim 15, wherein each of the n composite memory devices is a printed circuit board (PCB) and the m discrete memory devices and the bridge device are packaged devices having package leads connected to conductive tracks in the PCB.

18. The memory system of claim 15, wherein the global command includes global memory control signals having a first format, and an address header for addressing the selected composite memory device and the selected discrete memory device.

19. The memory system of claim 18, wherein the address header includes a global device address corresponding to the selected composite memory device and a local device address corresponding to the selected discrete memory device.

20. The memory system of claim 19, wherein the bridge device includes

a bridge device input/output interface having an input port for receiving the global command and an output port for providing the global command, the bridge device comparing the global device address to a predetermined address stored in a global device address register;

a format conversion circuit for converting the global memory control signals of the global command from a first format to the local memory control signals having a second format when the global device address matches the predetermined address; and,

a memory device interface for providing the local memory control signals to the selected discrete memory device in response to the local device address.

21. The memory system of claim 20, wherein the format conversion circuit comprises:

a command format converter for converting the global memory control signals in the first format to the local memory control signals having the second format; and

a data format converter for converting read data from the selected discrete memory device from the second format to the first format.

22. The memory system of claim 20, wherein the global command further includes write data, and the format conversion circuit comprises:

a command format converter for converting the global memory control signals in the first format to the local memory control signals having the second format; and

a data format converter for converting the write data from the first format to the second format.

23. The memory system of claim 20, wherein the m discrete memory devices include discrete memory devices of different types, and the bridge device includes a number of format conversion circuits corresponding to each of the different types of discrete memory devices.

24. A composite memory device package comprising:

at least one discrete memory device for executing memory operations in response to local memory control signals having a first format; and

a bridge device for receiving global memory control signals having a second format and for converting the global memory control signals into the local memory control signals, the bridge device and the at least one discrete memory device being positioned in a stacked manner in relation to each other.

25. The composite memory device package of claim 24, wherein the bridge device is stacked on top of the at least one discrete memory device.

26. The composite memory device package of claim 24, wherein the composite memory device package includes a plurality of discrete memory devices, each of the plurality of discrete memory devices being stacked upon each other in a staggered step pattern to expose bond pads of each of the plurality of discrete memory devices.

27. The composite memory device package of claim 26, wherein each of the plurality of discrete memory devices have their respective bond pads facing in an upward direction relative to a substrate of the composite memory device package.

28. The composite memory device package of claim 27, wherein the bridge device includes:

a memory device interface having a local input/output port connected to each of the plurality of discrete memory devices; and,

a bridge device input/output interface having:

a global input port to receive the global memory control signals, and

a global output port to provide one of the global memory control signals and read data from the at least one of the plurality of discrete memory devices.

29. The composite memory device package of claim 28, wherein local communication terminals electrically couple input/output ports of each of the plurality of the discrete memory devices to the local input/output port of the memory device interface of the bridge device.

30. The composite memory device package of claim 28, wherein a channel of local communication terminals electrically couple a clock signal from a clock port of the memory device interface and a plurality of parallel data input/output ports of the memory device interface to one of the plurality of discrete memory devices.

31. The composite memory device package of claim 30, wherein i channels of local communication terminals are electrically coupled to corresponding i discrete memory devices, where i is an integer value of at least 1.

32. The composite memory device package of claim 30, wherein the channel of local communication terminals is electrically connected in parallel to each of the plurality of discrete memory devices.

33. The composite memory device package of claim 32, wherein the channel includes pre-formed conductive tracks in a substrate of the composite memory device package.

34. The composite memory device package of claim 28, wherein local communication terminals wirelessly couple input/output ports of each of the plurality of the discrete memory devices to the local input/output port of the memory device interface of the bridge device.

35. The composite memory device package of claim 28, wherein global communication terminals electrically couple the global input port and the global output port of the bridge device input/output interface to leads of the composite memory device package.

36. The composite memory device package of claim 28, wherein global communication terminals wirelessly couple the global input port and the global output port of the bridge device input/output interface to leads of the composite memory device package.

37. The composite memory device package of claim 28, wherein the local input/output port, the global input port and the global output port are electrically coupled to leads of the composite memory device package.

38. The composite memory device package of claim 28, wherein the global memory control signals are received in a global command, the global command further including an address header.

39. The composite memory device package of claim 38, wherein the address header includes a global device address corresponding to a selected composite memory device and

a local device address corresponding to a selected discrete memory device of the at least one discrete memory device in the selected composite memory device.

40. The composite memory device package of claim 24, wherein the first format includes a serial data interface format and the second format includes an asynchronous flash memory format.

41. The composite memory device package of claim 24, wherein the first format includes an ONFi specification interface format and the second format includes an asynchronous flash memory format.

42. The composite memory device package of claim 26, wherein the plurality of discrete memory devices are of the same type.

43. The composite memory device package of claim 26, wherein the plurality of discrete memory devices are of different types.

44. The composite memory device package of claim 26, wherein the plurality of discrete memory devices are asynchronous NAND flash memory devices.

45. A memory module comprising:

at least one packaged discrete memory device having memory device leads bonded to conductive tracks of a printed circuit board, the at least one packaged memory device for executing memory operations in response to local memory control signals having a first format; and

a packaged bridge device having bridge device leads bonded to the conductive tracks of the printed circuit board, the at least one packaged bridge device for receiving global memory control signals having a second format and for converting the global memory control signals into the local memory control signals.

46. The memory module of claim 45, wherein the packaged bridge device includes:

a memory device interface having a local input/output port connected to the at least one packaged discrete memory device; and,

a bridge device input/output interface having:

a global input port to receive the global memory control signals, and

a global output port to provide one of the global memory control signals and read data from the at least one discrete memory device.

47. The memory module of claim 46, wherein local communication terminals electrically couple input/output ports of the at least one packaged discrete memory device to the local input/output port of the memory device interface of the packaged bridge device via pre-formed conductive tracks of the printed circuit board.

48. The memory module of claim 46, wherein global communication terminals electrically couple the global input port and the global output port of the bridge device input/output interface to pre-formed conductive tracks of the printed circuit board.

49. The memory module of claim 46, wherein a channel of local communication terminals electrically couple a clock signal from a clock port of the memory device interface and a plurality of parallel data input/output ports of the memory device interface to one of the plurality of packaged memory devices.

50. The memory module of claim 49, wherein i channels of local communication terminals are electrically coupled to corresponding i packaged memory devices, where i is an integer value of at least 1.

51. The memory module of claim 49, wherein the channel of local communication terminals is electrically connected in parallel to each of the plurality of packaged memory devices.

52. The memory module of claim 51, wherein the channel includes the conductive tracks of the printed circuit board.

53. The memory module of claim 45, wherein the global memory control signals are received in a global command, the global command further including an address header.

54. The memory module of claim 53, wherein the address header includes a global device address corresponding to a selected composite memory device and a local device address corresponding to a selected discrete memory device of the at least one packaged discrete memory device in the selected composite memory device.

55. The memory module of claim 45, wherein the first format includes a serial data interface format and the second format includes an asynchronous flash memory format.

56. The memory module of claim 45, wherein the first format includes an ONFi specification interface format and the second format includes an asynchronous flash memory format.

57. The memory module of claim 45, wherein the memory module includes a plurality of packaged discrete memory devices and the plurality of the packaged memory devices are of the same type.

58. The composite memory device package of claim 45, wherein the memory module includes a plurality of packaged discrete memory devices and the plurality of the packaged memory devices are of different types.

59. The composite memory device package of 45, wherein the memory module includes plurality of packaged discrete memory devices and the plurality of the packaged memory devices are asynchronous NAND flash memory devices.

60. A bridge device to access a discrete memory device in response to global signals having a global format, the bridge device comprising:

a bridge device input/output interface communicating the global signals having the global format to and from the bridge device; and,

a bridge device memory device interface communicating local signals having a local format between the bridge device and the discrete memory device, the local signals corresponding in function to the global signals and having a local format different from the global format.

61. The bridge device of claim 60, wherein the bridge device memory interface includes a local input/output port connected to the discrete memory device to communicate the local signals.

62. The bridge device of claim 60, wherein the bridge device input/output interface includes a global input port for receiving the global signals, and a global output port for providing one of the global signals and read data from the discrete memory device.

63. The bridge device of claim 60, further comprising:

a format converter to convert the global signals having the global format to the local signals having the local format and to convert the local signals having the local format to the global signals having the global format.

64. The bridge device of claim 63, wherein the global signal includes global commands and global command signals, and the format converter includes a command format converter to convert the global commands and the global command signals in the global signal having the global format to the local format.

65. The bridge device of claim 63, wherein the format converter includes a data format converter to convert data between the global format and the local format.

66. The bridge device of claim 65, wherein the global signals are received in a global command, the global command further including an address header.

67. The bridge device of claim 66, wherein the address header includes a global device address corresponding to a selected composite memory device and a local device address corresponding to a selected discrete memory device of the at least one discrete memory device in the selected composite memory device.

68. The bridge device of claim 60, wherein the global format includes a serial data interface format and the local format includes an asynchronous flash memory format.

69. The bridge device of claim 60, wherein the global format includes an ONFi specification interface format and the local format includes an asynchronous flash memory format.

70. A memory system comprising:

a memory controller for providing a global command corresponding to a memory operation;

n composite memory devices connected in parallel with each other and the memory controller, each of the n composite memory devices having m discrete memory devices and a bridge device, the bridge device of a selected composite memory device of the n composite memory devices receiving the global command for providing local memory control signals corresponding to the memory operation to a selected discrete memory device of the m discrete memory devices, where n and m are integer values greater than 0.

71. The memory system of claim 70, wherein each of the n composite memory devices has a clock port for receiving a clock signal and a plurality of data input/output ports for receiving commands and write data, and for providing read data.

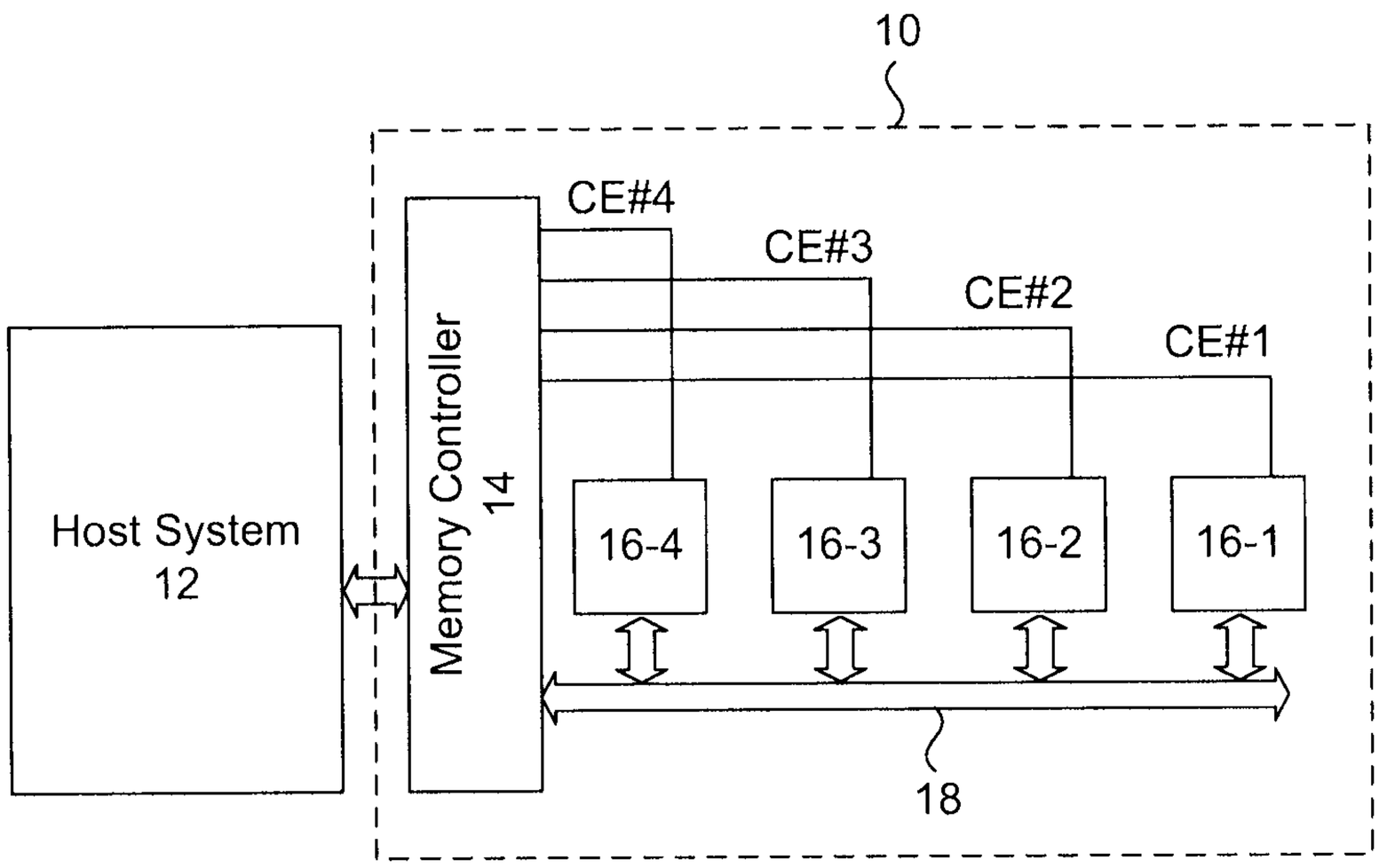
10
Host System
12
Memory Controller
14
CE#4
CE#3
CE#2
CE#1
16-4
16-3
16-2
16-1
18

FIG. 1A

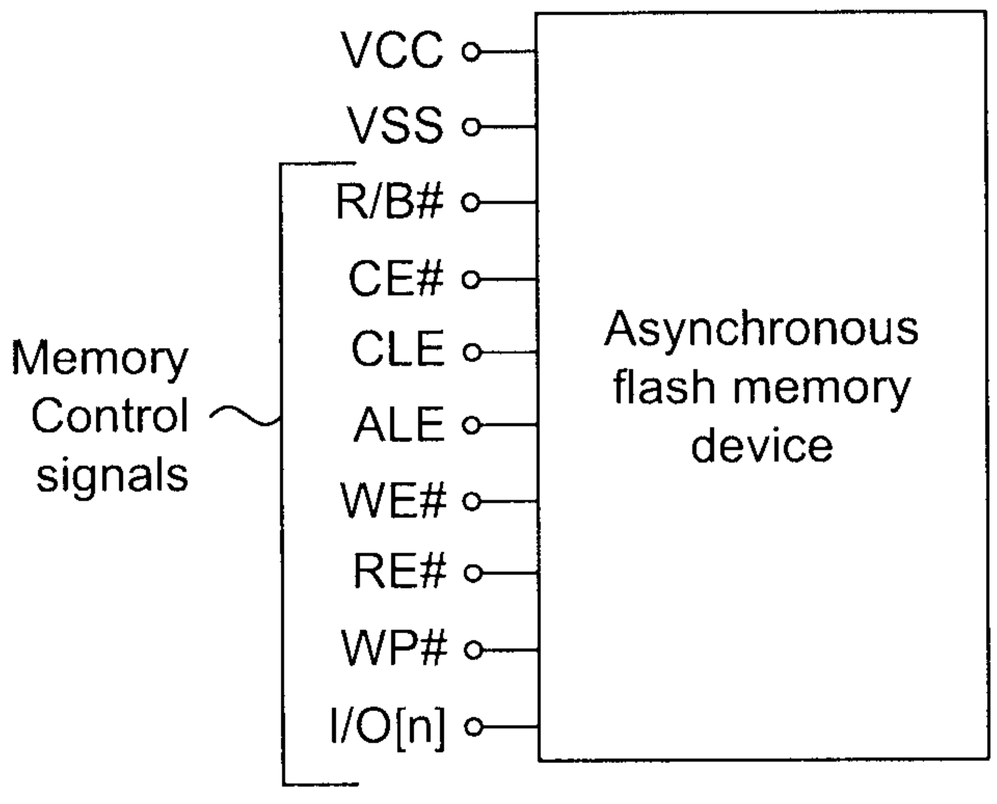
VCC
VSS
R/B#
CE#
CLE
ALE
WE#
RE#
WP#
I/O[n]
Memory
Control
signals
Asynchronous
flash memory
device

FIG. 1B

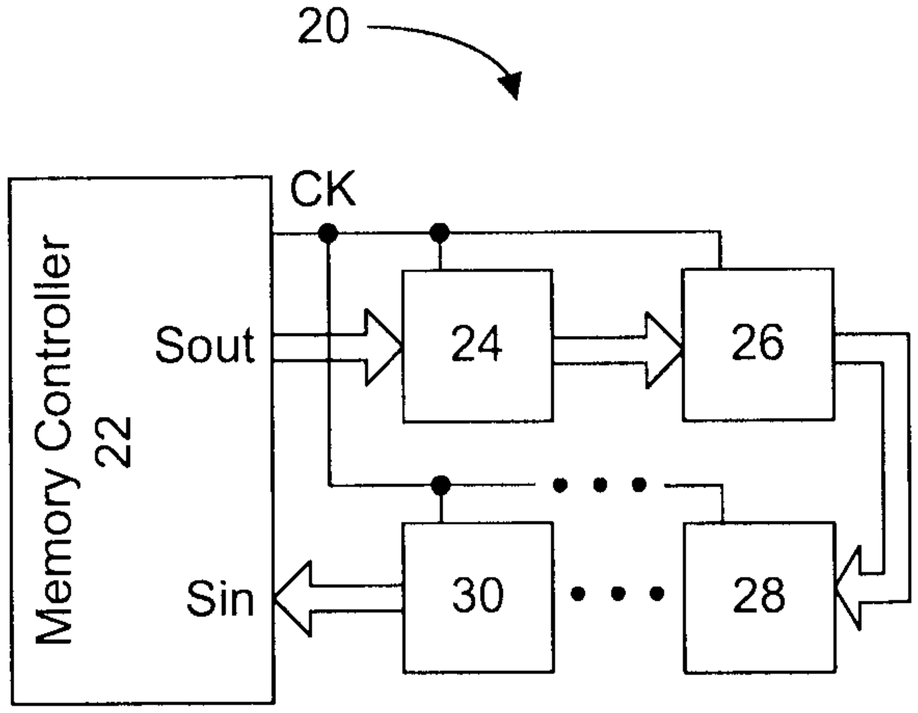
20
Memory Controller
22
CK
Sout
Sin
24
26
30
28

FIG. 2A

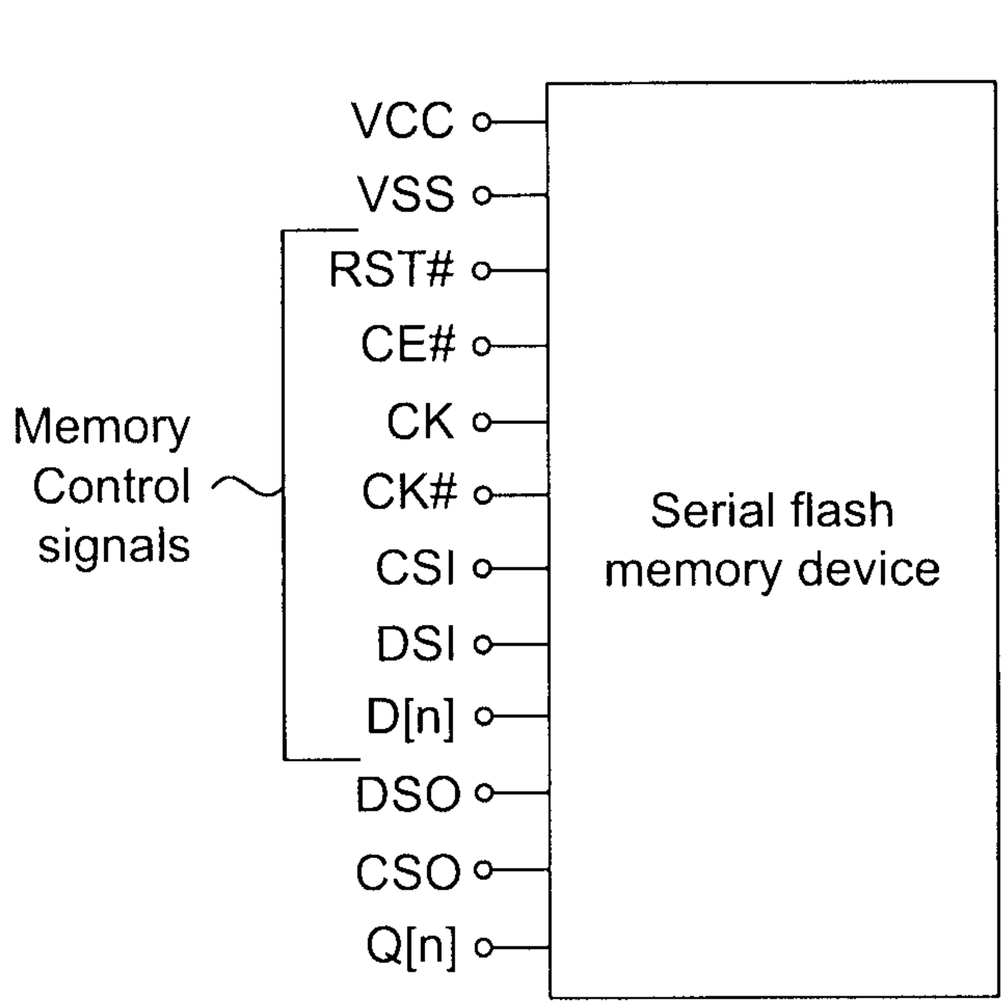
VCC
VSS
RST#
CE#
CK
CK#
CSI
DSI
D[n]
DSO
CSO
Q[n]
Memory
Control
signals
Serial flash
memory device

FIG. 2B

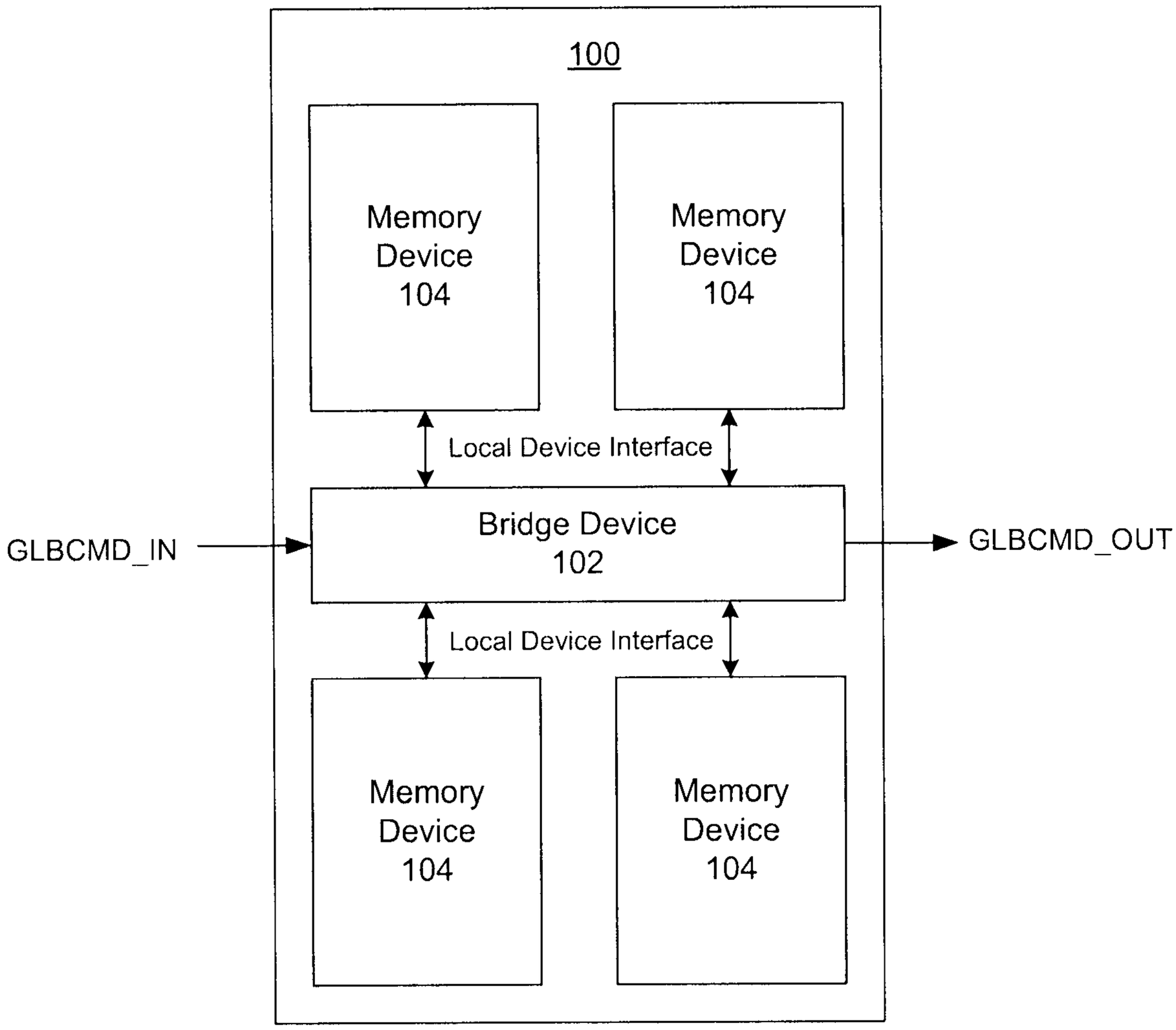
100
Memory Device 104
Memory Device 104
Local Device Interface
GLBCMD_IN
Bridge Device 102
GLBCMD_OUT
Local Device Interface
Memory Device 104
Memory Device 104

FIG. 3A

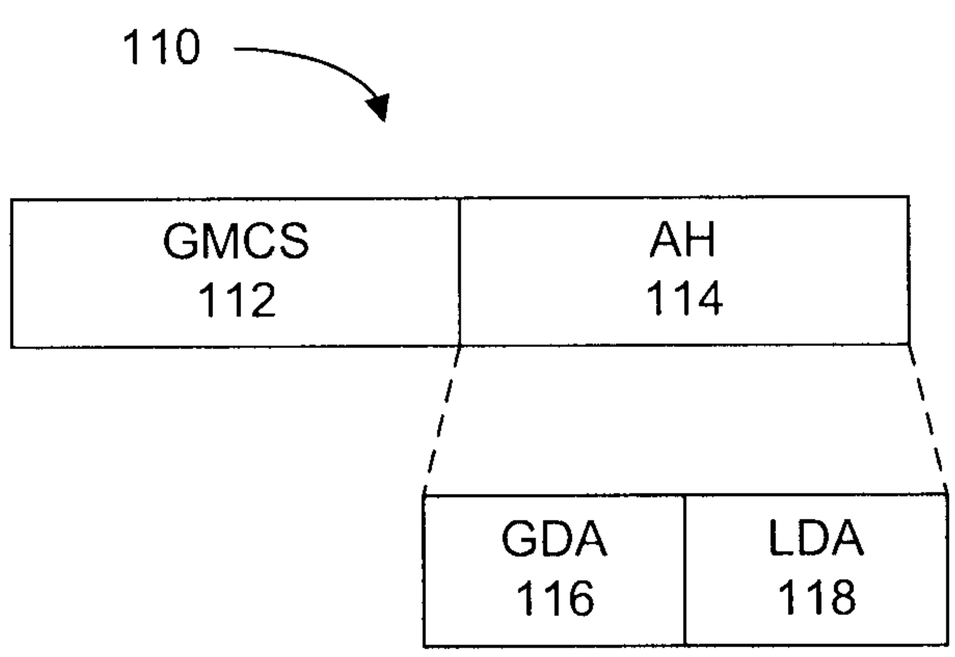
110
GMCS 112
AH 114
GDA 116
LDA 118

FIG. 3B

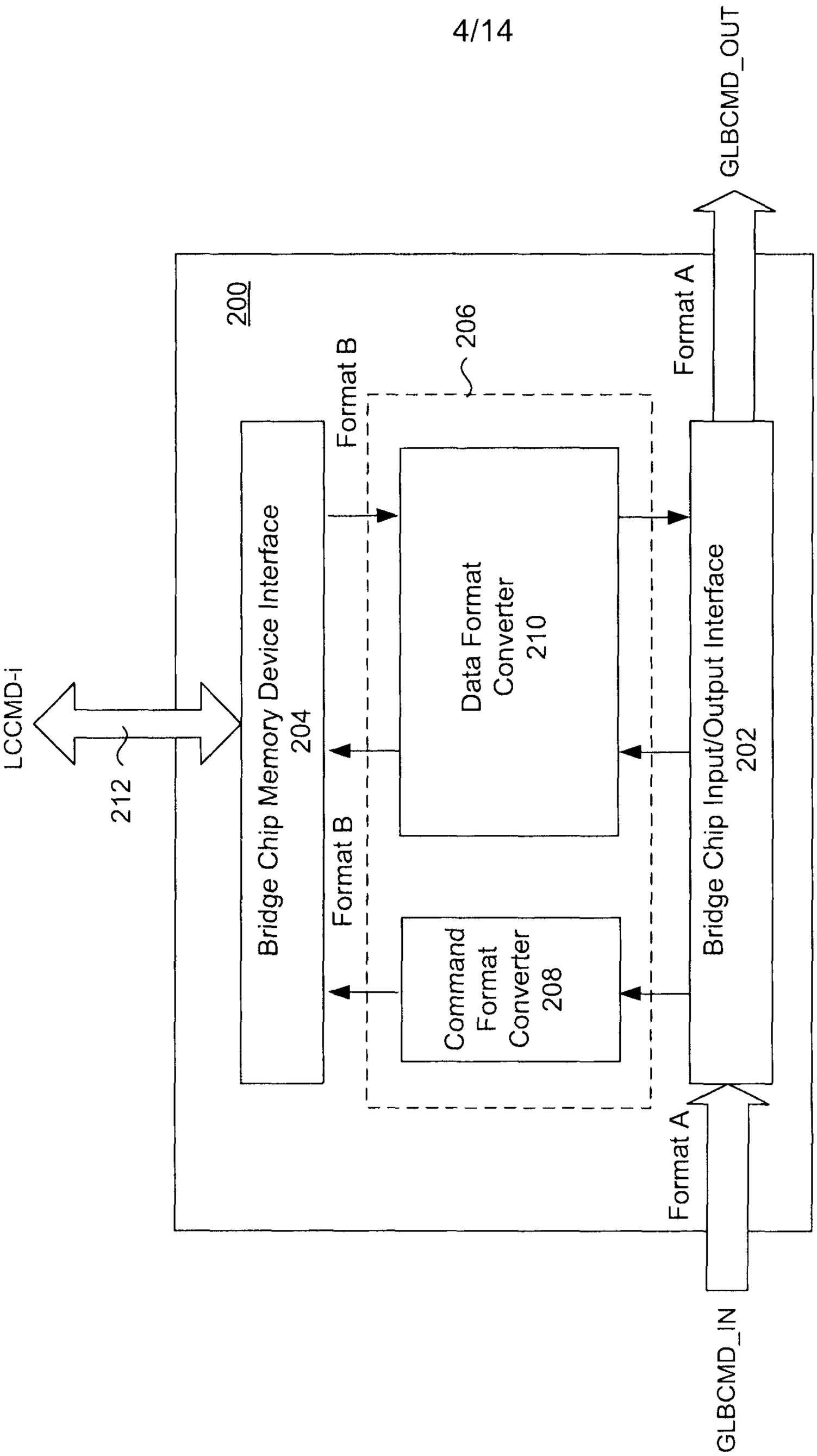
GLBCMD_OUT
200
206
Format A
Format B
LCCMD-i
212
Bridge Chip Memory Device Interface
204
Data Format
Converter
210
Bridge Chip Input/Output Interface
202
Format B
Command
Format
Converter
208
Format A
GLBCMD_IN

FIG. 4

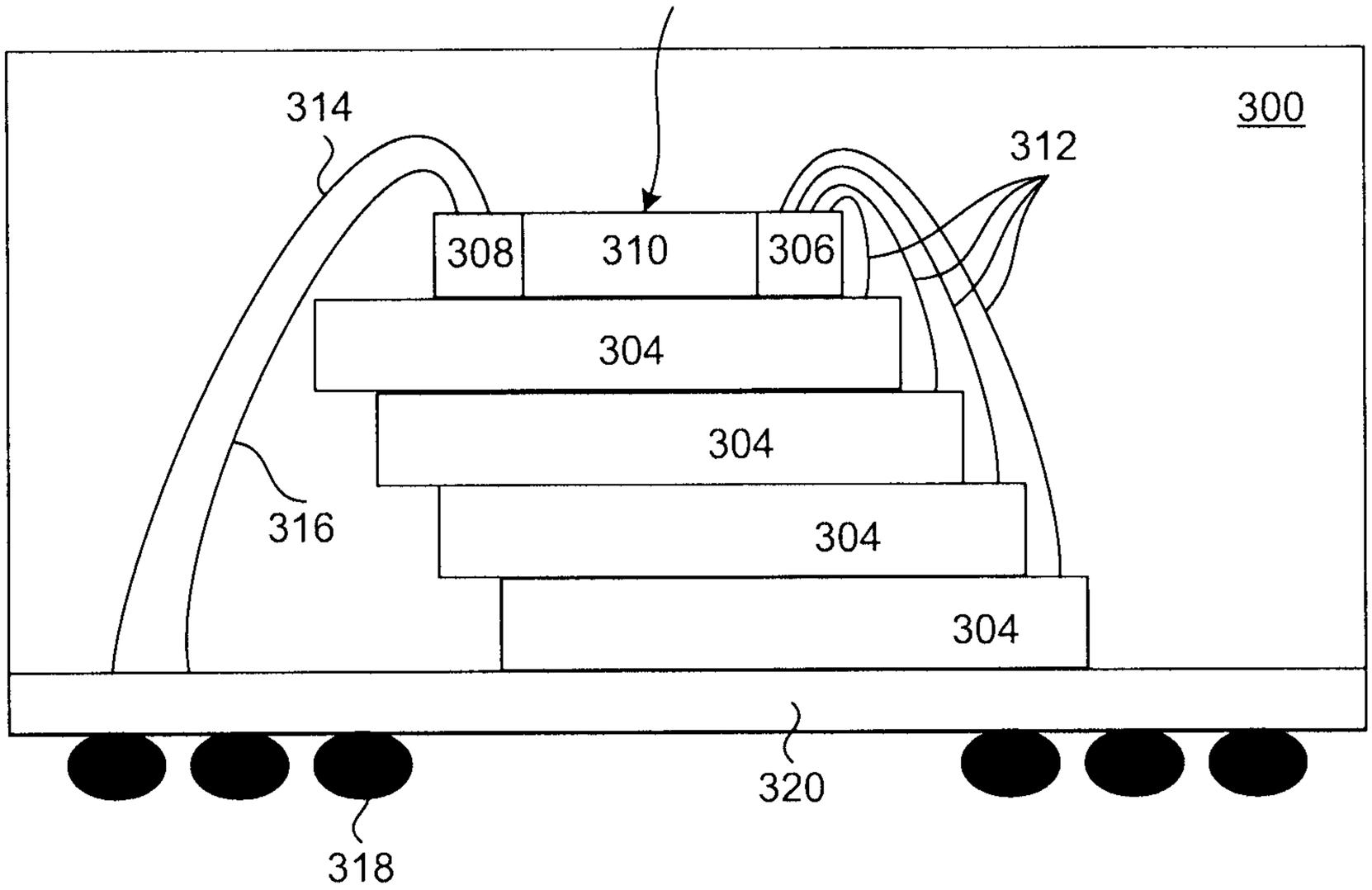
302
314
300
312
308
310
306
304
304
304
316
320
318

FIG. 5A

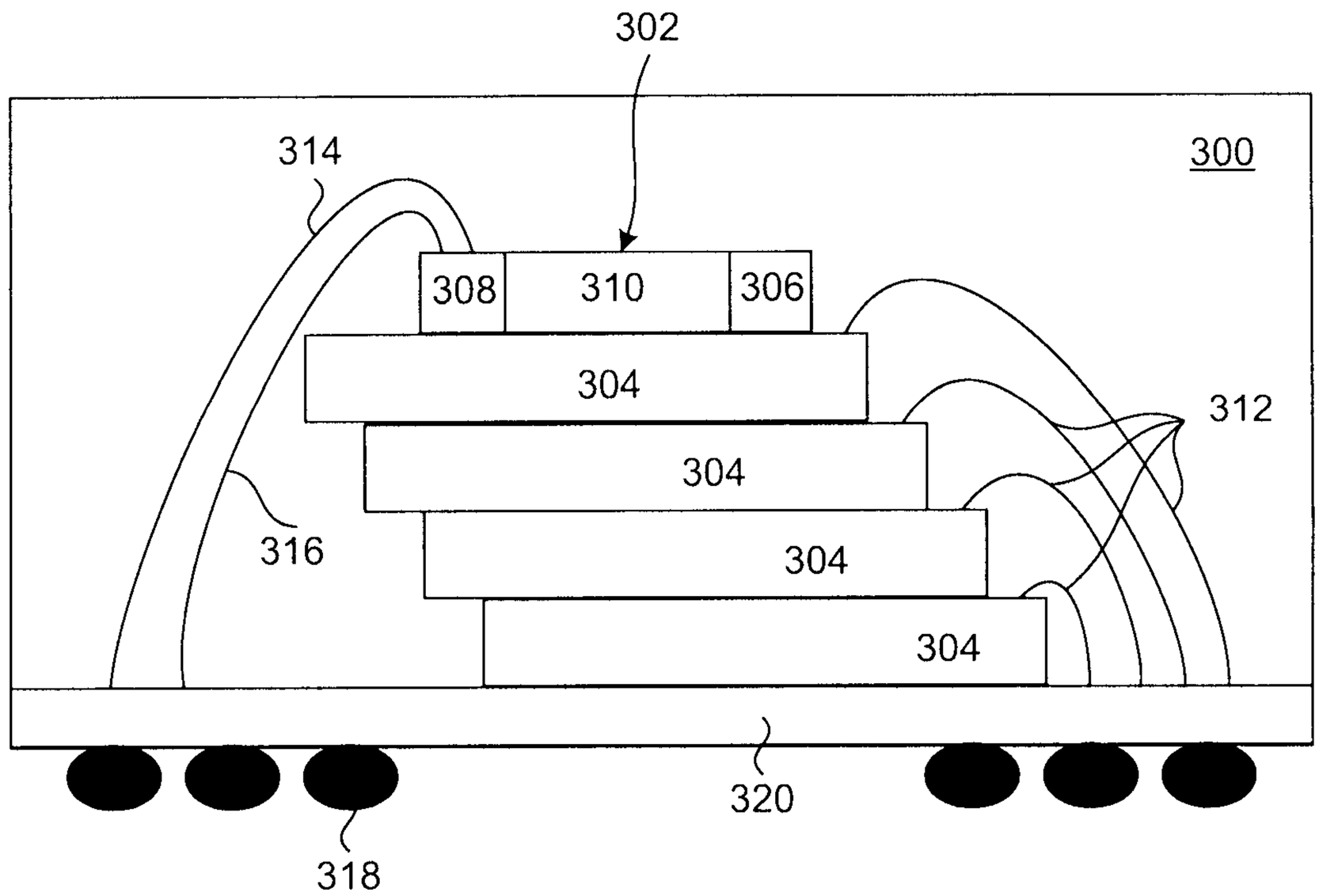
302
314
300
308
310
306
304
304
304
304
312
316
320
318

FIG. 5B

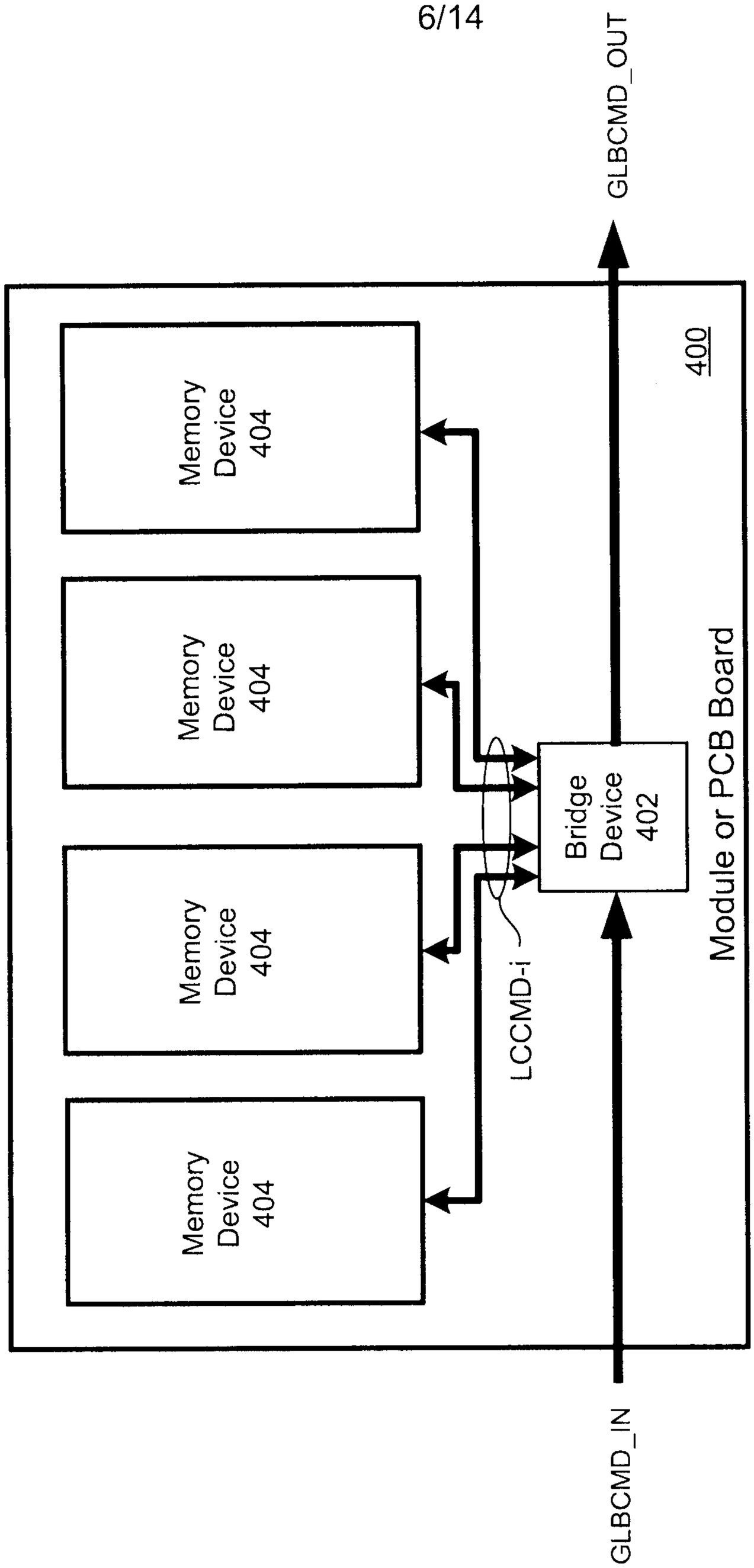
GLBCMD_OUT
400
Module or PCB Board
Memory Device 404
Memory Device 404
Memory Device 404
Memory Device 404
Bridge Device 402
LCCMD-i
GLBCMD_IN

FIG. 6

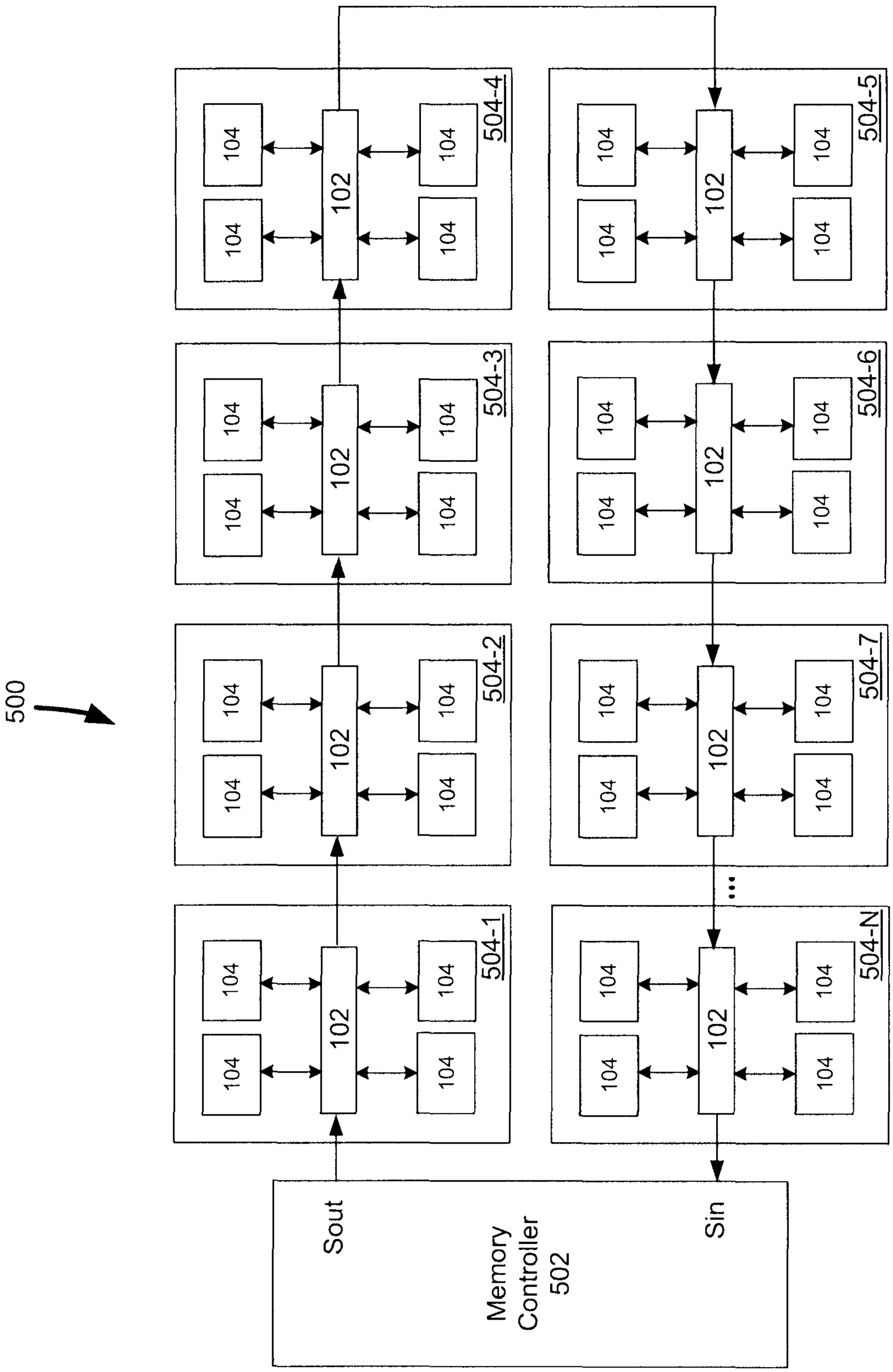
500
504-1
504-2
504-3
504-4
504-5
504-6
504-7
504-N
102
104
Sout
Sin
Memory Controller 502

FIG. 7

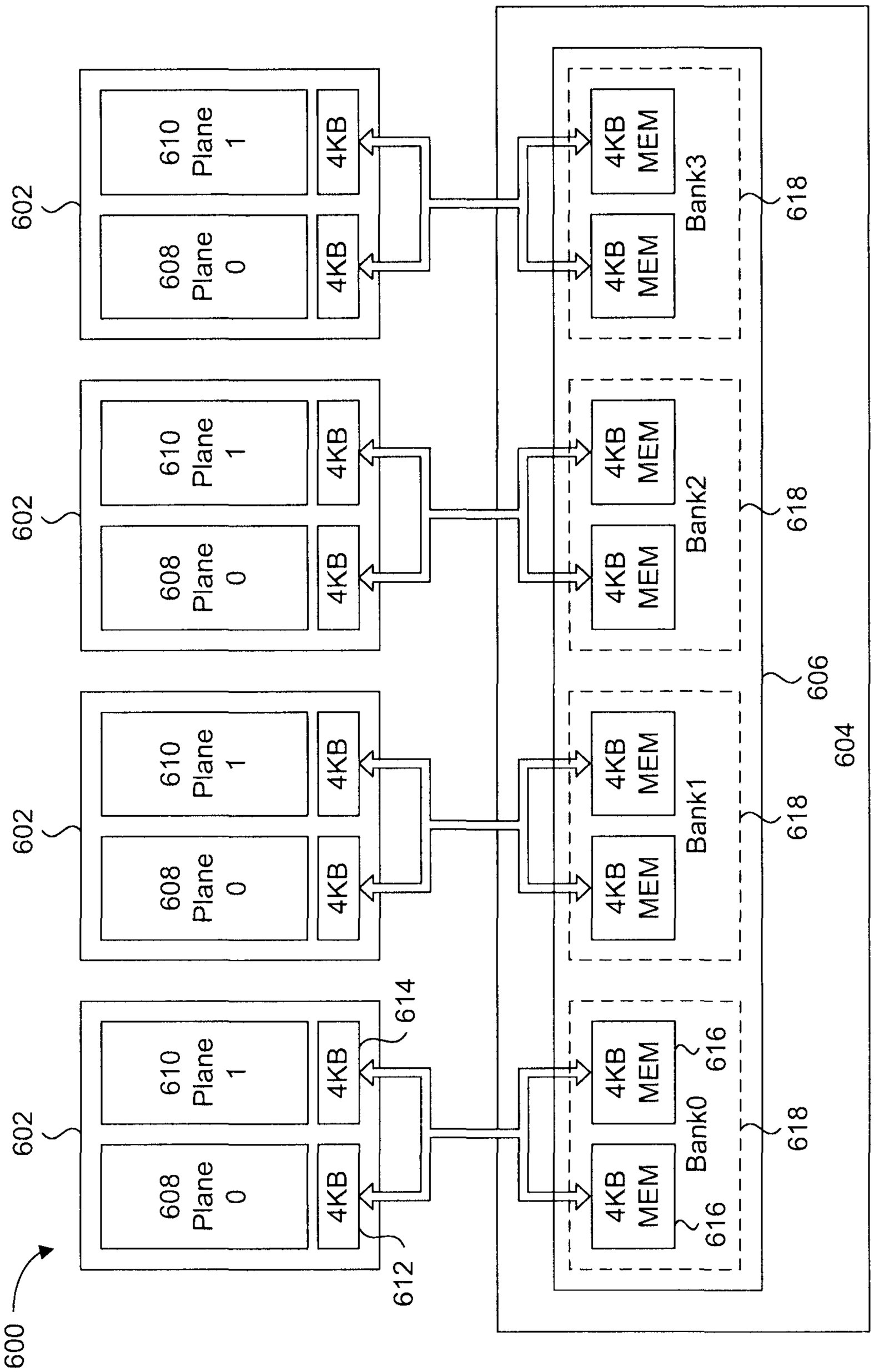
600
602
608 Plane 0
610 Plane 1
4KB
612
614
604
606
616
618
Bank0
Bank1
Bank2
Bank3
4KB MEM

FIG. 8

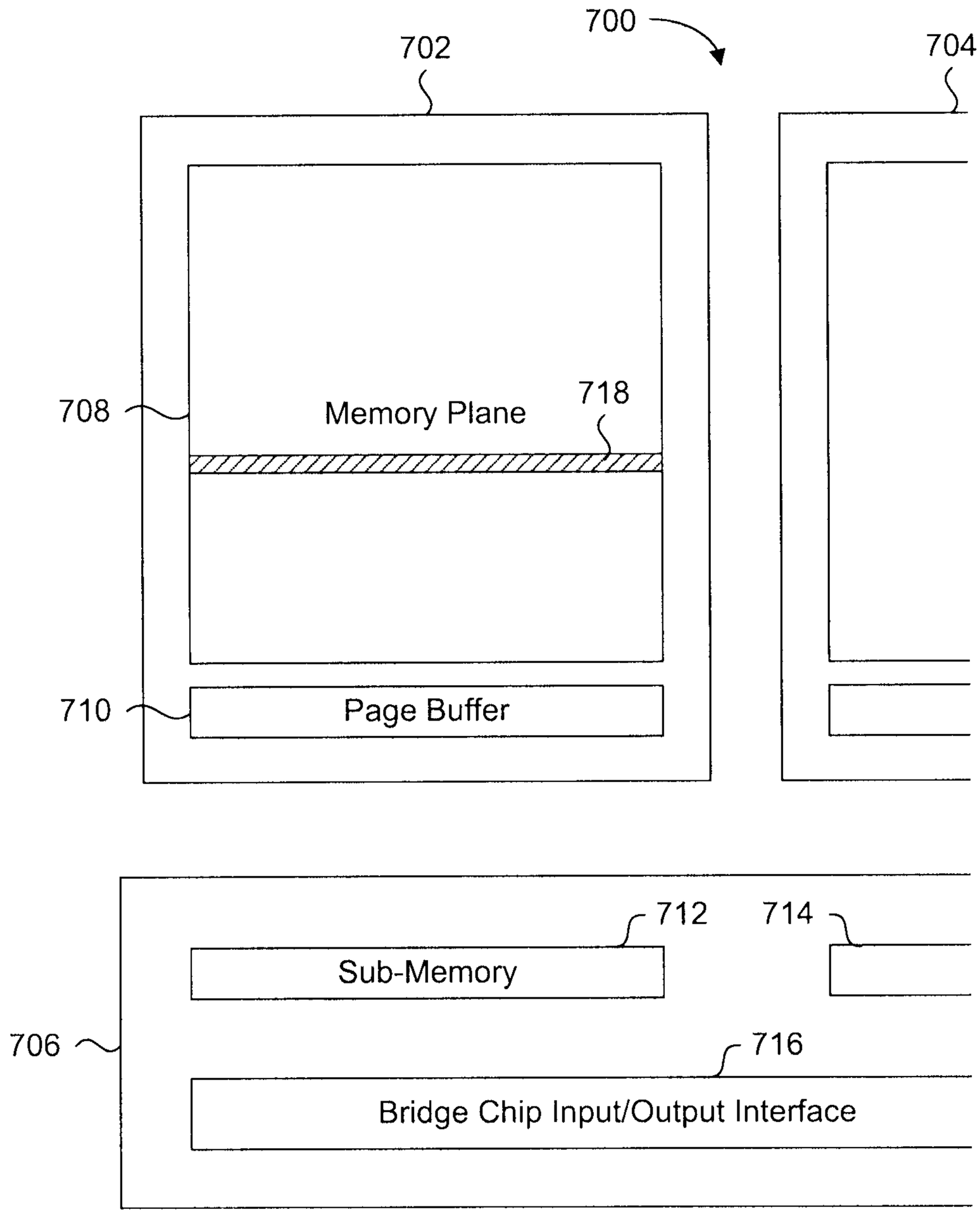
700
702
704
708
Memory Plane
718
710
Page Buffer
706
712
714
Sub-Memory
716
Bridge Chip Input/Output Interface

FIG. 9A

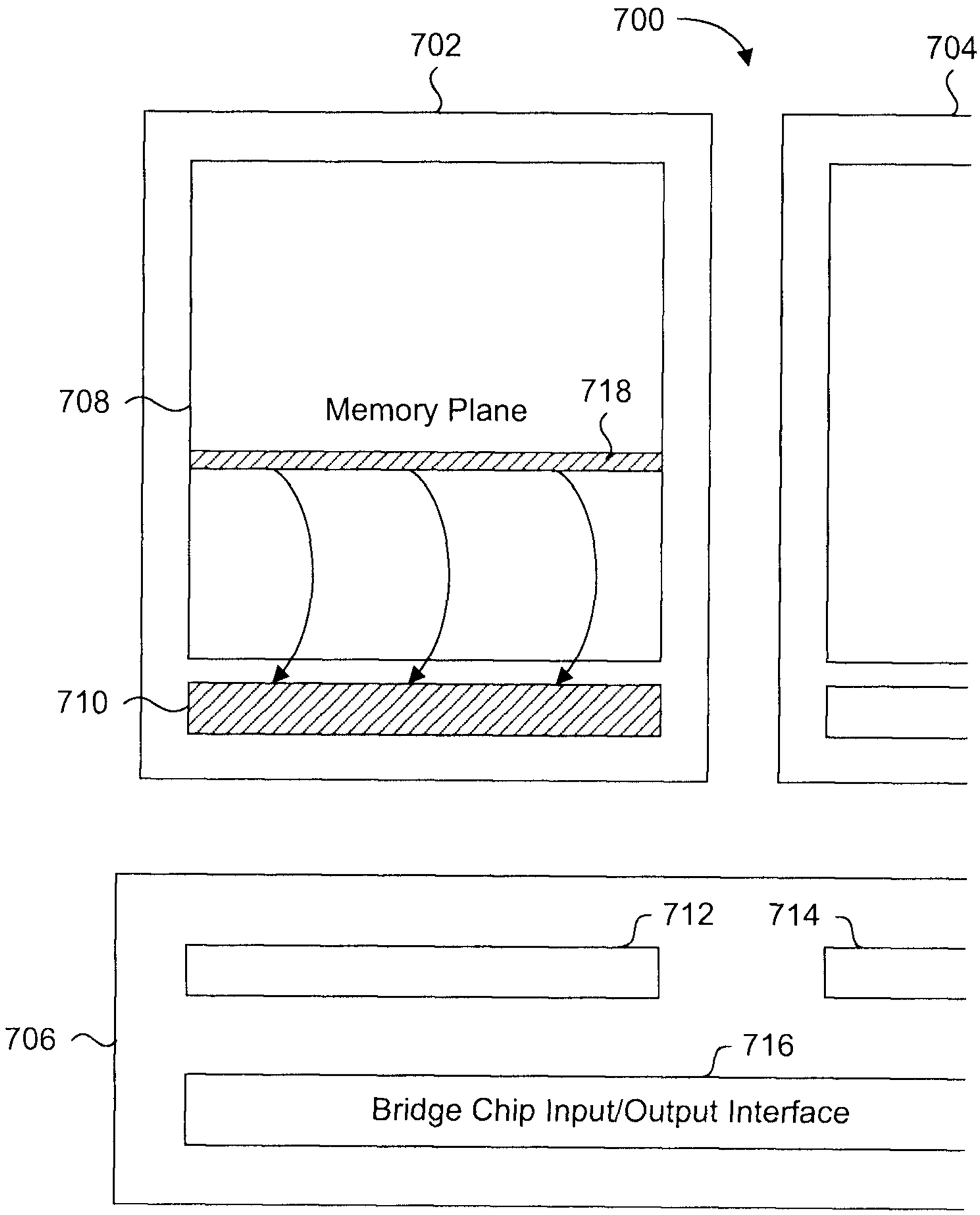
700
702
704
708
Memory Plane
718
710
712
714
706
716
Bridge Chip Input/Output Interface

FIG. 9B

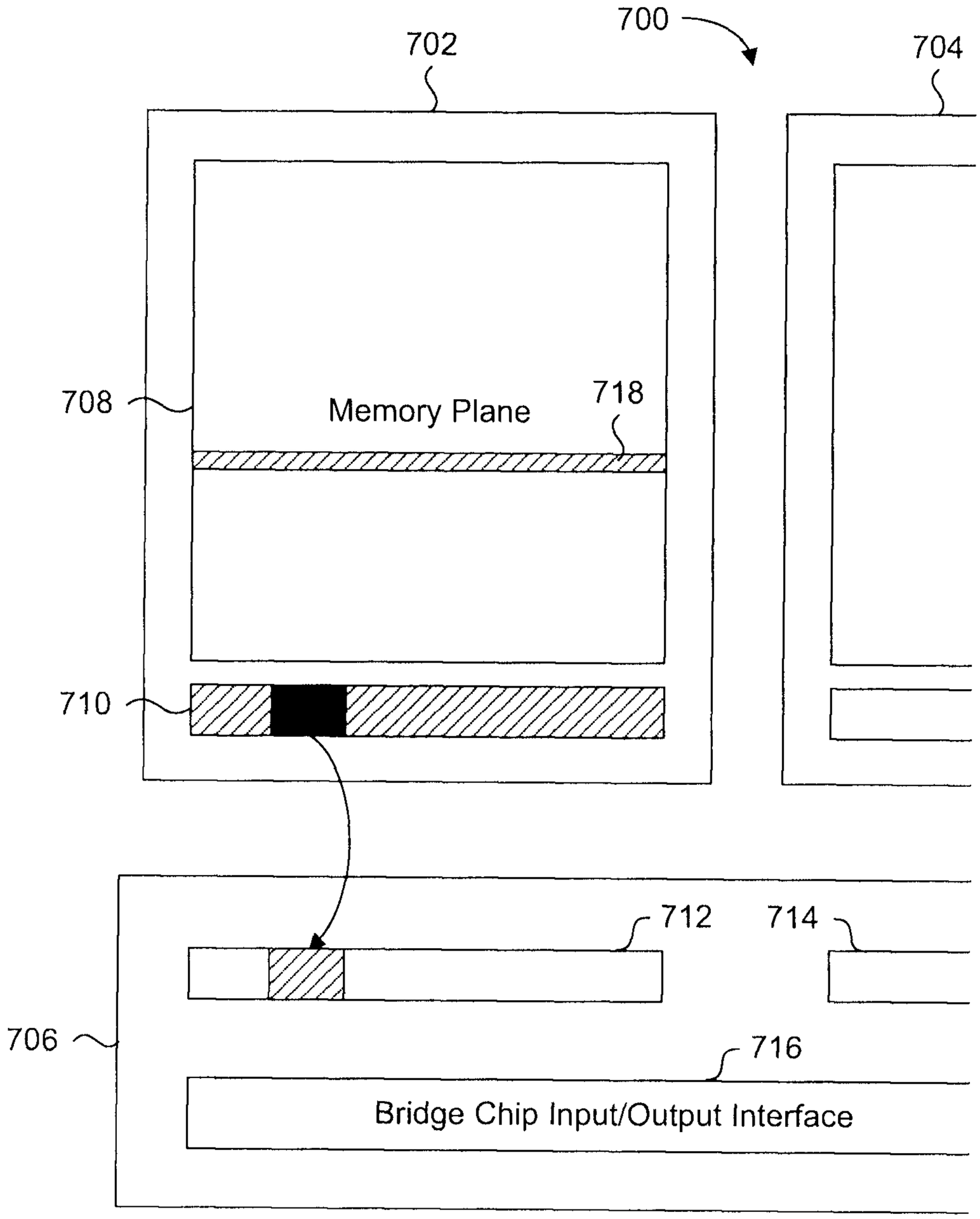
700
702
704
708
Memory Plane
718
710
712
714
706
716
Bridge Chip Input/Output Interface

FIG. 9C

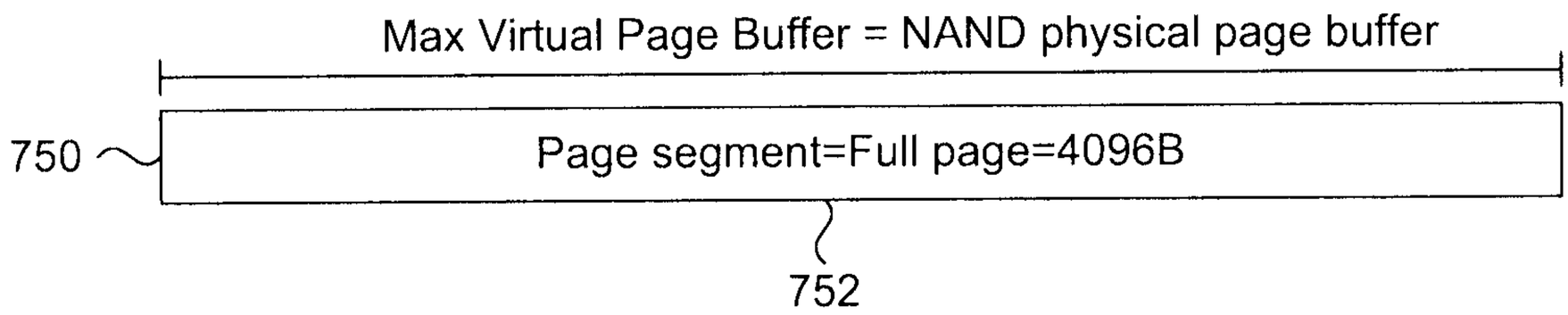

FIG. 10A

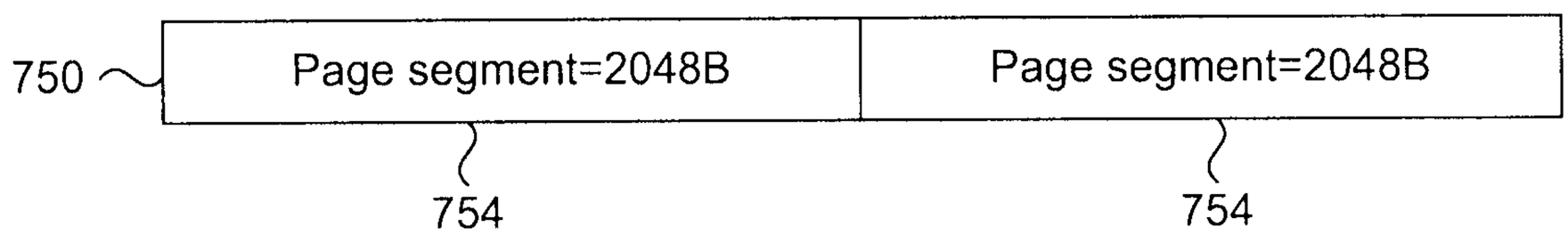

FIG. 10B

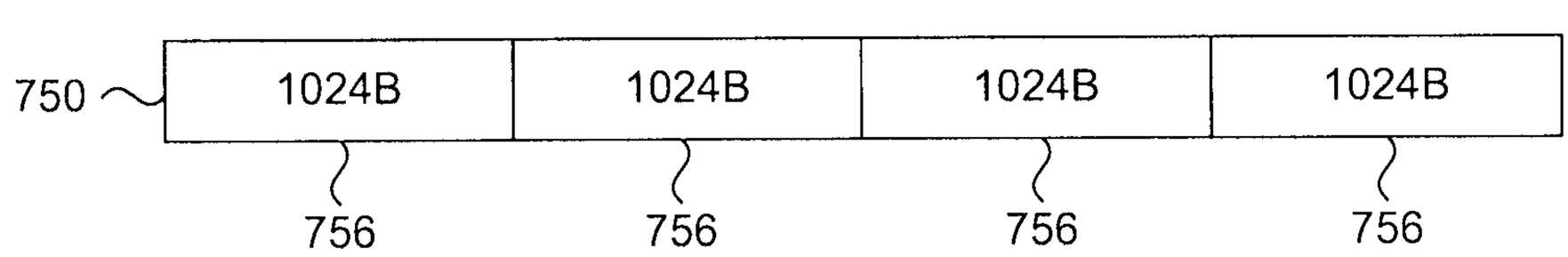

FIG. 10C

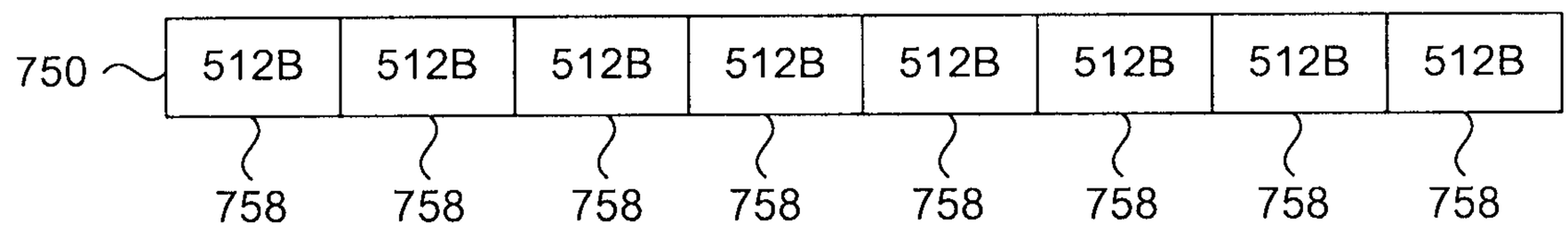

FIG. 10D

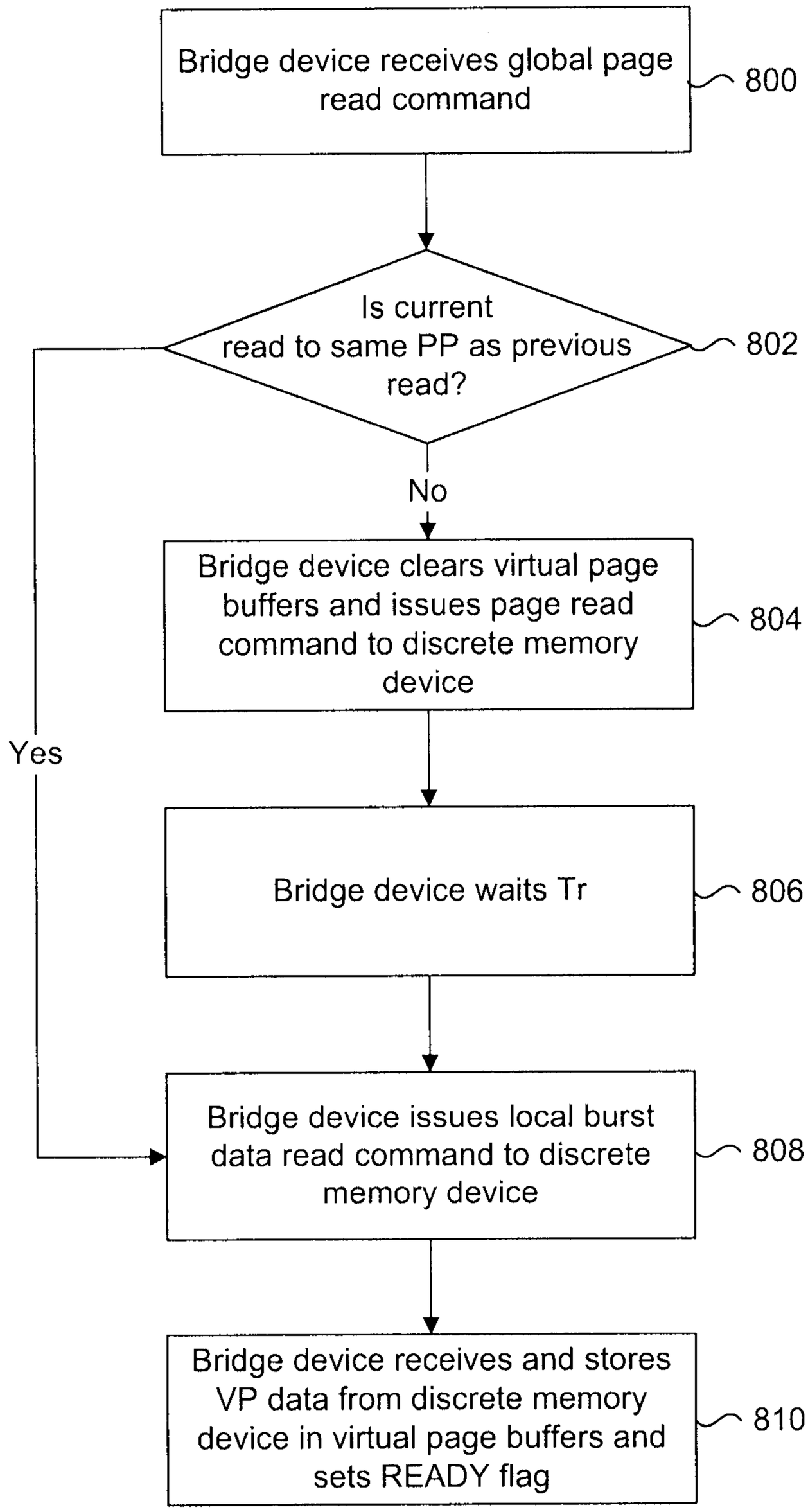
Bridge device receives global page read command
800
Is current read to same PP as previous read?
802
No
Yes
Bridge device clears virtual page buffers and issues page read command to discrete memory device
804
Bridge device waits Tr
806
Bridge device issues local burst data read command to discrete memory device
808
Bridge device receives and stores VP data from discrete memory device in virtual page buffers and sets READY flag
810

FIG. 11

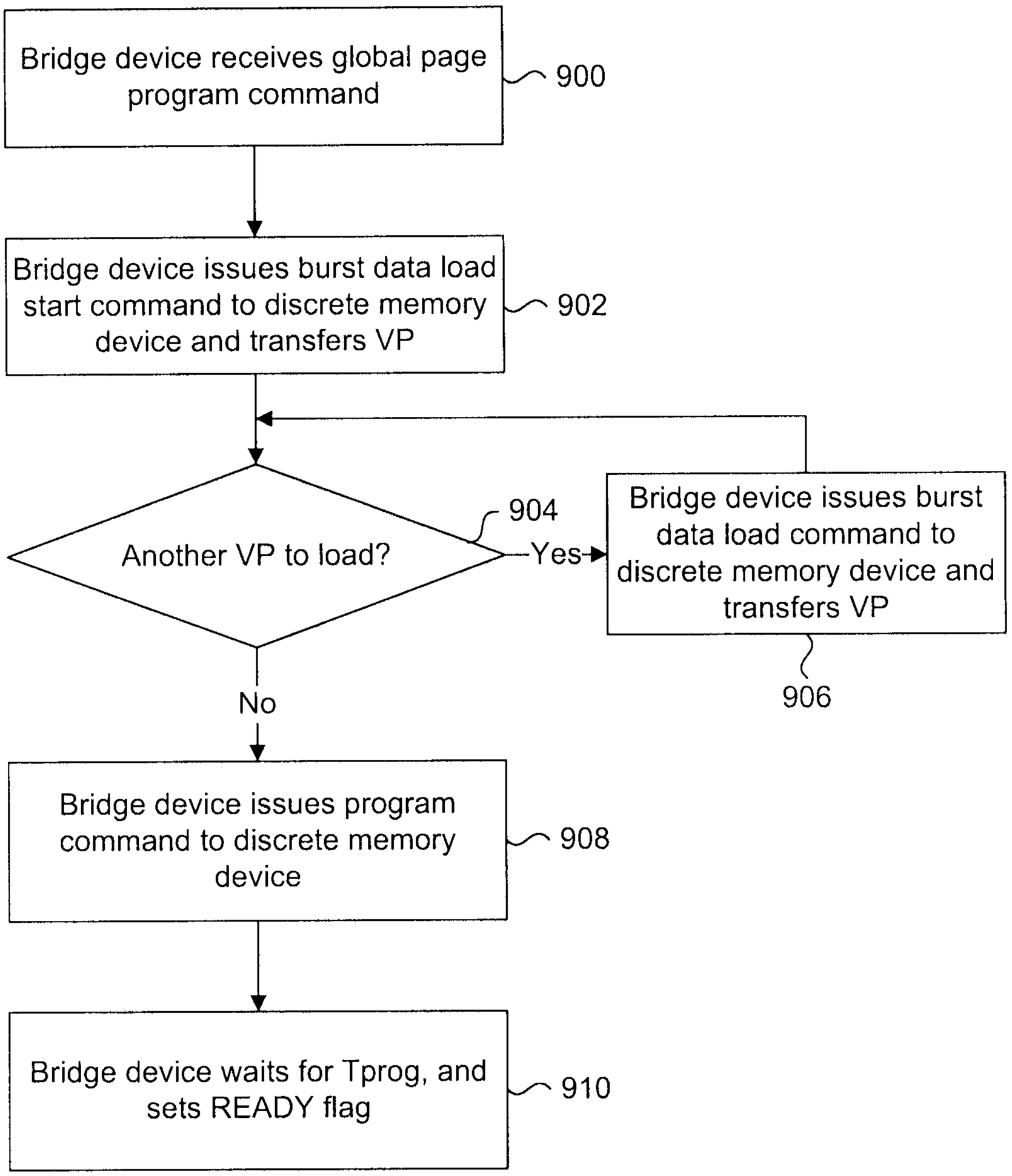
Bridge device receives global page program command
900
Bridge device issues burst data load start command to discrete memory device and transfers VP
902
Another VP to load?
904
Yes
No
Bridge device issues burst data load command to discrete memory device and transfers VP
906
Bridge device issues program command to discrete memory device
908
Bridge device waits for Tprog, and sets READY flag
910

FIG. 12

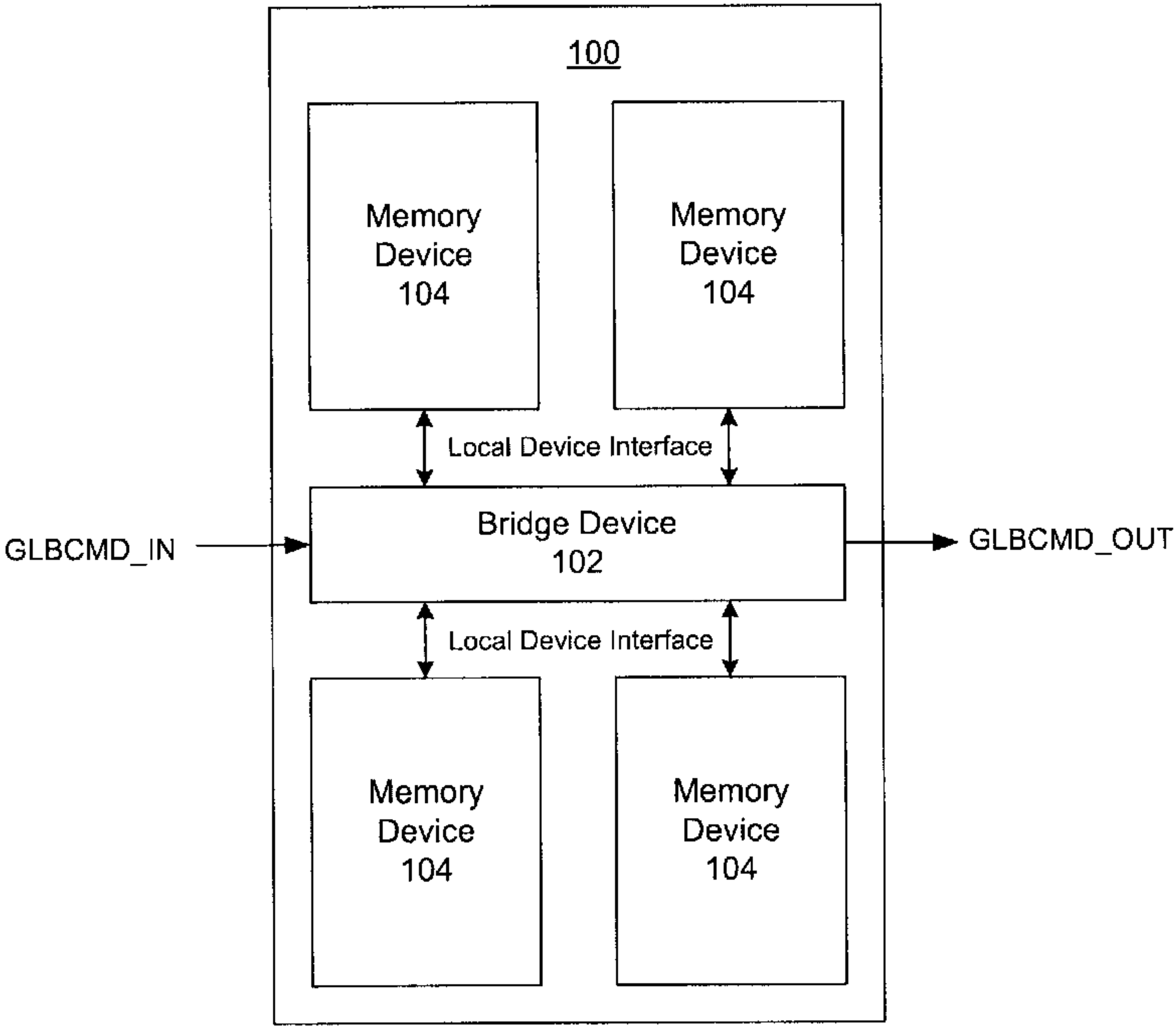
100
Memory Device 104
Memory Device 104
Local Device Interface
Bridge Device 102
GLBCMD_IN
GLBCMD_OUT
Local Device Interface
Memory Device 104
Memory Device 104

FIG. 3A