(19) DANMARK

Patent- og
Varemærkestyrelsen

(10) **DK/EP 2681969 T3**

(12)
Oversættelse af europæisk patentskrift

---

(51) Int.Cl.: *H 05 B 33/08 (2006.01)* *H 05 B 39/04 (2006.01)* *H 05 B 39/08 (2006.01)*

(45) Oversættelsen bekendtgjort den: **2019-03-25**

(80) Dato for Den Europæiske Patentmyndigheds
bekendtgørelse om meddelelse af patentet: **2019-01-09**

(86) Europæisk ansøgning nr.: **11794283.9**

(86) Europæisk indleveringsdag: **2011-11-16**

(87) Den europæiske ansøgnings publiceringsdag: **2014-01-08**

(86) International ansøgning nr.: **US2011061033**

(87) Internationalt publikationsnr.: **WO2012128794**

(30) Prioritet: **2010-11-16 US 414291 P** **2011-11-16 US 201113298002**

(84) Designerede stater: **AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR**

(73) Patenthaver: **Signify Holding B.V., High Tech Campus 48, 5656 AE Eindhoven, Holland**

(72) Opfinder: **MELANSON, John, L., 901 West 9th Street 201, Austin, TX 78703, USA**
KING, Eric, J., 1050 Trail Head Circle, Dripping Springs, TX 78620, USA

(74) Fuldmægtig i Danmark: **NORDIC PATENT SERVICE A/S, Bredgade 30, 1260 København K, Danmark**

(54) Benævnelse: **BAGKANTSDÆMPERKOMPATIBILITET MED FORUDSIGELSE OM HØJ DÆMPNINGSMODSTAND**

(56) Fremdragne publikationer:
EP-A2- 2 232 949
WO-A1-2008/029108
US-A1- 2009 284 182

DESCRIPTION

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates in general to the field of electronics, and more specifically to a method and system for trailing edge dimmer compatibility with dimmer high resistance prediction.

DESCRIPTION OF THE RELATED ART

[0002] The development and use of energy efficient technologies continues to be a high priority for many entities including many companies and countries. One area of interest is the replacement of incandescent lamps with more energy efficient lamps such as lamps based on electronic light sources. For this description, electronic light sources are light emitting diodes (LEDs) and compact fluorescent lamps (CFLs). The development of electronic light source based lamps and are not without many challenges. One of the challenges is developing electronic light source based lamps that are compatible with existing infrastructure. The following discussion focuses on LED-based lighting systems but is also applicable to CPL-based lighting systems and combination LED and CFL based lighting systems.

[0003] Many electronic systems include circuits, such as switching power converters that interface with a dimmer. The interfacing circuits deliver power to a load in accordance with the dimming level set by the dimmer. For example, in a lighting system, dimmers provide an input signal to a lighting system. The input signal represents a dimming level that causes the lighting system to adjust power delivered to a lamp, and, thus, depending on the dimming level, increase or decrease the brightness of the lamp. Many different types of dimmers exist. In general, dimmers generate a digital or analog coded dimming signal that indicates a desired dimming level. A trailing edge dimmer phase cuts a trailing edge of an alternating current ("AC") supply voltage.

[0004] Figure 1 depicts a lighting system 100 that includes a trailing edge, phase-cut dimmer 102. Figure 2 depicts an exemplary, trailing edge phase cut voltage graph 200 and a dimmer control signal 201 associated with the lighting system 100. Referring to Figures 1 and 2, the lighting system 100 receives an AC supply voltage V_{IN} from voltage supply 104. The supply voltage V_{IN}, indicated by voltage waveform 202, is, for example, a nominally 60 Hz/110 V line voltage in the United States of America or a nominally 50 Hz/220 V line voltage in Europe. The trailing edge dimmer 102 phase cuts trailing edges, such as trailing edges 202 and 204, of each half cycle of supply voltage V_{IN}. Since each half cycle of supply voltage V_{IN} is 180 degrees of the supply voltage V_{IN}, the trailing edge dimmer 102 phase cuts the supply voltage V_{IN} at an angle greater than 0 degrees and less than 180 degrees. The phase cut, input voltage V_{Φ_IN} to the lighting system 100 represents a dimming level that causes the lighting system 100 to adjust power delivered to a lamp 106, and, thus, depending on the dimming level, increase or decrease the brightness of the lamp 106. The lamp 106 is an incandescent lamp and can generally be modeled as a resistor 108.

[0005] The dimmer 102 includes a timer controller 110 that generates dimmer control signal DCS to control a duty cycle of switch 112. The duty cycle of switch 112 is a pulse width, e.g. times t_1-t_0, divided by a period of the dimmer control signal, e.g. times t_3-t_0, for each cycle of the dimmer control signal DCS. The timer controller 110 converts a desired dimming level into the duty cycle for switch 112. The duty cycle of the dimmer control signal DCS is increased for lower dimming levels, i.e. higher brightness for lamp 106, and decreased for higher dimming levels. During a pulse, e.g. pulse 206 and pulse 208, of the dimmer control signal DCS, the switch 112 conducts, i.e. is ON, and the dimmer 102 enters a low resistance state. In the low resistance state of the dimmer 102, the resistance of the switch 112 is, for example, less than or equal to 10 ohms. During the low resistance state of switch 112, the phase cut, input voltage V_{Φ_IN} tracks the input supply voltage V_{IN} and the dimmer 102 transfers a dimmer current i_{DIM} to the lamp 106.

[0006] When the timer controller 110 causes the pulse of the dimmer control signal 206 to end, the dimmer control signal 206 turns the switch 112 OFF, which causes the dimmer 102 to enter a high resistance state, i.e. turns OFF. In the high resistance state of the dimmer 102, the resistance of the switch 112 is, for example, greater than 1 kohm. The dimmer 102 includes a capacitor 114, which charges to the supply voltage V_{IN} during each pulse of the timer control signal DCS. In both the high and low resistance states of the dimmer 102, the capacitor 114 remains connected across the switch 112. When the switch 112 is OFF and the dimmer 102 enters the high resistance state, the voltage V_C across capacitor 114 decays, e.g. between times t_1 and t_2 and between times t_4 and t_5. The rate of decay is a function of the amount of capacitance C of capacitor 114 and the dimmer current i_{DIM} that is transferred through the resistance R of lamp 108. Equation [1] represents the relationship between the capacitance C of capacitor 114, the dimmer current i_{DIM}, and the rate of decay dV_{Φ_IN}/dt of the phase cut, input voltage V_{Φ_IN}:

$$i_{DIM} = C \cdot dV_{\Phi\_IN}/dt \quad [1]$$

[0007] The resistance value R of lamp 106 is relatively low and permits a high enough value of the dimmer current i_{DIM} to allow the phase cut, input voltage V_{Φ_IN} to decay to a zero crossing, e.g. at times t_2 and t_5, before the next pulse of the dimmer control signal DCS.

[0008] Trailing edge dimmers, such as trailing edge dimmer 102, have some favorable characteristics. For example, trailing edge dimmer 102 does not have an abrupt voltage increase when the dimmer 102 begins to conduct, e.g. at times t_0 and t_3, and has a decaying decrease when the dimmer 102 enters the high resistance state. Thus, harmonic frequencies are lower, and the dimmer 102 generates less electromagnetic interference.

[0009] As previously discussed, electronic light sources have a higher energy efficiency than incandescent lamps of comparable light out. Thus, electronic light sources are being retrofitted into existing infrastructure that includes trailing edge dimmers, such as trailing edge dimmer 102. An electronic light source has lower power requirements and, thus, less dimmer current i_{DIM} is transferred to the electronic light sources. Thus, in accordance with Equation [1] for a smaller dimmer current i_{DIM}, the decay rate dV_{Φ_IN}/dt is less. If the decay rate dV_{Φ_IN}/dt is too low, the phase cut, input voltage V_{Φ_IN} does not reach a zero crossing prior to a beginning of a next cycle of the supply voltage V_{IN}. Failure to reach a zero-crossing can cause some trailing edge dimmers to malfunction.

[0010] Figure 3 depicts a lighting system 300 that includes the trailing edge dimmer 102 and LED(s) 302. The dimmer 102 functions as previously described and provides a phase cut, input voltage V_{Φ_IN} and a dimmer current to a full bridge diode rectifier 304. The rectifier 304 provides the phase cut, rectified voltage V_{Φ_R} to a power converter 306. The power converter 306 respectively converts the phase cut, rectified voltage V_{Φ_R} and the rectified input current i_R into an approximately constant output voltage V_{OUT} and an output current i_{OUT}. The output current i_{OUT} adjusts with the dimming level indicated by the phase angle of the phase cut, input voltage V_{Φ_IN} and is approximately constant for any given dimming level.

[0011] The controller 308 includes a current controller 310 to control the transfer of current i_R to the power converter 306 and regulate the power delivered to the LED(s) 302. The LED(s) require substantially less power to provide the equivalent light output of an incandescent bulb. For example, the LED(s) 302 use 4W of power to provide the equivalent light output of a 60W incandescent bulb. The output voltage V_{OUT} is generally boosted by the power converter 306 to, for example, 400V. Since the power P provided to the LED(s) 302 is approximately $P = V_{OUT} \cdot i_{OUT}$, a maximum current i_R transferred to the power converter 306 is typically only 50 mA, which is less than the approximately 545 mA maximum current drawn by a 60W bulb from a 110 V supply input voltage V_{IN}. Thus, the decay time dV_{Φ_IN}/dt for the lighting system 300 increases in accordance with Equation [1]. The controller 308 includes a comparator 312 to detect trailing edges, such as trailing edges 314 and 316, of the phase cut, rectified voltage V_{Φ_R}.

[0012] Detection of the trailing edge of the phase cut, rectified voltage V_{Φ_R} is not a simple task. The trailing edges of rectified input voltage $V_{\Phi R\_IN}$ at times t_1 and t_4 are generally noisy and may contain other distortions. To detect the trailing edges, the controller 308 utilizes a comparator 312 to detect the trailing edge at a more stable portion of the phase cut, rectified

voltage V_{Φ_R}. The comparator 312 receives the phase cut, rectified voltage V_{Φ_R} or a scaled version of the phase cut, rectified voltage V_{Φ_R} at an inverting input of the comparator 312. The comparator 312 compares the phase cut, rectified voltage V_{Φ_R} with a fixed, trailing edge detection voltage threshold, such as +20V, and generates a trailing edge detection signal TE_DETECT. The trailing edge detection signal TE_DETECT signal is a logical 0 prior to detection of a trailing edge of phase cut, rectified voltage V_{Φ_R} and transitions to a logical 1 upon detection of the trailing edge. Once the trailing edge detection signal TE_DETECT indicates detection of the trailing edge, the current controller 310 increases a transfer of current i_{DIM} through the dimmer 102 to increase the rate of decay d V_{Φ_IN}/dt and, thus, increase the rate of decay of the phase cut, rectified voltage V_{Φ_R} at, for example times t_2 and t_5. Increasing the rate of decay at times t_2 and t_5 helps ensure that the phase cut, rectified voltage V_{Φ_R} reaches a zero crossing prior to a beginning of a next cycle of the phase cut, rectified voltage V_{Φ_R}. The trailing edge detection threshold value is set low enough to avoid prematurely detecting a trailing edge. However, because the rate of decay d V_{Φ_IN}/dt is greater for electronic light sources, the low value of the trailing edge detection threshold also means that the trailing edge might not be detected before a zero crossing of the phase cut, rectified voltage V_{Φ_R} for large phase angles. Increasing the value of the trailing edge detection threshold can result in transferring an unnecessary amount of current from the voltage supply 104.
WO2008/029108 shows an example of prior art that only address the problem of minimum current for triggering the dimmer.

[0013] It is desirable to improve compatibility with trailing edge dimmers.

SUMMARY OF THE INVENTION

[0014] The invention is more defined in the annexed set of claims
In one embodiment of the present invention, an apparatus includes a controller to provide compatibility between a lamp and a trailing edge dimmer. The controller is capable to predict an estimated occurrence of a high resistance state of the trailing edge dimmer. The high resistance state occurs when the trailing edge dimmer begins phase cutting an alternating current (AC) voltage signal. The controller is further capable to operate in a high current mode based on the estimated predicted occurrence of the high resistance state of the trailing edge dimmer. The controller is also capable to operate in a low impedance mode after the AC voltage signal reaches a low voltage threshold.

[0015] In a further embodiment of the present invention, a method to provide compatibility between a lamp and a trailing edge dimmer includes predicting an estimated occurrence of a high resistance state of the trailing edge dimmer. The high resistance state occurs when the trailing edge dimmer begins phase cutting an alternating current (AC) voltage signal. The method further includes operating a controller of at least a power converter in a high current mode based on the estimated predicted occurrence of the high resistance state of the trailing edge dimmer. The method also includes operating the controller in a low impedance mode after the AC voltage signal reaches a low voltage threshold.

[0016] In another embodiment of the present invention, an apparatus includes a controller that is a capable to predict an estimated occurrence of a high resistance state of a trailing edge dimmer. The high resistance state occurs when the trailing edge dimmer begins phase cutting an alternating current (AC) voltage signal of a phase cut AC voltage. The controller is further capable to accelerate a transition of the AC voltage from the trailing edge to a predetermined voltage threshold.

[0017] In a further embodiment of the present invention, a method includes predicting an estimated occurrence of a high resistance state of a trailing edge dimmer. The high resistance state occurs when the trailing edge dimmer begins phase cutting an alternating current (AC) voltage signal of a phase cut AC voltage. The method further includes accelerating a transition of the AC voltage from the trailing edge to a predetermined voltage threshold.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the several figures designates a like or similar element.

Figure 1 (labeled prior art) depicts a lighting system that includes a trailing edge dimmer.

Figure 2 (labeled prior art) depicts a dimmer control signal and voltage waveform associated with the trailing edge dimmer of Figure 1.

Figure 3 (labeled prior art) depicts a lighting system that includes a trailing edge dimmer 102 and LED(s).

Figure 4 depicts a lighting system that includes a controller that provides compatibility between the trailing edge dimmer and an electronic light source.

Figure 5 depicts exemplary voltage and current waveforms during operation of the lighting system of Figure 4.

Figure 6 depicts an exemplary trailing edge compatibility operational flow chart that represents one embodiment of providing compatibility between the trailing edge dimmer and electronic the light source of Figure 4.

Figure 7 depicts a lighting system that represents one embodiment of the lighting system of Figure 4.

Figure 8 depicts a zero crossing and active period detector.

Figure 9 depicts a current control module.

DETAILED DESCRIPTION

[0019] In at least one embodiment, an electronic system includes a controller, and the controller provides compatibility between an electronic light source and a trailing edge dimmer. In at least one embodiment, the controller is capable of predicting an estimated occurrence of a trailing edge of a phase cut AC voltage and accelerating a transition of the phase cut AC voltage from the trailing edge to a predetermined voltage threshold. The terms "predict" and derivatives thereof, such as "predicting" and "prediction" mean to declare or indicate in advance. Thus, in at least one embodiment, predicting an estimated occurrence of a trailing edge of a phase cut AC voltage declares or indicates in advance the estimated occurrence of the trailing edge of the phase cut AC voltage. In at least one embodiment, the controller predicts an estimated occurrence of the trailing edge of the phase cut AC voltage on the basis of actual observations from one or more previous cycles of the phase cut AC voltage.

[0020] In at least one embodiment, to provide compatibility between a trailing edge dimmer and an electronic light source, the controller predicts an estimated occurrence of a high resistance state of the trailing edge dimmer. The trailing edge of a phase cut AC voltage begins when a trailing edge dimmer enters a high resistance state. Thus, the high resistance state occurs when the trailing edge dimmer begins phase cutting an alternating current (AC) voltage signal. Based on the prediction of the estimated occurrence of the high resistance state of the trailing edge dimmer, the controller is capable of and configured to further operate in a high current mode to increase a transfer of current from the trailing edge dimmer. Operating in the high current mode increases a decay rate of the phase cut AC voltage and, in at least one embodiment, ensures that the phase cut AC voltage reaches a low voltage threshold prior to beginning another cycle. Once the phase cut AC voltage reaches the low voltage threshold, the controller is capable of and configured to operate in a low impedance mode to hold the phase cut AC voltage at or below the low voltage threshold.

[0021] Figure 4 depicts a lighting system 400 that includes a controller 402 that provides compatibility between the trailing edge dimmer 404 and the light source 410. The trailing edge dimmer 404 can be any trailing edge dimmer, such as trailing edge dimmer 102, that phase cuts a trailing edge of the input supply voltage V_{IN} from voltage supply 104. The full-bridge diode rectifier 408 rectifies the phase cut, input voltage V_{Φ_IN} to generate the phase cut, rectified voltage V_{Φ_R}. The power converter 406 receives the phase cut, rectified voltage V_{Φ_R} and the rectified current i_R generates an output voltage V_{OUT} and an output current i_{OUT}. The output voltage V_{OUT} and the output current i_{OUT} provide power for the light source 410. In at least one embodiment, the light source 410 is an electronic light source that includes one or more LEDs, one or more CFLs, or a combination of one or more LEDs and one or more CFLs. The power converter 406 can be any type of power converter and can include, for example, a boost converter, a buck converter, a boost-buck converter, or a Cuk converter.

[0022] Figure 5 depicts exemplary voltage and current waveforms 500 during operation of the lighting system 400. Figure 6 depicts an exemplary trailing edge compatibility operational flow chart 600 that represents one embodiment of providing compatibility between the trailing edge dimmer 404 and the light source 410. Referring to Figures 4, 5, and 6, the phase cut, rectified voltage V_{Φ_R} has an active period from a first zero crossing to the second zero crossing of each cycle. The waveforms 500 depict a series of active periods $T_A(n)$ - $T_A(n\text{-}N)$ of the phase cut, rectified voltage V_{Φ_R}, where n is an integer index and *N* is an integer greater than or equal to one. The "active time period $T_A(n\text{-}X)$" refers to the portion of the phase cut AC voltage that is not equal to approximately zero for "X" ranging from 0 to *N*. In at least one embodiment, the controller 402 predicts an estimated active time period $T_A(n)_{EST}$ of the nth cycle of the phase cut, rectified voltage V_{Φ_R} that spans from a first approximate zero crossing at time $t_{ZC}(n)_1$ until the next approximate zero crossing $t_{ZC}(n)_2$ of the active time period $T_A(n)$. $T_A(n)_{EST}$ represents the predicted estimate of the active time period $T_A(n)$ for the present nth cycle

[0023] In at least one embodiment, controller 402 includes a trailing edge dimmer high resistance state predictor 412 to predict the estimated active time period $T_A(n)_{EST}$ of the nth cycle using the actual measured active time periods $T_A(n\text{-}1)$ through $T_A(n\text{-}N)$ of N previous cycle(s) of the phase cut, rectified voltage V_{Φ_R}, where *N* is an integer greater than or equal to 1. The trailing edge high resistance state predictor 412 senses the phase cut, rectified voltage V_{Φ_R} at node 414. Each active time period $T_A(n\text{-}X)$ equals the time between a first zero crossing $t_{ZC}(n\text{-}X)_1$ and the second zero crossing $t_{ZC}(n\text{-}X)_2$ of the (n-X)th cycle of the rectified input voltage $V_{\Phi R\_IN}$. Thus, in at least one embodiment, in operation 602, the trailing edge high resistance state predictor 412 detects the time between approximate zero crossings $t_{ZC}(n\text{-}X)_1$ and $t_{ZC}(n\text{-}X)_2$ of each cycle of the phase cut, rectified voltage V_{Φ_R} to determine the active periods $T_A(n\text{-}X)$ of the phase cut, rectified voltage V_{Φ_R} for X ranging from 1 to *N*.

[0024] In operation 603, the trailing edge high resistance state predictor 412 predicts an estimated active period $T_A(n)_{EST}$ of nth cycle of the phase cut, rectified voltage V_{Φ_R}. The particular algorithm for predicting the estimated active period $T_A(n)_{EST}$ is a matter of design choice. In at least one embodiment, the trailing edge high resistance state predictor 412 assumes that the estimated active period $T_A(n)_{EST}$ is equal to the previous actual measured active period $T_A(n\text{-}1)$. In at least one embodiment, the trailing edge high resistance state predictor 412 utilizes an algorithm that reflects a trend of the durations of the active periods $T_A(n\text{-}X)$ for the previous *N* cycles of the phase cut, rectified voltage V_{Φ_R}. For example, in at least one embodiment, *N* equals 2, and the trailing edge high resistance state predictor 412 determines a trend in the durations of the active periods using Equation [2] to predict the estimated n^{th} active period $T_A(n)_{EST}$:

$$T_A(n)_{EST} = T_A(n-1) + T_A(n-1)-T_A(n-2) = 2\cdot T_A(n-1) - T_A(n-2) \quad [2].$$

In Equation [2], $T_A(n)_{EST}$ represents the predicted active time period for the n^{th} cycle, $T_A(n-1)$ represents an approximate actual time period for the previous (n-1) cycle, and $T_A(n-2)$ represents an approximate actual measured time period for the previous (n-2) cycle. As discussed in more detail in conjunction with Figure 8, the trailing edge high resistance state predictor 412 detects approximate actual zero crossings of each active cycle of the phase cut, rectified voltage V_{Φ_R}. From the detection of the actual zero crossings, in at least one embodiment, the trailing edge high resistance state predictor 412 determines an approximate actual active time period $T_A(n)$. The determined, approximate actual time period $T_A(n)$ becomes the approximate actual time period $T_A(n-1)$ used in Equation [2] when estimating the active time period for the next cycle of phase cut, rectified voltage V_{Φ_R} and becomes the approximate actual time period $T_A(n-2)$ used in Equation [2] when estimating the active time period for the cycle of phase cut, rectified voltage V_{Φ_R} after the next cycle.

[0025] In at least one embodiment, the trailing edge high resistance state predictor 412 segregates the odd and even cycles of the phase cut, rectified voltage V_{Φ_R} because the odd and even cycles correlate better with each other. When segregating the odd and even cycles, the trailing edge high resistance state predictor 412 determines the trend in the durations of the even active periods using Equation [3] to predict the estimated n^{th} active period $T_A(n)_{EST}$:

$$T_A(n)_{EST} = T_A(n-2) + T_A(n-2)-T_A(n-4) = 2\cdot T_A(n-2) - T_A(n-4) \quad [3].$$

When segregating the odd and even cycles, the trailing edge high resistance state predictor 412 determines the trend in the durations of the odd active periods using Equation [4] to predict the estimated n+1 active period $T_A(n)_{EST}$:

$$T_A(n+1)_{EST} = T_A(n-1) + T_A(n-1)-T_A(n-3) = 2\cdot T_A(n-1) - T_A(n-3) \quad [4].$$

[0026] In operation 604, the trailing edge high resistance state predictor 412 detects the first, approximate zero crossing $t_{ZC}(n)_1$ of the present n^{th} cycle of the phase cut, rectified voltage V_{Φ_R}. From a known first zero crossing time $t_{ZC}(n)_1$ of the n^{th} cycle and the predicted, estimated zero crossing time period $T_A(n)_{EST}$, the trailing edge high resistance state predictor 412 predicts when the second zero crossing time $t_{ZC}(n)_2$ will occur.

[0027] In operation 606, the trailing edge high resistance state predictor 412 predicts an estimated occurrence of a high resistance state of the trailing edge dimmer 404 based on the duration of n prior cycles of the phase cut, rectified voltage V_{Φ_R} and detection of first, approximate zero crossing $t_{ZC}(n)_1$ of the present n^{th} cycle. In at least one embodiment, the trailing edge high resistance state predictor 412 determines a predicted, estimated occurrence of the high resistance state of the trailing edge dimmer 404 for the n^{th} cycle by assuming that the occurrence of the high resistance state of the trailing edge dimmer 404 equals the predicted second zero crossing $t_{ZC}(n)_2$ of the n^{th} cycle less an estimated decay time $T_{DC}(n)$ of the trailing edge 502 of the phase cut, rectified voltage V_{Φ_R} for the n^{th} cycle.

[0028] The method of obtaining the estimated decay time $T_{DC}(n)$ is a matter of design choice. In at least one embodiment, the trailing edge high resistance state predictor 412 utilizes a pre-stored estimated decay time $T_{DC}(n)$, such as 180 µsec, based on a worst case value of a capacitor, such as capacitor 114 (Figure 1), of the trailing edge dimmer 404 and an amount of current i_{DIM} controlled by the current control module 416. In other embodiments, the trailing edge high resistance state predictor 412 utilizes any of a number of algorithms to determine the estimated decay time $T_{DC}(n)$ of the phase cut, rectified voltage V_{Φ_R}. For example, in at least one embodiment, estimated decay times are stored in a look-up table (not shown) for various capacitance values of the trailing edge dimmer 404 and the phase cut angles of phase cut, rectified voltage V_{Φ_R} and accessed by the trailing edge high resistance state predictor 412. In at least one embodiment, a value of the capacitance of the trailing edge dimmer 404 is stored in an optional memory 417 of the trailing edge high resistance state predictor 412. In at least one embodiment, the trailing edge high resistance state predictor 412 measures or determines the decay time $T_{DC}(n-1)$ for the previous $(n-1)^{th}$ cycle of the phase cut, rectified voltage V_{Φ_R} and utilizes the decay time $T_{DC}(n-1)$ from the previous $(n-1)^{th}$ cycle as the decay time $T_{DC}(n)$ for the present n^{th} cycle of the phase cut, rectified voltage V_{Φ_R}. In at least one embodiment, the decay times for the light source 410 at particular phase cut angles are empirically determined in a laboratory setting using actual dimmers and actual light sources, such as LEDs and/or CFLs. The decay times of the phase cut, rectified voltage V_{Φ_R} are then stored in an optional nonvolatile memory 417 via a terminal 419 of the controller 402 and utilized by the trailing edge high resistance state predictor 412 to predict the estimated occurrence of a high resistance state of the trailing edge dimmer 404.

[0029] In at least one embodiment, the operation 606 takes into consideration that the phase angle of the phase cut, rectified voltage V_{Φ_R} can decrease from cycle-to-cycle as a dimming level is decreased. To compensate for a potential decrease in the phase angle, the trailing edge high resistance state predictor 412 subtracts a dynamic dimming level compensation time T_{DDLC} from the second zero crossing time $t_{ZC}(n)_2$ to obtain a predicted occurrence of the high resistance state of the dimmer at time $t_{HR}(n)$. The value of the dynamic dimming level compensation time t_{DDLC} is a matter of design choice, and, in at least one embodiment, represents the largest possible change between the predicted estimates of the active periods $T_A(n)_{EST}$ and $t_A(n-1)_{EST}$. In at least one embodiment, the dynamic dimming level compensation time t_{DDLC} is 120 µsec. Thus, in at least one embodiment, the predicted occurrence of the high resistance state of the dimmer $t_{HR}(n)$ equals $t_{ZC}(n)_2$ - $(T_{DC}$ - $T_{DDLC})$. In at least one embodiment, the dynamic dimming level compensation time t_{DDLC} is a percentage, such as 50-75%, of the decay time $T_{DC}(n)$. The trailing edge high resistance state predictor

412 provides the HRSTATE_PREDICTION signal to the current control module 416 to indicate the predicted occurrence of the high resistance state of the dimmer $t_{HR}(n)$.

[0030] In operation 608, at the predicted occurrence of the dimmer high resistance state $t_{HR}(n)$, the trailing edge high resistance state predictor 412 increases an amount of dimmer current i_{DIM} transferred to the power converter 406 through the trailing edge dimmer 404. The increase in the dimmer current i_{DIM} decreases the decay time T_{DC} and, thus, accelerates transition of the trailing edge of the n^{th} cycle of the phase cut, rectified voltage V_{Φ_R} to a predetermined threshold voltage value. In at least one embodiment, the predetermined voltage threshold is in the range between 0 and 65V. In the exemplary depiction of the current i_R, which is a rectified version of the dimmer current i_{DIM}, the current i_R tracks the phase cut, rectified voltage V_{Φ_R} until the predicted occurrence of the dimmer high resistance state $t_{HR}(n)$. At the predicted occurrence of the dimmer high resistance state $t_{HR}(n)$, the current control module 416 increases the current i_R transferred through the trailing edge dimmer 404 to the power converter 406 to a trailing accelerator current value i_{R_ACCEL} than normal operation.

[0031] The particular value of the trailing accelerator current value i_{R_ACCEL} is a matter of design choice. Increasing the trailing accelerator current value i_{R_ACCEL} decreases the decay time T_{DC} and increases the dimming range of the lighting system 400. Decreasing the trailing accelerator current value i_{R_ACCEL} increases the decay time T_{DC} and decreases the dimming range of the lighting system 400. The dimming range of the lighting system 400 is increased because the range of phase cut angles, which correlate to dimming levels, is increased while still assuring that the phase cut, rectified voltage V_{Φ_R} reaches a zero crossing prior to the next zero crossing. However, increasing the value of the trailing accelerator current value i_{R_ACCEL} also potentially increases the amount of power to be dissipated by the power converter 406. Furthermore, increasing the value of the trailing accelerator current value i_{R_ACCEL} can result in the power converter 406 having higher current rated and, thus, more expensive components.

[0032] In at least one embodiment, the current control module 416 dynamically adjusts the value of the trailing accelerator current value i_{R_ACCEL} to ensure operation in discontinuous current mode (DCM) while minimizing power dissipation. In at least one embodiment, the controller 402 can switch between operation in DCM, continuous conduction mode (CCM), and/or critical conduction mode (CRM) to allow the current control module 416 flexibility in selecting the value of the trailing accelerator current value i_{R_ACCEL}. DCM is when the phase cut, rectified voltage V_{Φ_R} reaches a second zero crossing $t_{ZC}(n-X)_2$ prior to the first zero crossing $t_{ZC}(n-X+1)_1$ of the next cycle of the phase cut, rectified voltage V_{Φ_R}. CCM is when the phase cut, rectified voltage V_{Φ_R} does not reach a second zero crossing $t_{ZC}(n-X)_2$ prior to the first zero crossing $t_{ZC}(n-X+1)_1$ of the next cycle of the phase cut, rectified voltage V_{Φ_R}. CRM is when the second zero crossing $t_{ZC}(n-X)_2$ is the same as the first zero crossing t_{ZC}(n-

X+1)$_1$ of the next cycle of the phase cut, rectified voltage V_{Φ_R}.

[0033] In at least one embodiment, the trailing accelerator current value i_{R_ACCEL} is 100-500% higher than the peak normal operational value of the current i_R. In at least one embodiment, the normal operational current peaks at approximately 100 mA, and the trailing edge accelerator current value i_{R_ACCEL} is approximately 500 mA. In at least one embodiment, the power converter 406 includes one or more optional power dissipation circuits 418 to transfer the additional current i_R and dissipate power associated with the additional current i_R. Exemplary power dissipation circuits are described in (i) U.S. Patent Application No. 13/289,845, filed November 4, 2011, entitled "Controlled Power Dissipation in a Switch Path in a Lighting System", and inventors John L. Melanson and Eric J. King, (ii) U.S. Patent Application No. 13/289,931, filed November 4, 2011, entitled "Controlled Power Dissipation in a Lighting System", and inventors John L. Melanson and Eric J. King, and (iii) 13/289,967 filed November 4, 2011, entitled "Controlled Power Dissipation in a Link Path in a Lighting System", and inventors John L. Melanson and Eric J. King.

[0034] In at least one embodiment, because the voltage supply 104 is able to provide an amount of current that greatly exceeds the trailing accelerator current value i_{R_ACCEL}, if the dimming level and, thus, the phase angle of the phase cut, rectified voltage V_{Φ_R} increases rather than decreases, the trailing accelerator current value i_{R_ACCEL} will not distort the phase cut, rectified voltage V_{Φ_R} waveform.

[0035] In at least one embodiment, at each second zero crossing $t_{ZC}(n-X)_2$, the current control module 416 transfers current i_R through the dimmer 404 so that the power converter 406 enters a low impedance state. In at least one embodiment, the current in the low impedance state is referred to as a glue current and is, for example, generally described in U.S. Patent Application. No. 12/858,164, filed August 17, 2010, entitled: "Dimmer Output Emulation", and inventor: John L. Melanson (referred to herein as "Melanson I") and U.S. Patent Application No. 13/217,174, filed August 24, 2011, entitled: "Multi-Mode Dimmer Interfacing Including Attach State Control", and inventors: Eric J. King and John L. Melanson.

[0036] The particular implementation of the trailing edge high resistance state predictor 412 is a matter of design choice. The trailing edge high resistance state predictor 412 can be implemented using analog, digital, or analog and digital circuits and can be implemented using discrete components. In at least one embodiment, the controller 402 is an integrated circuit, and the trailing edge high resistance state predictor 412 and current control module 416 are implemented as part of the integrated circuit. In at least one embodiment, the controller 402 includes a processor (not shown) and a memory (not shown) to store and execute code that implements one or more embodiments of the exemplary trailing edge compatibility operational flow chart 600.

[0037] Figure 7 depicts a lighting system 700, which is one embodiment of the lighting system

400. The lighting system 700 includes controller 702, which includes the trailing edge dimmer high resistance state predictor 412. The trailing edge dimmer high resistance state predictor 412 generates the HRSTATE_PREDICTION signal and provides the HRSTATE_PREDICTION signal to the current control module 704 to indicate the predicted occurrence of the high resistance state of the dimmer $t_{HR}(n)$ as previously described with reference to lighting system 400. The current control module 704 controls the boost-type switching power converter 706 using the same current and voltage profiles as discussed with reference to lighting system 400 and as depicted in the exemplary voltage and current waveforms 500 (Figure 5). The switching power converter 706 includes a boost switch 707, and the current control module 704 controls power factor correction and regulates the link voltage V_{LINK} across link capacitor 708 as, for example, described in U.S. Patent Application No. 11/967,269, entitled "Power Control System Using a Nonlinear Delta-Sigma Modulator With Nonlinear Power Conversion Process Modeling", filed on December 31, 2007, inventor John L. Melanson (referred to herein as "Melanson I"), U.S. Patent Application No. 11/967,275, entitled "Programmable Power Control System", filed on December 31, 2007, and inventor John L. Melanson (referred to herein as "Melanson II"), U.S. Patent Application No. 12/495,457, entitled "Cascade Configured Switching Using at Least One Low Breakdown Voltage Internal, Integrated Circuit Switch to Control At Least One High Breakdown Voltage External Switch", filed on June 30, 2009 ("referred to herein as "Melanson III"), and inventor John L. Melanson, and U.S. Patent Application No. 12/174,404, entitled "Constant Current Controller With Selectable Gain", filing date June 30, 2011, and inventors John L. Melanson, Rahul Singh, and Siddharth Maru.

[0038] The switching power converter includes capacitor 710, which filters high frequency components from rectified voltage $V_{\Phi R\_IN}$. Gate bias voltage V_G biases the gate of switch 707. The particular value of the gate bias voltage V_G is a matter of design choice and, for example, depends on the operational parameters of the switch 707. In at least one embodiment, the gate bias voltage V_G is+12V. To control the operation of switching power converter 108, controller 110 generates a control signal CS_1 to control conductivity of field effect transistor (FET) switch 707. The control signal CS_1 is a pulse width modulated signal. Each pulse of control signal CS_1 turns switch 707 ON (i.e. conducts), and the inductor current i_R increases to charge inductor 712. Diode 714 prevents current flow from link capacitor 708 into switch 707. When the pulse ends, the inductor 712 reverses voltage polarity (commonly referred to as "flyback"), and the inductor current i_R decreases during the flyback phase. The inductor current i_R boosts the link voltage across the link capacitor 708 through diode 714. The switching power converter 706 is a boost-type converter, and, thus, the link voltage V_{LINK} is greater than the phase cut, rectified voltage V_{Φ_R}. The load with electronic light source 716 includes, for example, a transformer-based interface circuit to provide power to the electronic light sources.

[0039] Figure 8 depicts one embodiment of a zero crossing and active time detector 800, which is used in one embodiment of the trailing edge high resistance state predictor 412 (Figure 4) to detect the approximate values of zero crossings $t_{ZC}(n)_1$ and $t_{ZC}(n)_2$ of the phase cut, rectified voltage V_{Φ_R}. The zero crossing detector 800 includes a comparator 802 to compare the phase cut, rectified voltage V_{Φ_R} and a phase cut, rectified voltage VΦ_R_TH threshold value. The phase cut, rectified voltage VΦ_R_TH threshold value is, for example, in the range of 0-15V. When the comparator 802 detects that the phase cut, rectified voltage V_{Φ_R} has transitioned to become greater than the phase cut, rectified voltage VΦ_R_TH threshold, the ZC_DETECT output signal of the comparator 802 indicates the transition by changing from a logical 1 to a logical 0. The transition indicates detection of the first zero crossing $t_{ZC}(n)_1$. Then, the timer 804 begins counting at a frequency much greater than the frequency of phase cut, rectified voltage V_{Φ_R}. For example, in at least one embodiment, the timer 804 counts at a frequency of 10 kHz or greater. When the comparator 802 detects that the phase cut, rectified voltage V_{Φ_R} is less than the phase cut, rectified voltage VΦ_R_TH threshold, the ZC_DETECT output signal of the comparator 802 indicates the detection by changing from a logical 0 to a logical 1. The transition from logical 0 to logical 1 of the ZC_DETECT output signal indicates detection of the second zero crossing $t_{ZC}(n)_2$. The timer 804 then indicates the time between the detection of the two zero crossings, which is the approximate actual active time $T_A(n)$.

[0040] Figure 9 depicts a current control module 900, which represents one embodiment of a current control module 704. The current control module 900 includes a controllable current source 902. The current source 902 includes FETs 904 and 906, which are configured as a current mirror. Referring to Figures 7 and 9, in at least one embodiment, the controller 908 modulates the control signal CS_1 to control current through switch 707 to control power factor correction and regulate the link voltage V_{LINK} of the switching power converter 706, generate the trailing accelerator current value i_{R_ACCEL}, generate the low impedance state of the switching power converter 706, and dissipate excess power, as previously described.

[0041] Current source 902 supplies a reference current i_{REF}, which flows through FET 906. In at least one embodiment, control signal CS_1 turns boost switch 707 ON. The size of FET 904 is scaled to the size of FET 906 by a scaling factor of Z. The value of the scaling factor Z is a positive number and a matter of design choice. The value of the scaling factor Z times the value of the reference current i_{REF} sets the trailing accelerator current value i_{R_ACCEL}. Thus, when the trailing edge high resistance state predictor 412 predicts the occurrence of the high resistance state of the dimmer $t_{HR}(n)$, the controller 908 causes the controllable current source 902 to transfer the trailing accelerator current value i_{R_ACCEL} to the switching power converter 706.

[0042] Thus, an electronic system includes a controller, and the controller provides compatibility between an electronic light source and a trailing edge dimmer. In at least one embodiment, the controller is capable of predicting an estimated occurrence of a trailing edge of a phase cut AC voltage and accelerating a transition of the phase cut AC voltage from the trailing edge to a predetermined voltage threshold.

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- WO2008029108A **[0012]**
- US28984511A **[0033]**
- US28993111A **[0033]**
- US13289967B **[0033]**
- US85816410A **[0035]**
- US21717411A **[0035]**
- US96726907A **[0037]**
- US96727507A **[0037]**
- US49545709A **[0037]**
- US17440411A **[0037]**

Patentkrav

1. Anordning, der omfatter:

en effektomformer (406) og

en styreenhed (402) til at tilvejebringe kompatibilitet mellem en lampe (410) og en bagkantsdæmper (404), **kendetegnet ved, at** styreenheden omfatter:

et forudsigelsesmiddel (412) til at forudsige en estimeret forekomst af en høj modstandstilstand for bagkantsdæmperen (404), hvor den høje modstandstilstand forekommer, når bagkantsdæmperen starter faseskæring af et vekselstrøms- (AC) spændingssignal;

et strømstyringsmodul (416), der er forbundet med effektomformeren og konfigureret til at:

fungere i en første modus, hvori den øger en strøm (i_R) overført gennem bagkantsdæmperen (404) til effektomformeren (406) baseret på den estimerede forudsagte forekomst af den høje modstandstilstand for bagkantsdæmperen på en sådan måde, at øgningen af strømmen (i_R) accelererer en overgang af AC-spændingen fra bagkanten til en forudbestemt spændingstærskel.

2. Anordning ifølge krav 1, hvor forudsigelsesmidlet (412) forudsiger den estimerede forekomst af en høj modstandstilstand for bagkantsdæmperen baseret på en profil af spændingssignalet for N tidligere cyklusser af spændingssignalet, der forekom før en aktuel cyklus, hvor N er et heltal større end eller lig med 1.

3. Anordning ifølge krav 1, hvor

styreenheden fungerer i den anden modus indtil AC-spændingssignalets næste omtrentlige nulgennemgang efter faseskæringen af AC-spændingssignalet.

4. Anordning ifølge krav 1, hvor

styreenheden fungerer i den første modus, før bagkantsdæmperen starter faseskæring af et vekselstrøms- (AC) spændingssignal.

5. Anordning ifølge krav 4, hvor
styreenheden fungerer i den første modus inden for 0,1 millisekund, før bagkantsdæmperen starter faseskæring af et vekselstrøms- (AC) spændingssignal.

6. Anordning ifølge krav 1, hvor
styreenheden fungerer i den første modus for den estimerede forudsagte forekomst af den høje modstandstilstand for bagkantsdæmperen.

7. Anordning ifølge krav 2, hvor profilen er en profil af strøm trukket af lampen, eller hvor profilen er en spændingsprofil for lampen.

8. Anordning ifølge krav 7, der endvidere omfatter:
bestemmelse af spændingsprofilen baseret på en ændring af spændingen over tid for AC-spændingssignalet.

9. Anordning ifølge krav 1,
hvor strømstyringsmodulet (416) er konfigureret til at fungere i en anden modus, efter at AC-spændingssignalet når en lavspændingstærskel, hvor effektomformeren (406) overgår til lavimpedans.

10. Anordning ifølge krav 1, hvor forudsigelsesmidlet (412) er konfigureret til at forudsige den estimerede forekomst af en høj modstandstilstand for bagkantsdæmperen i en aktuel cyklus af AC-spændingssignalet baseret på en tendens for aktuelle forekomster af den høje modstandstilstand i *N* umiddelbart tidligere cyklusser af AC-spændingssignalet, hvor *N* er et heltal større end eller lig med 2.

11. Anordning ifølge krav 1, hvor AC-spændingssignalet er ensrettet AC-spænding afledt af en faseskærings-AC-indgangsforsyningsspænding.

12. Anordning ifølge krav 1, hvor styreenheden styrer effektomformeren, og hvor effektomformeren er koblet til bagkantsdæmperen og én eller flere elektroniske lyskilder inkluderet i lampen.

13. Anordning ifølge krav 1, hvor lampen omfatter et element af en gruppe bestående af: én eller flere lysdioder, én eller flere kompakte lysstofpærer, og én eller flere lysdioder og én eller flere kompakte lysstofpærer.

14. Fremgangsmåde til at tilvejebringe kompatibilitet mellem en lampe og en bagkantsdæmper, hvilken fremgangsmåde er **kendetegnet ved**:

forudsigelse af en estimeret forekomst af en høj modstandstilstand for bagkantsdæmperen, hvor den høje modstandstilstand forekommer, når bagkantsdæmperen starter faseskæring af et vekselstrøms- (AC) spændingssignal; anvendelse af en effektomformers (406) styreenhed i en første modus, hvori styreenheden øger en strøm (i_R) overført gennem bagkantsdæmperen (404) til effektomformeren (406) baseret på den estimerede forudsagte forekomst af den høje modstandstilstand for bagkantsdæmperen, og hvor strømøgningen accelererer en overgang af AC-spændingen fra bagkanten til en forudbestemt spændingstærskel.

15. Fremgangsmåde ifølge krav 14, hvor:
forudsigelse af den estimerede forekomst af faseskåret forkant af vekselstrøms- (AC) spændingssignalet er baseret på en profil af spændingssignalet for N tidligere cyklusser af spændingssignalet, der forekom før en aktuel cyklus, hvor *N* er et heltal større end eller lig med 1.

16. Fremgangsmåde ifølge krav 14, hvor fremgangsmåden endvidere omfatter en anden modus, efter at AC-spændingssignalet når en lavspændingstærskel, hvor effektomformeren (406) overgår til lavimpedans.

17. Fremgangsmåde ifølge krav 14, hvor forudsigelse af den estimerede forekomst af en høj modstandstilstand for bagkantsdæmperen sker i en aktuel cyklus af AC-spændingssignalet baseret på en tendens for aktuelle forekomster af den høje modstandstilstand i *N* umiddelbart tidligere cyklusser af AC-spændingssignalet, hvor *N* er et heltal større end eller lig med 2.

DRAWINGS

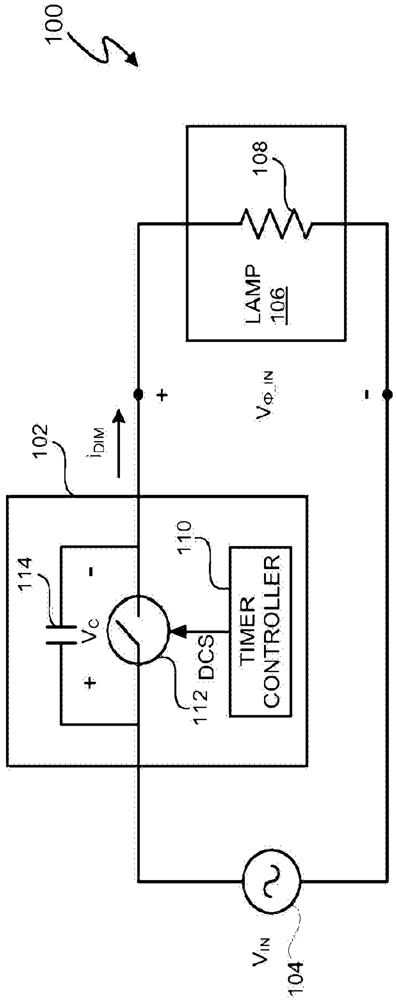

FIG. 1 (Prior Art)

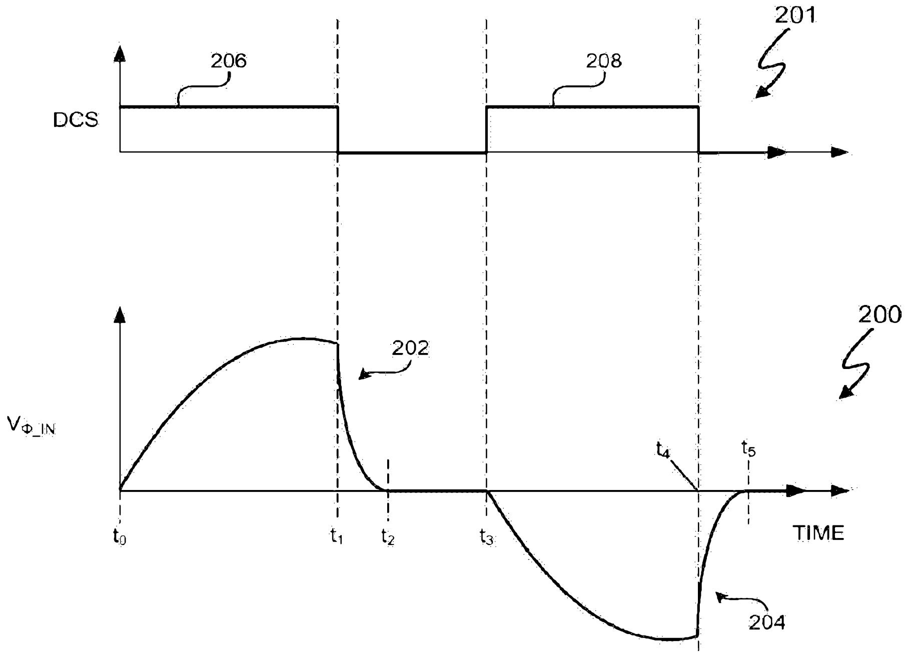

FIG. 2 (Prior Art)

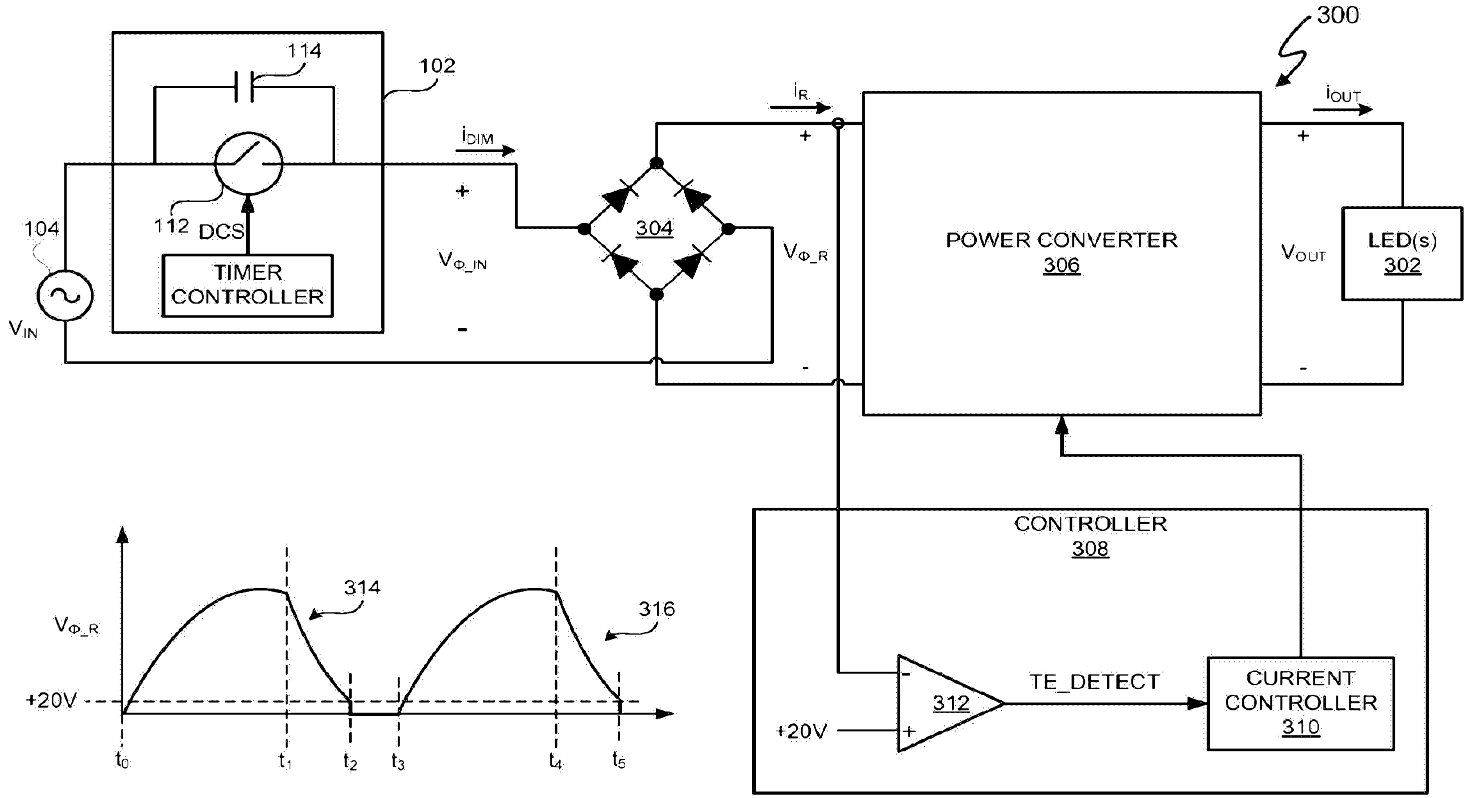

FIG. 3 (PRIOR ART)

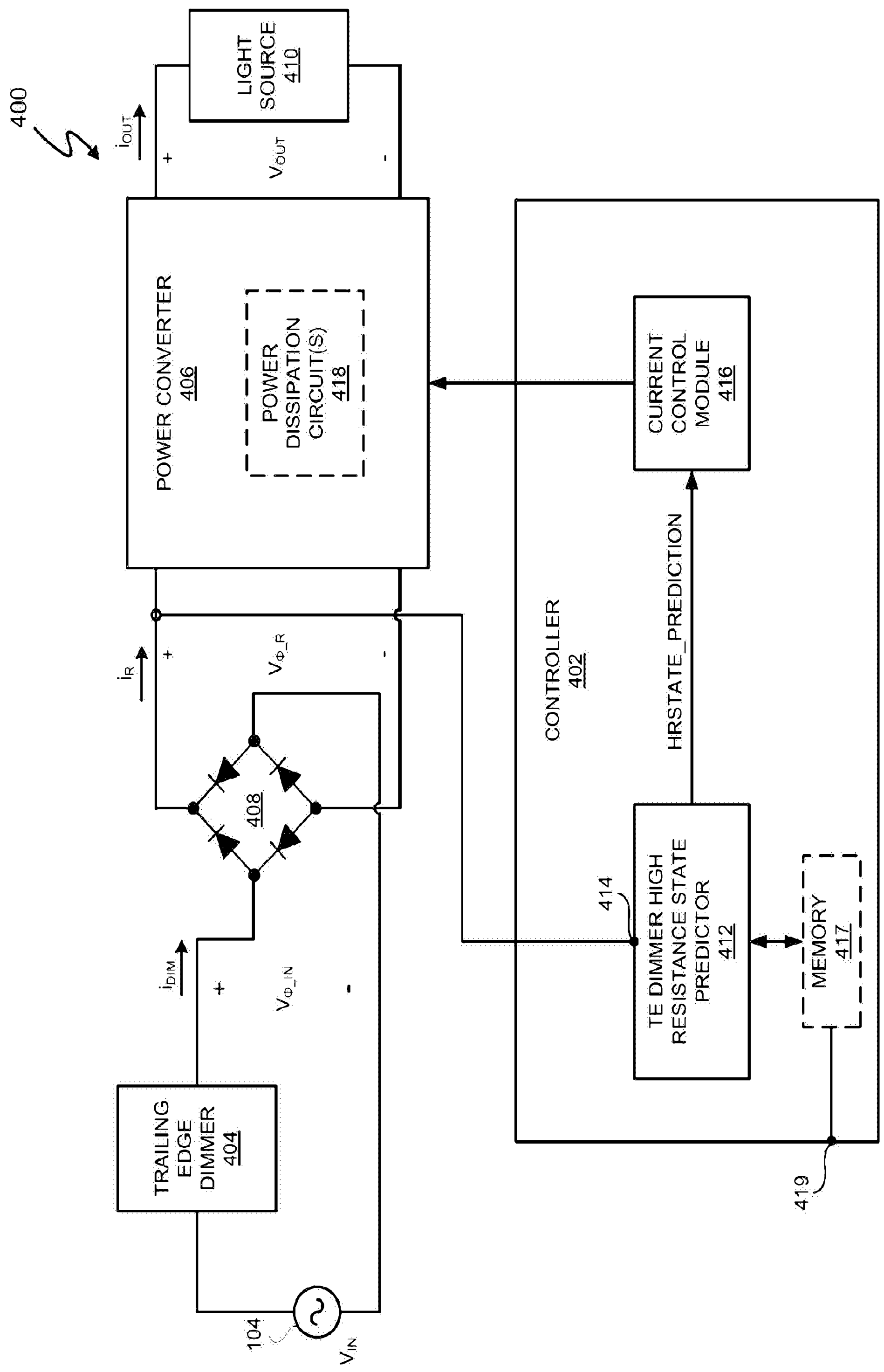
400
LIGHT SOURCE 410
i_{OUT}
+
V_{OUT}
-
POWER CONVERTER 406
POWER DISSIPATION CIRCUIT(S) 418
CURRENT CONTROL MODULE 416
HRSTATE_PREDICTION
CONTROLLER 402
i_R
+
V_{Φ_R}
-
408
414
TE DIMMER HIGH RESISTANCE STATE PREDICTOR 412
MEMORY 417
i_{DIM}
+
V_{Φ_IN}
-
TRAILING EDGE DIMMER 404
419
104
V_{IN}

FIG. 4

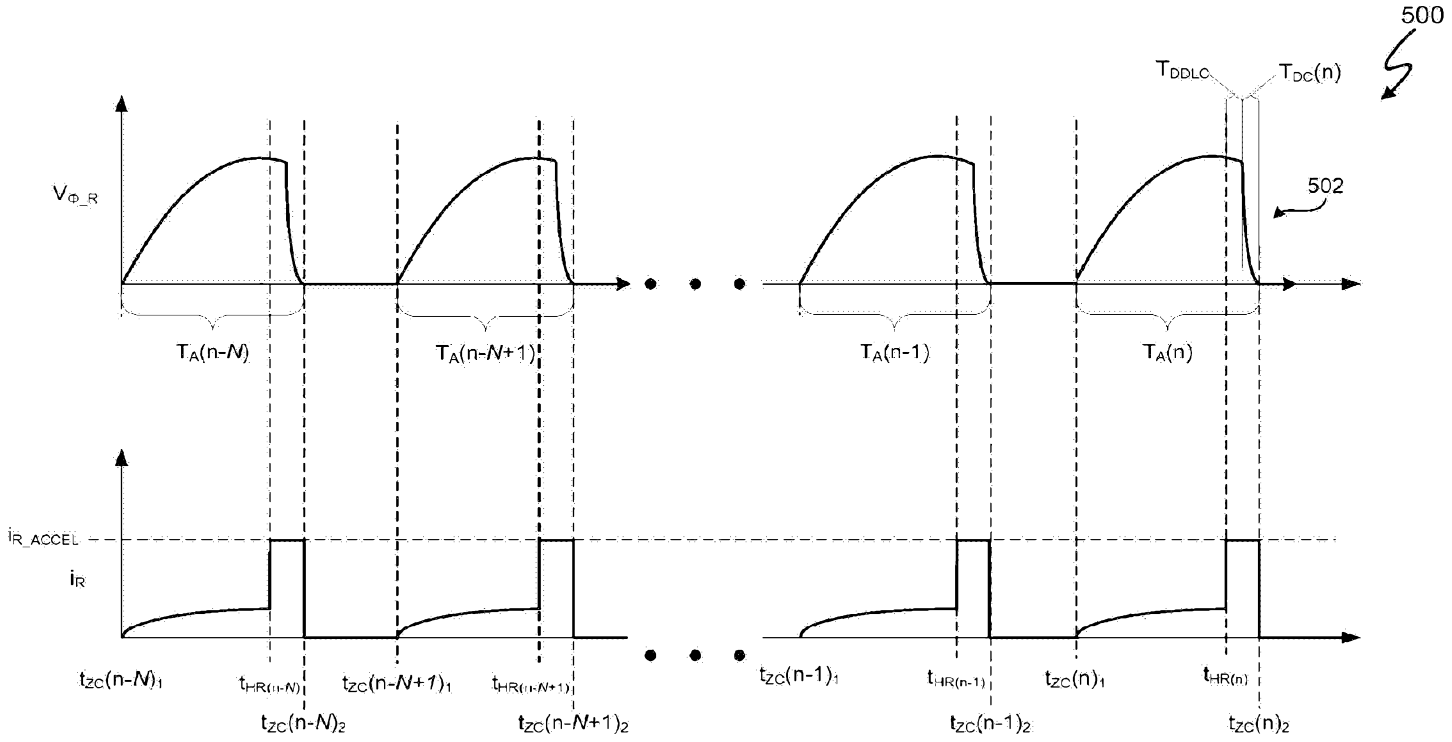
500
T_{DDLC}
$T_{DC}(n)$
502
V_{Φ_R}
$T_A(n-N)$
$T_A(n-N+1)$
$T_A(n-1)$
$T_A(n)$
i_{R_ACCEL}
i_R
$t_{ZC}(n-N)_1$
$t_{HR(n-N)}$
$t_{ZC}(n-N)_2$
$t_{ZC}(n-N+1)_1$
$t_{HR(n-N+1)}$
$t_{ZC}(n-N+1)_2$
$t_{ZC}(n-1)_1$
$t_{HR(n-1)}$
$t_{ZC}(n-1)_2$
$t_{ZC}(n)_1$
$t_{HR(n)}$
$t_{ZC}(n)_2$

FIG. 5

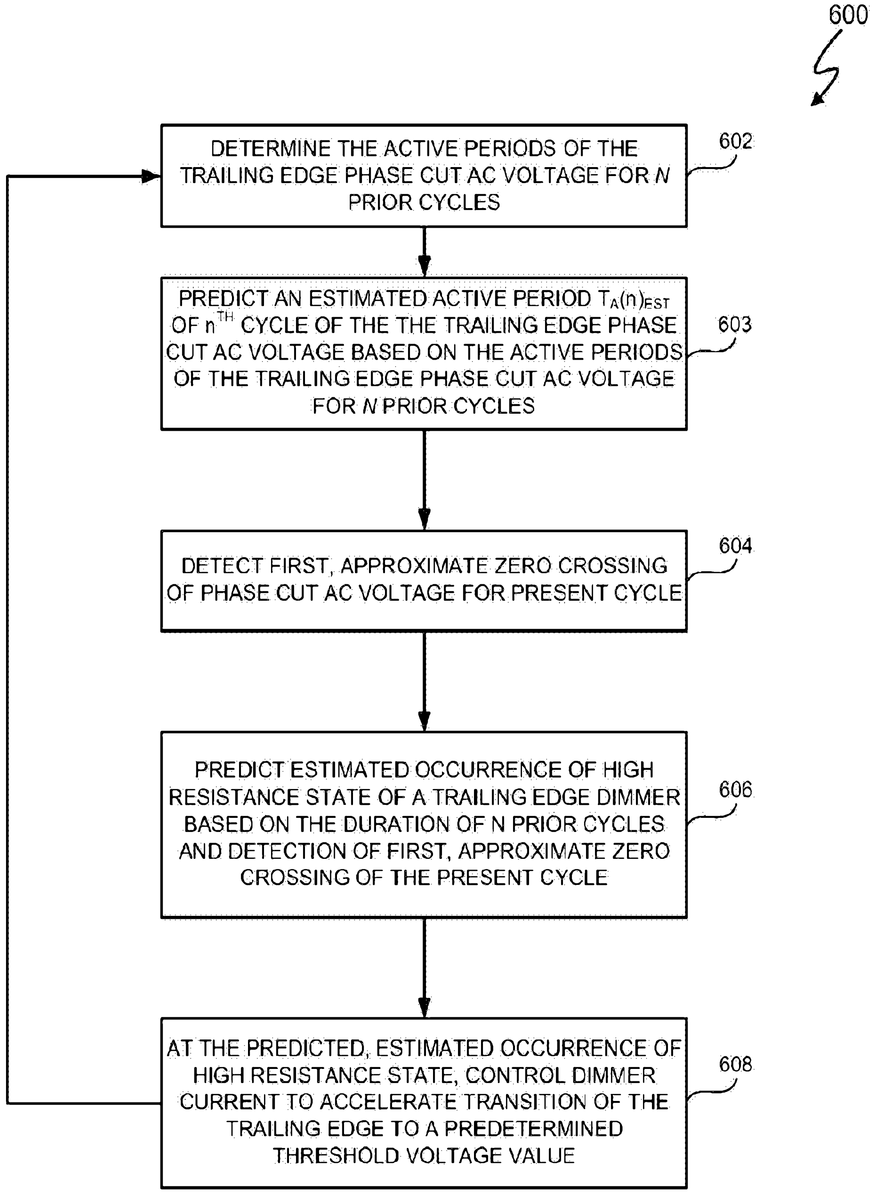
600
602
DETERMINE THE ACTIVE PERIODS OF THE TRAILING EDGE PHASE CUT AC VOLTAGE FOR N PRIOR CYCLES
603
PREDICT AN ESTIMATED ACTIVE PERIOD $T_A(n)_{EST}$ OF n^{TH} CYCLE OF THE THE TRAILING EDGE PHASE CUT AC VOLTAGE BASED ON THE ACTIVE PERIODS OF THE TRAILING EDGE PHASE CUT AC VOLTAGE FOR N PRIOR CYCLES
604
DETECT FIRST, APPROXIMATE ZERO CROSSING OF PHASE CUT AC VOLTAGE FOR PRESENT CYCLE
606
PREDICT ESTIMATED OCCURRENCE OF HIGH RESISTANCE STATE OF A TRAILING EDGE DIMMER BASED ON THE DURATION OF N PRIOR CYCLES AND DETECTION OF FIRST, APPROXIMATE ZERO CROSSING OF THE PRESENT CYCLE
608
AT THE PREDICTED, ESTIMATED OCCURRENCE OF HIGH RESISTANCE STATE, CONTROL DIMMER CURRENT TO ACCELERATE TRANSITION OF THE TRAILING EDGE TO A PREDETERMINED THRESHOLD VOLTAGE VALUE

FIG. 6

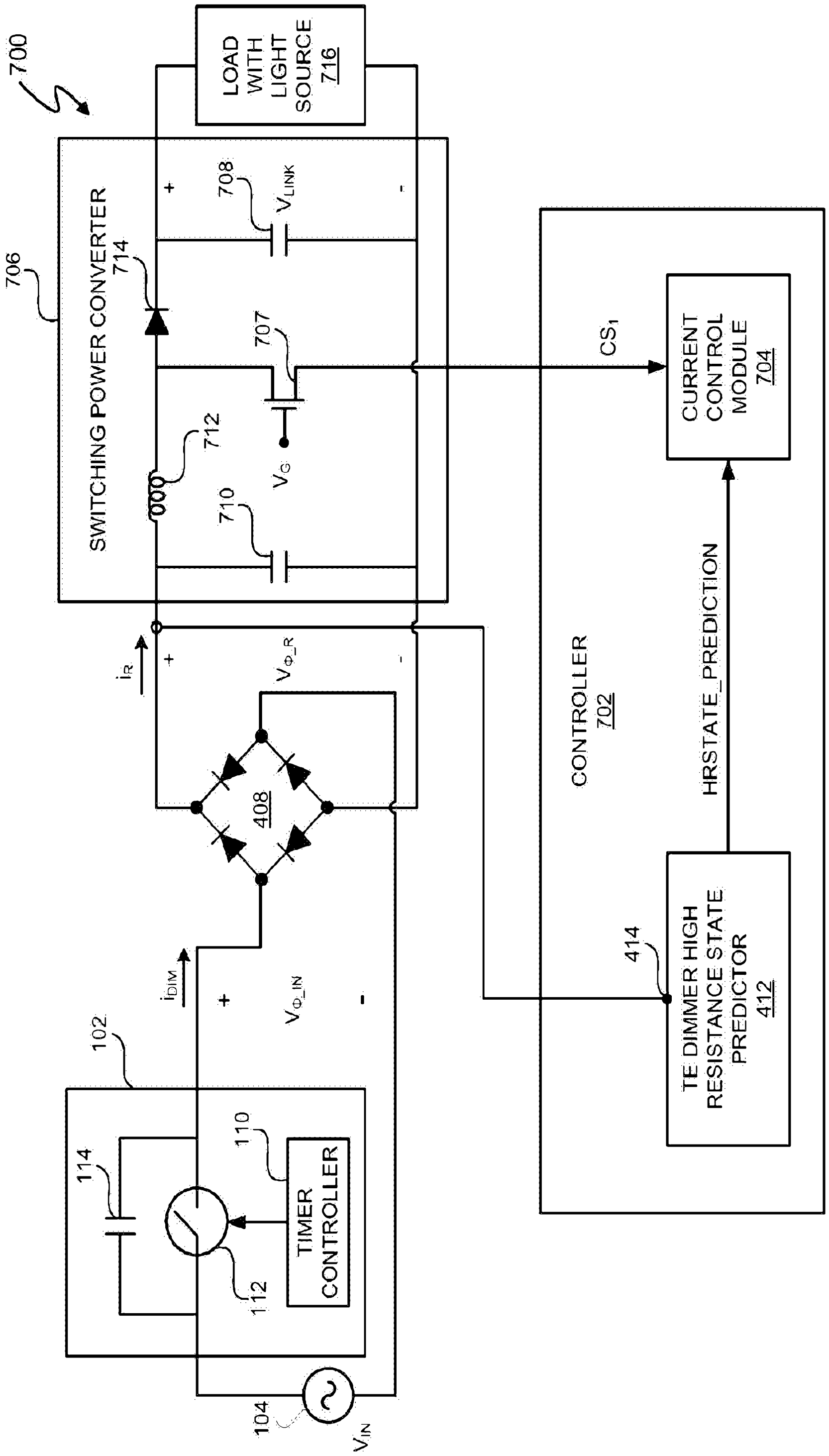
700
706
SWITCHING POWER CONVERTER
714
LOAD WITH LIGHT SOURCE 716
708
V_{LINK}
+
-
707
712
710
V_G
CS_1
CURRENT CONTROL MODULE 704
CONTROLLER 702
HRSTATE_PREDICTION
i_R
+
V_{Φ_R}
-
408
414
TE DIMMER HIGH RESISTANCE STATE PREDICTOR 412
i_{DIM}
+
V_{Φ_IN}
-
102
114
110
TIMER CONTROLLER
112
104
V_{IN}

FIG. 7

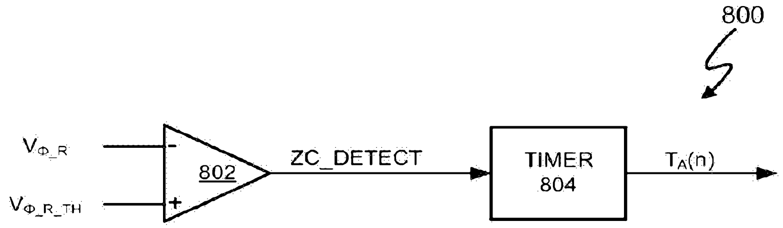
800
V_{Φ_R}
$V_{\Phi\_R\_TH}$
-
+
802
ZC_DETECT
TIMER
804
$T_A(n)$

FIG. 8

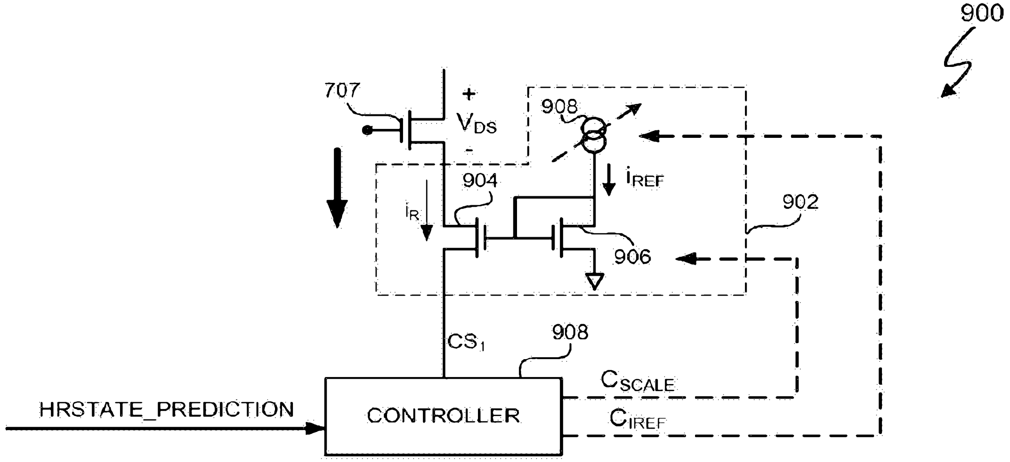
900
707
+
V_{DS}
-
908
i_{REF}
904
i_R
902
906
CS_1
908
C_{SCALE}
C_{IREF}
HRSTATE_PREDICTION
CONTROLLER

FIG. 9