



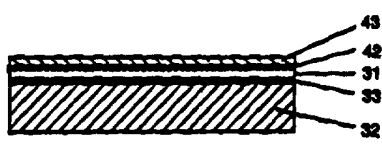
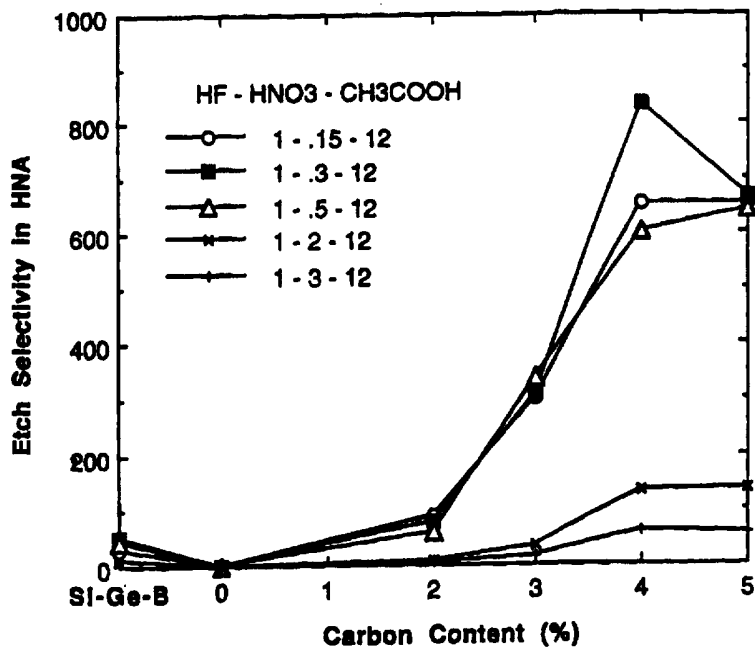
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<p>(21) International Application Number: PCT/US95/13883 (22) International Filing Date: 26 October 1995 (26.10.95) (30) Priority Data: 08/336,949 10 November 1994 (10.11.94) US (71) Applicant: LAWRENCE SEMICONDUCTOR RESEARCH LABORATORY, INC. [US/US]; 2300 W. Huntington Drive, Tempe, AZ 85282 (US). (72) Inventors: ROBINSON, McDonald; 5880 Hidden Lane, Goleta, CA 93117 (US). WESTHOFF, Richard, C.; 2559 N. Tamarisk Street, Chandler, AZ 85224 (US). HUNT, Charles, E.; 1224 Fordham Drive, Davis, CA 95616 (US). LING, Li; Apartment 68, 6300 S.W. 188th Court, Aloha, OR 97007 (US). ATZMON, Ziv; 3330 W. Frankfurt Drive, Chandler, AZ 85226 (US). (74) Agent: MOLL, Robert; Wilson, Sonsini, Goodrich &amp; Rosati, 650 Page Mill Road, Palo Alto, CA 94304-1050 (US).</p>		<p>(81) Designated States: CA, JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>

(54) Title: SILICON-GERMANIUM-CARBON COMPOSITIONS AND PROCESSES THEREOF

(57) Abstract

Silicon-germanium-based compositions comprising silicon, germanium, and carbon (i.e. Si-Ge-C), methods for growing Si-Ge-C epitaxial layers(s) (42) on a substrate (32), etchants especially suitable for Si-Ge-C etch-stops (42), and novel method of use for Si-Ge-C compositions are provided. In particular, the invention relates to Si-Ge-C compositions, especially for use as etch-stops and related processes and etchants useful for microelectronic and nanotechnology fabrication.



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**SILICON-GERMANIUM-CARBON COMPOSITIONS AND PROCESSES THEREOF****Background:**

The present invention relates to silicon-germanium-based compositions comprising silicon, germanium, and carbon (Si-Ge-C), methods for growing Si-Ge-C epitaxial layer(s) on a substrate, etchants especially suitable for Si-Ge-C etch-stops, and novel methods of use for Si-Ge-C compositions. In particular, the present invention relates to Si-Ge-C compositions, especially for use as etch-stops, related processes and etchants useful for microelectronic and nanotechnology fabrication.

10 In etching we remove a film or layer from a substrate, in some instances defining the layer to be removed by photolithography. One way to etch is to immerse the substrate in a bath of some chemical that attacks the film. Preferably, the chemical should react with and etch the film or layer in a smooth and reproducible manner, producing soluble products that can be carried away from the substrate. In particular, an ideal etchant will not attack any layer underneath the film being  
15 etched, so that the etch process will be self-limiting. Unfortunately, the etching is often not self-limiting and therefore goes below the desired depth. Etch-stops are designed to address this problem.

Semiconductors have the interesting property that when they are alloyed with certain elements, the rate of wet chemical etch in the alloy will vary from that of the unalloyed semiconductor. Alloys  
20 with different etch rates can be used to cause etching to slow at a pre-defined interface. Typically, a layer with a particular composition etches at a known rate in a etchant. A second adjacent layer may etch at a different rate because it has a different composition. The layer with the lower etch rate is often referred to as the etch-stop layer.

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Etch-stops are used to fabricate devices for a wide variety of applications. Membranes and diaphragms formed via etch-stops are used in sensors such as pressure transducers, as elements in experimental x-ray lithography systems, as windows for high energy radiation, and as low thermal mass supports for microcalorimeter and bolometric radiation detectors. Additional uses for  
30 selective etch-stops are in micromachining applications such as accelerometers, gears, micro-beams,

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miniature fluid lines, pumps and valves, and in flow sensors. Another application with a potentially large commercial market is in fabricating silicon-on-insulator (SOI) substrates by the bond-and-etch-back silicon-on-insulator (BESOI) process.

- 5 Silicon-based selective chemical etch-stop layers such as Si-B, Si-Ge, Si-Ge-B, Si-P, and Si-As have major problems and disadvantages which are overcome by the present invention. The disadvantages can be illustrated by examining examples pertaining to the commonly used Si-Ge-B etch-stops. First, the specially doped layer (e.g. Si-Ge-B) and the lightly doped silicon have limited selectivity. Selectivity is defined as the etch rate of lightly doped silicon divided by the etch rate  
10 of the etch-stop layer, or in some cases its reciprocal as discussed below. Limited selectivity increases the manufacturing cost by creating a need for tightly controlled, and sometimes labor-intensive processing to prevent the etch from going beyond the intended depth. This problem is exacerbated when fabricating the thin layers that are required for submicron electronic devices.
- 15 Certain chemical solutions etch a lightly doped silicon layer more rapidly than a heavily doped layer. For this purpose lightly doped means less than approximately  $1E17$  dopant atoms per  $cm^3$ , and heavily doped means more than approximately  $1E19$  dopant atoms per  $cm^3$ . For example, 21 weight percent (wt%) potassium hydroxide in  $H_2O$  (KOH- $H_2O$ ) at about  $70^\circ C$ , etches the (100) plane of lightly doped silicon rapidly (approximately 1 micrometer per minute), but the etch rate  
20 becomes slow (less than 0.01 micrometer per minute), making possible selective etching, as the boron concentration in the silicon increases to more than about  $5E19$  atoms per  $cm^3$ .

The conventional formulations of these etchants have serious problems when used with the above-mentioned etch-stop layers. For example, KOH- $H_2O$ , an inexpensive etchant, is prone to  
25 producing a rough surface when it etches silicon. Ethylenediamine pyrocatechol in water (EDP- $H_2O$ ) provides somewhat better etch selectivity and is less prone to developing surface roughness than KOH- $H_2O$ , but has limited application in that it emits extremely toxic vapors and is relatively expensive. Another etchant cesium hydroxide in water, (CsOH- $H_2O$ ), can provide smoother surfaces than KOH- $H_2O$  for conventional etch-stop layers but is even more expensive  
30 than EDP- $H_2O$ .

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Surface roughness arises from the anisotropic etch properties of the solutions that preferentially etch lightly doped silicon. These solutions etch certain crystallographic directions in the material faster than other directions. For example, a chemical solution consisting of 21 wt% KOH-H<sub>2</sub>O at 70°C will rapidly etch the (100) plane of lightly doped silicon, but only slowly etch the (111) plane.

5 This leads to the etched surface being rough as illustrated in Figures 1A-B. As shown in Figure 1A, a solution of KOH-H<sub>2</sub>O (11) will rapidly etch lightly doped silicon (12). If a small particle such as particle (13) adheres to the surface of the lightly doped silicon (12), the etch rate will be locally retarded under the particle (13). Slow etching planes (14) on the (111) plane will form as the particle (13) is undercut by the etch solution. This leads to the formation of a slow-etching

10 pyramid under the particle (13). If the etch selectivity is not sufficiently high these pyramids will propagate into the etch-stop layer (15) shown in Figure 1A as peaks (16), resulting in a rough surface.

Another problem with conventional etch-stop compositions, especially those containing a high

15 boron concentration, is they leave an insoluble staining residue on the surface of the substrate. This residue both roughens and contaminates the substrate surface. Increasing the KOH concentration of the etch solution, for example, from 21 wt% to 40 wt% will eliminate the surface staining, but also substantially decreases the etch selectivity.

20 In contrast to the above etchants, conventional formulations of 1:3:8 and 1:3:12 parts by volume of HF-HNO<sub>3</sub>-CH<sub>3</sub>COOH (HNA) etch lightly doped silicon somewhat less rapidly than heavily doped silicon and are therefore used to preferentially remove etch-stop layers. In this case, selectivity is defined as the etch rate of etch-stop layer divided by the etch rate of the lightly doped silicon. The above formulations of HNA have major drawbacks, including relatively low selectivity,

25 and selectivity decreasing rapidly with time during etching due to reduction of the HNO<sub>3</sub> to HNO<sub>2</sub>.

Still another problem with conventional etch-stop compositions is that the impurity which provides the etch selectivity is also a donor or acceptor dopant in the silicon. Thus, for example, when a Si-Ge-B etch-stop is used to fabricate a BESOI substrate, boron diffusing out from the etch-stop

30 layer during a bonding anneal causes unwanted electrically active dopant in the device layer. This problem is illustrated in Figures 2A-B which show concentration profiles of boron and germanium

as a function of depth in a substrate layer, an etch-stop layer, and a device layer, before a bonding anneal (Figure 2A) and after the anneal (Figure 2B). Figure 2A illustrates the boron (21) and germanium (22) concentration profiles in the substrate (23), the etch-stop layer (24), and in the device layer (25) after epitaxial layer growth and before the bonding anneal. Figure 2B shows the  
5 changed boron (26) and germanium (27) concentration profiles after the bonding anneal. Because boron diffuses through the material faster than germanium during the bonding anneal, its profile is broadened such that significant "diffusion tails" extend from the etch-stop layer into the substrate (23) and the device layer (25). In a BESOI structure the boron diffusion tail causes an unacceptable level of electrically active dopant to exist in the device layer (25).

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There are reports in the literature of Si-Ge-C layer fabrication. However, to the best of applicants' knowledge, none of the existing processes for forming Si-Ge-C are suitable for producing Si-Ge-C layers as part of a large scale manufacturing process. Feijóo et al., Etch Stop Barriers in Silicon Produced by Ion Implantation of Electrically Non-Active Species, *Journal of the Electrochemical*  
15 *Society* (1992) describe silicon layers implanted with silicon, germanium, and carbon at doses between  $1E14$  and  $3E16$  ions/cm<sup>2</sup> and energies between 35 and 200 keV and testing them as etch-stop barriers in an EDP-H<sub>2</sub>O based solution (p. 2309, Abstract). When ions are implanted in this range of dose and energies, the lattice structure is damaged. Feijóo states the results obtained indicate that the effectiveness of the etch-stop is influenced (i.e. improved) by both the implantation  
20 damage and the chemical interaction between the implanted ions and the defective crystal (Abstract). The resulting damage greatly restricts the number of useful commercial applications for Feijóo's etch-stop barriers. Accordingly, Feijóo's methods and results are substantially different from the present invention.

25 U.S. Patent No. 4,885,614 to Furukawa et al., Semiconductor Device with Crystalline Silicon-Germanium-Carbon Alloy, describes another process of producing a silicon-germanium-carbon alloy film principally by molecular beam epitaxy, but also by plasma enhanced chemical vapor deposition (CVD), photoenhanced CVD, microwave excited CVD, thermal CVD and metal-organic chemical vapor deposition methods. Molecular beam epitaxy  
30 (MBE) might provide good crystalline quality but is a slow and expensive process. With regard to a description of the thermal CVD process (col. 10, lines 37-43) Furukawa describes that the

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surface of a silicon substrate was cleaned and the temperature thereof adjusted to 650°C. Gaseous SiH<sub>4</sub>, GeH<sub>4</sub>, and CH<sub>4</sub> were allegedly introduced into a reactor so as to give a total pressure of 100 torr. Thus, a Si-Ge-C alloy film was purportedly formed on the substrate by a thermal CVD method. However, applicants believe methane at the stated process temperature is far too stable  
5 to function as a carbon source for thermal CVD formation of the silicon-germanium-carbon film. Further, Furukawa et al. do not recognize or discuss the use of Si-Ge-C as an etch-stop.

Regolini et al., Growth and characterization of strain compensated Si<sub>1-x-y</sub>Ge<sub>x</sub>C<sub>y</sub> epitaxial layers, *Materials Letters* (1993) describe metal-organic chemical vapor deposition (MOCVD) for  
10 fabricating epitaxial Si-Ge-C layers with less than 1 atomic percent carbon, which is far less than desirable for etch-stops. Further, there is no mention in the Regolini et al. publication of using Si-Ge-C as an etch-stop.

**Summary of Invention:**

- This invention describes a silicon-based etch-stop which is composed of an alloy containing silicon, germanium and carbon (Si-Ge-C). In one embodiment, this alloy demonstrates etch selectivity of 8000 to 1 compared with lightly doped silicon. High etch selectivity is demonstrated for both the case in which the Si-Ge-C epitaxial layer acts as the etch-stop, and for the opposite case in which the Si-Ge-C layer is preferentially removed.
- 10 This invention further describes a method by which the etch-stop layer is grown epitaxially and with excellent crystal quality by CVD onto a silicon substrate. One or more high quality, undoped or deliberately doped epitaxial silicon-based layers can be grown before and/or after the etch-stop layer.
- 15 This invention further describes an innovative range of etch solution compositions which, combined with the unique composition of the etch-stop layer, enhance the selectivity for removal of the etch-stop layer by more than two orders of magnitude over previous processes for etch-stop layer removal, and compared with previous formulations, provide an etch rate which varies far less with time. Further advantages will be apparent from the following description of the preferred
- 20 embodiments.



**Brief Description of the Drawings:**

Figures 1A-B are cross-sections illustrating surface roughness of conventional etch-stop layers.

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Figures 2A-B are graphs illustrating the dopant diffusion tail that is common with conventional etch-stop layers.

Figure 3 is a perspective view illustrating a SOI substrate.

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Figures 4A-F are cross-sections illustrating a BESOI process using an etch-stop layer.

Figures 5A-B are cross-sections illustrating reduced surface roughness with a Si-Ge-C etch-stop layer.

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Figures 6A-B are graphs illustrating the absence of an electrically active dopant tail with a Si-Ge-C etch-stop layer.

Figures 7A-F are ball-and-stick representations of crystal structure illustrating the effect of carbon and germanium atoms on stress in silicon alloys.

20

Figure 8 is a graph illustrating the superior etch selectivity of Si-Ge-C in KOH-H<sub>2</sub>O compared with Si-Ge-B.

Figure 9 is a graph illustrating the superior etch selectivity of Si-Ge-C in HNA compared with Si-Ge-B.

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Figures 10A-C are cross-sections illustrating a process for making a membrane using an etch-stop layer

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Figures 11A-C are cross-sections illustrating a process for making a cantilever beam using an etch-stop layer.

Figure 11D is a perspective view illustrating the cantilever beam formed using the process of  
5 Figures 11A-C.

**Detailed Description of the Preferred Embodiments:****Example: BESOI Fabrication:**

- 5 One important application of the present invention is in fabricating BESOI substrates. BESOI is used for advanced integrated circuit applications in which the device semiconductor layer (31) shown in Figure 3 is isolated from the base wafer (32) by an insulating layer (33). The following description illustrates advantages of the invention.
- 10 An embodiment of a BESOI process is illustrated in Figures 4A-F. As shown in Figure 4A, BESOI fabrication starts with two substrates, a base wafer (32) of a silicon wafer which can be either a lightly or heavily doped silicon wafer doped with either P-type or N-type dopant, such as boron or phosphorous, and a device wafer (41) of lightly doped silicon wafer of either of the same P-type or N-type dopants, and preferably a P-type dopant, such as boron. A Si-Ge-C layer (42) is grown
- 15 epitaxially onto the device wafer (41), and a device epitaxial silicon layer (31) is grown epitaxially onto the Si-Ge-C layer. The Si-Ge-C layer (42) is 50-500 nm thick, is preferably 75-200 nm thick, and is most preferably about 100 nm thick. The Si-Ge-C layer (42) includes 2-6 atomic percent carbon, preferably 4-5 atomic percent carbon, and most preferably about 4.5 atomic percent carbon, and includes 18-65 atomic percent germanium, preferably 35-50 atomic percent
- 20 germanium, and most preferably about 40 atomic percent germanium. The device silicon epitaxial layer (31) is 500-2000 nm thick, is preferably 100-150 nm thick, and is most preferably about 120 nm thick, and contains electrically active dopant of the P-type or N-type in the range of  $1E13$ - $1E19$  atoms per  $cm^3$ , preferably  $1E14$ - $1E18$  atoms per  $cm^3$ , and most preferably about  $1E15$  atoms per  $cm^3$ .
- 25 In the next step, thermal oxide layers (43, 44) shown in Figure 4B are grown by a conventional technique such as exposing the surface of either one or preferably both of the wafers (32, 41) to water vapor at 800-1000°C for about 5-300 minutes. W. S. Ruska, Microelectronic Processing (1987) describes such conventional techniques and is hereby incorporated by reference in its
- 30 entirety. The base wafer oxide layer (43) thickness is 50-1000 nm, preferably 100-500 nm, and most preferably about 200-300 nm. The device wafer oxide (44) thickness is 20-100 nm,

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preferably 40-70 nm, and most preferably about 50-60 nm. The oxide layer thickness is preferably less on the device wafer (41) than on the base wafer (32) so that the thermal oxidation step will not diffuse or precipitate the carbon out of the Si-Ge-C layer.

- 5 The next step is to invert the device wafer (41) and to bond it to the base wafer (32) by contacting the respective oxide surfaces (44, 43) firmly together to form an oxide layer (33) as shown in Figure 4C.

Figure 4D illustrates that in the next step most of the device wafer (41) is removed by lapping or  
10 grinding, and optionally polished by a conventional technique to form a sacrificial silicon layer (43). The thinning is preferably stopped when approximately 10 to 50 micrometers of the sacrificial layer (43) remains over the etch-stop layer (42).

Figure 4E illustrates the structure after the first selective etch step in which the final 10 to 50  
15 micrometers of the sacrificial layer (43) is removed using a chemical solution such as 10 to 45 wt% and preferably 21 wt% KOH-H<sub>2</sub>O, and in a temperature range of from 50 to 100°C, and preferably at about 70°C, which will etch the sacrificial layer (43), but will substantially stop etching when it reaches the etch-stop layer (42).

20 Figure 4F illustrates the result of the final etch step in which the etch-stop layer (42) shown in Figure 4E is removed using a chemical solution such as HNA at room temperature which etches the Si-Ge-C layer rapidly, but essentially stops etching when it reaches the lightly doped epitaxial device layer (31). The final structure, shown also in Figure 3, is the lightly doped epitaxial device layer (31) separated from the substrate (32) by the insulating oxide (33).

25 .

Figures 5A-B illustrate how the present invention solves the surface roughness problem involved in BESOI processing by the conventional method shown in Figure 1B. Figure 5A again shows a solution of KOH-H<sub>2</sub>O (11) will rapidly etch lightly doped silicon (12). Again if a small particle (13) adheres to the surface of the lightly doped silicon (12), the etch rate is locally retarded under the  
30 particle (13), and the slow etching planes (14) on the (111) plane form as the particle (13) is undercut by the etch solution. However, in the present invention, the resulting pyramidal defect

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will no longer propagate into the etch-stop layer (15) because of the improved selectivity of the etch-stop layer. As shown in Figure 5B, the surface roughness (51) is substantially reduced when the etch front reaches the etch-stop layer (15) due to the pyramidal defects being substantially etched away before the etch front significantly proceeds into the etch-stop layer (15).

5

Chemical vapor deposition of an epitaxial Si-Ge-C layer on silicon:

One aspect of the present invention is that we have discovered a method to grow Si-Ge-C layers epitaxially by a commercially viable CVD method onto silicon at temperatures that are low enough to "quench" carbon into the epitaxial layer. Low temperature is important because whereas the germanium-silicon system exhibits complete solid solubility, carbon is nearly insoluble in silicon. The maximum solubility of carbon in silicon is about 1 part per million at the melting point of silicon. Thus, to incorporate several atomic percent carbon into silicon the epitaxial layer growth takes place at a low enough temperature so that the carbon atoms are essentially immobile in the silicon lattice. In practice the growth temperature is preferably less than about 800°C. Numerous publications on the CVD growth of silicon carbide suggest that for most hydrocarbon gases a growth temperature greater than 1100°C is required to decompose the hydrocarbon precursor gases to supply a gas source of carbon. In the present invention, we discovered that cyclopropane or ethylene can provide a source of carbon that is sufficiently reactive to deposit carbon-containing layers in a CVD process at temperatures as low as 600°C.

We have further discovered that certain novel processes significantly improve the ability to grow high quality Si-Ge-C layers. For example, the following process produces Si-Ge-C epitaxial layers with 42 atomic percent germanium, 5 atomic percent carbon, and a low defect density. A lightly doped, P-type (100) 200 mm diameter prime silicon substrate is cleaned and loaded into a CVD reactor using a robotic transfer arm. A suitable reactor for this application is an Epsilon One, Model E-2, manufactured by ASM America, Phoenix Arizona. Initially, the reactor temperature is held in the range from 25-900°C, preferably 800-900°C, and most preferably about 850°C. Hydrogen gas is introduced into the reactor at preferably atmospheric pressure, or at reduced pressure of, for example, 5-100 torr, at a flow rate of 10-100 standard liters per minute (slm), preferably 15-40 slm, most preferably about 20 slm. Next, the substrate is heated to 1000-1200°C,

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preferably to 1100-1190°C, and most preferably to about 1150°C. The reactor is most preferably held at about 1150°C for 30 to 600 seconds, preferably 60 to 300 seconds, and most preferably about 90 seconds to remove the native oxide layer from the substrate. The substrate is then cooled to 900°C in the H<sub>2</sub> atmosphere before the deposition of silicon. At 900°C, 5 to 200 standard cubic centimeters per minute (sccm), preferably 10 to 50 sccm, and most preferably about 20 sccm of SiH<sub>2</sub>Cl<sub>2</sub> (dichlorosilane) is introduced into the reactor atmosphere to initiate deposition of the undoped or lightly doped epitaxial silicon. Deposition continues as the substrate is cooled further, and at 700°C a low flowrate (e.g., 0.1 sccm) of GeH<sub>4</sub> (germane) is added to the deposition atmosphere. The substrate is cooled still further, and at 550-750°C, preferably 600-700°C, and most preferably about 625°C the low flowrate of GeH<sub>4</sub> is increased over a span of 15 seconds to a final flowrate of from 1.0 to 20.0 sccm, preferably 1.4 to 5.0 sccm, and most preferably about 1.8 sccm. Just as the GeH<sub>4</sub> flowrate reaches its final value, C<sub>3</sub>H<sub>6</sub> (cyclopropane) is added at a low flowrate (e.g. 25 sccm) to the deposition atmosphere. The low flowrate of cyclopropane is increased over a span of 15 seconds to a final flowrate of from 50 to 200 sccm, preferably 75 to 150 sccm, and most preferably about 100 sccm. All final gas flowrates are then held constant for 1 to 100 minutes, preferably 5 to 10 minutes, and most preferably about 6.5 minutes while a Si-Ge-C layer of approximately 200 nm thickness is grown. Following deposition the reactor is purged with 20 slm of pure H<sub>2</sub> for about 45 seconds. Afterward the robotic transfer arm removes the substrate from the reactor. In an alternative embodiment, an alkene, such as ethylene can be substituted for cyclopropane in a similar process.

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The reasons for the above process improvements are as follows. The surface of silicon forms a tenacious silicon dioxide ( $\text{SiO}_2$ ) when exposed to air. This oxide is removed from silicon during heating in hydrogen to high temperature such as  $1150^\circ\text{C}$ , but the oxide tends to reform when the silicon surface is exposed to trace amounts of oxygen or water vapor at lower temperature. By starting the CVD silicon growth at  $900^\circ\text{C}$ , and by adding a small concentration of  $\text{GeH}_4$  to the gas at  $700^\circ\text{C}$ , we prevent trace amounts of oxygen and water vapor in the deposition atmosphere from causing oxide nuclei to form as the temperature is lowered to the level that is favorable for Si-Ge-C deposition. As this protective Si-Ge layer is deposited the  $\text{GeH}_4$  concentration is held low and ramped up quickly to keep the thickness and stress of the layer well below the critical thickness for formation of misfit dislocations. The  $\text{C}_3\text{H}_6$  flowrate is ramped from a low value to the final value for a totally different reason. In developing this process we discovered that the best crystalline quality is obtained by starting the Si-Ge-C deposition with a low concentration of hydrocarbon and then ramping the flowrate up until the desired carbon concentration is obtained. The reason may be related to the low solubility of carbon in silicon. Starting the Si-Ge-C deposition with a low surface concentration of carbon may be important in establishing a steady-state growth process in which carbon is incorporated in non-equilibrium concentrations into the silicon-germanium lattice.

An economical epitaxial layer growth process is important if the epitaxial single Si-Ge-C layers are to be used for commercial applications. As will be demonstrated in the examples which follow, the process which we discovered can be operated in a commercial CVD epitaxial reactor, at rates sufficiently high that the Si-Ge-C layers can be produced at prices comparable to present epitaxial silicon layers. A suitable reactor for this application is again the Epsilon One, Model E-2, manufactured by ASM America, Phoenix Arizona. The reactor can be configured for single wafer, automated processing using vacuum-compatible load lock ports and a nitrogen-purged robotic wafer transfer chamber. The load lock ports and the wafer transfer chamber effectively isolate the process chamber from atmospheric contamination. Evacuation of the load lock ports is important to prevent air from entering the process chamber and to remove adsorbed moisture from the surfaces of the substrates before processing.

High purity materials are important for low temperature, defect-free production of epitaxial Si-Ge-C layers. Hydrogen and nitrogen liquid sources having impurity levels less than 10 parts per billion (ppb) can be obtained from Air Products & Chemicals, Inc., in Allentown, PA. Dichlorosilane gas of Ultraplus grade can be obtained from Praxair, in Kingman, AZ; and a 1:99  
5 volume ratio and a 10:90 volume ratio of germane:hydrogen of Megabit grade can be obtained from Solktronic Chemicals, in Fairfield, NJ. The 10:90 volume ratio of cyclopropane:helium of semiconductor grade can be obtained from Air Products & Chemicals. The hydrogen, nitrogen, germane and cyclopropane gases can be further purified by point-of-use Nanochem purifiers made by Semi-Gas Systems, in Santa Clara, CA.

10

Additional processes and embodiments for the formation of thin heteroepitaxial films of Si-Ge-C grown on silicon substrates using CVD and  $C_2H_2$  gas as a carbon source at the relatively low temperature of  $625^\circ C$  are described in the unpublished manuscript by Z. Atzmon et al. Chemical Vapor Deposition Of Heteroepitaxial  $Si_{1-x}Ge_xC_y$  Films On (100)Si Substrates (Appendix A) which  
15 entire manuscript is hereby incorporated herein by reference.

#### Advantages of Si-Ge-C being isoelectronic:

An additional advantage of the Si-Ge-C etch-stop over the most commonly used Si-Ge-B etch-stop  
20 is that all three components of the Si-Ge-C alloy are isoelectronic, i.e., none supplies an electrically active dopant. Thus, if there is slight diffusion of one of the elements into the silicon device layer, the electrically active dopant concentration will not be affected. Further, since germanium and carbon affect the band structure and bandgap of silicon, it will be advantageous for some applications to leave the Si-Ge-C etch-stop layer in place to become part of the device structure.  
25 Figures 6A-B illustrate the point. Figure 6A illustrates carbon (61) and germanium (62) concentration profiles over a substrate (63), on which an epitaxial Si-Ge-C etch-stop layer (64) and a lightly doped device layer (65) have been epitaxially grown before a bonding anneal. This structure represents the starting point for a BESOI process, which can be compared to the Si-Ge-B structure shown in Figures 2A-B. In Figures 6A, the boron concentration (66) is deliberately low  
30 throughout the concentration profile. The substrate (63) is shown with a boron concentration of about  $1E17$  atoms per  $cm^3$ , and the epitaxial layers (64, 65) are grown with a boron concentration



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of about  $2E15$  atoms per  $cm^3$ . Figure 6B shows the concentration profiles after the bonding anneal. The carbon (67) and boron (68) profiles broaden during the anneal due to diffusion. In contrast to the Si-Ge-B etch-stop in Figure 2B, the carbon (69) in the device layer (65) of Figure 6B does not contribute electrical carriers and the substrate boron diffusion tail (70), residing in the etch-stop layer (64), does not contribute electrical carriers to the device layer (65).

Advantages of Si-Ge-C permitting strain control:

The present invention also permits strain control in the Si-Ge-C layer. Germanium and carbon atoms both differ in size from silicon. The fourfold covalent atomic radius of germanium, is about 5% larger than silicon, whereas carbon is about 50% smaller. The effects of germanium and carbon addition to silicon are shown schematically in Figures 7A-F. In undoped silicon there is naturally occurring spacing (71) between the silicon atoms represented as solid dots in Figure 7A. When germanium atoms are added to silicon, the lattice parameter or atomic spacing (72) in the crystalline structure is increased by the larger germanium atoms represented by the large white dots in Figure 7B. By contrast when carbon atoms represented by the small grey dots are added to silicon the atomic spacing (73) is decreased as shown in Figure 7C. As shown in Figure 7D, when a Si-Ge epitaxial layer represented by the upper three rows of solid and white dots is grown onto a silicon substrate represented by the lower five rows of solid dots, a compressive in-plane stress arises as the Si-Ge layer is forced to assume the atomic spacing (71) of the unstrained silicon substrate. The Si-Ge lattice expands in a direction normal to the silicon substrate to form spacing (74) causing a tensile strain in that direction. Conversely, when a Si-C layer is grown epitaxially onto a silicon substrate, the Si-C layer is under an in-plane tensile strain and a compressive strain in the direction normal to the silicon substrate. Thus, when either a Si-Ge or a Si-C layer is grown epitaxially onto silicon the growing layer experiences a stress that increases with the thickness of the layer and with the concentration of Ge or C. At some critical thickness the stress exceeds the yield stress, the point at which dislocations nucleate at the epitaxial layer-substrate interface and propagate to form a two-dimensional defect array (75) as illustrated in Figure 7E for the case of Si-Ge. This array of misfit dislocations allows the epitaxial layer to assume its unstrained atomic spacing (72), and in doing so relieves the stress in the epitaxial layer. If, however, the epitaxial layer includes Ge and C in a ratio defined by:  $(\text{atomic radius Si} - \text{atomic radius C})/(\text{atomic radius$

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Ge - atomic radius Si), about 9:1 Ge:C, the epitaxial layer will have similar atomic spacing (71) to undoped silicon and be free of stress as shown in Figure 7F. In this case, the epitaxial layer-substrate interface remains free of misfit dislocations.

5 In different applications it will be advantageous to grow Si-Ge-C layers that (1) are strain-free, or (2) have strain that is grown-in to a pre-defined level, or (3) have lattice parameter misfit at so high a level as to cause misfit dislocations to form. Fabrication of a cantilever beam in an accelerometer application is an example in which the layer should be grown stress free so that the beam will not be bowed. On the other hand when a Si-Ge-C layer is to be made into a membrane, a slightly  
10 tensile stress, created by increasing the carbon-to-germanium ratio, is desirable so that the membrane will be smooth and "tight". For semiconductor devices, both strain and composition are means by which the bandgap and band structure can be varied for particular applications. At the same time it is usually important for electronic applications that the epitaxial layers, whether strained or unstrained, must be free of defects including misfit dislocations. For some mechanical  
15 applications, on the other hand, it may be desirable to create an array of misfit dislocations. Such dislocations can strengthen the silicon by a process known as "work hardening".

The above-referenced interface misfit stress can be measured in any of several ways. One is to measure the interatomic spacing of a Si-Ge-C layer grown epitaxially onto a silicon substrate, in  
20 the direction perpendicular to the substrate surface, by precision X-ray diffraction. As long as the critical stress for formation of misfit dislocations has not been exceeded, the difference in lattice parameter between the epitaxial layer and the substrate is proportional to the stress in the grown layer. Another method is to measure the bow of a silicon substrate before and after depositing the epitaxial Si-Ge-C layer. The change in bow is related by a simple formula to the stress in the  
25 Si-Ge-C layer (P. Singer, "Film Stress and How to Measure It", Semiconductor International, October 1992, p. 58, which is incorporated by reference in its entirety).

Advantages of Si-Ge-C having high etch selectivity:

30 As Figures 8 and 9 illustrate the etch selectivity of the Si-Ge-C epitaxial layer is much higher than that of Si-Ge-B in both KOH-H<sub>2</sub>O and HNA etch solutions. In Figure 8, the etch selectivity of

Si-Ge-C in 21 wt% KOH-H<sub>2</sub>O is plotted against carbon content in the epitaxial layer, with the etch selectivity of a Si-Ge-B layer having 1E21 atoms per cm<sup>3</sup> of Ge and 2E20 atoms per cm<sup>3</sup> of B is shown on the left side of Figures 8 and 9 for comparison. The germanium content of the carbon-containing etch-stop layers increases approximately in proportion to the carbon content to  
 5 compensate strain, in atomic percent as follows:

	<u>Carbon</u>	<u>Germanium</u>	<u>Silicon</u>
	2 %	18 %	80 %
10	3 %	27 %	70 %
	4 %	36 %	60 %
	5 %	42 %	53 %

Here etch selectivity in KOH-H<sub>2</sub>O is defined as the etch rate of lightly doped silicon divided by the  
 15 etch rate of the etch-stop layer. Figure 8 is a graph of the selectivity of Si-Ge-C and Si-Ge-B etch stops with respect to lightly doped silicon. A selectivity of 8000:1 in 21 wt% KOH-H<sub>2</sub>O at 70°C has been measured by employing black wax to mask the etch-stop layer before exposing to the etchant, measuring the resultant step in the etch-stop layer and comparing that distance against the etch depth in lightly doped silicon under the same etchant. However, it is believed that by  
 20 employing a silicon nitride mask, the selectivity of the Si<sub>0.53</sub>Ge<sub>0.42</sub>C<sub>0.05</sub> etch-stop will be even higher. In any event, the selectivity of the Si-Ge-C etch-stop is apparently higher than that of SiO<sub>2</sub> and is a significant improvement over Si-Ge-B which shows a maximum selectivity of 2000:1 under the same conditions.

25 Figure 9 compares the etch selectivity of Si-Ge-B and Si-Ge-C as a function of carbon concentration in five HNA solutions. For etch-stop removal in HNA, etch selectivity is defined as the etch rate of the etch-stop layer divided by the etch rate of lightly doped silicon. Figure 9 illustrates that in HNA solution, the selectivity of the etch-stop layer is enhanced by two innovations. The five HNA solutions are prepared from standard aqueous reagents which are as  
 30 follows: 49 wt% HF, 70 wt% HNO<sub>3</sub>, and 99 wt% CH<sub>3</sub>OOH. First, we discovered that selectivity increases with carbon content, reaching a maximum selectivity at about 4 atomic percent carbon.

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Second, we discovered that selectivity increases as the  $\text{HNO}_3$  content of the HNA solution decreases, reaching maximum selectivity of more than 800:1 with the  $\text{HF}:\text{HNO}_3:\text{CH}_3\text{COOH}$  volume ratio of 1:0.3:12 and 4 atomic percent carbon. A further benefit of reducing the  $\text{HNO}_3$  concentration in the HNA solution is that the solution is stable against the chemical reduction of  $\text{HNO}_3$  to  $\text{HNO}_2$ , a problem that plagues users of the conventional 1:3:8 and 1:3:12 HNA compositions. It is an important advantage that our etch solutions remain colorless and etch selectivity is independent of time for etch times of 30 minutes or more (1:3:8 and 1:3:12 HNA solutions turn yellow and lose selectivity rapidly over the first few minutes of use). We discovered that the novel HNA formulations also will increase the etch selectivity of Si-Ge-B as the  $\text{HNO}_3$  concentration of the solution is decreased reaching a maximum of 50.

The unique properties of the Si-Ge-C etch-stop layers combined with the new HNA etch compositions are suggested by the behavior of the Si-Ge-C surface in the etch solution. The etch solution is believed to work by simultaneously oxidizing the surface (performed by the  $\text{HNO}_3$ ) and etching the oxide (performed by the HF). Si-Ge-C surfaces are hydrophilic when they emerge from the HNA solutions for all etch compositions from 1:3:12 to 1:0.1:12 in contrast to lightly doped Si with hydrophobic surfaces, indicating that the oxide removal performed by HF dominates the etching rate of Si-Ge-C layers.

Favorable results are believed to be obtained for etch selectivity in HNA when the silicon is in the range of 50 to 90 atomic percent, the germanium is in the range of 9 to 50 atomic percent, and the carbon is in the range of 1 to 10 atomic percent, preferably in the range of 3 to 6 atomic percent. More preferably, the Si-Ge-C is in the range for Si, Ge and C of 50-60 atomic percent, 36-45 atomic percent, and 4-5 atomic percent, respectively.

25

We believe that the some of useful ranges of Si-Ge-C compositions are: silicon in a range of 0 to 99.9 atomic percent, preferred 45 to 83 atomic percent, further preferred about 55.5 atomic percent, germanium in a range of 1 to 92 atomic percent, preferred 15 to 50 atomic percent, and further preferred about 40 atomic percent, and carbon in the range of 0.1 to 10 atomic percent, preferred 2 to 6 atomic percent, and further preferred about 4.5 atomic percent.

30

Examples: Si-Ge-C Etch-Stop in Nanotechnology ApplicationsA. Membrane

5 One example of silicon membrane fabrication is illustrated in Figures 10A-C. As shown in Figure 10A, Si-Ge-C layer (101) is epitaxially grown onto a lightly doped, conventional polished silicon substrate (102). Favorable results can be achieved by using the processes described earlier in the section on epitaxial growth of Si-Ge-C layers by CVD on silicon. The silicon substrate (102) and Si-Ge-C layer (101) form a structure which is inverted as shown in Figure 10B and an oxide layer  
10 (104) is formed on the back side of the silicon substrate (102). A positive photoresist (not shown) is applied to the oxide layer (104), and then exposed through openings in the mask. The exposed and developed photoresist is removed and then the underlying exposed oxide layer is removed with a conventional HF solution. The exposed portion of the back side of the silicon substrate (102) is etched by a 21 wt% KOH-H<sub>2</sub>O etchant that rapidly removes the lightly doped silicon substrate  
15 (102) as indicated by surface (103) formed during an intermediate stage of the etch, but then etches at a slower rate when it reaches the Si-Ge-C (101) as shown in Figure 10C. As shown in Figure 10C, when the etching is complete the Si-Ge-C layer (101) remains as a membrane supported by a silicon substrate frame (105) defined the remaining portions of the silicon substrate (102). The carbon-to-germanium ratio in the etch-stop layer is adjusted so that the Si-Ge-C membrane (101) is preferably in tension. This ensures that the membrane (101) is "tight" and well supported by the  
20 frame (105).

B. Cantilever Beam

25 Another example of a micromechanical application of a Si-Ge-C epitaxial etch-stop layer is in fabricating a cantilever beam as illustrated in Figures 11A-C. In Figure 11A, a Si-Ge-C etch-stop layer (111) and a lightly doped silicon layer (112) are grown onto a silicon substrate (113). A masking oxide (114) shown in Figure 11B is grown and patterned using a technique like that used in the membrane fabrication, and the exposed portion of the lightly doped silicon (112) is etched  
30 by a 21 wt% KOH-H<sub>2</sub>O etchant that rapidly removes the lightly doped silicon but etches very slowly when it reaches the Si-Ge-C layer (111). Next, the Si-Ge-C layer (111) is etched by HNA

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that rapidly removes the exposed Si-Ge-C layer (111) as shown in Figure 11C, but only etches lightly doped silicon very slowly. In this way the cantilever beam (115) formed from the lightly doped silicon layer (112) is freed from the surrounding silicon substrate. Figure 11D is a perspective drawing showing the finished cantilever beam (115) attached to the rest of the lightly doped silicon layer (112) at one end. Other precision micro-miniature structures can be fabricated using processes like this.

It will be appreciated by those of ordinary skill in the art that many variations in the foregoing embodiments are possible while remaining within the scope of the present invention. Thus, the invention has applications well beyond those enumerated. The present invention should thus not be considered limited to the preferred embodiments.

CHEMICAL VAPOR DEPOSITION OF HETEROEPITAXIAL  
 $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  FILMS ON (100)Si SUBSTRATES

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Thin heteroepitaxial films of  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  have been grown on (100)Si substrates using atmospheric pressure Chemical Vapor Deposition (CVD) at 625°C. The crystallinity, composition and microstructure of the SiGeC films were characterized using Rutherford backscattering spectrometry, secondary-ion-mass-spectrometry and cross-sectional transmission electron microscopy. The crystallinity of the films was very sensitive to the flow rate of  $\text{C}_2\text{H}_2$  which served as the C source. Films with up to 2% C were epitaxial with good crystallinity and very few interfacial defects. Between 800 and 900 sccm of 10%  $\text{C}_2\text{H}_2$  in He, the C content increased dramatically from 2% to 10% and the as-grown films changed from crystalline to amorphous. In order to establish deposition conditions for the crystalline-amorphous phase transformation, one SiGeC film was deposited as the 10%  $\text{C}_2\text{H}_2$  flow was increased linearly from 500 to 1500 sccm during growth. When the C content reached ~4%, the film developed considerable stacking defects and disorder, and at around 11% C, the film became amorphous.

APPENDIX A

The significant successes of semiconductor electronic devices are closely connected to the concept of band gap engineering. The band gap of Si-based materials has been successfully engineered by alloying with Ge and by forming strained layer superlattices<sup>1</sup>. The band gap decreases monotonically as the Ge concentration increases, although compressive strain in pseudomorphic  $\text{Si}_{1-x}\text{Ge}_x$  grown epitaxially on (100)Si substrates causes stability problems and limits the film thickness. In many applications it is desirable to have a wider band gap than that of pure Si. Carbon in its diamond form is an elemental group-IV insulator (wide band gap of 5.5 eV) with a lattice parameter of 0.3545 nm, much smaller than that of Si (0.5431 nm) or Ge (0.5646 nm). Adding substitutional carbon into SiGe alloy layers may increase the band gap<sup>2</sup> and, at the same time, result in strain compensation<sup>3,4</sup>. In fact, strain in  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  alloy layers can be adjusted over a wide range from compressive all the way to tensile, depending on the Ge/C concentration ratio. If Vegard's law is applied to the SiGeC ternary system, then we expect compensation of 8.2 at% Ge by 1 at% C in the pseudomorphic  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  film<sup>5</sup>. Recently, strain compensation by sequential implantation of C in SiGe alloy layers has been investigated by forming  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  layers embedded in Si<sup>6,7</sup>. However, since the maximum solubility limit of C in Si is  $2 \times 10^{-3}$  at%, precipitation of silicon carbide has been a severe problem, particularly since higher temperatures are required to grow the structure and repair implantation damage. This paper is focused on the growth of pseudomorphic  $\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  layers on (100)Si substrates using Chemical Vapor Deposition (CVD).

$\text{Si}_{1-x-y}\text{Ge}_x\text{C}_y$  layers were epitaxially grown on (100)Si in an EPSILON ONE, model E-2 single wafer, automated CVD reactor using  $\text{SiH}_2\text{Cl}_2$  as a Si source,  $\text{GeH}_4$  as a Ge source, and  $\text{C}_2\text{H}_2$  as the C source at atmospheric pressure. Point of use purifiers on the gas lines provide purity levels in the parts-per-billion range in the process chamber. Nitrogen purged load locks exclude air from the system. Four different samples were grown at 625°C at various  $\text{C}_2\text{H}_2$  flows while the flows of the other two precursors were held constant. The growth conditions are summarized in Table I. Rutherford backscattering spectrometry (RBS) in the channeling mode and the  $^{12}\text{C}(\alpha,\alpha)^{12}\text{C}$  elastic resonance reaction at 4.265 MeV were used to determine the composition.



thickness and crystalline quality of the grown layer. The distribution of carbon within the films was characterized by secondary-ion-mass spectroscopy (SIMS), and the morphology of the grown layers was examined by cross-sectional transmission electron microscopy (TEM).

Figures 1 a and b show the 2.0 MeV He<sup>2+</sup> RBS random and (100) channeled spectra for the as-grown A-6 and B-6 samples, respectively. The measured values for  $\chi_{\min}$  ranged from 0.05 to 0.08 for sample A-6 and 0.13 to 0.22 for sample B-6, with the higher values obtained close to the SiGeC/Si interface in both samples. A significant yield enhancement was observed in the Si substrate region of the spectrum. This enhancement was caused by dechanneling which suggested the presence of misfit dislocations at the SiGeC/Si interface. The carbon content of these samples was measured by the <sup>12</sup>C( $\alpha,\alpha$ )<sup>12</sup>C elastic resonance reaction using a 4.28 MeV beam of He<sup>++</sup> ions. It was found that the fractions of Ge and C in the Si<sub>1-x-y</sub>Ge<sub>x</sub>C<sub>y</sub> layer were x=0.37 and y=0.012 for sample A-6 and x=0.36 and y =0.02 for sample B-6. The SIMS carbon profiles for these samples showed that the carbon was distributed uniformly in the alloy layer.

Figure 2 shows the 2.0 MeV He<sup>2+</sup> RBS random and (100) channeled spectra for the as-grown sample C-6. The overlapping of the random and aligned spectra that exists in the SiGeC region indicates that this layer was not grown epitaxially on the (100)Si substrate. The fraction of C in the alloy, as measured by resonance analysis, was y=0.10 while the Ge fraction was x=0.27. SIMS analysis showed that carbon was distributed uniformly in the alloy layer, and cross-sectional TEM showed that the SiGeC layer was amorphous. It was observed that for a relatively small increase in the C<sub>2</sub>H<sub>2</sub> flow (from 800 to 900 sccm) the carbon content increased dramatically and the layer went from crystalline to amorphous. Thus under these growth conditions it appears that there is a critical level of C<sub>2</sub>H<sub>2</sub> flow that changes the growth from epitaxial to amorphous, while the incorporated carbon increases from 2 at% to 10 at%. Determination of this critical flow level may be very important since this parameter affects directly the maximum concentration of carbon that can be incorporated into the single crystal SiGe matrix during the epitaxial growth that takes place in this CVD system.

In order to investigate this critical flow level, another sample was grown (sample D-6) using the same conditions (shown in Table I), except that the  $C_2H_2$  flow was increased linearly from 500 sccm at the beginning of growth to 1500 sccm at the end. Figure 3 shows the 2.0 MeV  $He^{2+}$  RBS random and (100) channeled spectra for this sample. We observe that the channeled spectrum overlaps the random spectrum for both Si and Ge signals at the region near the surface, indicating the presence of an amorphous layer, while for the region of the spectrum closer to the SiGeC/Si interface the yield of the channeled spectrum decreases sharply. These observations reveal that at the beginning of the growth process the SiGeC was grown epitaxially, but that a crystalline-amorphous phase transformation occurred sometime during the growth process. The random spectrum shows that the Ge concentration decreases monotonically from the interface to the surface while the Si concentration does not change significantly.

A cross-sectional TEM micrograph and calibrated carbon SIMS profile of sample D-6, shown in figure 4, corroborate the RBS results. Based on these results, the SiGeC layer can be roughly divided into three regions. Immediately adjacent to the SiGeC/Si interface there is a crystalline region, ~90 nm thick, with a roughly linear increase in carbon concentration up to ~4 at%. The next region, 30-40 nm thick, is highly defective and contains many lattice defects such as stacking faults and twins. The carbon concentration in this region increases sharply from 4 to ~10 at%. The third region near the surface is completely amorphous, ~80 nm thick, and the carbon concentration is ~10-12 at%.

The concentration of the alloy obtained at the crystalline/defective region interface is  $Si_{0.62}Ge_{0.34}C_{0.04}$  (shown in Fig. 4), which is probably the highest C content that can be achieved without defects in the crystalline layer under these CVD conditions. The Ge:C ratio at this point is 8.5:1, which is very close to the fully strain-compensated value (8.2:1) that was calculated using Vegard's law<sup>5</sup>. This Ge:C ratio decreases dramatically in the defective region to a minimum value of 2.9:1 at the defective region/amorphous interface. Thus when tensile strain appears during growth (Ge:C < 8.2:1) the SiGeC layer becomes defective; at very high tensile strain when Ge:C < 3:1 the layer completely loses crystallinity and an amorphous layer is formed.

In spite of the fact that the  $C_2H_2$  flow was increased linearly during growth, the carbon profile, as depicted by SIMS analysis, has a sigmoidal shape. This result indicates that carbon atoms can be incorporated into the SiGe matrix of the grown layer much more easily when it is in an amorphous state, i. e. the  $C_2H_2$  precursor is more reactive when it comes into contact with an amorphous substrate relative to a crystalline one. The  $GeH_4$  precursor behaves in the opposite manner, since the Ge concentration decreases during growth. The reactivity of the  $SiH_2Cl_2$  precursor, however, did not change.

In summary, CVD of  $Si_{1-x-y}Ge_xC_y$  alloy layers on (100)Si substrates is reported. Alloy layers with up to 2 at% of carbon have been grown epitaxially, and have good crystallinity. Above a critical level of  $C_2H_2$  flow, when the Ge:C ratio of the deposited layer is higher than 8.5:1, the grown layer becomes increasingly defective, and when Ge:C < ~3:1, an amorphous layer is eventually formed.

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**FIGURES CAPTIONS**

**Fig. 1:** 2.0 MeV He<sup>2+</sup> RBS random and (100) channeled spectra for: (a) sample A-6; (b) sample B-6. The dechanneling observed close to the SiGeC/Si interface suggested the presence of misfit dislocations.

**Fig. 2:** 2.0 MeV He<sup>2+</sup> RBS random and (100) channeled spectra for sample C-6. The SiGeC was not grown epitaxially on the (100)Si substrate.

**Fig. 3:** 2.0 MeV He<sup>2+</sup> RBS random and (100) channeled spectra for sample D-6. The SiGeC was initially grown epitaxially. A subsequent c-a phase transformation occurred.

**Fig. 4:** Cross-sectional TEM micrograph and corresponding calibrated carbon SIMS profile of sample D-6. The SiGeC can be roughly divided into three regions: crystalline, highly defective and amorphous region.

LIST OF TABLES

Table I: Sample growth conditions in CVD system.

Figure 1a

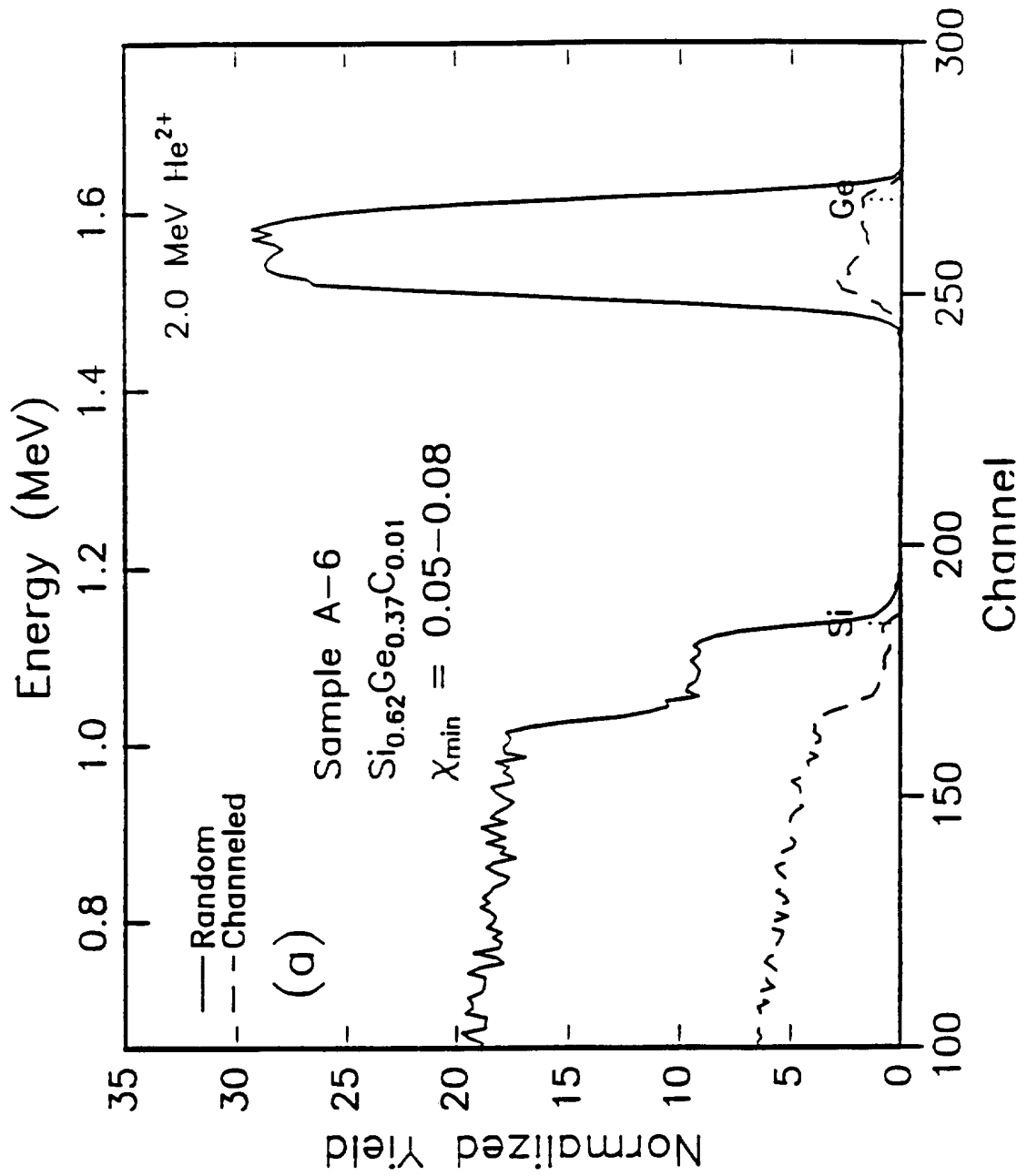


Figure 1b

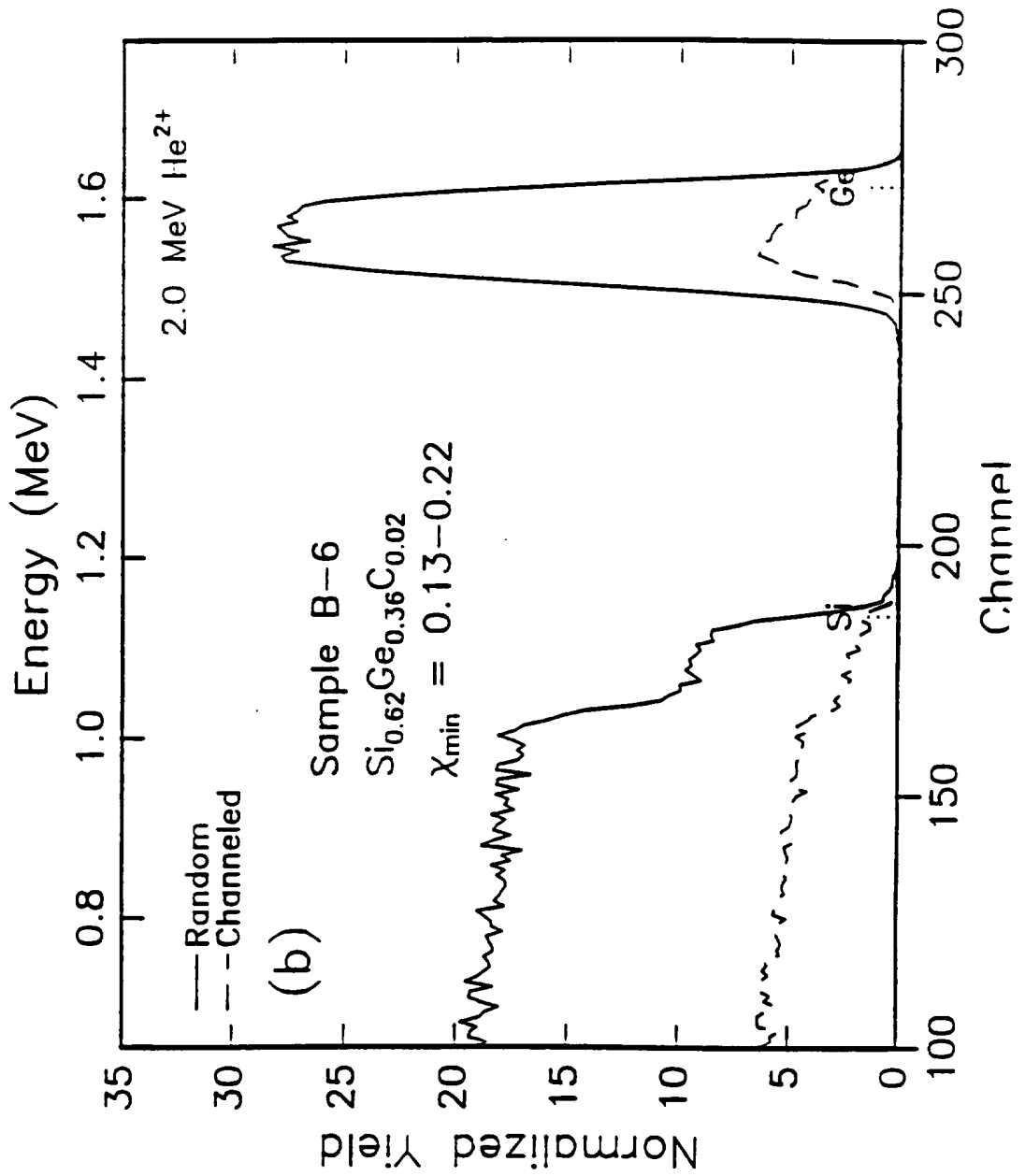




Figure 2

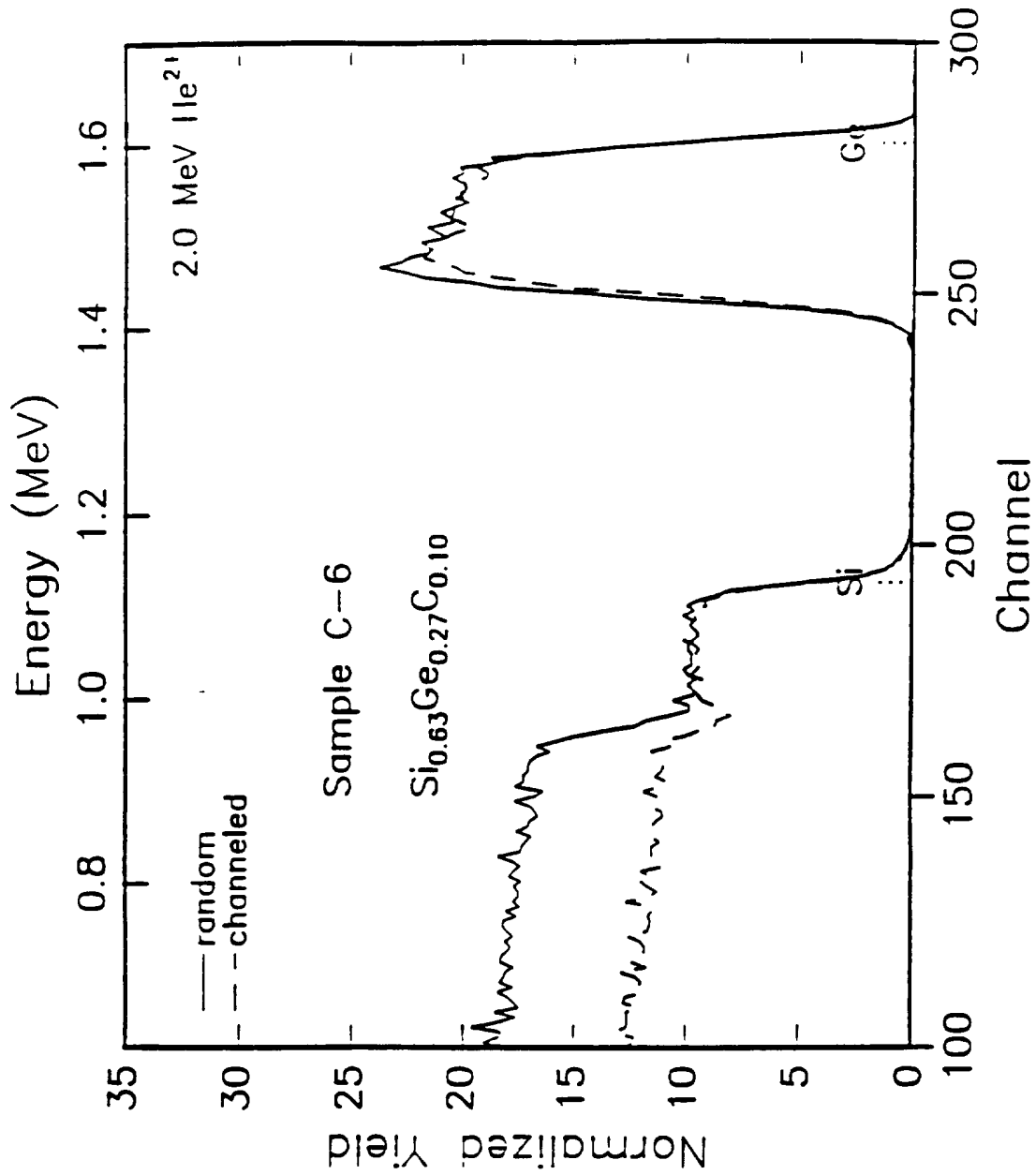


Figure 3

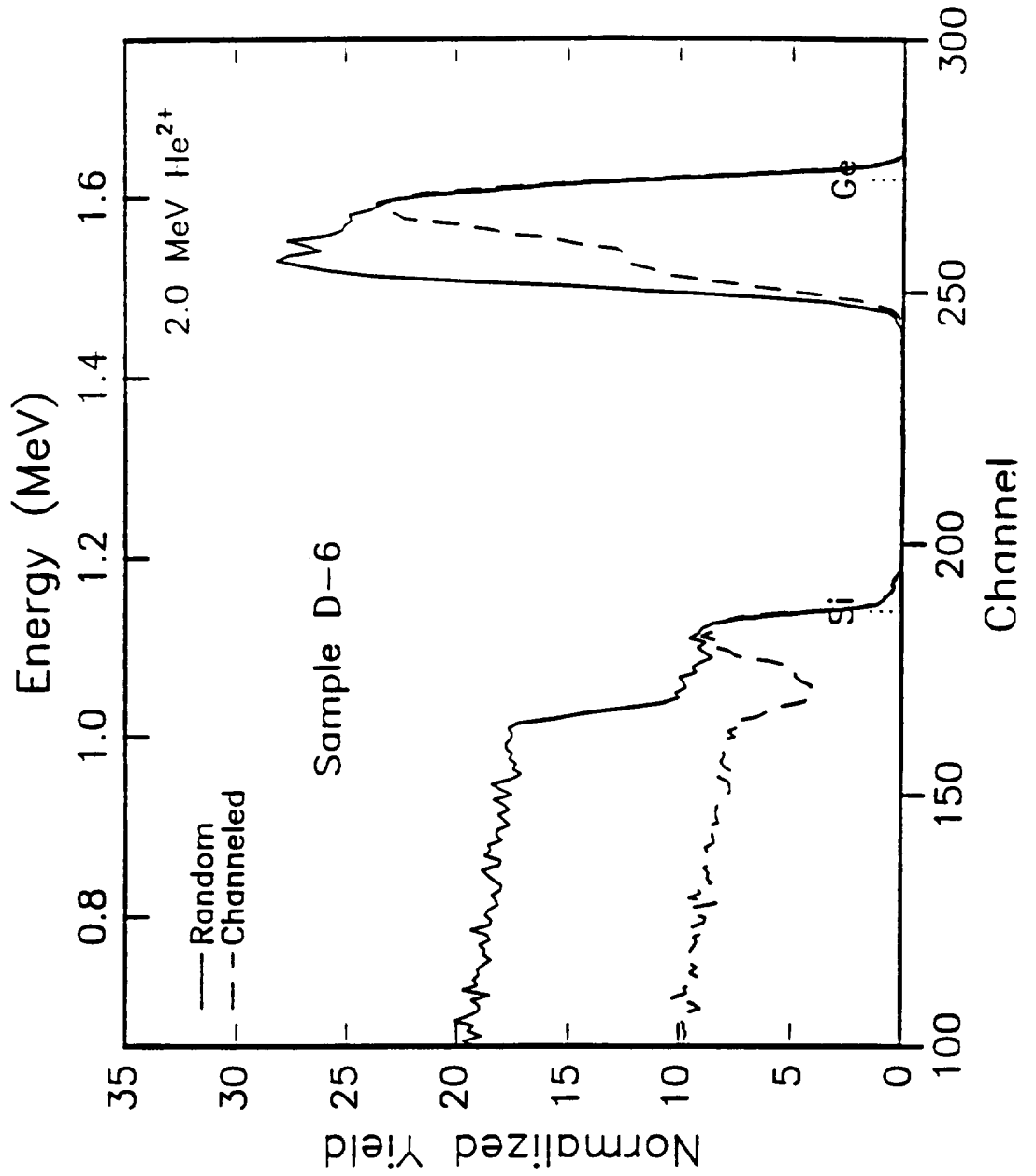


Figure 4

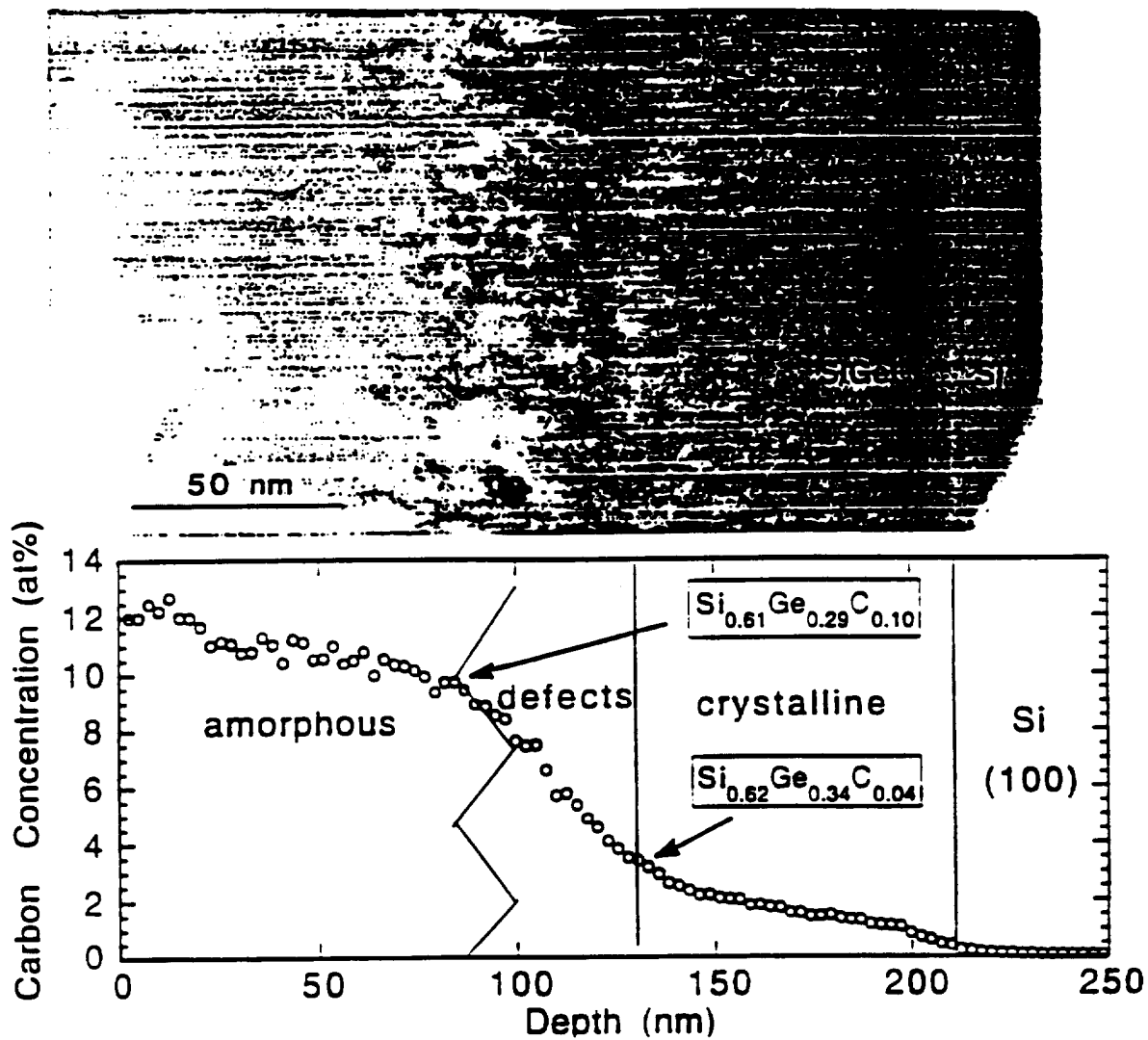


Table I

Sample	Deposition Temperature (°C)	SiH <sub>2</sub> Cl <sub>2</sub> (sccm)	GeH <sub>4</sub> 1% in H <sub>2</sub> (sccm)	10% C <sub>2</sub> H <sub>4</sub> in He start (sccm)	10% C <sub>2</sub> H <sub>4</sub> in He end (sccm)
A-6	625	20	180	504	504
B-6	625	20	180	800	800
C-6	625	20	180	900	900
D-6	625	20	180	500	1500

What is claimed is:

1. An etch-stop structure, comprising:  
a substrate;  
5 one or more epitaxial layers grown sequentially, starting at the substrate, at least one of which comprises Si-Ge-C, wherein carbon is present in the Si-Ge-C layer(s) in an amount sufficient for preferential etch selectivity over the substrate and/or adjacent epitaxial layers, the Si-Ge-C layer(s) comprising:  
0-99.9 atomic percent Si,  
10 1-92 atomic percent Ge, and  
0.1-10 atomic percent C.
2. The structure of claim 1, comprising:  
45-83 atomic percent Si,  
15 15-50 atomic percent Ge, and  
2-5 atomic percent C.
3. The structure of claim 1, comprising:  
55.5 atomic percent Si,  
20 40 atomic percent Ge, and  
4.5 atomic percent C.
4. The structure of claim 1, comprising:  
28-90 atomic percent Si,  
25 9-67 atomic percent Ge, and  
1-5 atomic percent C.
5. The structure of claim 1, comprising:  
60 atomic percent Si,  
30 36 atomic percent Ge, and  
4 atomic percent C.

6. The structure of claim 1, comprising:  
53 atomic percent Si;  
42 atomic percent Ge; and  
5 atomic percent C.
- 5
7. The structure of claim 1, comprising:  
70 atomic percent Si;  
27 atomic percent Ge; and  
3 atomic percent C.
- 10
8. A method for using Si-Ge-C as an etch-stop in conjunction with a silicon substrate, comprising:  
growing one or more epitaxial layers, the first layer being grown on the substrate, wherein at least one of the epitaxial layers comprises Si-Ge-C; and  
15 etching the one or more layers adjacent to the Si-Ge-C layer and/or the Si-Ge-C layer.
9. The method of claim 8, wherein the carbon in the Si-Ge-C layers is present in an amount sufficient for preferential etch selectivity over the one or more layers adjacent to the Si-Ge-C layer.
- 20
10. The method of claim 8, wherein the Si-Ge-C layer etches slower than the one or more adjacent epitaxial layers.
11. The method of claim 8, wherein the Si-Ge-C layer etches faster than the one or more adjacent epitaxial layers.
- 25
12. The method of claim 8, wherein the Si-Ge-C layer etches slower than the silicon substrate.
13. The method of claim 8, wherein the Si-Ge-C layer etches faster than the silicon substrate.
- 30
14. The method of claim 8, 9, 10, 11, 12, or 13, wherein the Si-Ge-C is grown on the substrate by thermal chemical vapor deposition.

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15. The method of claim 8, 9, 10, 11, 12, or 13, wherein the carbon is in the range of 1 to 10 atomic percent.

16. A method for using Si-Ge-C as an etch-stop in conjunction with a silicon, germanium, or silicon-germanium substrate, comprising:

growing one or more epitaxial layers sequentially, starting at the substrate, at least one of which comprises Si-Ge-C, wherein carbon is present in the Si-Ge-C layer(s) in an amount sufficient for preferential etch selectivity over the substrate and/or adjacent epitaxial layers; and

etching the one or more layers adjacent to the Si-Ge-C layer and the Si-Ge-C layer.

10

17. A method for using Si-Ge-C as an etch-stop, comprising:

providing a silicon substrate; and

epitaxially growing one or more layers on the silicon substrate, wherein at least one of the epitaxial layers comprises Si-Ge-C.

15

18. A wet chemical etchant, comprising:

3.5 - 15.8 mole percent of HF;

0.2 - 9.7 mole percent of HNO<sub>3</sub>;

34.8 - 82.6 mole percent of CH<sub>3</sub>COOH; and

12.3 - 46.5 mole percent of H<sub>2</sub>O.

20

19. A wet chemical etchant, comprising:

6.2 - 8.2 mole percent of HF;

0.3 - 6.9 mole percent of HNO<sub>3</sub>;

53.8- 71.1 mole percent of CH<sub>3</sub>COOH; and

20.4 - 33.1 mole percent of H<sub>2</sub>O.

25

20. A process for making an etchant, comprising the step of mixing the following reagents:

0.5 to 2 parts by volume of 49 wt% HF;

0.1 to 3 parts by volume of 70 wt% HNO<sub>3</sub>; and

8 to 12 parts by volume of 99 wt% CH<sub>3</sub>COOH.

30

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21. A process for making an etchant, comprising the step of mixing the following reagents:  
6.2 - 8.2 mole percent of HF;  
0.5 - 8.4 mole percent of HNO<sub>3</sub>;  
43.7 - 70.7 mole percent of CH<sub>3</sub>COOH; and  
5 20.7 - 40.4 mole percent of H<sub>2</sub>O.
22. A process for making an etchant, comprising the step of mixing the following reagents:  
6.8 - 8.1 mole percent HF;  
0.6 - 5.0 mole percent HNO<sub>3</sub>;  
10 58.7 - 70.3 mole percent CH<sub>3</sub>COOH; and  
21.0 - 29.5 mole percent H<sub>2</sub>O.
23. A process for etching a structure including one or more epitaxial layer(s) and/or a substrate,  
comprising:  
15 immersing the structure, at least partially in the etchant of claim 18 or 19; and  
rinsing the etchant from the structure.
24. The process of claim 23, wherein the etchant is in a temperature range of 15-50°C.
- 20 25. The process of claim 16, wherein the etchant is 10-45 wt% KOH H<sub>2</sub>O and is maintained  
at a temperature in the range of 50 to 100°C.
26. A process for etching a structure, comprising:  
immersing the structure, at least partially in the etchant of claim 18 or 19; and  
25 rinsing the etchant from the structure.
27. The process of claim 16, wherein the etchant is 21 wt% KOH-H<sub>2</sub>O and is maintained at a  
temperature in the range of 50 to 100°C.
- 30 28. A process for forming epitaxial Si-Ge-C, comprising the steps of:  
loading a silicon substrate in a thermal chemical vapor deposition reactor;



epitaxially growing one or more layers on the silicon substrate of which one of the layers comprises Si-Ge-C; and  
terminating the process.

- 5 29. The process of claim 28, further comprising:  
cleaning the substrate before loading the substrate in the reactor.
30. The process of claim 28, further comprising the step of removing a native oxide layer from  
the substrate by immersing the substrate in dilute HF and/or baking the substrate at 850-1200°C  
10 in H<sub>2</sub> in the reactor.
31. The process of claim 28, further comprising:  
adjusting the temperature of the reactor to a deposition temperature.
- 15 32. The process of claim 28, wherein the epitaxially growing step includes the step of supplying  
gaseous sources of Si, Ge, C, and H and/or B, As, P to a growing surface.
33. The process of claim 28, further comprising:  
purging the gases with H<sub>2</sub> or an inert gas from reactor;  
20
34. The process of claim 28, 29, 30, 31, 32, or 33, wherein the carbon source is cyclopropane  
or ethylene.
35. The process of claim 28, wherein the concentration of the carbon containing gas supplied  
25 to the growing surface is ramped up over time.
36. The process of claim 28, wherein the concentration of the carbon containing gas supplied  
to the growing surface increases linearly with respect to time.
- 30 37. A product made in accordance with the processes defined in claim 28, 29, 30, 31, 32, or  
33.

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38. A layered epitaxial structure, comprising:  
a single crystal substrate; and  
one or more epitaxial layers, the first layer being grown on the silicon substrate, of which  
at least one of the layers comprises Si-Ge-C, wherein the substrate and the one or more of the etch-  
5 stop layers include P-type dopant and/or N-type dopant.
39. A layered epitaxial structure, comprising:  
a single crystal substrate; and  
one or more epitaxial layers on the silicon substrate of which one of the layers comprises  
10 Si-Ge-C, wherein the atomic percent ratio of germanium to carbon in the Si-Ge-C layer is outside  
the range of 6.7 to 1 and 12 to 1.
40. The layered epitaxial structure of claim 38 or 39, wherein the atomic percent of carbon is  
up to 10.  
15
41. The layered epitaxial structure of claim 38 or 39, wherein the atomic percent of carbon is  
in the range of 1 to 10.
42. The layered epitaxial structure of claim 38 or 39, wherein the concentration of electrically  
20 active dopant in and adjacent to the Si-Ge-C layer is lightly doped.
43. The layered epitaxial structure of claim 38 or 39, wherein the concentration of electrically  
active dopant in and adjacent to the Si-Ge-C layer is heavily doped.
- 25 44. The layered epitaxial structure of claim 38 or 39, wherein the concentration of electrically  
active dopant in and adjacent to the Si-Ge-C layer is less than  $1E15$  atom per  $cm^3$ .
45. A method of forming a silicon-on-insulator material, the method comprising the steps of:  
forming a carbon-silicon alloy epitaxial layer having a carbon concentration sufficient to  
30 function as an etch-stop and a germanium concentration 6.7 - 12 times larger than the carbon

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concentration, wherein the carbon alloy resides on a surface of a first semiconductor silicon substrate;

forming a second silicon epitaxial layer on the carbon-silicon alloy layer;

providing a first oxide layer on a surface of the second epitaxial layer;

5 providing a second oxide layer on a second semiconductor silicon substrate;

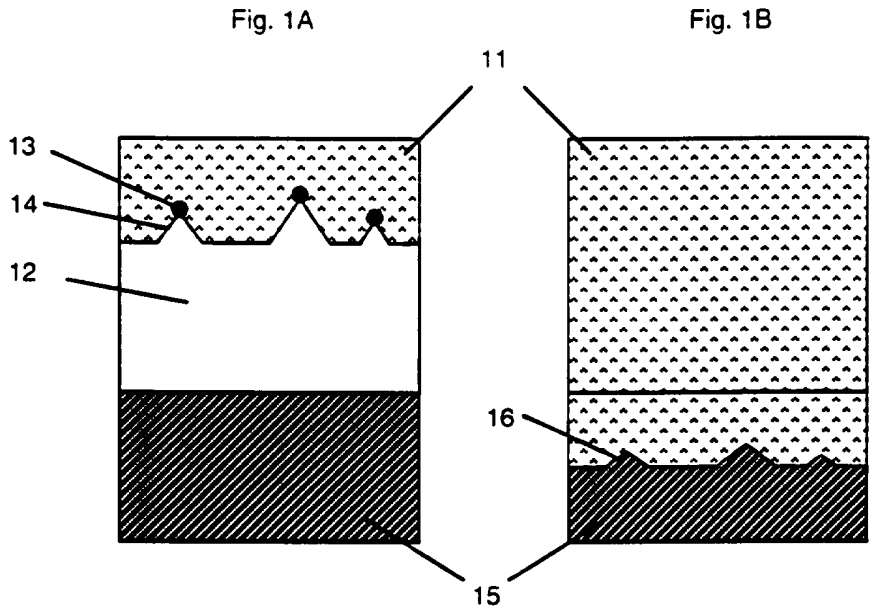
bringing into contact the first and second oxide layers thereby bonding together the first and second semiconductor substrates to thereby form a laminated structure;

removing most of the first silicon substrate;

10 exposing the laminate to an anisotropic etch for the first silicon substrate until the remainder of the first silicon substrate is removed, but only a part of the carbon-silicon alloy layer is removed; and

exposing the resultant structure to a second isotropic etch for the carbon-silicon alloy layer for a time sufficient only to remove the remainder of the carbon-silicon alloy layer thereby producing a silicon-on-insulator material.

15



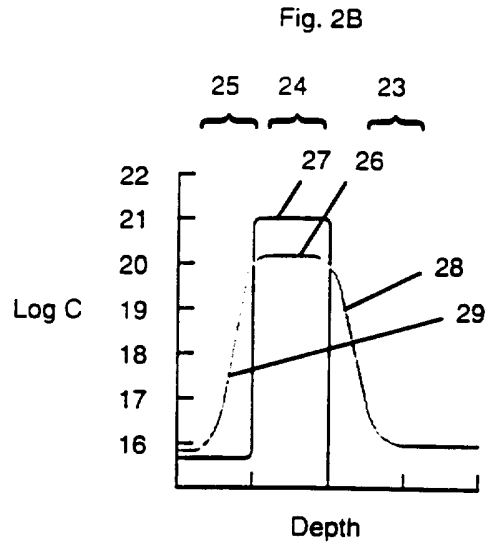
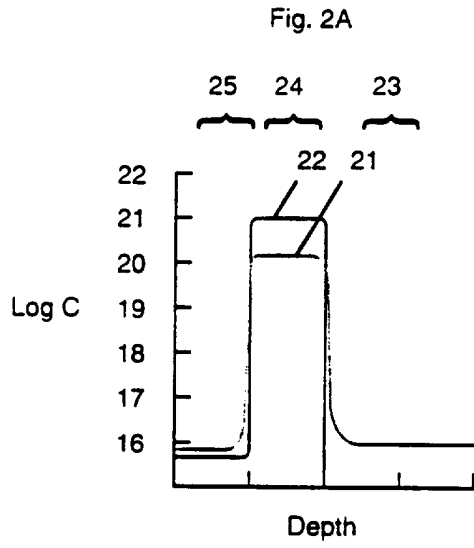
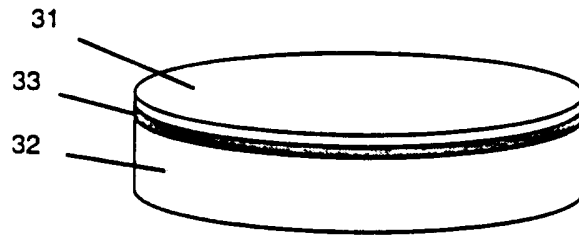


Fig. 3



Base wafer

Device wafer

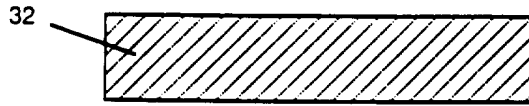


Fig. 4A

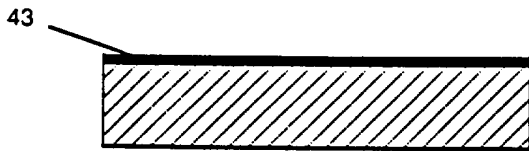
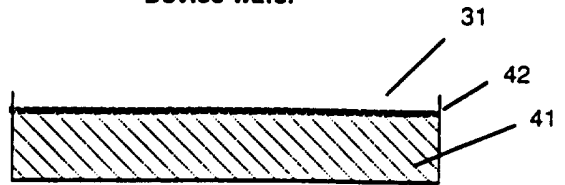


Fig. 4B

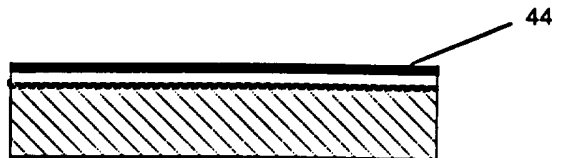


Fig. 4C

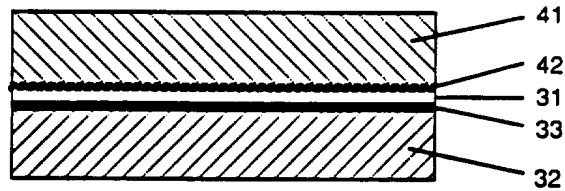


Fig. 4D

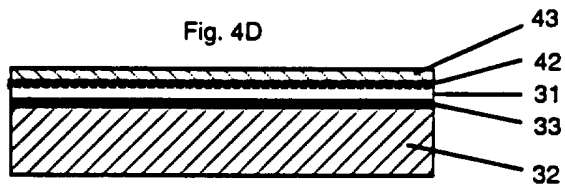


Fig. 4E

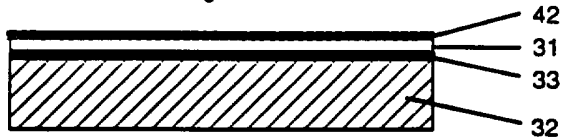


Fig. 4F



Fig. 5A

Fig. 5B

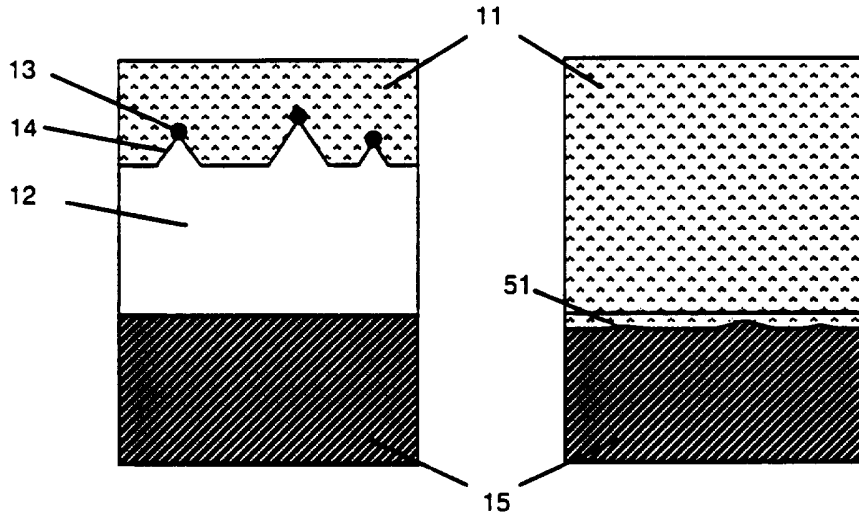




Fig. 6A

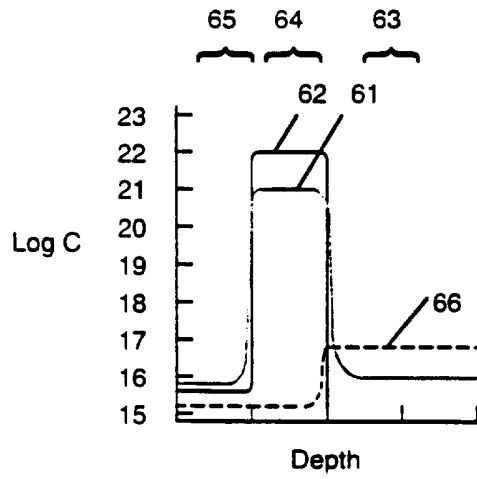
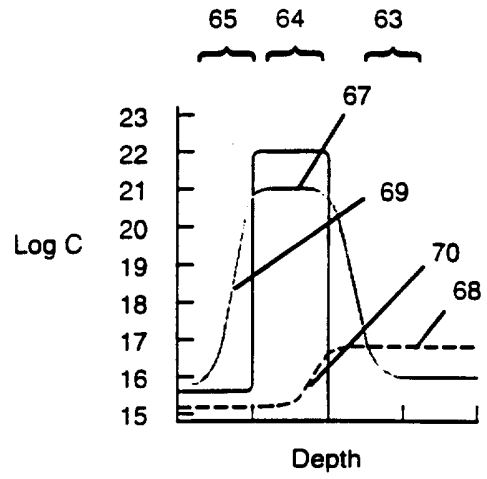
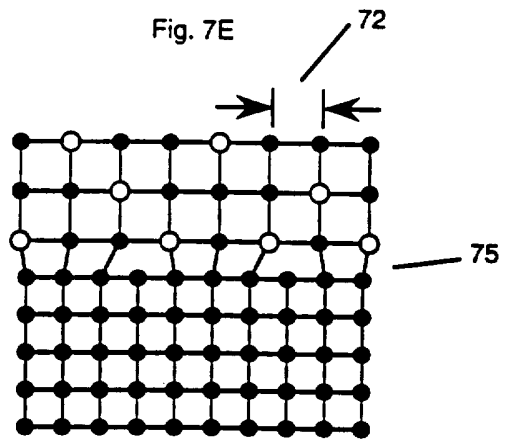
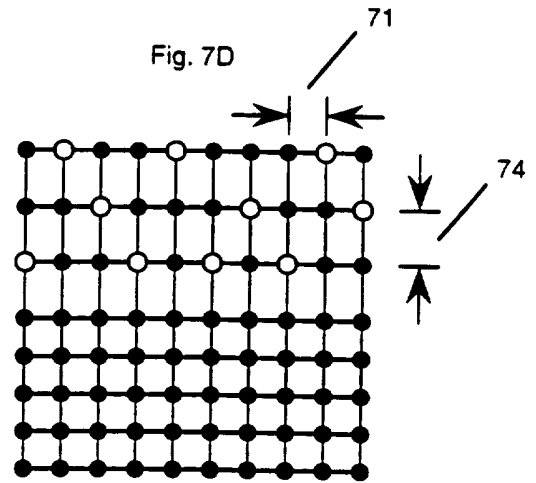
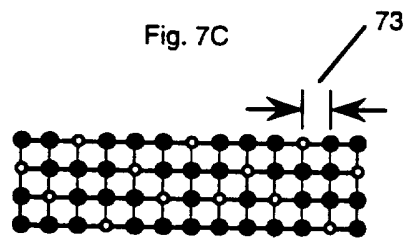
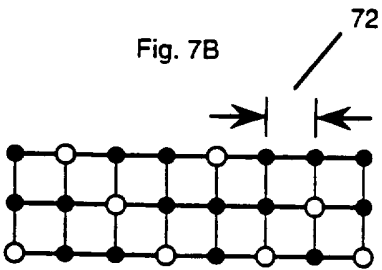
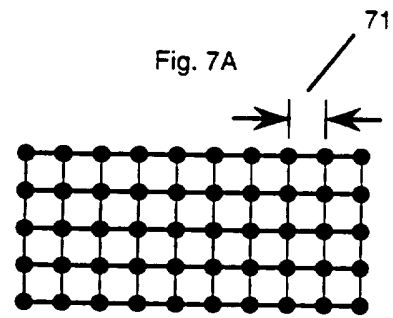


Fig. 6B





- Silicon
- Germanium
- Carbon

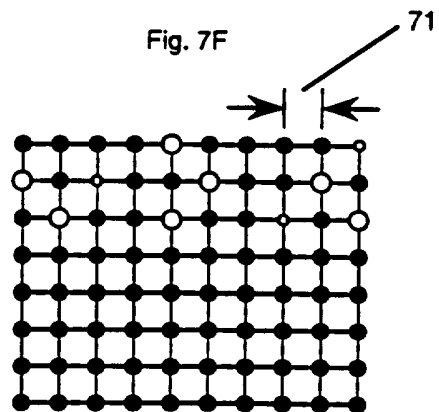
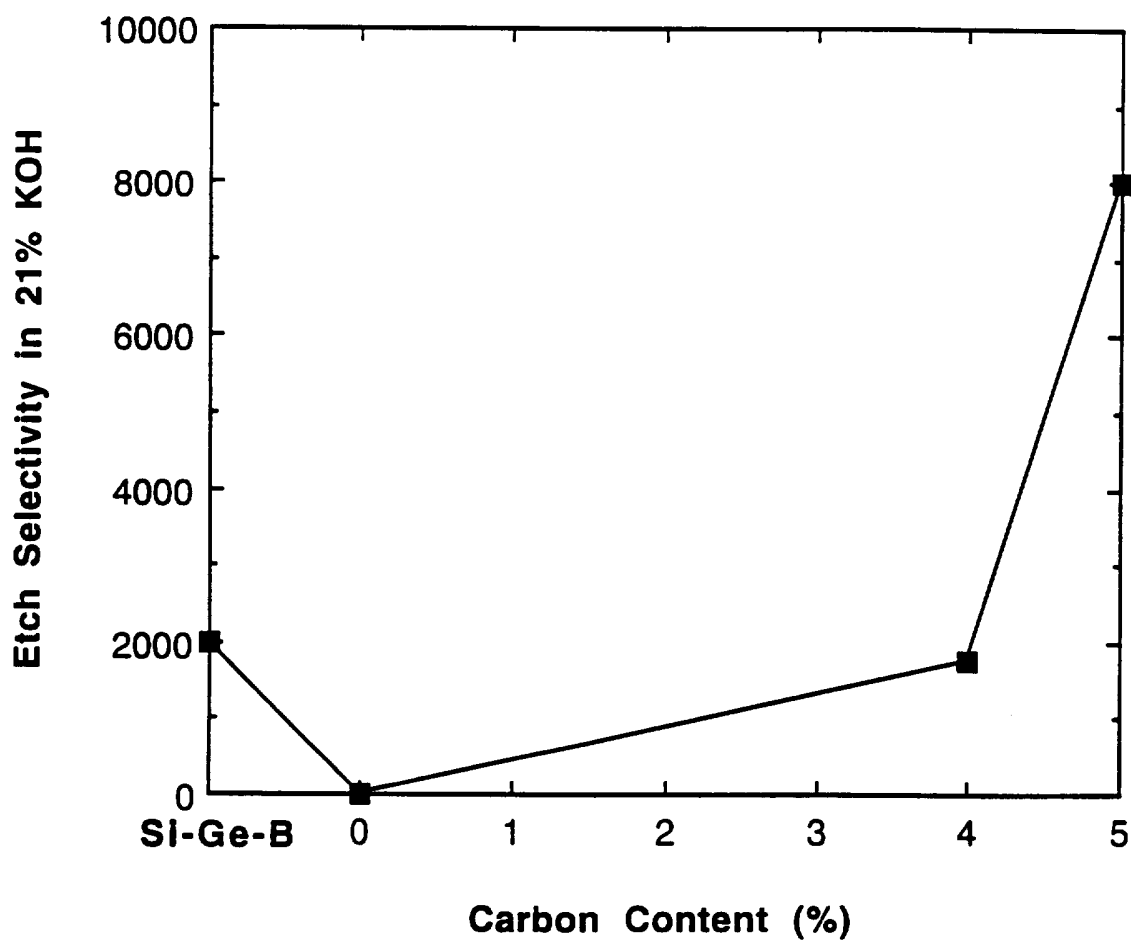


Fig. 8



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Fig. 9

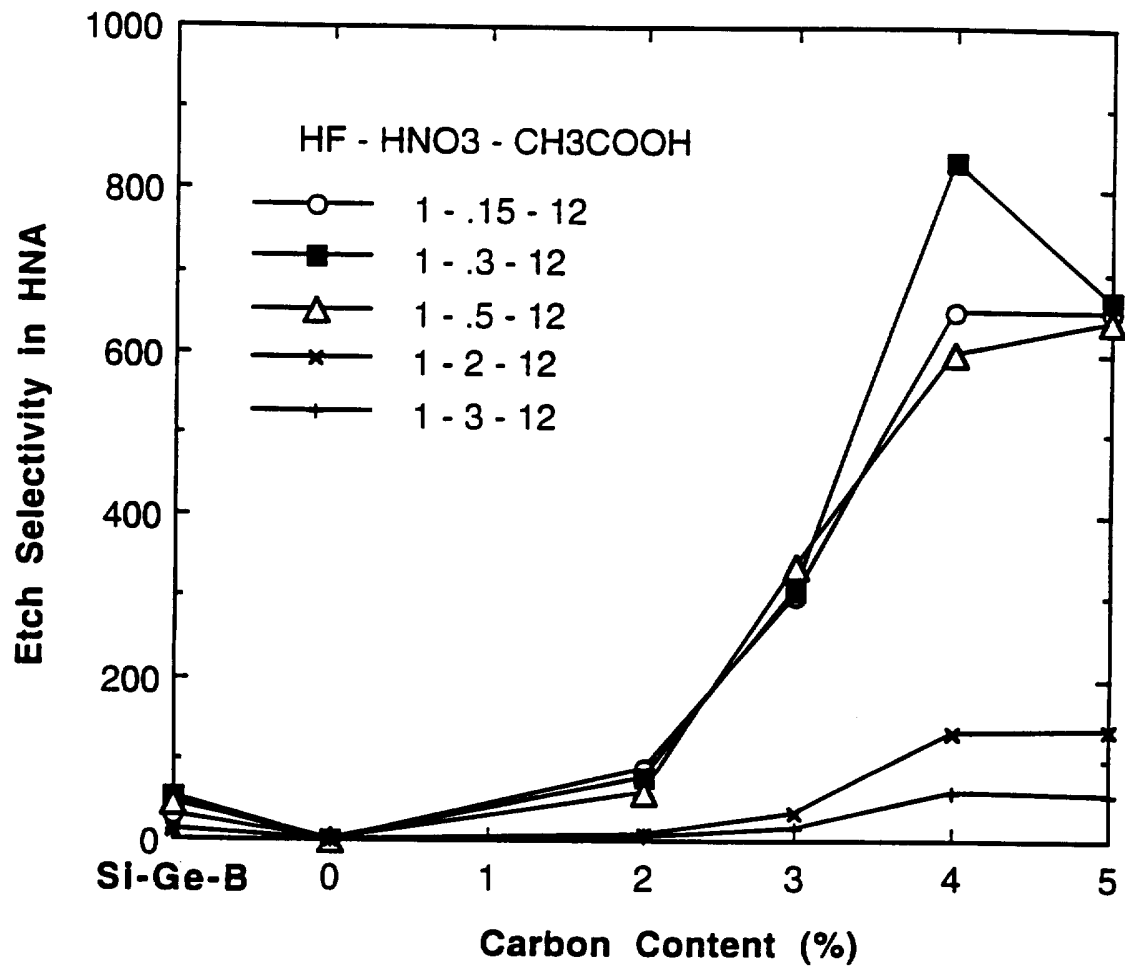


Fig. 10A

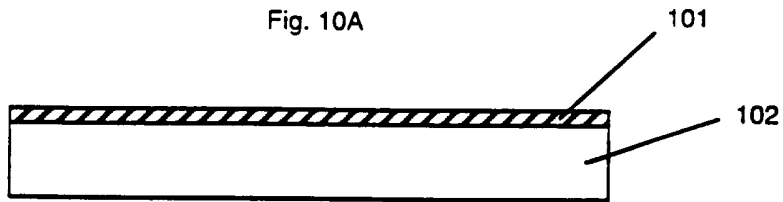


Fig. 10B

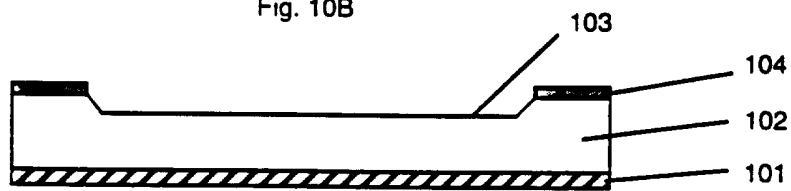


Fig. 10C

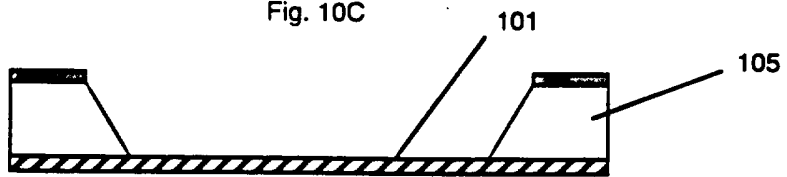


Fig. 11A

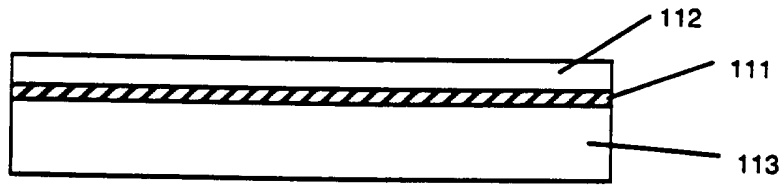


Fig. 11B

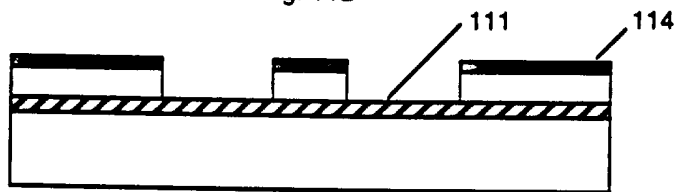


Fig. 11C

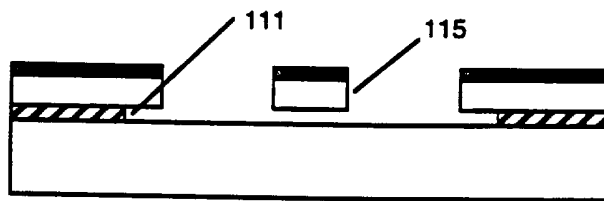
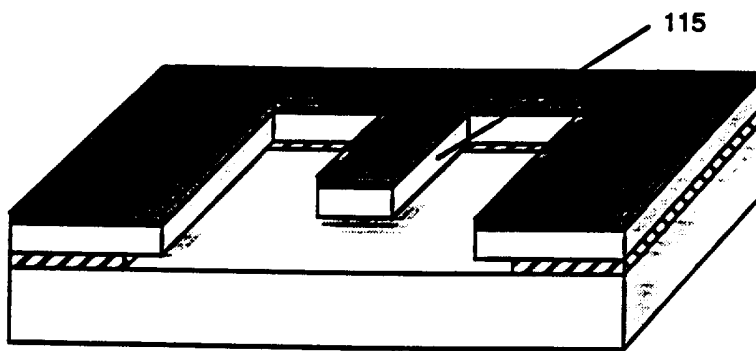


Fig. 11D



**INTERNATIONAL SEARCH REPORT**

International application No.  
PCT/US95/13883

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC(6) :H01L 21/20, 29/12; C30B 1/00; B44C 1/22  
 US CL :148/33.3; 156/657.1; 252/79.3; 156/625.1; 437/126; 117/4  
 According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 148/33.4, 33.6, Dig 59; 437/965, 126; 257/616; 117/4; 156/657.1, 625.1

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Automated Patent System - US Pat File; Jap Patent File; Search terms HF, HNO3, CH3OOH, SiGe

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,885,614 (Furukawa et al) 05 December 1989, entire document	1-7 & 38-45
Y	US, A, 5,357,899 (Bassous et al) 25 October 1994, column 3 lines 9-20	1-17 & 28-45
X	US, A, 4,370,510 (Stirn) 25 January 1983, column 7 line 2	18-27
A	US, A, 5,413,679 (Godbey) 09 May 1995	1-45
A	US, A, 5,344,524 (Sharma et al) 06 September 1994	1-45

Further documents are listed in the continuation of Box C.  See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principles or theory underlying the invention
*A* document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
*B* earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A* document member of the same patent family
*O* document referring to an oral disclosure, use, exhibition or other means	
*P* document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

10 JANUARY 1996

Date of mailing of the international search report

13 MAR 1996

Name and mailing address of the ISA/US  
 Commissioner of Patents and Trademarks  
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 Washington, D.C. 20231

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Authorized officer

  
 GEORGE FOURSON

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INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US95/13883

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I - claims 1-17 & 28-45  
Group II - claims 18-27

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest  The additional search fees were accompanied by the applicant's protest.  
 No protest accompanied the payment of additional search fees.