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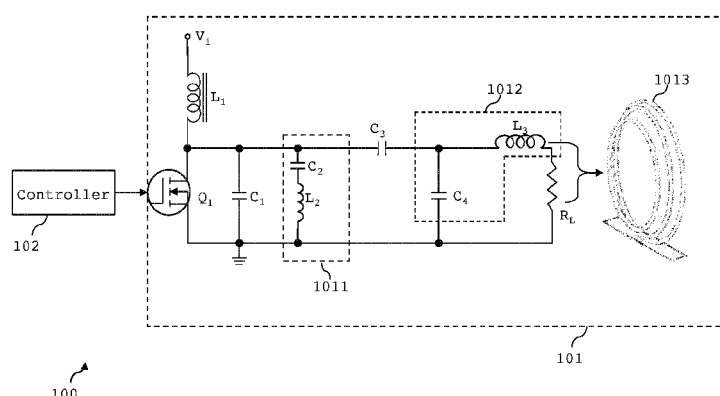


FIG. 1

(57) **Abstract:** An inverter for inductive power transfer is disclosed. The inverter comprises a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency, and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is an integer multiple, greater than one, of the first frequency.

Inverter for Inductive Power Transfer

[Technical Field]

The present invention relates generally to the field of inductive power transfer and more specifically to an inverter
5 for use in inductive power transfer applications.

[Background]

Inductive Power Transfer is a well-known type of power transfer permitting the transmission of electrical power from a power source to a consuming power device without using
10 conductors. In general terms, it comprises the use of time-varying electromagnetic fields typically transmitted across an air gap to the consuming device. The power is transferred through induction which relies on a magnetic field generated in a transmitter (or primary coil) by an electric current to
15 induce a current in a receiver (or secondary coil). This is the action employed in, for example, a transformer where the primary coil and secondary coil are not connected.

However, the primary and secondary coils of a transformer are in very close proximity with a high coupling factor. For other
20 applications, to maintain a high power of transmission, there is a need for more efficient, powerful and/or multi-megahertz switching resonant inverters.

[Summary]

According to the present invention there is provided an
25 inverter for inductive power transfer, the inverter comprising: a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the
30 first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank

circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency, and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is an integer multiple, greater than one, of the first frequency.

The present invention also provides an inductive power transfer transmitter comprising an inverter as described above and a controller operable to switch the switching element of the inverter at the first frequency.

Moreover, the present invention provides an inductive power transfer system comprising an inductive power transfer transmitter as defined above and an inductive power transfer receiver comprising a receiver coil spaced apart from the transmitter coil of the inductive power transfer transmitter.

The present invention also provides a method for inductive power transfer, comprising: providing an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a

second tank circuit in parallel with the first capacitance;
and a third capacitance in series with the first inductor
between the first tank circuit and the second tank circuit,
wherein the second tank circuit comprises a transmitter coil
5 and a fourth capacitance, the fourth capacitance being
arranged in parallel or series with the transmitter coil;
wherein the fourth capacitance is selected such that the
resonant frequency of the second tank circuit is not equal to
the first frequency; and wherein the second inductor and the
10 second capacitance are selected such that the resonant
frequency of the first tank circuit is double the first
frequency; and wherein the ratio of the first capacitance to
the second capacitance is greater than or equal to 0.7 and
less than or equal to 1; and switching the switching element
15 at the first frequency with a duty cycle greater than or equal
to 0.35 and less than or equal to 0.40.

The present invention also provides a method for inductive
power transfer, comprising: providing an inverter comprising
a first inductor and a switching element in series between
20 power supply terminals, the switching element being operable
to be switched at a first frequency; a first capacitance in
parallel with the switching element between the first inductor
and a power supply terminal; a first tank circuit in parallel
with the first capacitance, the first tank circuit comprising
25 a second inductor and a second capacitance, wherein the second
capacitance is arranged in series with the second inductor; a
second tank circuit in parallel with the first capacitance;
and a third capacitance in series with the first inductor
between the first tank circuit and the second tank circuit,
30 wherein the second tank circuit comprises a transmitter coil
and a fourth capacitance, the fourth capacitance being
arranged in parallel or series with the transmitter coil;
wherein the fourth capacitance is selected such that the
resonant frequency of the second tank circuit is not equal to

the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than 1 and less than 5; and switching the switching element at the first frequency with a duty cycle greater than 0.35 and less than 0.40.

The present invention also provides a method for inductive power transfer, comprising: providing an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 20; switching the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

[List of Figures]

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which like reference numbers are used for like elements, and in which:

Figure 1 schematically illustrates an inductive power transfer transmitter comprising a controller and an inverter according to an embodiment of the present invention;

Figure 2 depicts a modification to the inverter disclosed in Figure 1 with the removal of the first capacitance;

Figure 3 is a diagram of an inductive power transfer system;

Figure 4 depicts a first method of operating an inverter;

Figure 5 depicts a second method of operating an inverter;

Figure 6 depicts a third method of operating an inverter;

Figure 7 depicts a circuit for analysis of the special modes of an inverter;

Figures 8a and 8b show numerically solved values of p and ϕ as a function of k and the duty cycle D for $q_1 = 2$.

Figures 9a and 9b show numerically solved values of p and ϕ as a function of k and the duty cycle D for $q_1 = 3$.

Figures 10a and 10b show numerically solved values of p and ϕ as a function of k and the duty cycle D for $q_1 = 4$.

Figure 11 shows switch's voltage and current waveforms and the current of inductor L_2 for selected values of duty cycle and k for $q_1 = 2$;

Figure 12 shows switch's voltage and current waveforms and the current of inductor L_2 for selected values of duty cycle and k for $q_1 = 3$;

Figure 13 shows switch's voltage and current waveforms and the current of inductor L_2 for selected values of duty cycle and k for $q_1 = 4$;

5 Figures 14a - 14c show the variation of the normalised DC resistance with duty cycle and k . For Figure 14a, $q_1 = 2$, Figure 14b with $q_1 = 3$ and Figure 14c $q_1 = 4$;

Figures 15a and 15b depict maximum switch voltage and current for $q_1 = 2$;

10 Figures 16a and 16b depict maximum switch voltage and current for $q_1 = 3$;

Figures 17a and 17b depict maximum switch voltage and current for $q_1 = 4$;

Figures 18a - 18d depict the variation of output power capability for $q_1 = 2$;

15 Figures 19a and 19b depict the variation of output power capability for $q_1 = 3$;

Figures 20a and 20b depict the variation of output power capability for $q_1 = 4$;

20 Figures 21a and 21b depict the path of maximum output capability as k and the duty cycle vary;

Figures 22a - 22d depict the variation of characterising parameters along the maximum output power capability path;

Figures 23a and 23b depict the variation of the switch's peak drain voltage and current with k ;

25 Figures 24a - 24d depict the variation of R_L , R_x , C_1 and C_2 with k for maximum output power capability;

Figure 25 depicts the voltage and current waveforms for maximum output power capability;

Figure 26 depicts the voltage and current waveforms for the steady state case;

Figures 27a - 27c depict the variation of $\omega R_L C_1$ with k ;

Figure 28 depicts the voltage and current waveforms for the maximum switching frequency case;

Figure 29 compares the efficiencies of all special cases as the load resistance varies;

Figure 30a and 30b depicts the setup of a semi-resonance mode;

Figure 31 depicts how the equivalent resistance and the equivalent inductance change according to C_{res} in a hypothetical inductive power transfer system;

Figures 32a - 32d depict the MOSFET's drain voltage and output current waveforms for each of the special cases and a Class E inverter;

Figures 33a - 33d depict the output current for a Class E, Class EF_2 , Class E/ F_3 and Class EF_4 inverter;

Figures 34a - 34c depict the harmonic content of the output current for the Class E, Class EF_2 , Class E/ F_3 and Class EF_4 inverter;

Figure 35 depicts voltage and current waveforms for the tuning of the first tank circuit being slightly greater than twice the first frequency f_s ;

Figure 36 depicts voltage and current waveforms for the tuning of the first tank circuit being slightly less than twice the first frequency f_s .

[Detailed Description of Embodiments]

At present, inductive power transfer inverters are based on either a Class D or Class E type of inverter. The Class D type

inverters consist of two switching elements and deliver a limited output power at minimum voltage and with low current stresses across the switching elements. Class E type inverters consist of a single switching element and deliver a higher
5 output power, but with higher voltage and higher current stresses across the switching element.

Inverters that can deliver a high output power capability are severely limited by the high voltage and current stresses that are present across the switching elements. Previously, this
10 has meant employing higher-specified, and therefore more expensive, components. The present inventors have addressed this problem by devising a new inverter.

One embodiment of the new inverter is depicted in Figure 1, which schematically shows an inverter 101 connected to a
15 controller 102 to form an inductive power transfer transmitter 100. The inverter 101 comprises a switching element Q_1 , which, in this embodiment, is a transistor, although other types of switching element can be employed instead. The inverter 101 has features which decrease the voltage stress across the
20 switching element Q_1 without significantly increasing the current stress. This has the benefit of allowing the use of a smaller switching element Q_1 which maintains the same power level as previous inverters but reduces power losses due to a decreased on-state resistance. Alternatively, the new inverter
25 101 permits higher output power capabilities using the same switching element Q_1 as in previous inverters.

The inverter 101 depicted in Figure 1 is for inductive power transfer and comprises a first inductor L_1 and the switching element Q_1 in series between the power supply terminals to
30 which a power supply (not shown) is connected. The switching element Q_1 is operable to be switched by the controller at a first frequency f_s , which may be a predefined frequency (this

frequency being interchangeably referred to herein as a first frequency or a switching frequency). In this embodiment, the controller 102 is operable to switch the switching element Q_1 at a first frequency f_s greater than 6MHz.

- 5 In this embodiment, the switching element Q_1 is a MOSFET, although other types of transistor can be employed instead.

In this embodiment, the inverter 101 also comprises a first capacitance C_1 in parallel with the switching element Q_1 between the first inductor L_1 and a power supply terminal.

- 10 However, as will be explained below, the capacitance C_1 may be a capacitance of the switching element Q_1 and so a separate capacitor C_1 need not be provided.

- A first tank circuit 1011 is arranged in parallel with the first capacitance C_1 , the first tank circuit 1011 comprising a
15 second inductor L_2 and a second capacitance C_2 , wherein the second capacitance C_2 is arranged in series with the second inductor L_2 . The second inductor L_2 and the second capacitance C_2 are selected such that the resonant frequency of the first tank circuit 1011 is an integer multiple, greater than one, of
20 the first frequency f_s .

- The inverter 101 is therefore a hybrid inverter which can be referred to as a Class EF_n or Class E/F_n inverter. The subscript n refers to the ratio of the resonant frequency of the first tank circuit 1011 to the first frequency f_s of the
25 inverter 101 and is an integer multiple greater than or equal to 2. The EF_n term is used if n is an even integer and the E/F_n term is used if n is an odd integer.

- As will be explained in more detail below, the resonant frequency of the first tank circuit 1011 need not be precisely
30 an integer multiple (greater than one) of the first frequency

f_s to achieve the advantages described herein, but instead can be equal to the integer multiple ± 0.05 . Accordingly, when any of the terms "integer multiple", "twice", "double", "triple", "three times", etc. or the like are used herein to refer to the relationship between the resonant frequency of the first tank circuit 1011 and the first frequency f_s , these terms should be understood to encompass the ± 0.05 tolerance.

The inverter 101 also comprises a second tank circuit 1012 in parallel with the first capacitance C_1 .

The inverter 101 further comprises a third capacitance C_3 in series with the first inductor L_1 between the first tank circuit 1011 and the second tank circuit 1012.

The second tank circuit 1012 comprises a transmitter coil 1013, which is modelled as a third inductance L_3 and a resistance R_L in the circuit shown in Figure 1, and a fourth capacitance C_4 . The fourth capacitance C_4 is arranged in parallel or series with the transmitter coil 1013. The third inductance L_3 and resistance R_L represent the inductance of the transmitter coil and its reflected resistance respectively.

The fourth capacitance C_4 is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency f_s . As a result, the inverter 101 operates in a semi-resonant mode. For example, the fourth capacitance C_4 can be arranged in parallel with the transmitter coil 1013 and the fourth capacitance C_4 can be selected such that the resonant frequency of the second tank circuit 1012 is greater than the first frequency f_s . In this case, the fourth capacitance C_4 can be selected so that the ratio of the first frequency f_s to the resonant frequency of the second tank circuit 1012 may be set to greater than or equal to 0.5 and less than 1.

Alternatively, the fourth capacitance C_4 can be arranged in series with the transmitter coil 1013, and the fourth capacitance C_4 can be selected such that the resonant frequency of the second tank circuit 1012 is less than the first frequency f_s . In this case, the fourth capacitance C_4 can be selected so that the ratio of the first frequency f_s to the resonant frequency of the second tank circuit 1012 is greater than 1 and less than or equal to 1.5.

The overall effect of the inverter 101 is to reduce the peak voltage across the switching element Q_1 whilst increasing the output power capability delivered to a receiver and hence to a load. For example, the inventors have found that, by using a first tank circuit 1011 with a resonant frequency equal to the second harmonic frequency of the switching signal from the drain of the switching element Q_1 to ground, the peak voltage across the switching element Q_1 is reduced from 3.5 - 4 times the input voltage, as in a conventional Class E inverter, to twice the input voltage. The first tank circuit 1011 effectively: (1) removes the second harmonic of the voltage developed across the switching element Q_1 when the switching element Q_1 is off by storing its energy and (2) releases the stored energy back to the circuit when the switching element Q_1 is on.

The inverter 101 depicted in Figure 1 can be modified in a number of ways. For example, as depicted in Figure 2, the inverter 101 could be modified to remove the separate capacitance C_1 and instead rely on the non-linear output capacitance of the switching element Q_1 . In other words, in the embodiment of Figure 2, the first capacitance C_1 is part of the output capacitance of the switching element Q_1 .

Figure 3 depicts an inductive power transfer system, which comprises an inductive power transfer transmitter 100, as described previously, together with an inductive power transfer receiver 300. The inductive power transfer receiver
5 comprises a receiver coil 301 spaced apart from the transmitter coil 1013 of the inductive power transfer transmitter 100. The centres of the receiver coil 301 and transmitter coil 1013 are spaced apart by a distance d . Although the diagram depicts the coils as angled relative to
10 each other, this need not be the case and the coils are typically parallel to each other or may take any orientation with respect to each other. The inductive power transfer transmitter 100 transmits power via electromagnetic radiation to the receiver coil 1013 which is driven by the
15 electromagnetic radiation to induce a current in the inductive power transfer receiver 300.

As noted above, the first tank circuit 1011 in embodiments of the present invention may be tuned to any integer multiple of the first frequency f_s ; where the integer multiple is 2 or
20 greater. The inventors have carried out investigations to determine which integer multiples provide better harmonic distortion than a conventional Class E inverter. More particularly, a hypothetical inductive power transfer system was considered with a transmitting coil inductance of $1\mu\text{H}$, an
25 optimum reflected load of 6Ω , an output power of 100W and a frequency of operation of 6.78 MHz. For simplification, lossless operation was also assumed. The harmonic content was analysed using state-space analysis.

Figures 33a - d show the output current (or the current
30 flowing in the transmitting coil) for (i) a Class E inverter, (ii) an inverter of an embodiment in which the first tank circuit is tuned to twice the first frequency f_s (Class EF_2), (iii) an inverter of an embodiment in which the first tank

circuit is tuned to three times the first frequency f_s (Class E/ F_3), and (iv) an inverter of an embodiment in which the first tank circuit is tuned to four times the first frequency f_s (Class EF $_4$), respectively. In these figures, the total harmonic distortion, THD, is shown for each inverter. It can be seen that an inverter in which the first tank circuit is tuned to twice the first frequency and an inverter in which the first tank circuit is tuned to three times the first frequency are both advantageous in that they both provide lower harmonic distortion than a Class E inverter. It will also be seen that the output current has the lowest distortion and is closer to an ideal sinusoidal waveform when the first tank circuit 1011 is tuned to twice the first frequency f_s .

Figure 34 shows the harmonic content of the output current for all of the inverters. The harmonic corresponding to the tuned resonant frequency of the first tank circuit 1011 is removed leading to an improved total harmonic distortion for the cases where the first tank circuit 1011 is tuned to either twice or three times the first frequency f_s .

As will be explained in more detail below, the present inventors have also investigated how to optimise the new inverter 101 to achieve high output power capability, high switching frequency and/or steady state operation. The present inventors have found that, by selecting the capacitances C_1 and C_2 and the switching duty cycle of the switching element Q_1 (defined as the ratio of the time the switching element Q_1 is on to the total time of the period, i.e. the sum of the switching element Q_1 on-time and off-time in a period), the inductive power transfer transmitter 100 can be optimised for high output power capability, high switching frequency of the switching element Q_1 and/or steady state operation.

More particularly, for maximum output power capability in a transmitter 100 in which the first tank circuit 1011 of the inverter 101 is tuned to twice the first frequency f_s , or, taking into account tolerances between 1.95 and 2.05 of the first frequency f_s , the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is 0.867 or, taking into account tolerances between 0.767 and 0.967, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle of 0.375 or, taking into account tolerances, between 0.365 and 0.385.

To achieve 90% or greater of the maximum output power capability, the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is between 0.8 and 1, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle between 0.35 and 0.40.

To achieve 80% or greater of the maximum output power capability, the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is between 0.7 and 1, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle between 0.35 and 0.40.

Accordingly, a method for inductive power transfer in an embodiment is shown in Figure 4. Referring to Figure 4, at step S401 an inverter is provided comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second

capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 0.7 and less than or equal to 1.

At step S402, the switching element Q_1 is switched at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

For maximum switching frequency in a transmitter 100 in which the first tank circuit 1011 of the inverter 101 is tuned to twice the switching frequency f_s , or, taking into account tolerances between 1.95 and 2.05 of the first frequency f_s , the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is 1.567 or, taking into account tolerances between 1.467 and 1.667, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle of 0.3718 or, taking into account tolerances, between 0.3618 and 0.3818.

To achieve 90% or greater of the maximum switching frequency, the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is between 1.2 and

3.7, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle between 0.35 and 0.40.

To achieve 80% or greater of the maximum switching frequency, the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is between 1 and 5, and the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle between 0.35 and 0.40.

Accordingly, a method for inductive power transfer in an embodiment is shown in Figure 5. Referring to Figure 5, at step S501 an inverter is provided comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than 1 and less than 5.

At step S502, the switching element Q_1 is switched at the first frequency with a duty cycle greater than 0.35 and less than 0.40.

For a steady state in a transmitter 100 in which the first
5 tank circuit 1011 of the inverter 101 is tuned to twice the switching frequency f_s , or, taking into account tolerances between 1.95 and 2.05 of the first frequency f_s , the inventors have found that capacitances C_1 and C_2 should be selected such that the ratio of C_1 to C_2 is greater than or equal to 20, and
10 the controller 102 should be arranged to switch the switching element Q_1 with a duty cycle between 0.35 and 0.4.

Accordingly, a method for inductive power transfer in an embodiment is shown in Figure 6. Referring to Figure 6, at step S601 the inverter is provided comprising a first
15 inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with
20 the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor
25 between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the
30 resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first

frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 20.

At step S602 the switching element Q_1 is switched at the first frequency with a duty cycle greater than or equal to 0.35 and
5 less than or equal to 0.40.

The advantages set out above, and those described below, can still be achieved even when the resonant frequency of the first tank circuit 1011 is not precisely an integer multiple, greater than one, of the first frequency f_s . More

10 particularly, the present inventors have found that the integer multiple with a tolerance of ± 0.05 is sufficient to ensure correct operation. By way of example, when the resonant frequency of the first tank circuit 1011 is to be tuned to twice the first frequency f_s , then correct operation can be

15 achieved when the resonant frequency of the first tank circuit 1011 is between 1.95 and 2.05 times the first frequency f_s . In more detail, Figure 35 depicts the switching element Q_1

voltage and current waveforms found by the inventors for cases where the tuning is slightly greater than twice the first

20 frequency f_s . Figure 36 depicts the switching element Q_1 voltage and current waveforms found by the inventors for cases where the tuning is slightly less than twice the first frequency f_s . Similarly, when the resonant frequency of the

25 first tank circuit 1011 is to be tuned to three times the first frequency f_s , correct operation can be achieved when the resonant frequency of the first tank circuit 1011 is between 2.95 and 3.05 times the first frequency f_s . The ± 0.05 tolerances therefore apply to all integers higher than 3.

The following analysis provides further details of the above-
30 described inverter and its properties. The analysis below, for sake of simplicity, considers cases without the use of a semi-

resonant mode, but the analysis is equally applicable, without loss of generality, to the semi-resonant mode.

Figure 7 depicts a simplified equivalent circuit for the inverter 101 in Figure 1, without the first tank circuit 1011 that provides semi-resonant operation. The simplified equivalent circuit of Figure 7 will be used for the analysis described below. Inductor L_2 and capacitor C_2 make the first tank circuit 1011 in Figure 1. Inductor L_3 is divided into an inductance L that resonates with C_3 at the switching frequency and a residual inductance L_x . The analysis will be based on the following assumptions:

1. The switching element Q_1 is a transistor. The transistor and its body diode form an ideal switch whose ON resistance is zero, OFF resistance is infinity, and switching times are zero.
2. The choke inductance is high enough such that the input current I_{IN} is a DC current.
3. The loaded quality factor of the $L_3C_3R_L$ branch is high enough such that the current i_o through it is sinusoidal.
4. The shunt capacitance C_1 is assumed to be linear.
5. There are no losses in the circuit, all the power supplied by the source is delivered to the load R_L .

The output current i_o is sinusoidal and is given by

$$i_o(\omega t) = i_m \sin(\omega t + \phi) \quad (1)$$

where i_m is the output current's magnitude and ϕ is its phase. For the period $0 \leq \omega t < 2\pi D$ the switch is ON, therefore

$$v_{DS}(\omega t) = 0 \text{ for } 0 \leq \omega t < 2\pi D \quad (2)$$

$$i_{C_1}(\omega t) = 0 \text{ for } 0 \leq \omega t < 2\pi D. \quad (3)$$

By applying KCL at the switch's drain node the switch's current is

$$i_S(\omega t) = I_{IN} - i_{L_2}(\omega t) - i_o(\omega t) \text{ for } 0 \leq \omega t < 2\pi D. \quad (4)$$

Since the switch is ON, the total voltage across the series tuned L_2C_2 network is zero. The L_2C_2 network now is a source-free undamped circuit and its current (i_{L_2}) normalised with
 5 respect to the input DC current (I_{IN}) is given by

$$\frac{i_{L_2}}{I_{IN}}(\omega t) = A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t) \quad (5)$$

where q_1 is the ratio of the resonant frequency of L_2C_2 to the switching frequency and is given by

$$q_1 = n = \frac{1}{\omega \sqrt{L_2 C_2}}. \quad (6)$$

10 The coefficients A_1 and B_1 are to be determined based on equation's boundary conditions.

For the period $2\pi D \leq \omega t < 2\pi$ the switch is turned OFF, therefore

$$i_S(\omega t) = 0 \text{ for } 2\pi D \leq \omega t < 2\pi. \quad (7)$$

15 By applying KCL at the switch's drain node the current in the series tuned L_2C_2 network is

$$\begin{aligned} i_{L_2}(\omega t) &= I_{IN} - i_o(\omega t) - i_{C_1}(\omega t) \\ &= I_{IN} - i_m \sin(\omega t + \phi) - \omega C_1 \frac{dv_{DS}(\omega t)}{d\omega t}. \end{aligned} \quad (8)$$

The switch's voltage is equal to the total voltage across the L_2C_2 network and is given by

$$\begin{aligned} v_{DS}(\omega t) &= \omega L_2 \frac{di_{L_2}(\omega t)}{d\omega t} + \\ &\quad \frac{1}{\omega C_2} \int_{2\pi D}^{\tau} i_{L_2}(\omega t) d\omega t + v_{C_2}(2\pi D). \end{aligned} \quad (9)$$

20 Differentiating the above equation results in

$$\frac{dv_{DS}(\omega t)}{d\omega t} = \omega L_2 \frac{d^2 i_{L_2}(\omega t)}{d\omega t^2} + \frac{1}{\omega C_2} i_{L_2}(\omega t). \quad (10)$$

Substituting Eq.10 in Eq.8 and normalising with respect to the input current

$$\begin{aligned} \frac{i_{L_2}}{I_{IN}}(\omega t) = 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - \\ \omega^2 L_2 C_1 \frac{d^2 i_{L_2}}{d\omega t^2}(\omega t) - \frac{C_1}{C_2} \frac{i_{L_2}}{I_{IN}}(\omega t). \end{aligned} \quad (11)$$

Eq.11 is a linear non-homogeneous second-order differential equation which has the following general solution

$$\begin{aligned} \frac{i_{L_2}}{I_{IN}}(\omega t) = A_2 \cos(q_2 \omega t) + B_2 \sin(q_2 \omega t) \\ - \frac{q_2^2 p}{q_2^2 - 1} \sin(\omega t + \phi) + \frac{1}{k + 1} \end{aligned} \quad (12)$$

where

$$k = \frac{C_1}{C_2} \quad (13)$$

$$q_2 = \frac{1}{\omega} \sqrt{\frac{C_1 + C_2}{L_2 C_1 C_2}} = q_1 \sqrt{\frac{k + 1}{k}} \quad (14)$$

$$p = \frac{C_2}{C_1 + C_2} \frac{i_m}{I_{IN}} = \frac{1}{k + 1} \frac{i_m}{I_{IN}} \quad (15)$$

and the coefficients A_2 and B_2 are to be determined based on the equation's boundary conditions. The boundary conditions are determined from the current and voltage continuity conditions when the switch turns ON and OFF which can be described by

$$i_{L_2}(2\pi D^-) = i_{L_2}(2\pi D^+) \quad (16)$$

$$i_{L_2}(0) = i_{L_2}(2\pi) \quad (17)$$

$$\left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi D^-} = \left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi D^+} \quad (18)$$

$$\left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=0} = \left. \frac{di_{L_2}(\omega t)}{d\omega t} \right|_{\omega t=2\pi} \quad (19)$$

The current through capacitor C_1 for the period $2\pi D \leq \omega t < 2\pi$ is

$$i_{C_1}(\omega t) = I_{IN} - i_o(\omega t) - i_{L_2}(\omega t). \quad (20)$$

and normalising with respect to the input current and using Eq.13 gives

$$\frac{i_{C1}}{I_{IN}}(\omega t) = 1 - p(k+1) \sin(\omega t + \phi) - \frac{i_{L2}}{I_{IN}}(\omega t). \quad (21)$$

The drain voltage for the period $2\pi D \leq \omega t < 2\pi$ is

$$v_{DS}(\omega t) = \frac{I_{IN}}{\omega C_1} \int_{2\pi D}^{\omega t} \frac{i_{C1}}{I_{IN}}(\tau) d\tau \quad (22)$$

where τ is a dummy variable. Substituting the ZVS ($v_{DS}(2\pi) = 0$) and ZDS ($i_{C1}(2\pi) = 0$) conditions in the above equation gives the following two equations

$$\begin{aligned} 2\pi \frac{k}{k+1} (1-D) + p(\cos(2\pi D + \phi) - \cos \phi) \left(\frac{q_2^2}{q_2^2 - 1} - (k+1) \right) + \frac{A_2}{q_2} (\sin(2\pi D q_2) - \sin(2\pi q_2)) \\ + \frac{B_2}{q_2} (\cos(2\pi q_2) - \cos(2\pi D q_2)) = 0 \end{aligned} \quad (23)$$

$$\begin{aligned} \frac{k}{k+1} + p \sin \phi \left(\frac{q_2^2}{q_2^2 - 1} - (k+1) \right) - (A_2 \cos(2\pi q_2) + B_2 \sin(2\pi q_2)) = 0. \end{aligned} \quad (24)$$

Eqs.16-19 and Eqs.23-24 are six simultaneous equations that can be solved numerically to obtain the values of A_1 , A_2 , B_1 , B_2 , p and ϕ for specific values of q_1 , duty cycle D and k . Figures 8 - 10 show numerically solved values of p and ϕ as a function of k and the duty cycle D for $q = 2, 3$ & 4 . In particular, Figure 8 depicts numerically solved values of p and ϕ for $q_1 = 2$, Figure 9 for $q_1 = 3$ and Figure 10 for $q_1 = 4$.

[Voltage and Current Waveforms]

Eq.22 can be written as

$$v_{DS}(\omega t) = \frac{I_{IN}}{\omega C_1} \beta(\omega t) \quad (25)$$

where

$$\beta(\omega t) = \int_{2\pi D}^{\omega t} \frac{i_{C1}}{I_{IN}}(\tau) d\tau. \quad (26)$$

The DC component (or average) of the drain's voltage is equal to the input voltage supply, i.e.,

$$V_{IN} = \frac{I_{IN}}{2\pi\omega C_1} \int_{2\pi D}^{2\pi} \beta(\omega t) d\omega t. \quad (27)$$

By substituting Eq.27 in Eq.25, the normalised drain voltage with respect to the input voltage can be written as

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \begin{cases} 0 & \text{for } 0 \leq \omega t < 2\pi D \\ \frac{2\pi\beta(\omega t)}{\int_{2\pi D}^{2\pi} \beta(\omega t) d\omega t} & \text{for } 2\pi D \leq \omega t < 2\pi. \end{cases} \quad (28)$$

5 Using Eq.15 the normalised switch's current with respect to the input DC current can be written as

$$\frac{i_S}{I_{IN}}(\omega t) = \begin{cases} 1 - p(k+1) \sin(\omega t + \phi) - (A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t)) & \text{for } 0 \leq \omega t < 2\pi D \\ 0 & \text{for } 2\pi D \leq \omega t < 2\pi. \end{cases} \quad (29)$$

By using the numerical solutions for A_1 , A_2 , B_1 , B_2 , p and ϕ , the voltage and current waveforms throughout the inverter can be plotted for given values of q_1 , duty cycle and k . Figures 11 - 13 show switch's voltage and current waveforms and the current of inductor L_2 for selected values of q_1 , duty cycle and k . In particular, Figure 11 depicts voltage and current waveforms at difference duty cycle and k values for $q_1 = 2$,
 10 Figure 12 for $q_1 = 3$ and Figure 13 for $q_1 = 4$.
 15

It can be noticed from the plotted waveforms that the switch's peak drain voltage and peak drain current and the shape of their waveform change according to the duty cycle. As the duty cycle decreases the switch's peak drain voltage increases and its peak drain current decreases. The switch's peak drain voltage decreases and its peak drain current increase as the duty cycle increases. The shape of the current through inductor L_2 is mainly affected by the value of k . The current is almost sinusoidal at high k values and its frequency ratio to the switching frequency is equal to the value q_1 over the entire switching period. The current becomes less sinusoidal, or contains additional harmonics, at low k values. For the case when $q_1 = 2$ the slope of the switch's current at the
 20
 25

instant when it is turned OFF is positive at a higher k , and is negative at a lower k .

[Input DC Resistance]

The DC component (or average) of the switch's current is equal
5 to the DC input current, hence

$$\begin{aligned} & \frac{1}{2\pi} \int_0^{2\pi} \frac{i_S}{I_{IN}}(\omega t) d\omega t = 1 \\ & = \frac{p}{2\pi} (\cos(2\pi D + \phi) - \cos \phi)(k+1) + D - \\ & \quad \frac{1}{2\pi q_1} (A_1 \sin(2\pi D q_1) + 2B_1 \sin^2(\pi D q_1)). \end{aligned} \quad (30)$$

Solving Eq.30 for p

$$p = \frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{(k+1)(\cos(2\pi D + \phi) - \cos \phi)}. \quad (31)$$

Substituting Eq.31 in Eq.15 gives the normalised value of i_m
10 with respect to the input DC current

$$\frac{i_m}{I_{IN}} = \frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{\cos(2\pi D + \phi) - \cos \phi}. \quad (32)$$

All the power supplied by the source will be consumed in the load, thus

$$\begin{aligned} P_{IN} &= P_o \\ V_{IN} I_{IN} &= \frac{1}{2} i_m^2 R_L. \end{aligned} \quad (33)$$

15 Rearranging the above equation and using Eq.32 gives in the input DC resistance seen by the source

$$\frac{V_{IN}}{I_{IN}} = R_{DC} = \frac{1}{2} \left(\frac{i_m}{I_{IN}} \right)^2 R_L \quad (34)$$

$$\frac{R_{DC}}{R_L} = \frac{1}{2} \left(\frac{2\pi(1-D) + \frac{A_1}{q_1} \sin(2\pi D q_1) + \frac{2B_1}{q_1} \sin^2(\pi D q_1)}{\cos(2\pi D + \phi) - \cos \phi} \right)^2. \quad (35)$$

Figure 14 shows the variation of the normalised DC resistance with duty cycle and k . For Figure 14a, $q_1 = 2$, Figure 14b with
20 $q_1 = 3$ and Figure 14c with $q_1 = 4$. It can be noticed that the

value of k has a small effect on the DC resistance whereas the duty cycle has a much more significant effect.

[Voltage and Current Stresses]

The peak voltage across the switch can be calculated by differentiation Eq.28 and setting it to zero

$$\frac{d \frac{v_{DS}}{V_{IN}}(\omega t)}{d\omega t} = 0 \quad (36)$$

which leads to the following equation

$$\frac{d\beta(\omega t)}{d\omega t} = \frac{i_{C1}}{I_{IN}}(\omega t) = 0. \quad (37)$$

An explicit solution does not exist for Eq.37, it can however be solved numerically for specific values of q_1 , duty cycle and k . Another approach to determine the peak voltage across the switch is to search for a value for ωt that maximises the switch's voltage. The Matlab function `fminbnd()` can be used to determine the switch voltage peaks for a certain q_1 value over a duty cycle range and a k .

The peak switch current can either occur during the switch ON period $0 \leq \omega t < 2\pi D$ or at the end of the switch ON period $\omega t = 2\pi D$. The peak switch current during the switch ON period can be obtained by differentiating Eq.29 and setting it to zero and solved for ωt

$$\frac{d \frac{i_S}{I_{IN}}(\omega t)}{d\omega t} = 0. \quad (38)$$

The calculated value of ωt should be substituted back into Eq.29 and the evaluated peak switch current should be compared with the switch's current value at $\omega t = 2\pi D$ and the switch's maximum current is the greater value of the two. Alternatively, the peak switch current can be found by searching for a value for ωt that maximises the switch's current. Figures 15 - 18 show that the switch's maximum

voltage and current normalised with respect to the input voltage and input DC current respectively for $q_1 = 2$, $q_1 = 3$ and $q_1 = 4$. In particular Figure 15a depicts max switch voltage for $q_1 = 2$, Fig 16a for $q_1 = 3$ and Fig 17a for $q_1 = 4$.
 5 Fig 15b depicts max switch current $q_1 = 2$, Fig 16b for $q_1 = 3$ and Fig 17b for $q_1 = 4$. It can be noted from the figures that large values of k have a slight effect on the peak values of the switch's voltage and current whereas the duty cycle has a much more significant effect.

10 [Power output capability]

The power output capability is defined as the ratio of the output power to the maximum voltage and current stresses of the switch. It is an indication of the switch utilization for a certain output power. It can be represented as

$$15 \quad c_p = \frac{P_o}{v_{DSmax} i_{Smax}}. \quad (39)$$

Since it has been assumed that the inverter is ideal therefore all the power supplied by the source is consumed in the load, the output power capability can be written as

$$c_p = \frac{V_{IN} I_{IN}}{v_{DSmax} i_{Smax}}. \quad (40)$$

20 Using the solutions obtained from Eq.37 & 38 the output power capability can be calculated for specific values of q_1 . Figures 18 - 20 show the variation of the output power capability with duty cycle and k for $q_1 = 2$, $q_1 = 3$, $q_1 = 4$. In particular, Figures 18a and 18b show the variation of
 25 output power capability for $q_1 = 2$. Figure 18c depicts a graphical solution for 80% of the maximum output power capability level according to that depicted in Figure 18b. Similarly, Figure 18d depicts 90% of the maximum output power capability level according to that depicted in Figure 18b.
 30 Figures 19a and 19b for $q_1 = 3$. Figure 20a and 20b for $q_1 = 4$.

[Design Equations and Special Cases for the Class EF2 Inverter]

[Power output capability as a function of k]

Since the inverter can operate at any given value of q_1 , duty cycle and k , it is of interest to operate the inverter 101 at its highest power output capability point. It will be assumed that series L_2C_2 is tuned to the second harmonic of the switching frequency, i.e. $q_1 = 2$ (Class EF2). The aim now is for a given k to find the value of duty cycle that will result in the highest power output capability operation. Figures 21a and 21b show the path of maximum output capability as k and the duty cycle vary. Figure 22 shows the variation of the parameters A_1 , A_2 , B_1 , B_2 , q_2 , p and ϕ along the maximum output power capability path.

Figure 23a shows the variation of the switch's peak drain voltage with k . Figure 23b shows the variation of the switch's peak drain current with k .

It can be noticed from Figure 22 that as k increases the value of q_2 approaches the value of q_1 which is 2. The values of the coefficients A_1 and A_2 begin to approach each other and the values of the coefficients B_1 and B_2 approach each other as well. This means that the current in inductor L_2 becomes sinusoidal with a frequency equal to $q_1\omega$ or 2ω for the case when $q_1 = 2$.

Based on the previous analysis the graphical solutions of the normalised values of the input resistance R_{DC} , capacitors C_1 , C_2 and residual impedance L_x can be plotted as shown in Figure 20. It can be noticed in Figure 20a that for a k value below 12 the input resistance is higher than that of the Class E inverter, this means that at a certain input voltage and load resistance the Class EF inverter provides less power than

the Class E inverter. For k values higher than 12 the input resistance is lower than that of the Class E inverter, this means that the Class EF inverter will provide more power than the Class E inverter for a certain load resistance and input voltage. Using the Curve Fitting Toolbox in Matlab the following equations have been obtained that provide an accurate fit to the graphical solutions in Figure 20 which depicts the variation of R_L , R_x , C_1 and C_2 with k for maximum power output capability.

$$D(k) = \frac{0.39275k - 0.26593}{k - 0.62755} \quad (41)$$

$$\frac{R_{DC}}{R_L}(k) = \frac{1.6835k - 1.1984}{k - 1.0681} \quad (42)$$

$$\omega R_L C_1(k) = \frac{0.14069k + 0.08613}{k + 0.1315} \quad (43)$$

$$\omega R_L C_2(k) = \omega R_L C_1(k)k \quad (44)$$

$$\frac{\omega L_2}{R_L}(k) = \frac{1}{4\omega R_L C_2(k)} \quad (45)$$

$$\frac{\omega L_x}{R_L}(k) = \frac{0.58805k - 0.10034}{k - 0.82871} \quad (46)$$

$$\omega R_L C_3(k) = \frac{1}{Q_L - \frac{\omega L_x}{R_L}(k)} \quad (47)$$

Eqs.42-47 can be used to determine the values of capacitors C_1 , C_2 and C_3 and the required duty cycle for a given k, load resistance R_L , switching frequency and output network quality factor Q_L that will result in the highest power output capability operation.

[Special Case I: Solution for maximum power output capability operation]

For the case when $q_1 = 2$ the maximum power output capability is 0.1323 which occurs when the duty cycle is 0.375 and k is 0.867. In this case the values of $A_1 = -0.9394$, $A_2 = -0.8589$, $B_1 = -1.2405$, $B_2 = -1.2276$, $p = 1.9204$, $\phi = 2.5701$ rad, $q_2 = 2.9349$ and $\int_{2\pi D}^{2\pi} \beta(\omega t) = \int_{0.75\pi}^{2\pi} \beta(\omega t) = 5.3241$.

According to Figure 18c, 80% or above of the maximum output power capability can be obtained when k lies in the range of greater than equal to 0.7 and less than or equal to 1.0, while D is greater than or equal to 0.35 and less than or equal to 0.40.

According to Figure 18d, 90% or above of the maximum output power capability is obtained when k lies in the range of greater than equal to 0.8 and less than or equal to 1.0 while D is greater than or equal to 0.35 and less than or equal to 0.40.

The values of the normalised output current, input resistance and maximum voltage and current stresses are given in Table 2 at the end of this analysis.

The switch's voltage, switch's current and the current through inductor L_2 for this particular case are

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \begin{cases} 0 & \text{for } 0 \leq \omega t < 0.75\pi \\ -1.4510 + 0.5481\omega t - 1.6673 \sin(\omega t + 57.26^\circ) \\ \quad + 0.6024 \sin(2.9349\omega t - 55.02^\circ) & \text{for } 0.75\pi \leq \omega t < 2\pi \end{cases} \quad (48)$$

$$\frac{i_{DS}}{I_{IN}}(\omega t) = \begin{cases} 1 - 3.5853 \sin(\omega t + 147.25^\circ) + 1.5560 \sin(2\omega t - 142.86^\circ) & \text{for } 0 \leq \omega t < 0.75\pi \\ 0 & \text{for } 0.75\pi \leq \omega t < 2\pi \end{cases} \quad (49)$$

$$\frac{i_{L2}}{I_{IN}}(\omega t) = \begin{cases} 1.5560 \sin(2\omega t - 142.86^\circ) & \text{for } 0 \leq \omega t < 0.75\pi \\ 0.5356 + 1.4982 \sin(2.9349\omega t - 145.02^\circ) \\ \quad - 2.1726 \sin(\omega t + 147.25^\circ) & \text{for } 0.75\pi \leq \omega t < 2\pi. \end{cases} \quad (50)$$

Figure 25 shows the voltage and current waveforms for this particular case. The normalised maximum voltage across the switch is 2.3162 which occurs at $\omega t = 4.9349$, the normalised maximum switch current is 3.2632 which occurs at $\omega t = 1.1310$ and at $\omega t = 2\pi D = 2.3562$.

Next, the values of further components will be determined for this particular case. Starting with C_1 , referring to Eqs.26 & 27 the average voltage of the switch's voltage is

$$V_{IN} = \frac{I_{IN}}{2\pi\omega C_1} \int_{0.75\pi}^{2\pi} \beta(\omega t) d\omega t = 5.3241 \frac{I_{IN}}{2\pi\omega C_1} \quad (51)$$

and using Eq.35

$$\frac{V_{IN}}{I_{IN}} = R_{DC} = 6.4273 R_L = 5.3241 \frac{1}{2\pi\omega C_1}. \quad (52)$$

Therefore the normalised reactance value of C_1 with respect to the load is

$$\frac{1}{\omega R_L C_1} = 7.5851. \quad (53)$$

Using Eq.13 the normalised value of C_2 is

$$\frac{1}{\omega R_L C_2} = 6.5762. \quad (54)$$

Using Eq.6 the normalised value of L_2 is

$$\frac{\omega L_2}{R_L} = 1.6441. \quad (55)$$

The value of the residual impedance is equal to

$$\omega L_x = \frac{v_x}{i_m} \quad (56)$$

where v_x is the amplitude of the voltage across the residual impedance and is equal to

$$v_x = \frac{1}{\pi} \int_{2\pi D}^{2\pi} v_{DS}(\omega t) \cos(\omega t + \phi) d\omega t. \quad (57)$$

Using Eq.28 v_x is also equal to

$$\frac{v_x}{V_{IN}} = \frac{2 \int_{0.75\pi}^{2\pi} \beta(\omega t) \cos(\omega t + \phi) d\omega t}{\int_{0.75\pi}^{2\pi} \beta(\omega t) d\omega t} = 1.1346 \quad (58)$$

Using Eq.32 & 35 the normalised value of the residual impedance is

$$\frac{\omega L_x}{R_L} = 2.0339 \quad (59)$$

and the normalised reactance value of C_3 is

$$\frac{1}{\omega R_L C_3} = Q_L - \frac{\omega L_x}{R_L} = Q_L - 2.0339 \quad (60)$$

[Special Case II: Solution for operation at high k values]

Case II corresponds to the previously discussed steady state case.

The analysis and design equations can be simplified for operation at a value of k higher than 20. The following assumptions can be concluded based on the previous sections as k begins to increase

$$k > 20 \quad (61)$$

$$p \rightarrow 0 \quad (62)$$

$$q_2 \approx q_1 \quad (63)$$

$$A_2 \approx A_1 \quad (64)$$

$$B_2 \approx B_1 \quad (65)$$

Applying the above assumptions to Eqs.5 & 12 the current through inductor L_2 for the period $0 \leq \omega t < 2\pi$ can be written as

$$\frac{i_{L_2}}{I_{IN}}(\omega t) = A_1 \cos(q_1 \omega t) + B_1 \sin(q_1 \omega t) \text{ for } 0 \leq \omega t < 2\pi. \quad (66)$$

The above equation shows that the current through inductor L_2 is sinusoidal for the entire switching signal with a frequency equal to the resonant frequency of L_2 and C_2 which is equal to $q_1 \omega$. The current in the switch when it is turned ON is

$$\begin{aligned} \frac{i_S}{I_{IN}}(\omega t) &= 1 - \frac{i_o}{I_{IN}}(\omega t) - \frac{i_{L_2}}{I_{IN}}(\omega t) \\ &= 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - A_1 \cos(q_1 \omega t) - \\ &\quad B_1 \sin(q_1 \omega t) \text{ for } 0 \leq \omega t < 2\pi D. \end{aligned} \quad (67)$$

The harmonic content of the current in the switch consists of a DC component, a component at the fundamental switching frequency ω and a component at the resonant frequency of $L_2 C_2$ which here is $q_1 \omega$. The components with frequency $q_1 \omega$ can be

calculated using two quadrature current Fourier components at $q_1\omega$. These two quadrature Fourier components are equal to A_1 and B_1 respectively as follows

$$\begin{aligned} A_1 &= -\frac{1}{\pi} \int_0^{2\pi D} \frac{i_S}{I_{IN}}(\omega t) \cos(q_1 \omega t) d\omega t \\ &= -\frac{\sin(2\pi D q_1)}{q_1 \pi} \left(1 - \frac{B_1 \sin(2\pi D q_1)}{2} \right) + \frac{A_1}{\pi} \left(\frac{\sin(4\pi D q_1)}{4q_1} + \pi D \right) - \\ &\quad \frac{\frac{i_m}{I_{IN}}}{\pi} \left(\frac{\cos \phi}{q_1^2 - 1} + \frac{\cos(\phi + 2\pi D(q_1 + 1))}{2(q_1 + 1)} - \frac{\cos(\phi - 2\pi D(q_1 - 1))}{2(q_1 - 1)} \right) \end{aligned} \quad (68)$$

$$\begin{aligned} B_1 &= -\frac{1}{\pi} \int_0^{2\pi D} \frac{i_S}{I_{IN}}(\omega t) \sin(q_1 \omega t) d\omega t \\ &= -\frac{2 \sin^2(\pi D q_1)}{q_1 \pi} \left(1 - \frac{A_1}{4} \right) - \frac{B_1}{\pi} \left(\frac{\sin(4\pi D q_1)}{4q_1} - \pi D \right) - \\ &\quad \frac{\frac{i_m}{I_{IN}}}{\pi} \left(\frac{-\sin \phi}{q_1^2 - 1} + \frac{\sin(\phi + 2\pi D(q_1 + 1))}{2(q_1 + 1)} + \frac{\sin(\phi - 2\pi D(q_1 - 1))}{2(q_1 - 1)} \right). \end{aligned} \quad (69)$$

5

The current in capacitor C_1 when the switch is turned OFF is

$$\begin{aligned} \frac{i_{C_1}}{I_{IN}}(\omega t) &= 1 - \frac{i_o}{I_{IN}}(\omega t) - \frac{i_{L_2}}{I_{IN}}(\omega t) = 1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - \\ &A_1 \cos(q_1 \omega t) - B_1 \sin(q_1 \omega t) \quad \text{for } 2\pi D \leq \omega t < 2\pi. \end{aligned} \quad (70)$$

From Eq.28 the voltage developed across capacitor C_1 is

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \frac{2\pi \beta'(\omega t)}{\int_{2\pi D}^{2\pi} \beta'(\omega t) d\omega t} \quad \text{for } 2\pi D \leq \omega t < 2\pi \quad (71)$$

10 where

$$\begin{aligned} \beta'(\omega t) &= \int_{2\pi D}^{\omega t} \frac{i_{C_1}}{I_{IN}}(\tau) d\tau = \omega t - 2\pi D + \frac{i_m}{I_{IN}} (\cos(\omega t + \phi) - \\ &\cos(\phi + 2\pi D)) - \frac{A_1}{q_1} (\sin(q_1 \omega t) - \sin(2\pi D q_1)) + \\ &\frac{B_1}{q_1} (\cos(q_1 \omega t) - \cos(2\pi D q_1)). \end{aligned} \quad (72)$$

Substituting the ZVS ($v_{DS}(2\pi) = 0$) and ZDS ($i_{C_1}(2\pi) = 0$) conditions in Eq.71 gives the following two equations

$$\begin{aligned} 2\pi(1 - D) + \frac{i_m}{I_{IN}} (\cos \phi - \cos(2\pi D + \phi)) - \frac{A_1}{q_1} (\sin(2\pi q_1) \\ - \sin(2\pi D q_1)) + \frac{B_1}{q_1} (\cos(2\pi q_1) - \cos(2\pi D q_1)) = 0 \end{aligned} \quad (73)$$

$$1 - A_1 \cos(2\pi q_1) - B_1 \sin(2\pi q_1) - \frac{i_m}{I_{IN}} \sin \phi = 0. \quad (74)$$

Eqs.68, 69, 73 & 74 are four simultaneous equations that can be solved numerically for i_m/I_{IN} , ϕ , A_1 and B_1 for a given value of q_1 and duty cycle.

The peak drain current can be obtained by differentiating Eq.71 and setting it to zero which results in the following equation

$$A_1 q_1 \sin(q_1 \omega t) - B_1 q_1 \cos(q_1 \omega t) - \frac{i_m}{I_{IN}} \cos(\omega t + \phi) = 0 \quad (75)$$

which can be solved numerically. The peak drain voltage can be obtained by differentiating Eq.71 and setting it to zero which results in the following equation

$$1 - \frac{i_m}{I_{IN}} \sin(\omega t + \phi) - A_1 \cos(q_1 \omega t) - B_1 \sin(q_1 \omega t) = 0 \quad (76)$$

which can also be solved numerically. It should be noted that drain voltage may contain two local maximum points depending on the set duty cycle. Therefore the maximum drain voltage is the highest of the two local maximum voltages. The output power capability can then be calculated from Eq.40.

The above equations can be used to proceed with the calculations of the values of the components and other parameters. However, by observing Figure 21b, it can be noticed that the maximum output power capability and the associated duty cycle approach 0.115 and 0.392 respectively as k increases when $q_1 = 2$. By approximating the duty cycle value for maximum output power capability to 0.40, the solved values of $A_1 = 0.96012$, $B_1 = -0.18365$, $i_m/I_{IN} = 1.8099$, $\phi = 3.1196$ and $\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t = 1.3195$

From Eq. 34 the normalised input DC resistance is

$$\frac{R_{DC}}{R_L} = \frac{1}{2} \left(\frac{i_m}{I_{IN}} \right)^2 = 1.6379 \quad (77)$$

and the output power is

$$P_o = 0.6105 \frac{V_{IN}^2}{R_L}. \quad (78)$$

From Eqs.26 & 27 and using Eq.77 and the solved value of $\int \beta'(\omega t) d\omega t$ the normalised value of capacitor C_1 is

$$\frac{1}{\omega R_L C_1} = 2\pi \frac{R_{DC}}{R_L} \frac{1}{\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t} = 7.7993. \quad (79)$$

5 From Eq.58 the voltage across the residual impedance is

$$\frac{v_x}{V_{IN}} = \frac{2 \int_{0.8\pi}^{2\pi} \beta'(\omega t) \cos(\omega t + \phi) d\omega t}{\int_{0.8\pi}^{2\pi} \beta'(\omega t) d\omega t} = 0.62424. \quad (80)$$

From Eq.56 and using Eq.77 and the solved value of i_m/I_{IN} the normalised value of the residual impedance is

$$\frac{\omega L_x}{R_L} = 0.56491. \quad (81)$$

10 and from Eqs.60 the normalised value of capacitor C_3 is

$$\frac{1}{\omega R_L C_3} = Q_L - \frac{\omega L_x}{R_L} = Q_L - 0.56491. \quad (82)$$

The values of L_2 and C_2 should be chosen such that their resonant frequency is equal to 2ω and k is larger than 20. Figure 26 shows voltage and current waveforms for this particular case. The values of the normalised output current and maximum voltage and current stresses are given in Table 2.

[Special Case III: Maximum switching frequency]

The maximum frequency that the Class EF can operate at is when the value of C_1 equals the output capacitance of the switch C_o (assuming that the switch's output capacitance is linear). For the maximum output power capability case ($q_1 = 2$, $D = 0.375$, $k=0.867$) the maximum frequency at which the ZVS and ZDS conditions can be achieved is determined from Eq.53

$$f_{\max} = \frac{1}{7.5851 \times 2\pi R_L C_o} = \frac{0.02098}{R_L C_o} \quad (83)$$

which is about 0.7 times that of the Class E inverter. For the case when $k > 20$ the maximum frequency at which the ZVS and ZDS conditions can be achieved is determined from Eq.79

$$f_{\max} = \frac{1}{7.7993 \times 2\pi R_L C_o} = \frac{0.02041}{R_L C_o} \quad (84)$$

which is about 0.7 times that of the Class E inverter.

By examining Figure 24c the maximum frequency the Class EF inverter can operate at and at the same time operate at the maximum output power capability is at the maximum value of $\omega R_L C_1$. Figure 27 shows a closer look at the variation of $\omega R_L C_1$ with k , the peak value is 0.17588 when $k = 1.567$ and $D = 0.3718$. The maximum frequency at which the ZVS and ZDS conditions can be achieved is

$$f_{\max} = \frac{0.17588}{2\pi R_L C_o} = \frac{0.02799}{R_L C_o} \quad (85)$$

which approximately equals to the maximum frequency of the Class E inverter.

However, Figure 27b shows that for 80% or above of the maximum switching frequency is obtained with a k value greater than or equal to 1 and less than or equal to 5, while the corresponding D value is greater than or equal to 0.35 and less than or equal to 0.40.

Similarly, Figure 27c shows that for 90% or above of the maximum switching frequency is obtained with a k value greater than or equal to 1.2 and less than or equal to 3.7, while the corresponding D value is greater than or equal to 0.35 and less than or equal to 0.40.

The design equations for this new particular case (maximum frequency case), which can be calculated in a similar manner to what has been done for Case I, are given in Table 2. The

values of the normalised output current, maximum voltage and current stresses, input DC resistance and output power capability are also given in Table 2. Figure 28 shows the voltage and current waveforms for this particular case.

5 [Minimum input choke inductance]

The minimum inductance value of the input choke will be determined here for all of the special cases above. When the switch is ON, the voltage across the input choke is

$$v_{L_1}(\omega t) = V_{IN} \quad (86)$$

10 and the current through the choke inductance is

$$i_{L_1}(\omega t) = \frac{1}{\omega L_1} \int_0^{\omega t} v_{L_1}(\omega t) d\omega t + i_{L_1}(0) = \frac{V_{IN}}{\omega L_1} \omega t + i_{L_1}(0). \quad (87)$$

The current in the input choke at the end of the ON period is

$$i_{L_1}(2\pi D) = 2\pi D \frac{V_{IN}}{\omega L_1} + i_{L_1}(0). \quad (88)$$

Therefore the peak-to-peak ripple in the input current is

$$15 \quad \Delta i_{L_1} = i_{L_1}(2\pi D) - i_{L_1}(0) = 2\pi D \frac{V_{IN}}{\omega L_1}. \quad (89)$$

The minimum input choke inductance required for the maximum peak-to-peak current ripple is

$$L_{1min} = 2\pi D \frac{V_{IN}}{\omega \Delta i_{L_1max}}. \quad (90)$$

20 Using Eq.34 the minimum input choke inductance can be written as

$$L_{1min} = 2\pi D \frac{R_{DC}}{\omega \frac{\Delta i_{L_1}}{I_{IN}}}. \quad (91)$$

The above equation gives the minimum input choke inductance for a certain maximum input current ripple percentage. For the maximum output power capability case (Case I, $q_1 = 2$, $D =$

0.375, $k = 0.867$) the minimum inductance for a 10% ($\Delta i_{L1}/I_{IN} = 0.1$) input ripple current is

$$L_{1min} = 24.1024 \frac{R_L}{f} \quad (92)$$

which is about 2.7 times more than that of the Class E inverter.

For the case when $k > 20$ (Case II) the minimum inductance for a 10% ($\Delta i_{L1}/I_{IN} = 0.1$) input ripple current is

$$L_{1min} = 6.5516 \frac{R_L}{f} \quad (93)$$

which is about 0.8 times less than that of the Class E inverter.

For the maximum frequency case (Case III) the minimum inductance for a 10% ($\Delta i_{L1}/I_{IN} = 0.1$) input ripple current is

$$L_{1min} = 10.5952 \frac{R_L}{f} \quad (94)$$

which is about 1.2 times more than that of the Class E inverter.

[Efficiency]

The losses and efficiency will be considered for all special cases. The efficiency is defined as $\eta = P_o/P_{IN}$. Beginning with the input choke, it's losses can be represented by a series resistor r_f which includes the winding resistance and core losses. According to the first assumption, the current in the input choke is constant therefore the loss in the input choke is equal to

$$P_{L1} = I_{IN}^2 r_f = \frac{2}{\left(\frac{i_m}{I_{IN}}\right)^2} \frac{r_f}{R_L} P_o. \quad (95)$$

The switch conduction power loss due to its ON resistance r_{DS} is determined first by calculating the rms value of the switch's current from Eq.29 as follows

$$i_{S_{rms}} = I_{IN} \sqrt{\frac{1}{2\pi} \int_0^{2\pi D} \frac{i_S^2}{I_{IN}^2} (\omega t) d\omega t} \quad (96)$$

5 and the conduction power loss is

$$P_{DS} = i_{S_{rms}}^2 r_{DS} = \frac{1}{\pi \left(\frac{i_m}{I_{IN}} \right)^2} \int_0^{2\pi D} \frac{i_S^2}{I_{IN}^2} (\omega t) d\omega t \frac{r_{DS}}{R_L} P_o. \quad (97)$$

The power loss in the shunt capacitor C_1 due to its resistance r_{C_1} is determined first by calculation the rms value of it's current from Eq. 21 as follows

$$i_{C_1_{rms}} = I_{IN} \sqrt{\frac{1}{2\pi} \int_{2\pi D}^{2\pi} \frac{i_{C_1}^2}{I_{IN}^2} (\omega t) d\omega t} \quad (98)$$

and the power loss is

$$P_{C_1} = i_{C_1_{rms}}^2 r_{DS} = \frac{1}{\pi \left(\frac{i_m}{I_{IN}} \right)^2} \int_{2\pi D}^{2\pi} \frac{i_{C_1}^2}{I_{IN}^2} (\omega t) d\omega t \frac{r_{C_1}}{R_L} P_o. \quad (99)$$

The power loss in the series tuned L_2C_2 branch due to the ESR of the inductor r_{L_2} and the resistance loss of the capacitor r_{C_2} is first determined by calculated the rms current value of inductor L_2 as from Eqs.5 & 12 as follows

$$i_{L_2_{rms}} = I_{IN} \sqrt{\frac{1}{2\pi} \int_0^{2\pi} \frac{i_{L_2}^2}{I_{IN}^2} (\omega t) d\omega t} \quad (100)$$

and the total power loss is

$$\begin{aligned} P_{L_2C_2} &= i_{L_2_{rms}}^2 (r_{L_2} + r_{C_2}) \\ &= \frac{1}{\pi \left(\frac{i_m}{I_{IN}} \right)^2} \int_0^{2\pi} \frac{i_{L_2}^2}{I_{IN}^2} (\omega t) d\omega t \left(\frac{r_{L_2} + r_{C_2}}{R_L} \right) P_o. \end{aligned} \quad (101)$$

20 The power loss in the output load network L_3C_3 due to the inductor's ESR r_{L_3} and the capacitor's resistance r_{C_3} is

$$P_{L_3 C_3} = \frac{r_{L_3} + r_{C_3}}{R_L} P_o \quad (102)$$

The turn-ON switching power loss of the switch is assumed to be zero if the ZVS condition is achieved. The turn-OFF switching power loss can be estimated as follows (according to M. K. Kazimierczuk, RF Power Amplifiers, 2nd ed. Chichester, UK: John Wiley & Sons Ltd, 2015.). The switch current during turn-OFF t_f can be assumed to decrease linearly. Using Eq.29 the switch's current can be represented as

$$\frac{i_S}{I_{IN}}(\omega t) = \frac{i_S}{I_{IN}}(2\pi D) \left(1 - \frac{\omega t - 2\pi D}{\omega t_f} \right) \quad \text{for } 2\pi D < \omega t \leq 2\pi D + \omega t_f \quad (103)$$

and the current in the shunt capacitor C_1 can be approximated by

$$\frac{i_{C_1}}{I_{IN}}(\omega t) \approx \frac{i_S}{I_{IN}}(2\pi D) \left(\frac{\omega t - 2\pi D}{\omega t_f} \right) \quad \text{for } 2\pi D < \omega t \leq 2\pi D + \omega t_f. \quad (104)$$

The voltage across the switch is

$$\begin{aligned} v_{DS}(\omega t) &= \frac{I_{IN}}{\omega C_1} \frac{i_S}{I_{IN}}(2\pi D) \int_{2\pi D}^{\omega t} \frac{i_{C_1}}{I_{IN}}(\tau) d\tau \\ &= \frac{I_{IN}}{\omega C_1} \frac{i_S}{I_{IN}}(2\pi D) \frac{(\omega t - 2\pi D)^2}{\omega t_f} \end{aligned} \quad (105)$$

and using Eqs.26 & 27 the voltage across switch can be represented as

$$\frac{v_{DS}}{V_{IN}}(\omega t) = \frac{2\pi}{\int_{2\pi D}^{2\pi D + \omega t_f} \beta(\omega t) d\omega t} \frac{i_S}{I_{IN}}(2\pi D) \frac{(\omega t - 2\pi D)^2}{\omega t_f}. \quad (106)$$

The average power dissipated in the switch is

$$\begin{aligned} P_{t_f} &= \frac{V_{IN} I_{IN}}{2\pi} \int_{2\pi D}^{2\pi D + \omega t_f} \frac{i_S}{I_{IN}}(\omega t) \frac{v_{DS}}{V_{IN}}(\omega t) d\omega t \\ &\approx P_o \frac{\frac{i_S}{I_{IN}}(2\pi D)}{\int_{2\pi D}^{2\pi D + \omega t_f} \beta(\omega t) d\omega t} \int_{2\pi D}^{2\pi D + \omega t_f} \left(1 - \frac{\omega t - 2\pi D}{\omega t_f} \right) \frac{(\omega t - 2\pi D)^2}{\omega t_f} d\omega t \\ &= P_o \frac{\frac{i_S^2}{I_{IN}^2}(2\pi D)}{\int_{2\pi D}^{2\pi D + \omega t_f} \beta(\omega t) d\omega t} \frac{\omega t_f^2}{24} = P_o \frac{(\omega t_f)^2}{12}. \end{aligned} \quad (107)$$

The efficiency of the inverter is

$$\eta = \frac{1}{1 + P_{L_1} + P_{DS} + P_{C_1} + P_{L_2}C_2 + P_{L_3}C_3 + P_{t_f}}. \quad (108)$$

Table 1 lists the numerical evaluations for all the power loss equations for the special cases described in the previous section. Figure 29 compares the efficiencies of all special cases of the Class EF2 with the Class E as the load resistance varies. All of the special case Class EF2 inverters and the Class E have the same loss resistances of their components. It can be seen that the Class EF2 inverter at special cases I and II have the highest efficiencies especially at low load resistance values.

Normalised Power	Class EF_2 Case I (max c_p)	Class EF_2 Case II $k > 20$	Class EF_2 Case III (max f)	Class E $D = 0.5$
P_{L_1}	0.155 59	0.610 54	0.351 08	0.576 66
P_{DS}	0.454 21	1.8298	1.0876	1.3648
P_{C_1}	0.231 59	0.072 434	0.173 94	0.211 88
$P_{L_2}C_2$	0.354 97	0.291 70	0.244 49	-
P_{t_f}	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$	$\approx \frac{\omega t_f}{12}$

Table 1: Numerically calculated powers

[Summary of design equations and parameters for all special cases of the Class EF2 inverter]

Table 2 summarises all the design equations and parameters for all the special cases of the Class EF2 inverter in comparison with the Class E inverter.

Power	Class EF ₂ Case I (max c_p)	Class EF ₂ Case II $k \geq 20$	Class EF ₂ Case III (max f)	Class E $D = 0.5$
D	0.3750	0.4000	0.3718	0.5000
k	0.867	≥ 20	1.567	-
q_2	2.9349	≈ 2		-
$\frac{1}{\omega R_L C_1}$	7.5851	7.7993	5.6857	5.4466
$\frac{1}{\omega R_L C_2}$	6.5762	-	8.9095	-
$\frac{\omega L_x}{R_L}$	2.0339	0.5649	1.1167	1.1525
$\frac{f L_{1\min}}{R_L}$	24.1024	6.5516	10.5952	8.6685
$\frac{R_{DC}}{R_L}$	6.4273	1.6379	2.8497	1.7337
c_p	0.1323	0.1152	0.1199	0.0981
$\frac{1}{f_{\max} R_L C_o}$	47.6644	48.9956	35.7270	19.7394
$\frac{P_o R_L}{V_{IN}^2}$	0.1556	0.6105	0.3509	0.5768
$\frac{v_{DS}^{\max}}{V_{IN}}$	2.3162	2.2964	2.2433	3.5620
$\frac{i_S}{I_{IN}}^{\max}$	2.3562	3.7790	4.8561	2.8620

Table 2: Summary of all design equations and performance parameters

[Semi-resonant operation (Impedance transformation)]

- 5 The reflected load of the secondary side in an inductive power transfer system tends to be low, generally between 1-10Ω. Referring to Figure 29 the efficiency of the inverter is below 90% due to the increased current stresses. Power efficiency is important in an inductive power transfer system and therefore
- 10 it should be maximised as much as possible.

Figure 30 depicts an impedance transformation network which is referred to as semi-resonant operation and increases the power efficiency of the inverter 101. A capacitor C_{res} is connected in parallel with inductance L_3 (which could represent the

15 inductance of the transmitting coil in an inductive power transfer system) and the load resistance R_L (which could represent the reflected load in an inductive power transfer

system). Capacitor C_{Eq} will increase the load resistance seen by the inverter as long as its reactance at the switching frequency is below the reactance of inductor L_3 . It will also decrease the reactance of L_3 as seen by the inverter. Although
 5 semi-resonant operation may increase the load resistance seen by the inverter, the reduction of the reactance of L_3 as seen by the inverter will result in a lower loaded Q which may lead to an increase in harmonics.

The impedance of the equivalent resistance (R_{Eq}) and the
 10 equivalent inductance (L_{Eq}) due to the addition of C_{res} is

$$\begin{aligned} Z_{Eq} &= R_{Eq} + jX_{L_{Eq}} = \frac{-jX_{C_{res}}(R_L + jX_{L_3})}{R_L + jX_{L_3} - jX_{C_{res}}} \\ &= \frac{X_{C_{res}}^2 R_L - j(X_{L_3}^2 X_{C_{res}} - X_{L_3} X_{C_{res}}^2 + X_{C_{res}} R_L^2)}{R_L^2 + (X_{L_3} - X_{C_{res}})^2}. \end{aligned} \quad (109)$$

Therefore the equivalent resistance is

$$R_{Eq} = \frac{X_{C_{res}}^2 R_L}{R_L^2 + (X_{L_3} - X_{C_{res}})^2}, \quad (110)$$

the equivalent inductance is

$$L_{Eq} = \frac{1}{\omega} \frac{X_{L_3}^2 X_{C_{res}} - X_{L_3} X_{C_{res}}^2 + X_{C_{res}} R_L^2}{R_L^2 + (X_{L_3} - X_{C_{res}})^2} \text{ where } X_{C_{res}} < X_{L_3}, \quad (111)$$

and the equivalent loaded quality factor is

$$Q_{Eq} = \frac{\omega L_{Eq}}{R_{Eq}}. \quad (112)$$

Eqs.110 - 112 can be incorporated in the design equations for each special case of the Class EF_2 inverter above without
 20 changing the results.

Figure 31 shows how the equivalent resistance and the equivalent inductance change according to C_{res} in a hypothetical inductive power transfer system which has a

primary coil inductance of 4 μH and an optimum reflected load of 2 Ω operating at 6.78 MHz.

[Experimental Verification and Results]

Experimental verification for all of the defined special cases of the Class EF_2 inverter have been carried out on a 23W prototype with a switching frequency of 6.78 MHz was chosen for Cases I and II, and II a 8.60 MHz switching frequency was chosen for Case III to demonstrate its capability to operate at higher frequencies. In order to ensure a fair comparison, the same MOSFET, load resistance and inductance L_3 were used when verifying all of the special cases.

[Experimental set-up]

The inductance of the MOSFET's package should be as small as possible to allow for the megahertz switching frequencies to be achieved and to allow for 'clean' voltage waveforms to be recorded. In addition, the MOSFET's total gate charge should be reasonably low to reduce gate drive losses. Finally, the MOSFET's output capacitance should be as low as possible, ideally below 500pF at a certain input voltage. This is important to firstly prevent the MOSFET's output capacitance from achieving the desired switching frequencies and secondly, to reduce the effect of the non-linearity of the MOSFET's output capacitance on the performance of the inverter. The MOSFET SiS892ADN 100V, 28A from Vishay which is available in a surface mount 1212 package was found to be suitable. It's maximum ON resistance is 0.047 Ω and has a maximum input capacitance of approximately 850pF. Its output capacitance is below 400pF for DC drain voltages above 16V. The gate driver UCC27321 from Texas Instruments was used and a maximum gate drive voltage of 7.0V was set for all cases.

All the capacitors used were multilayer ceramic capacitors from AVX Corporation. The capacitors belong to the

manufacturer's 'Hi-Q' series and are designed for RF and microwave applications. Their ESR is below 0.04Ω for frequencies below 30MHz. Inductance L_3 had to be an air-core inductor to avoid the excessive power losses and saturation that are associated with using magnetic cores at high frequencies. It was formed using a coil that consisted of two turns with a diameter of approximately 15cm and using 4 AWG copper wire. It's inductance was measured to be approximately 1.25 μ H and its ESR is approximately 0.21Ω . The load consisted of three paralleled 15Ω 35W thick film resistors from Bourns. Each resistor had a maximum inductance of 0.1 μ H. The current probe N2783A from Keysight Technologies was used to record the output current. The total inductance of the current probe and the load resistors was assumed to be 0.1 μ H according to their datasheets and was added to the inductance of L_3 . The output power was calculated using the reading of the current probe which had accuracy of about 2%.

[Maximum power capability case (Case I)]

For Case I, the values of capacitors C_1 , C_2 and C_3 , in addition to all other parameters, were calculated for a switching frequency of 6.78MHz using the design equations given in Table 2 and their values are all listed in Table 3 below. The input voltage was calculated to be 30.25V and the MOSFET's output capacitance at this voltage was deducted for the calculated value of C_1 . Capacitors C_2 and C_3 each consisted of four parallel capacitors. The difference between the used total capacitance value of C_2 and the theoretical value is due to the parasitic capacitance of the PCB. The value of inductor L_2 was calculated to be 202.61nH. This inductor was formed by using two paralleled 430nH air-core inductors from Coilcraft (2929SQ series). The shape of the parallel coils were slightly altered to achieve the desired inductance. According to Eq. 50 the current in inductor L_2

contains several frequency components (1st, 2nd and 3rd), therefore the inductor's ESR will be different for each one of these components. For simplification, the ESRs at 6.78MHz, 13.56MHz and 20.34MHz were calculated according to the manufacturer's datasheet and their average was considered as a constant ESR for the entire switching period which was equal to 0.18Ω . Adding the DC resistance of the paralleled coils and the ESR of capacitor C_2 makes the total ESR in the L_2C_2 branch approximately 0.20Ω .

The measured input and output powers, input current and maximum MOSFET voltage are listed in Table 3 and are compared with their theoretical values. It can be noticed that error between measurements and theory is low. The recorded waveforms of the MOSFET's drain voltage and output current are shown in Figure 32a and the theoretical waveforms are shown in comparison. It can be noticed that recorded and theoretical waveforms are a close match. The phase shift in the recorded current waveform is due to the response behaviour of the current probe. The measured efficiency for this case was $91.1 \pm 2\%$.

[Maximum frequency case (Case III)]

The verification and design process for Case III was similar to that of Case I. The switching frequency was increased to 8.60MHz to show that this case can be operated at higher frequencies. Also, this specific frequency was chosen in order to keep the same parallel coils for inductor L_2 that were used in Case I. The average ESR for inductor L_2 was now approximately 0.25Ω .

The measured input and output powers, input current and maximum MOSFET voltage for this case are listed in Table 3. The error between measurements and theory for this case are minor. The recorded waveforms of the MOSFET's drain voltage

and output current are shown in Figure 32b. and the theoretical waveforms are shown in comparison. The recorded and theoretical waveforms are a close match as well. The measured efficiency for this case was $88.6 \pm 2\%$.

5 [k=20 case (Case II)]

For Case II, the switching frequency was decreased back to 6.78MHz. A k value of 20 was chosen in order to obtain the lowest inductance value for L_2 which was calculated to be 4.81 μ H. The magnetic core T106-2 from Mircometals had to be
10 used to achieve this inductance. The input voltage for a 23W output power was calculated to be approximately 15.5V. Although the MOSFET's output capacitance at this voltage was below the required C_1 capacitance, it's non-linearity in addition to the losses and saturation of the magnetic core of
15 inductor L_2 were quite significant and had an impact on inverter's performance. Therefore the SPICE model was used to verify the performance of the inverter in this case by simulating the experimental results. Table 2 compares the values of all components and the measured input and output
20 powers, input current and maximum MOSFET voltage in comparison with those of the SPICE simulation. Figure 32c compares between the recorded MOSFET's drain voltage and output current waveforms with the SPICE simulation. It can be noticed that the recorded waveforms are in good agreement with the SPICE
25 simulation. The calculated efficiency was $76 \pm 2\%$, the low efficiency is due to the excessive losses and possible saturation in the magnetic core used for inductor L_2 .

[Comparison with Class E operation]

The designed Class EF inverter was then compared with a Class
30 E inverter in order to prove that Case I and III can be more efficient. For the Class E inverter, the switching frequency was kept at 6.78MHz. The component values, input and output

powers, input current and maximum MOSFET voltage were calculated from the design equations in M. K. Kazimierczuk, RF Power Amplifiers, 2nd ed. Chichester, UK: John Wiley & Sons Ltd, 2015. The calculated input voltage was 16V and it was also found that the non-linearity of the MOSFET's output capacitance affected the performance of the inverter, therefore the SPICE model was used for verification.

The component values and measured parameters are listed in Table 3. The recorded MOSFET's drain voltage and output current waveforms shown in Figure 32d and an excellent agreement can be seen with the SPICE simulation. The calculated efficiency was $88.7 \pm 2\%$ which is lower than what had been achieved with Case I and is similar to what had been achieved with Case III as predicted by the theory.

Power	Class EF ₂		Class EF ₂		Class EF ₂		Class E	
	Case I (max c_p)		Case II ($k = 20$)		Case III (max f)		$D = 0.5$	
	Exp.	Theory	Exp.	SPICE	Exp.	Theory	Exp.	SPICE
C_1 (pF)	$257+C_o$	589.48	$47+C_o$	$50+C_o$	$257+C_o$	619.98	$330+C_o$	$220+C_o$
C_2 (pF)	667	679.92	29.30	28.66	392	395.65	-	-
C_3 (pF)	500	501.24	419.20	430.37	268	275.86	447	463
L_1 (μ H)	47	18.66	47		47	6.47	47	47
L_2 (nH)	215	202.61	4800	4810	215	216.41	-	-
L_3 (μ H)	1.35	1.35	1.35	1.35	1.35	1.35	1.35	1.35
R_L (Ω)	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
f (MHz)	6.78	6.78	6.78	6.78	8.60	8.60	6.78	6.78
D	-	0.375	-	0.400	-	0.37	-	0.500
V_{IN} (V)	30.0	30.25	17.49	17.50	20	20.38	16.0	16.0
I_{IN} (A)	0.83	0.83	1.49	1.40	1.20	1.24	1.31	1.38
P_{IN} (W)	24.9	24.97	26.06	24.55	24.0	25.15	20.96	22.08
P_o (W)	22.67	23.00	19.92	18.70	21.26	23.00	18.59	20.00
η (%)	91.1 ± 2	92.11	76.44 ± 2	76.17	88.6 ± 2	91.03	88.7 ± 2	90.6
$v_{DS \max}$	72	70.06	48.80	42.26	42.90	44.87	60.1	60.1

Table 3: Theoretical and measured parameters

[Conclusion]

The analysis above shows that the following conclusions can be made regarding the Class EF2 inverter:

1. The peak voltage across the MOSFET is about 2.2-2.3 times the input DC voltage compared to about 3.56 times the input DC voltage for the Class E inverter.
2. Class EF2 inverters in all special cases have a higher power output capability than Class E and Class D inverters. Their optimum duty cycle range is between 0.35-0.40 compared to a single optimum value of 0.50 for the Class E inverter.
3. It was shown that Class EF2 inverters can operate more efficiently with a low energy storage, or low Q , series resonant LC network especially at high frequencies. This is because air-core inductors can be used which can be easily designed to have low losses compared to a magnetic-core based inductor.
4. The maximum frequency of operation of the Class EF2 inverter, as defined in Case III, is slightly less than that of Class E inverters.
5. The power dissipation in the MOSFET's resistance is lower than that of the Class E inverter. This makes special Cases I and III of the Class EF2 inverter more efficient than Class E inverters especially for MOSFETs with ON resistances above 0.04Ω . The efficiency improvement becomes less significant for MOSFETs with very low ON resistances where the Class E inverter might be a better design choice because of its lower number of components.
6. For a given load resistance and required output power, the input voltage required for Cases I and III of the Class EF2 is higher than that of the Class E inverter. A higher input voltage might be beneficial because the input DC current and ripple will be lower, and the MOSFET's non-linear output capacitance will have a lower

impact of the inverter's performance as observed in the experimental results section.

7. Special Case II, the Class EF2 can deliver more power to a load compared to the Class E, however the efficiency will be lower due to the increased losses in the added resonant network.

The foregoing description of embodiments of the invention has been presented for the purpose of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Alternations, modifications and variations can be made without departing from the spirit and scope of the present invention.

CLAIMS

1. An inverter for inductive power transfer, the inverter comprising:

5 a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency;

a first capacitance in parallel with the switching element between the first inductor and a power supply
10 terminal;

a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor;

15 a second tank circuit in parallel with the first capacitance; and

a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit,

wherein the second tank circuit comprises a transmitter
20 coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil;

wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency, and

25 wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is an integer multiple, greater than one, of the first frequency.

30 2. The inverter according to Claim 1, wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double or triple the first frequency.

3. The inverter according to Claim 1 or Claim 2, wherein the fourth capacitance is arranged in parallel with the transmitter coil, and wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is greater than the first frequency.

4. The inverter according to Claim 1 or Claim 2, wherein the fourth capacitance is arranged in series with the transmitter coil, and wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is less than the first frequency.

5. The inverter according to any of Claims 1 - 4, wherein the first capacitance is part of the output capacitance of the switching element.

6. An inductive power transfer transmitter comprising:
an inverter according to any of Claims 1 - 5; and
a controller operable to switch the switching element of the inverter at the first frequency.

7. The inductive power transfer transmitter according to Claim 6, wherein:

the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency,

the ratio of the first capacitance to the second capacitance is greater than or equal to 0.7 and less than or equal to 1, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

8. The inductive power transfer transmitter according to Claim 7, wherein:

the ratio of the first capacitance to the second capacitance is greater than or equal to 0.8 and less than or equal to 1, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

9. The inductive power transfer transmitter according to Claim 7, wherein:

the ratio of the first capacitance to the second capacitance is greater than or equal to 0.767 and less than or equal to 0.967, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.365 and less than or equal to 0.385.

10. The inductive power transfer transmitter according to Claim 9, wherein the ratio of the first capacitance to the second capacitance is 0.867 and the controller is arranged to switch the switching element with a duty cycle of 0.375.

11. The inductive power transfer transmitter according to Claim 6, wherein:

the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency,

the ratio of the first capacitance to the second capacitance is greater than or equal to 1 and less than or equal to 5, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

5 12. The inductive power transfer transmitter according to Claim 11, wherein:

the ratio of the first capacitance to the second capacitance is greater than 1.2 and less than 3.7,

10 the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

13. The inductive power transfer transmitter according to Claim 12, wherein:

15 the ratio of the first capacitance to the second capacitance is greater than or equal to 1.467 and less than or equal to 1.667, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.3618 and
20 less than or equal to 0.3818.

14. The inductive power transfer transmitter according to Claim 13, wherein the ratio of the first capacitance to the second capacitance is 1.567, and the controller is arranged
25 to switch the switching element with a duty cycle of 0.3718.

15. The inductive power transfer transmitter according to Claim 6, wherein:

30 the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency,

the ratio of the first capacitance to the second capacitance is greater than or equal to 20, and

the controller is arranged to switch the switching element with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

5 16. An inductive power transfer system comprising:

an inductive power transfer transmitter according to Claims 6 - 15; and

an inductive power transfer receiver comprising a receiver coil spaced apart from the transmitter coil of the
10 inductive power transfer transmitter.

17. A method for inductive power transfer, comprising:

providing an inverter comprising a first inductor and a switching element in series between power supply terminals,
15 the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second
20 inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit,
25 wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to
30 the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to

the second capacitance is greater than or equal to 0.7 and less than or equal to 1; and

switching the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than
5 or equal to 0.40.

18. The method according to Claim 17, wherein:

the ratio of the first capacitance to the second capacitance is greater than or equal to 0.8 and less than or
10 equal to 1.0, and

the switching element is switched with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

19. The method according to Claim 18, wherein:

15 the ratio of the first capacitance to the second capacitance is greater than or equal to 0.767 and less than or equal to 0.967, and

the switching element is switched with a duty cycle greater than or equal to 0.365 and less than or equal to
20 0.385.

20. The method according to Claim 19, wherein the ratio of the first capacitance to the second capacitance is 0.867, and the switching element is switched with a duty cycle of 0.375.

25

21. A method for inductive power transfer, comprising:

providing an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a
30 first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second

inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor
5 between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the
10 resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to
15 the second capacitance is greater than 1 and less than 5; and
switching the switching element at the first frequency with a duty cycle greater than 0.35 and less than 0.40.

22. The method according to Claim 22, wherein:
20 the ratio of the first capacitance to the second capacitance is greater than 1.2 and less than 3.7, and
the switching element is switched with a duty cycle greater than 0.35 and less than 0.40.

25 23. The method according to Claim 23, wherein:
the ratio of the first capacitance to the second capacitance is greater than or equal to 1.467 and less than or equal to 1.667, and
the switching element is switched with a duty cycle
30 greater than or equal to 0.3618 and less than or equal to 0.3818.

24. The method according to Claim 24, wherein the ratio of the first capacitance to the second capacitance is 1.567, and the switching element is switched with a duty cycle of 0.3718.

5

25. A method for inductive power transfer, comprising:

providing an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 20;

switching the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

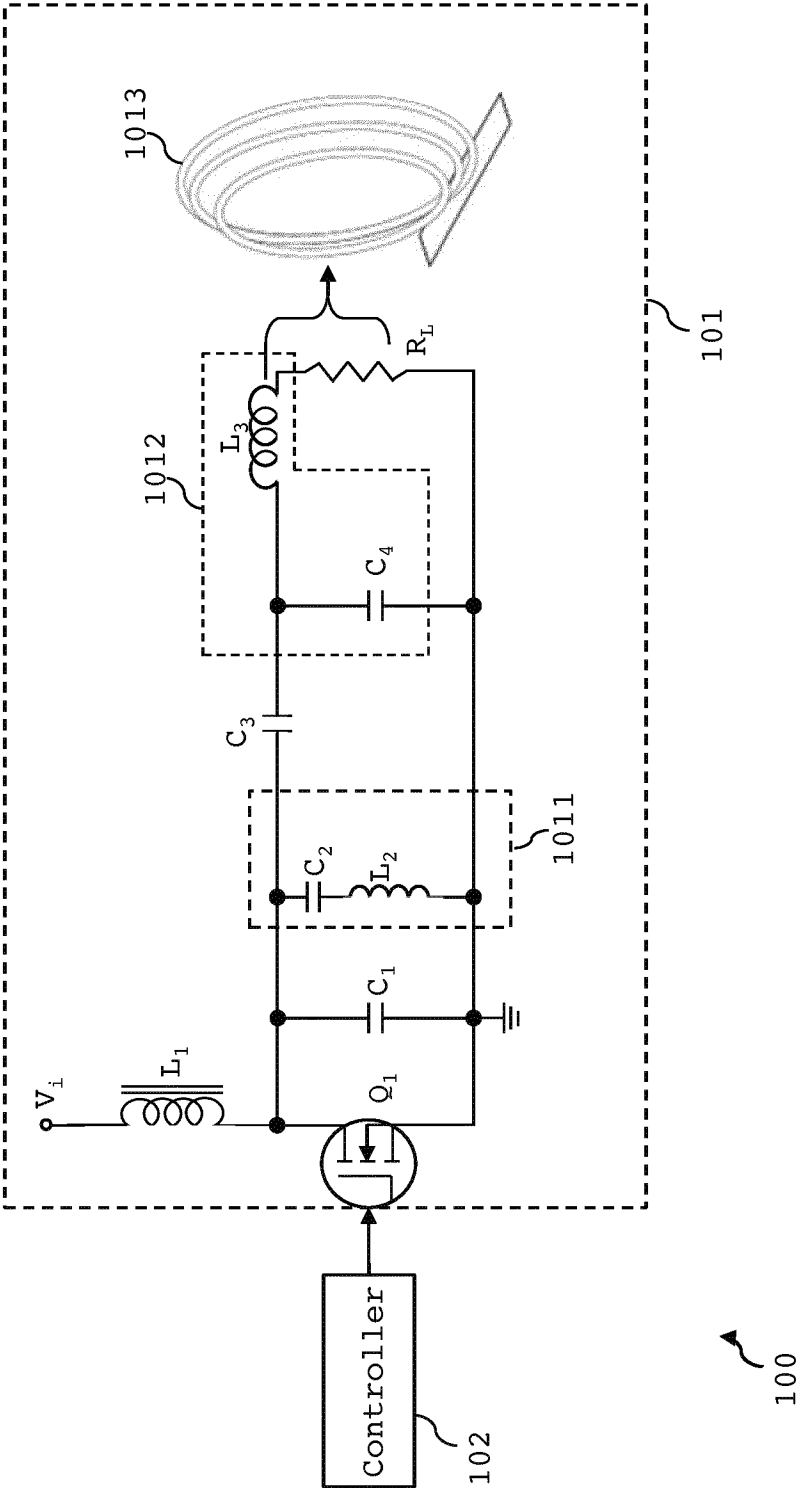


FIG. 1

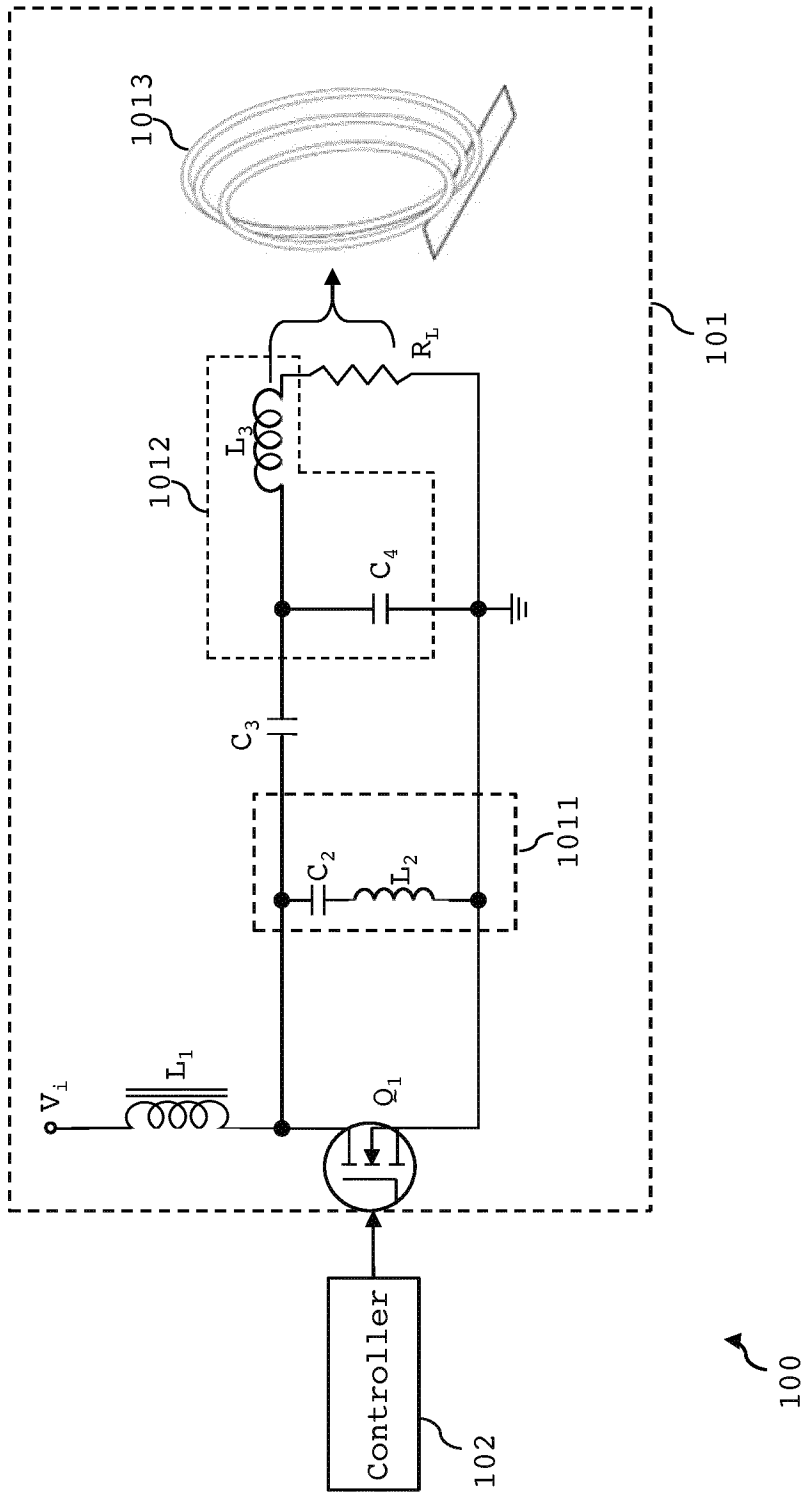


FIG. 2

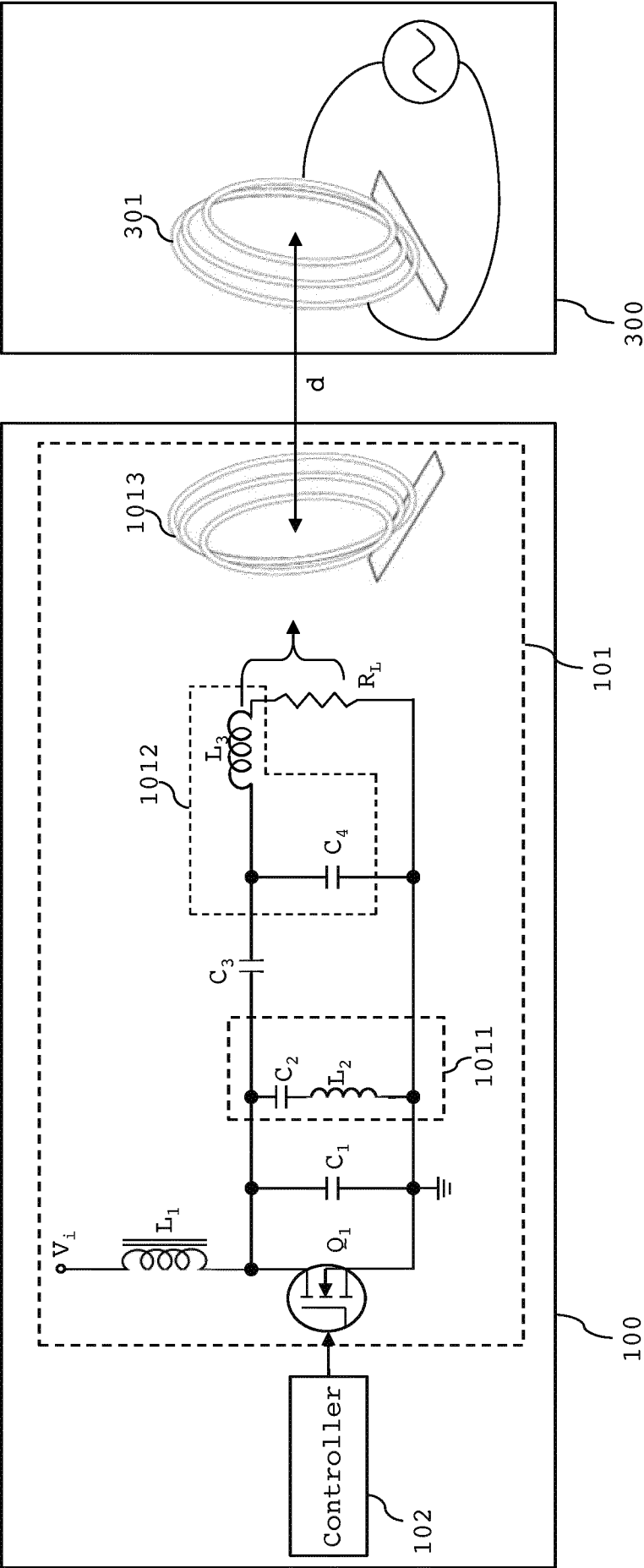


FIG. 3

Provide an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first inductor and a second capacitance, wherein the circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 0.7 and less than or equal to 1.

S401

Switch the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

S402

FIG. 4

Provide an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than 1 and less than 5.

S501

Switching the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

S502

FIG. 5

Provide an inverter comprising a first inductor and a switching element in series between power supply terminals, the switching element being operable to be switched at a first frequency; a first capacitance in parallel with the switching element between the first inductor and a power supply terminal; a first tank circuit in parallel with the first capacitance, the first tank circuit comprising a second inductor and a second capacitance, wherein the second capacitance is arranged in series with the second inductor; a second tank circuit in parallel with the first capacitance; and a third capacitance in series with the first inductor between the first tank circuit and the second tank circuit, wherein the second tank circuit comprises a transmitter coil and a fourth capacitance, the fourth capacitance being arranged in parallel or series with the transmitter coil; wherein the fourth capacitance is selected such that the resonant frequency of the second tank circuit is not equal to the first frequency; and wherein the second inductor and the second capacitance are selected such that the resonant frequency of the first tank circuit is double the first frequency; and wherein the ratio of the first capacitance to the second capacitance is greater than or equal to 20.

S601

Switch the switching element at the first frequency with a duty cycle greater than or equal to 0.35 and less than or equal to 0.40.

S602

FIG. 6

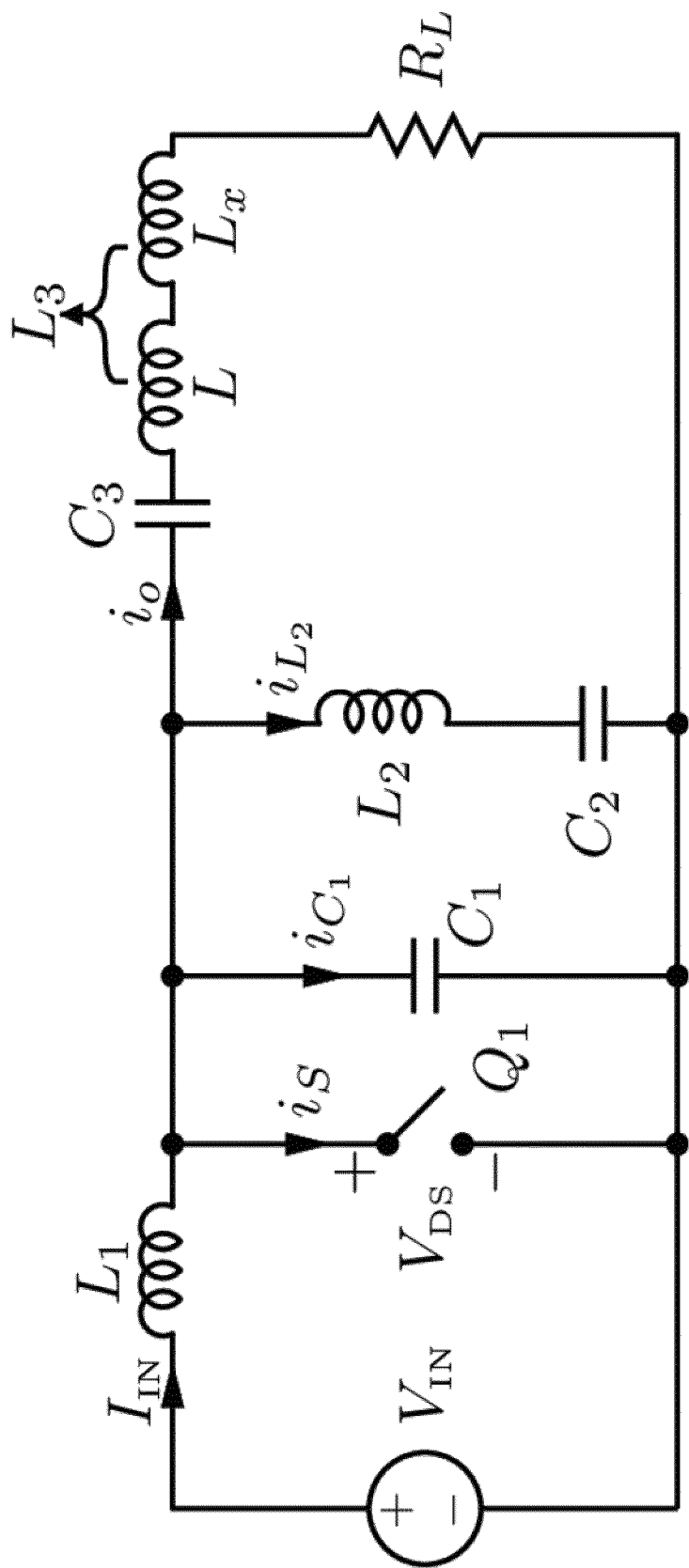


FIG. 7

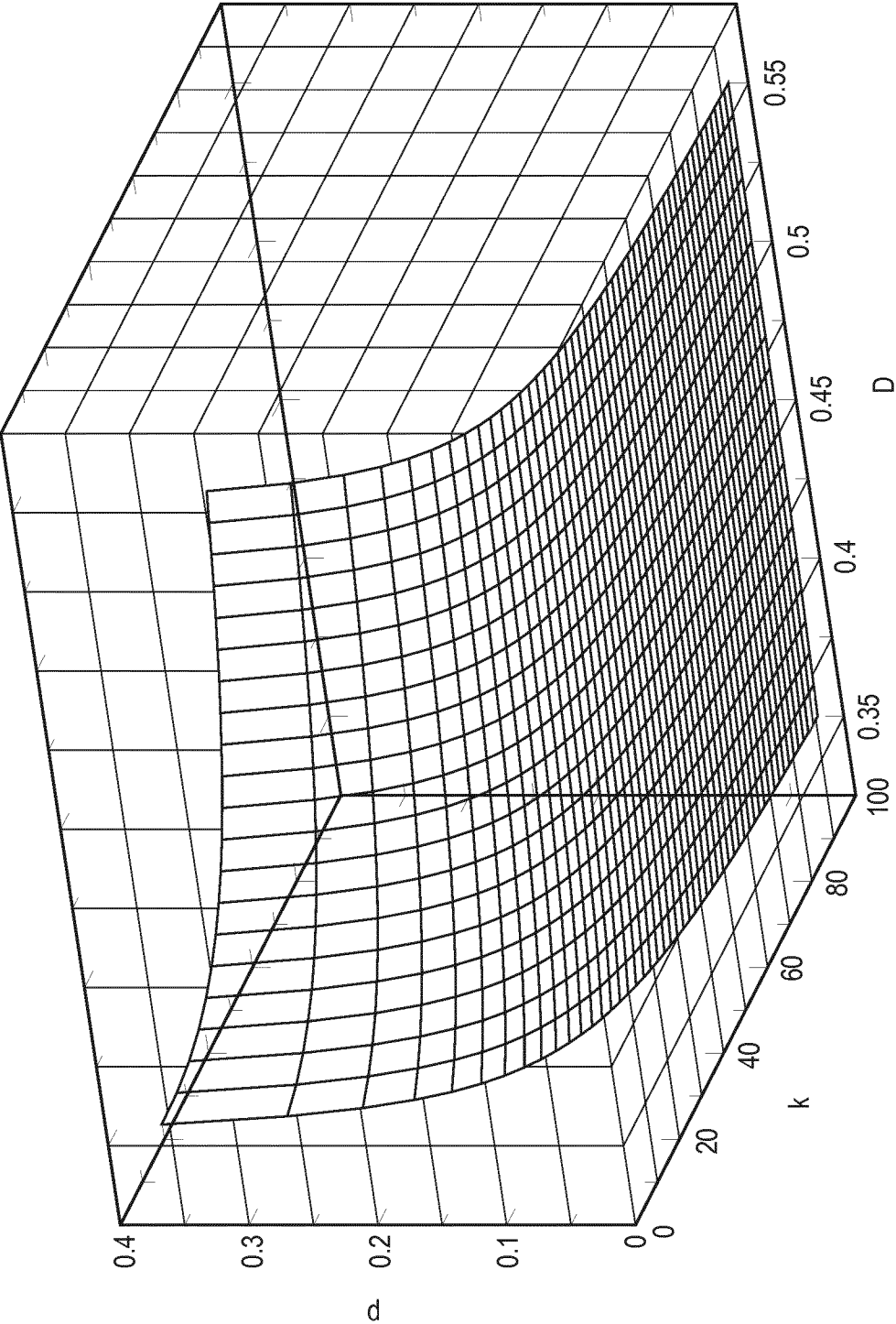


FIG. 8a

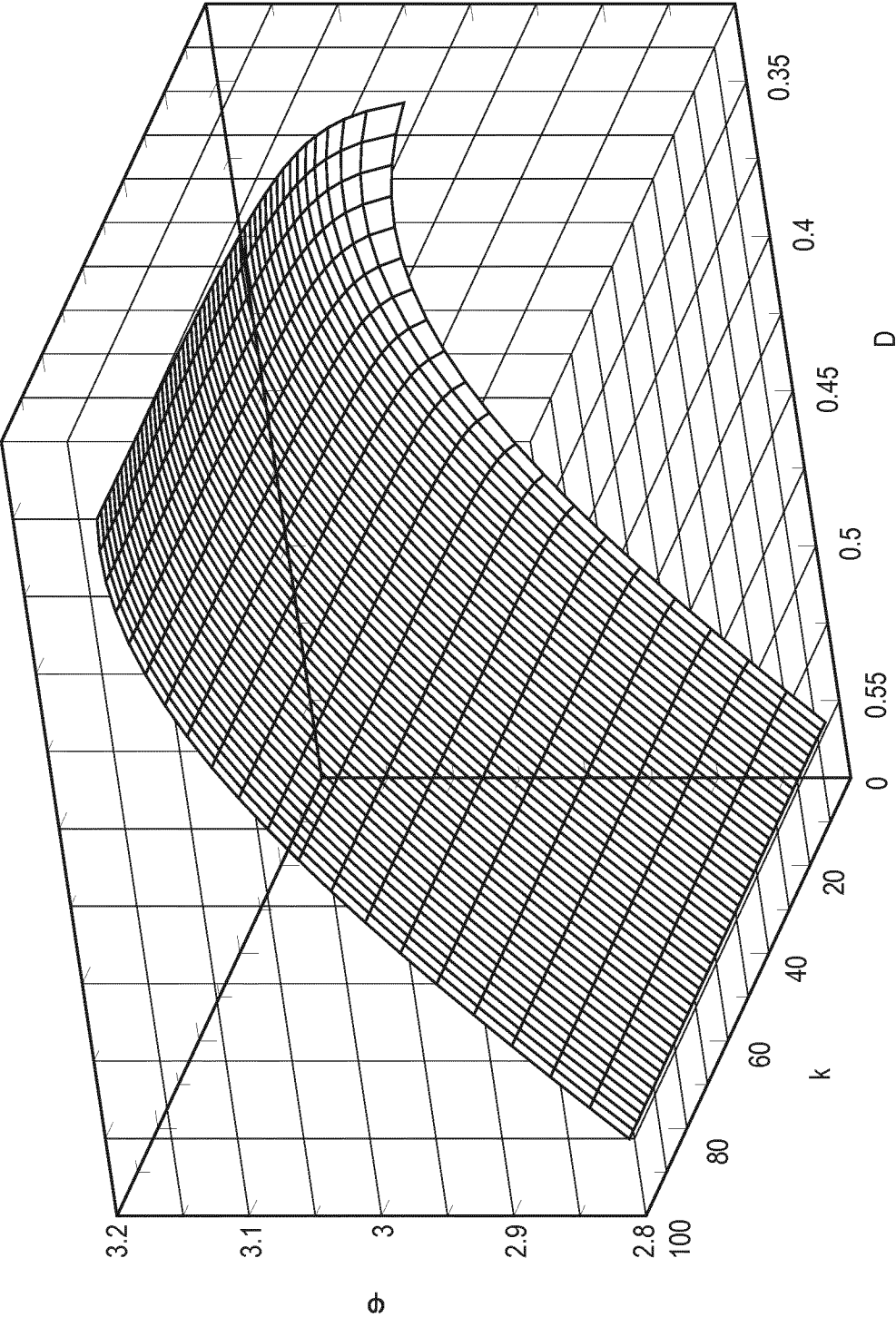


FIG. 8b

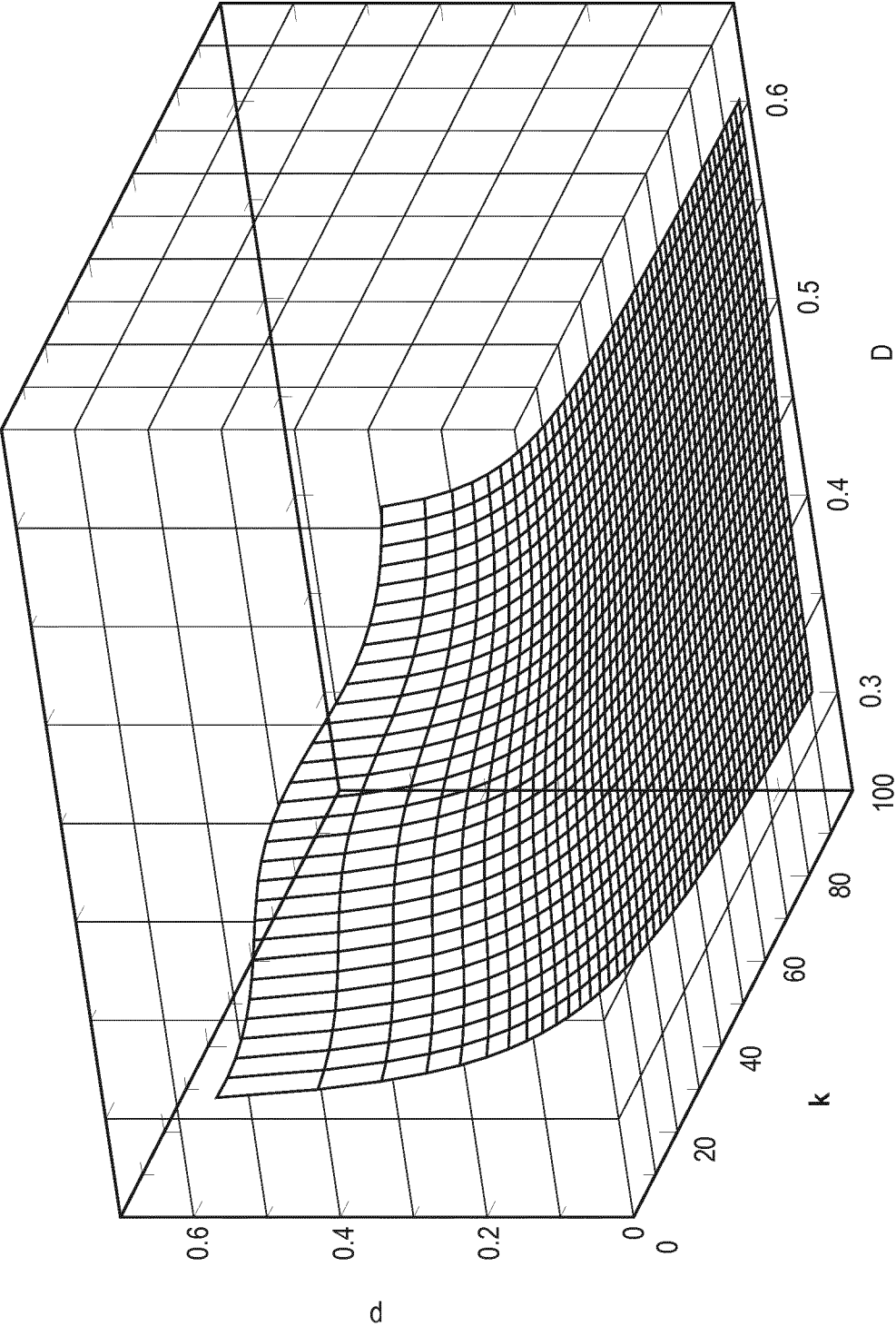


FIG. 9a

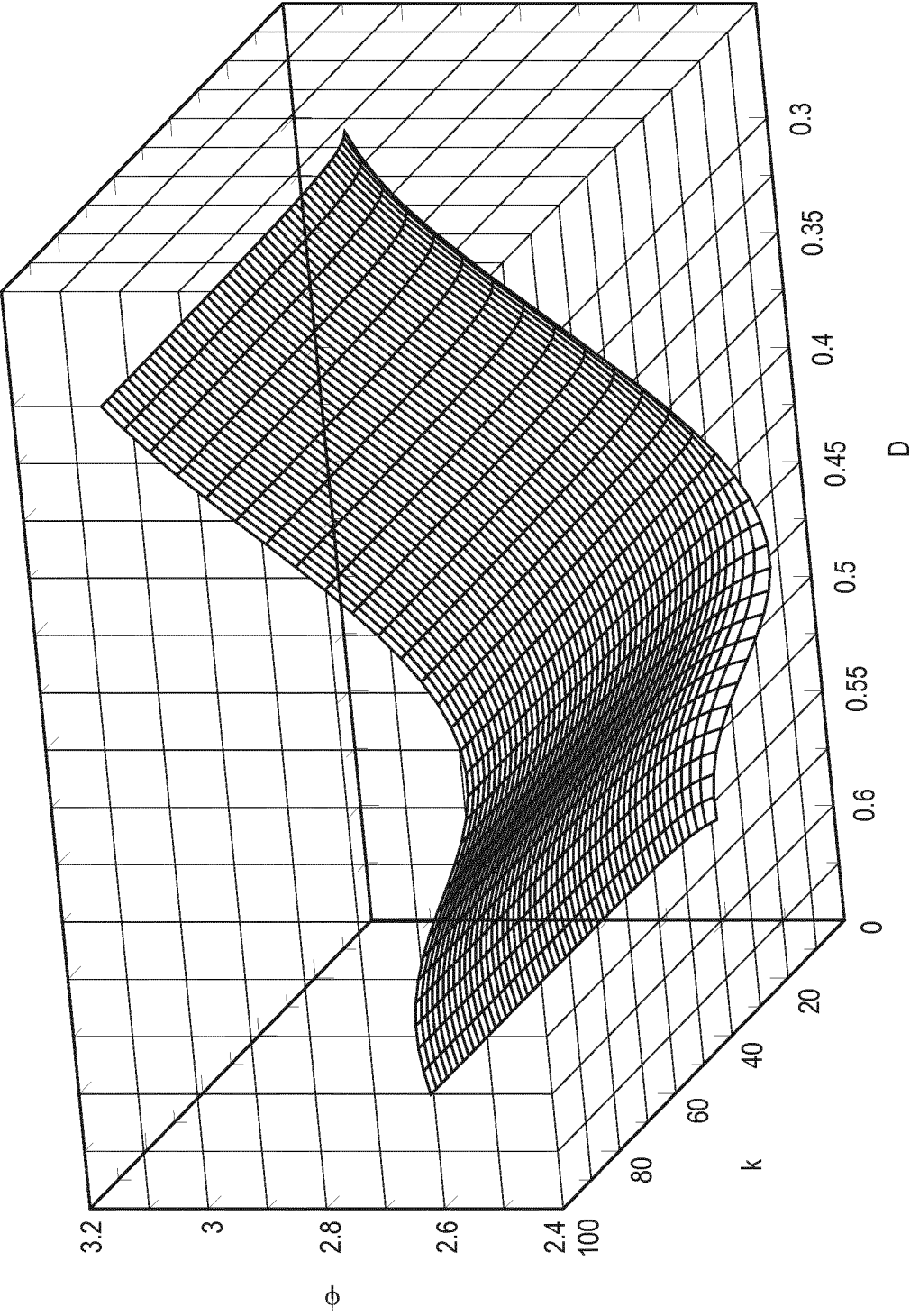


FIG. 9b

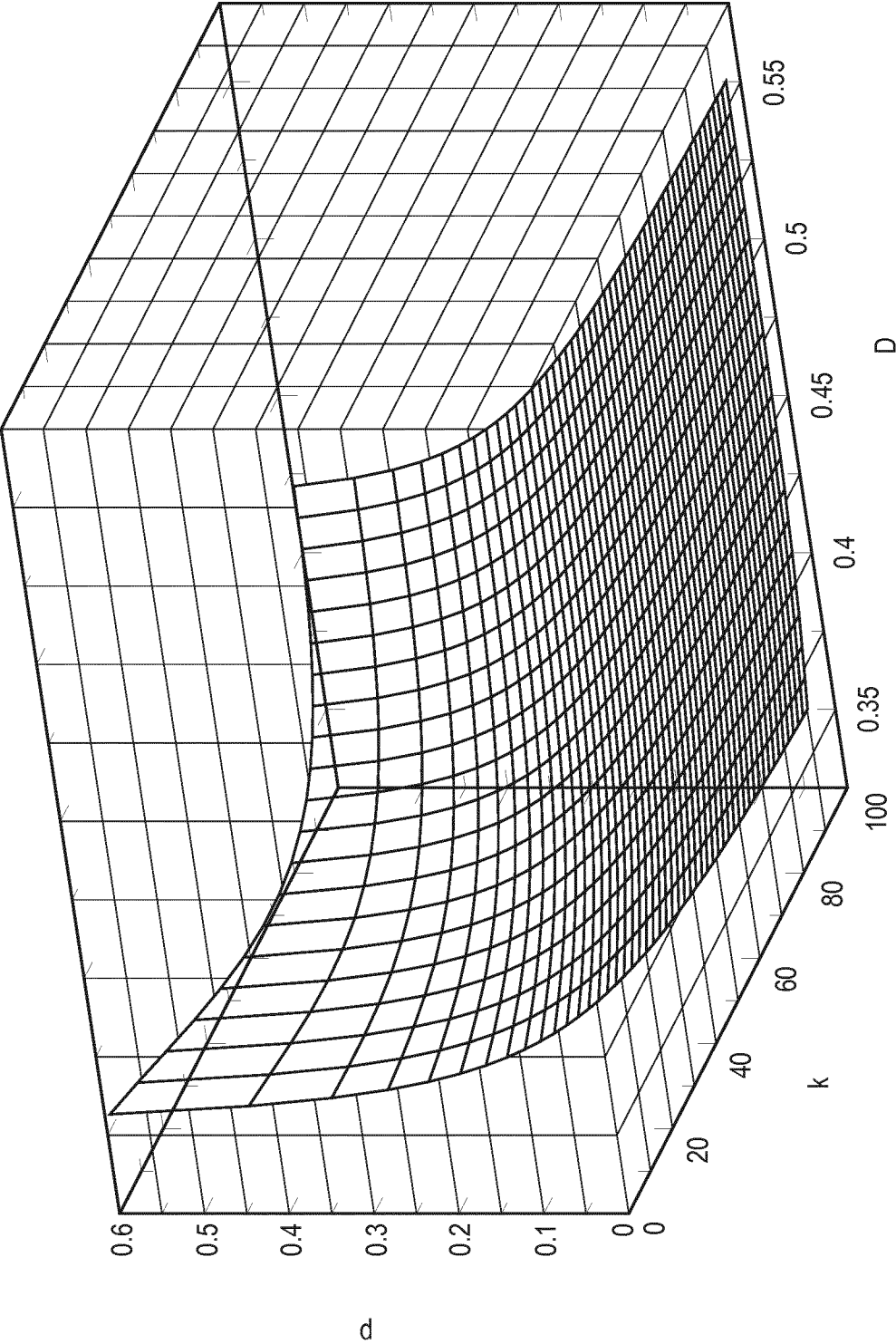


FIG. 10a

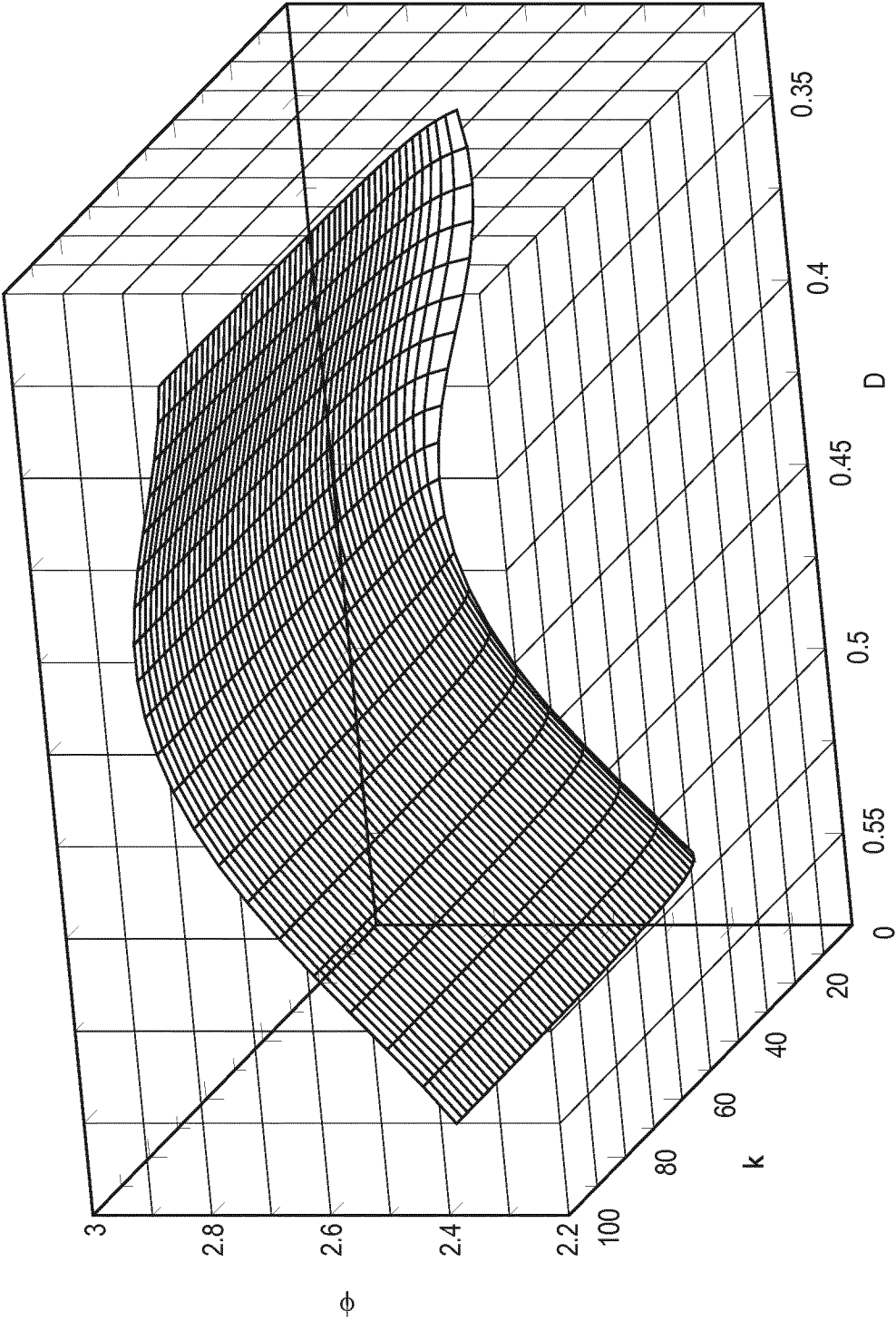


FIG. 10b

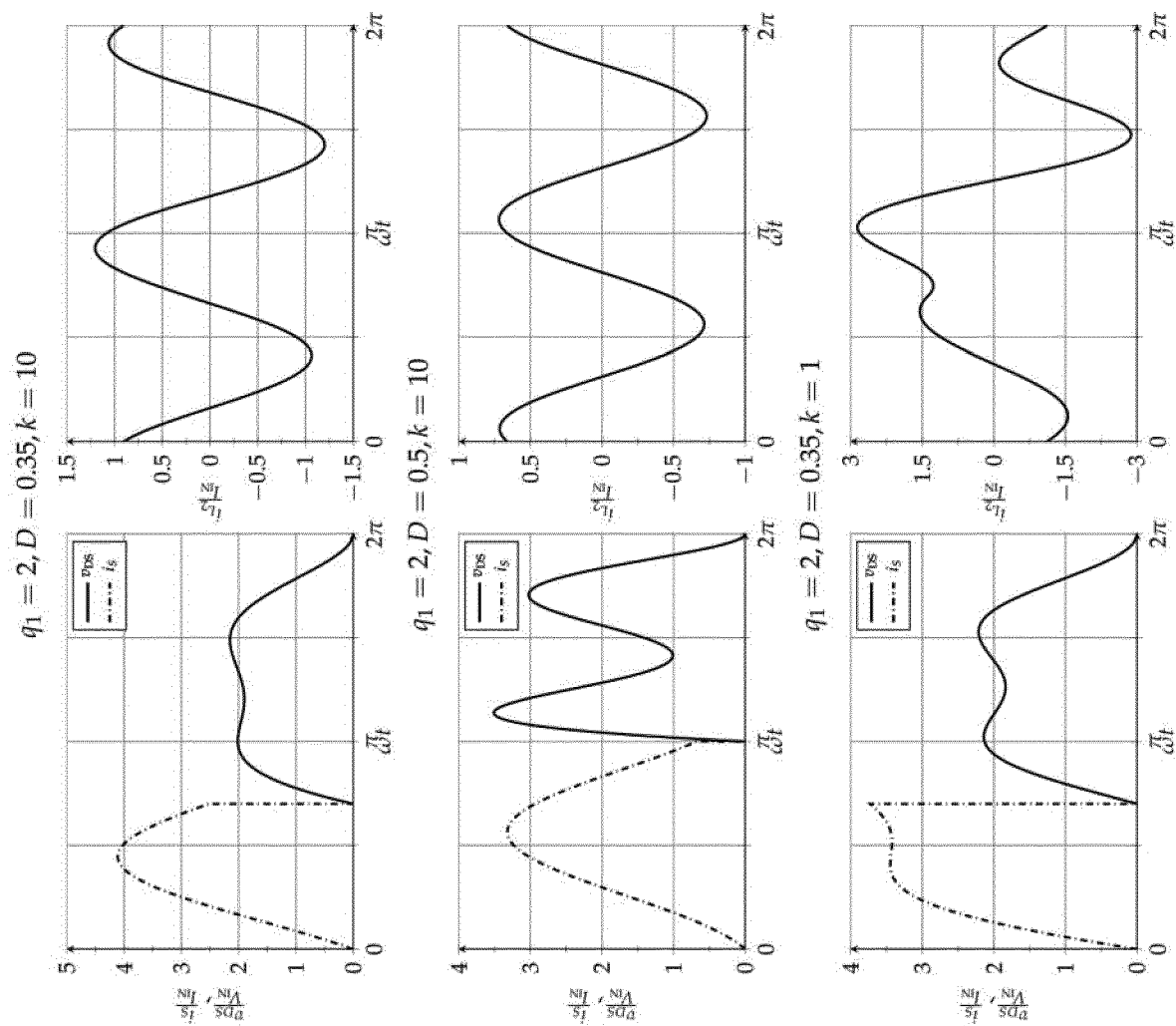


FIG. 11

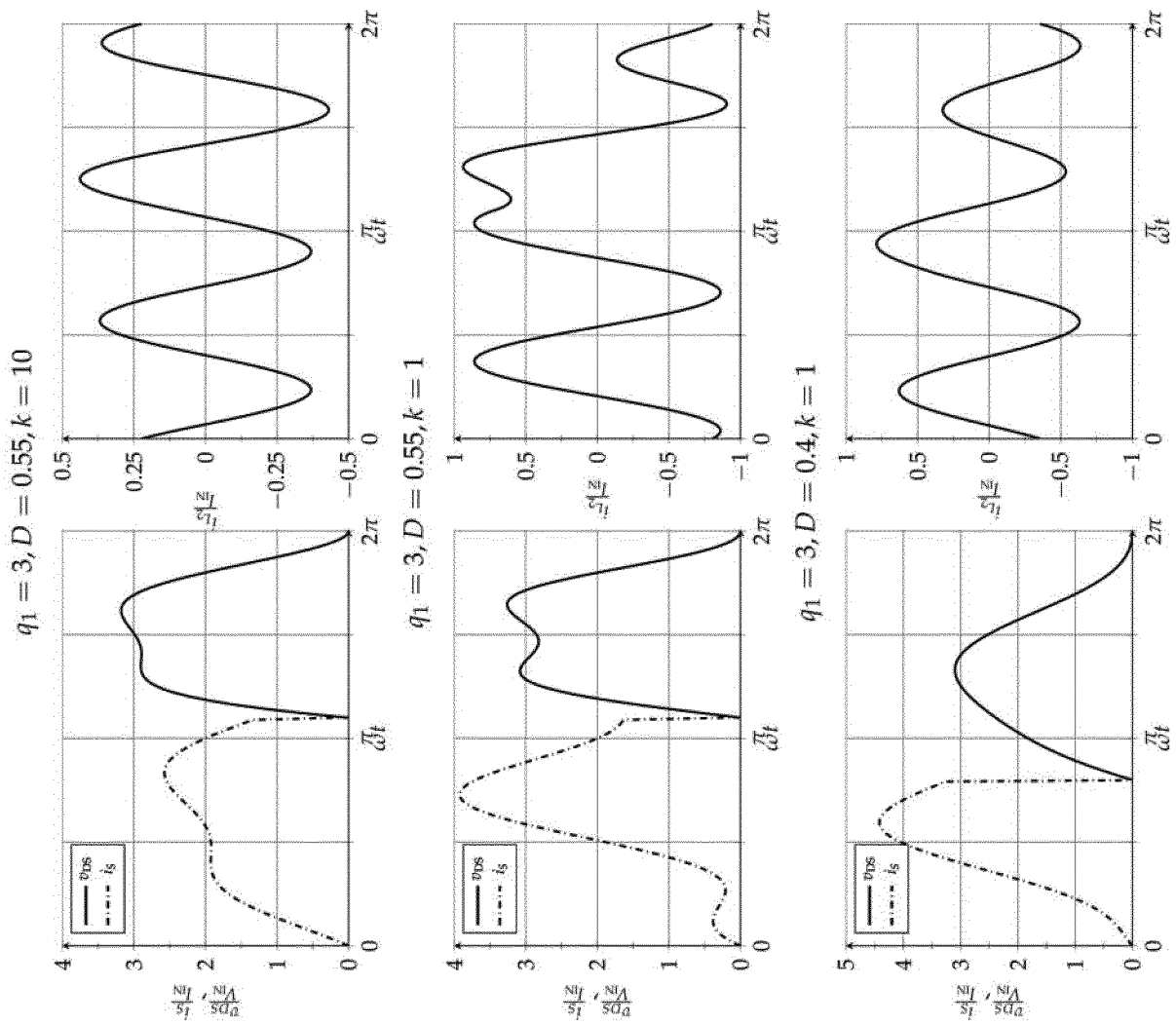


FIG. 12

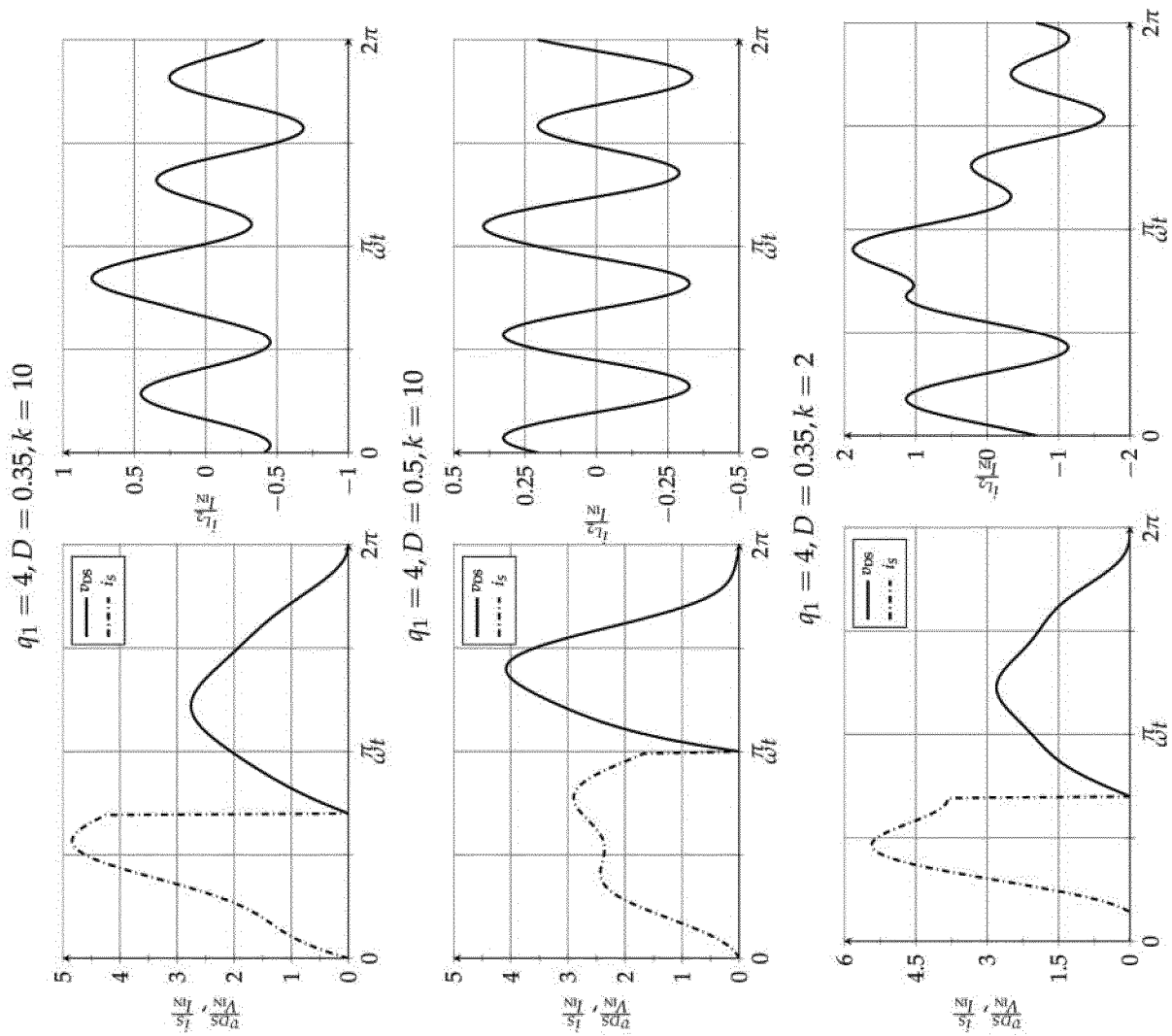


FIG. 13

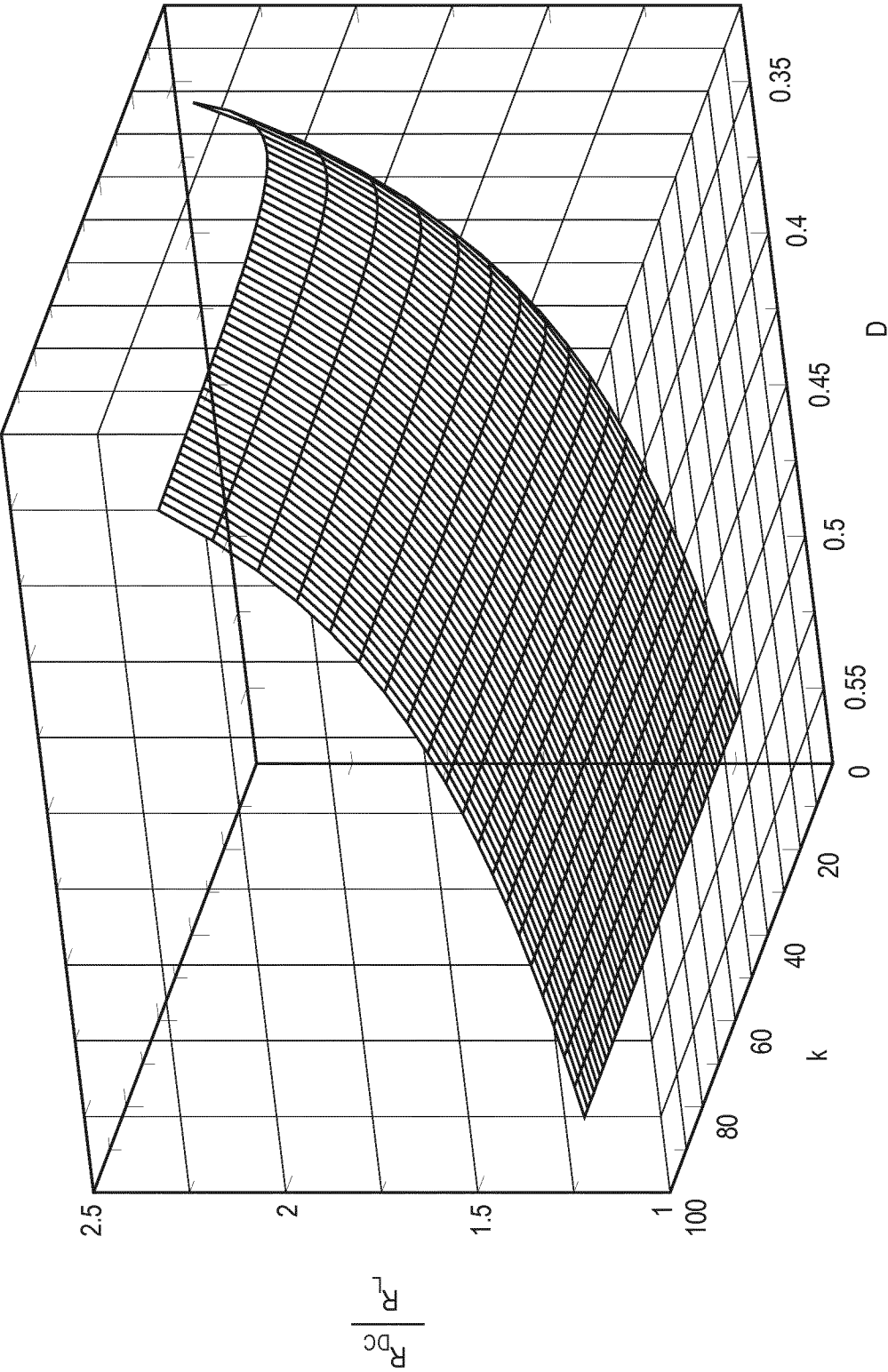


FIG. 14a

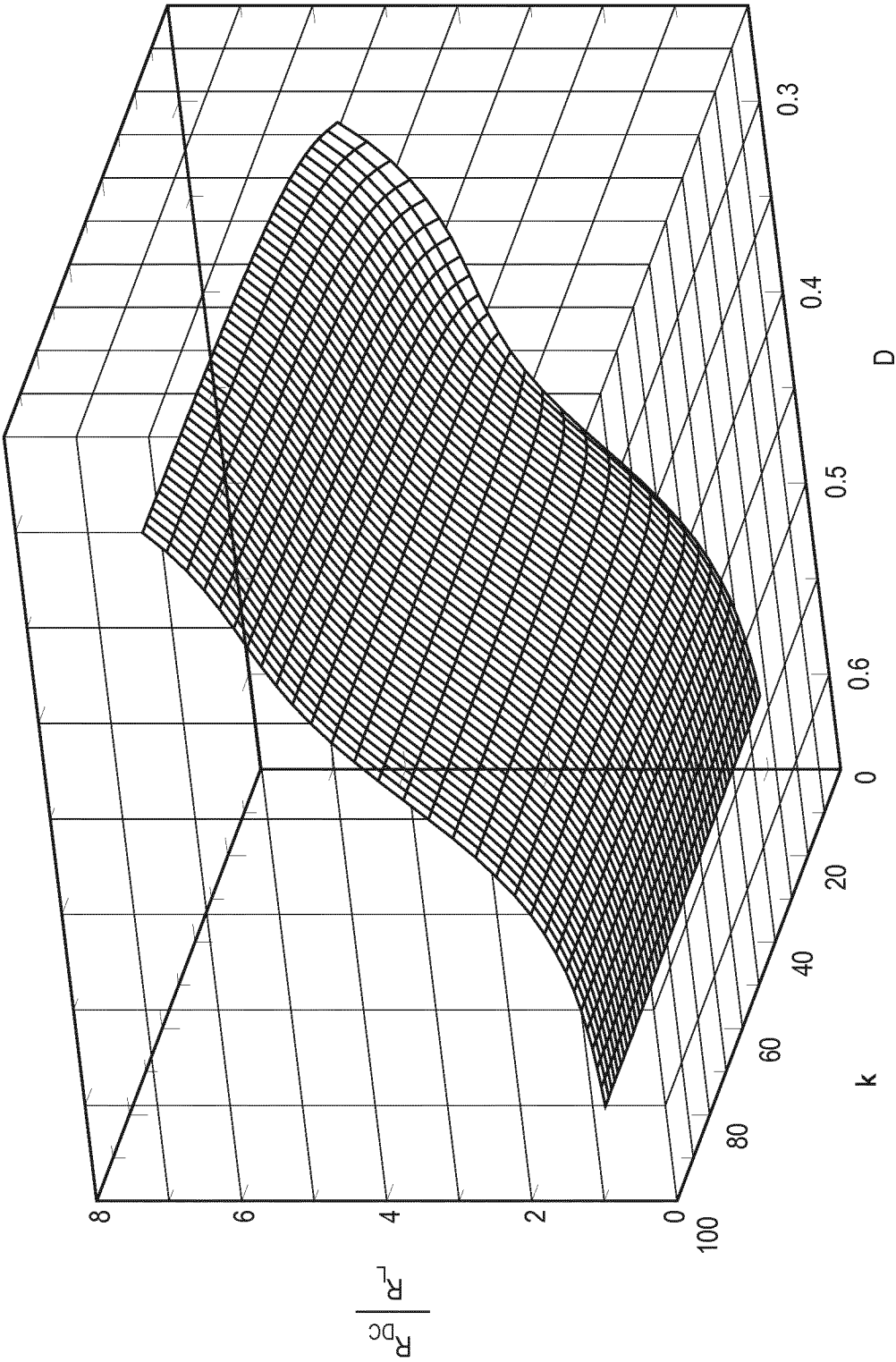


FIG. 14b

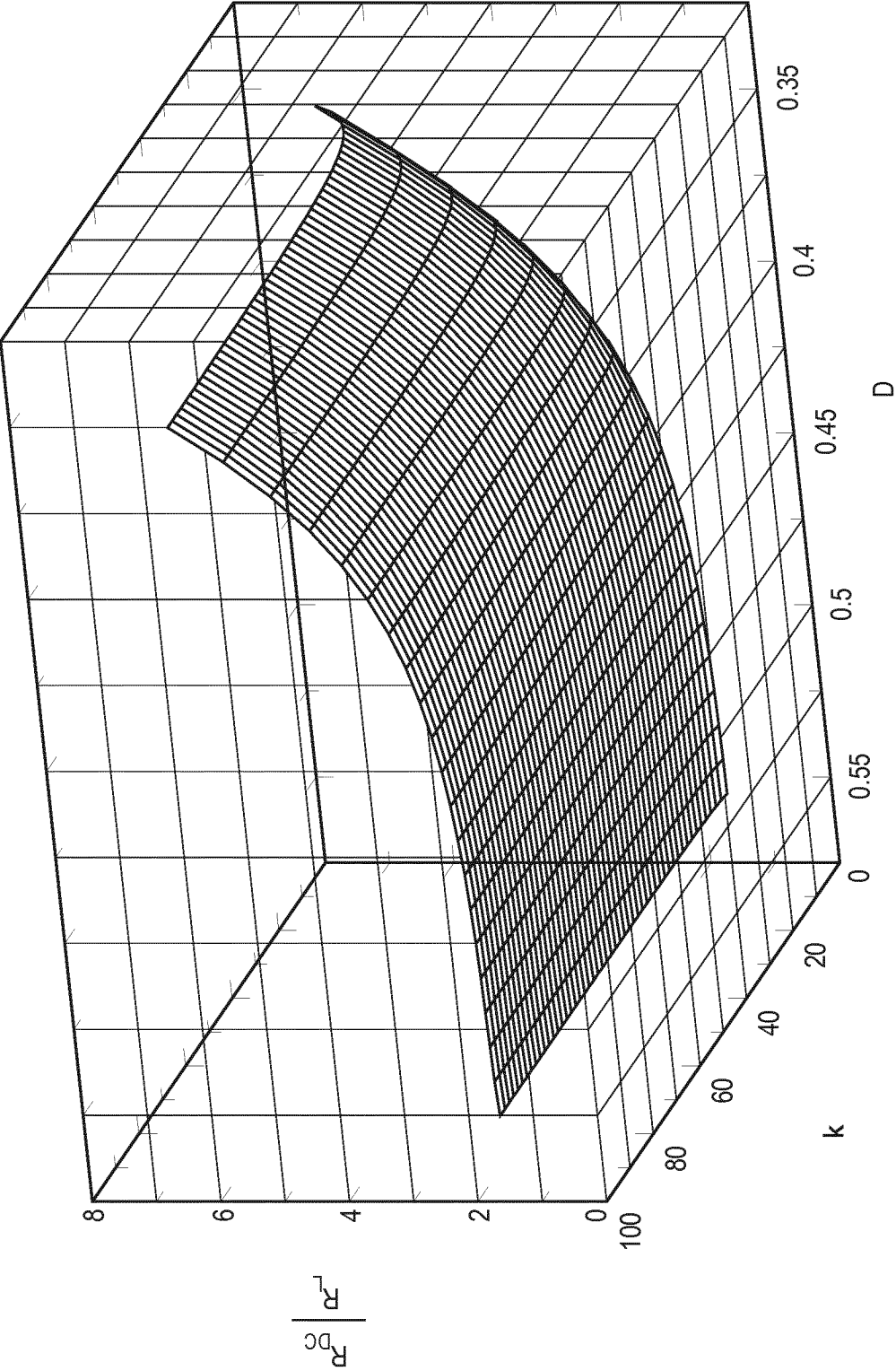


FIG. 14c

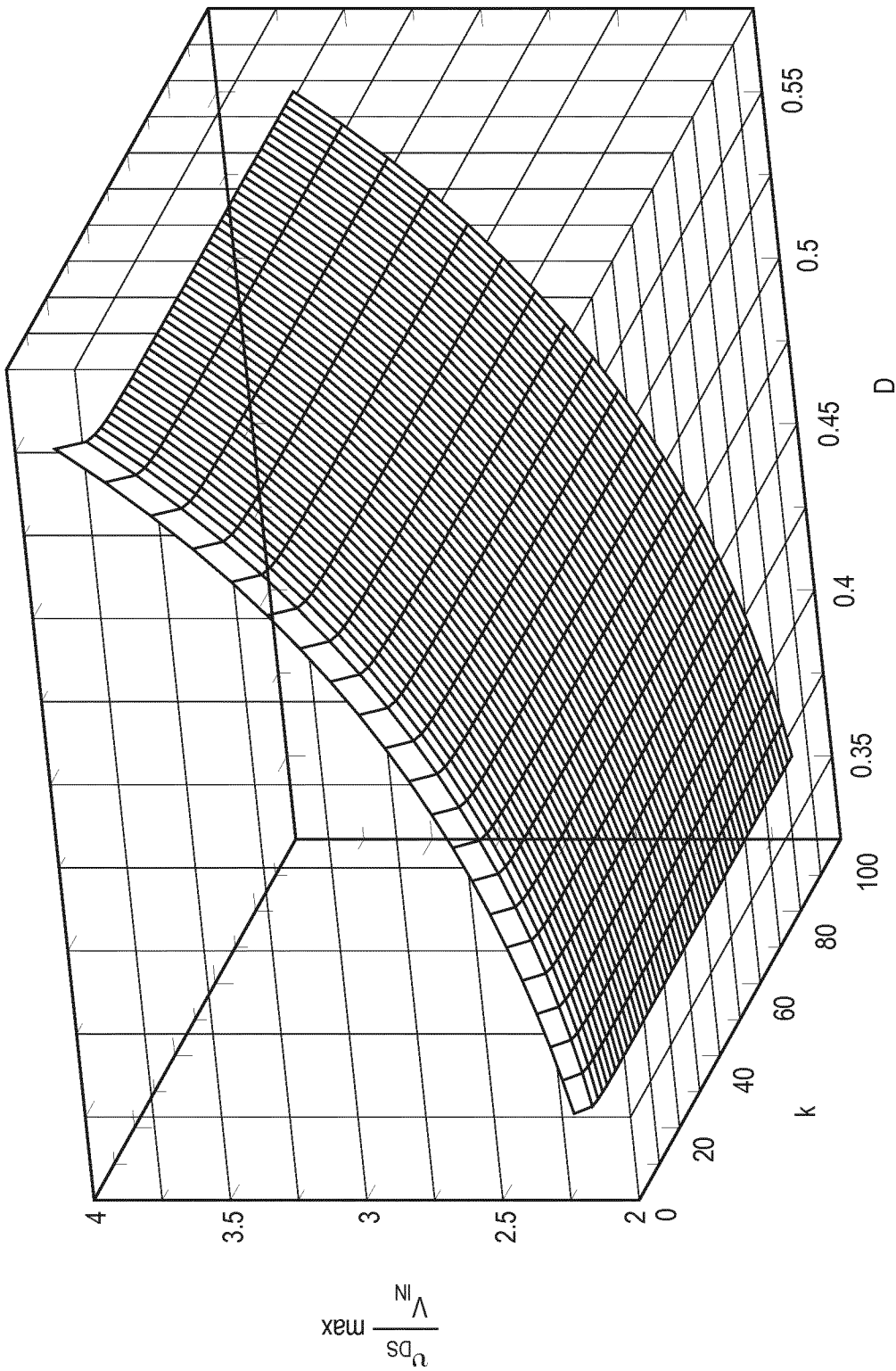


FIG. 15a

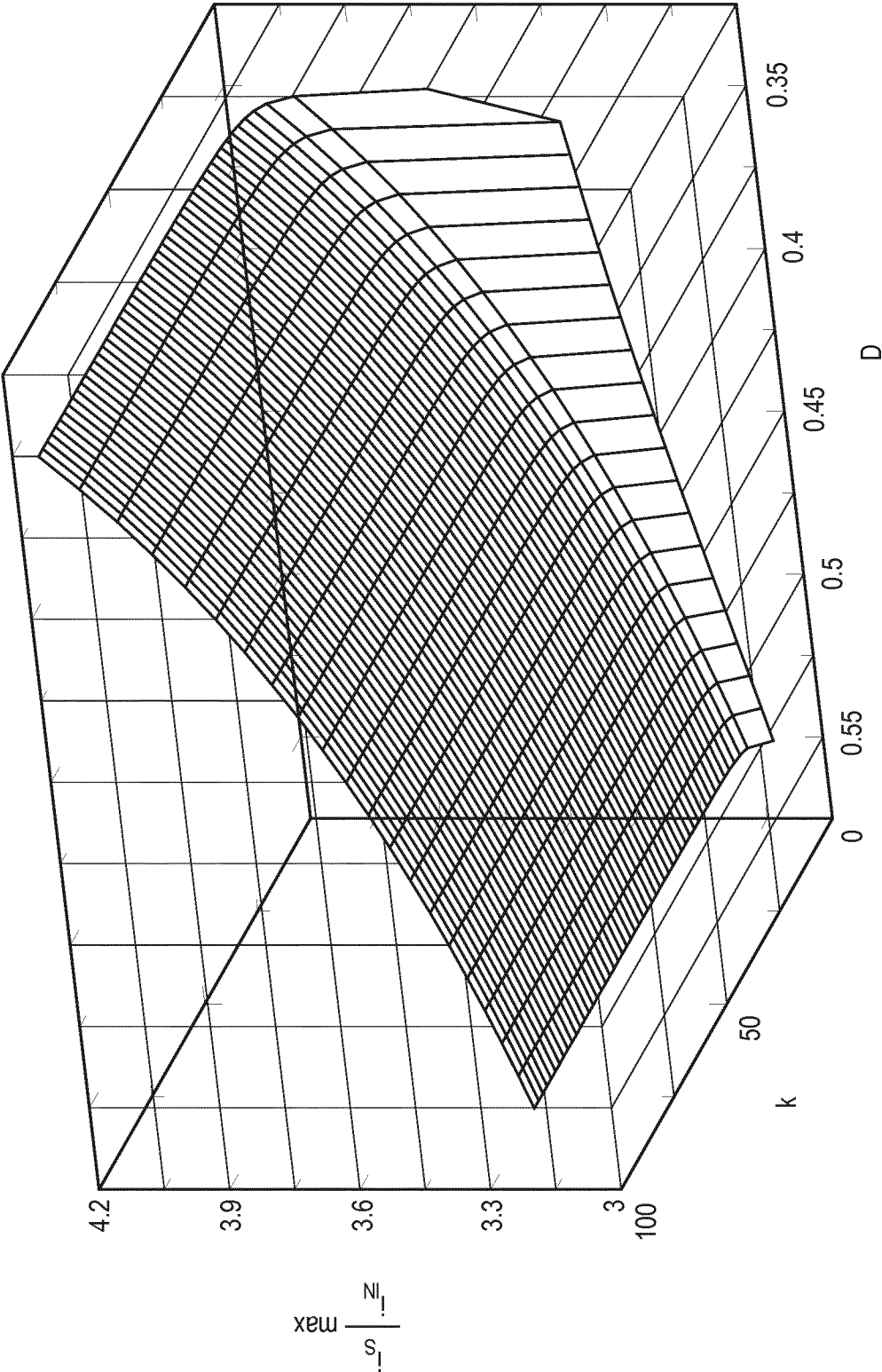


FIG. 15b

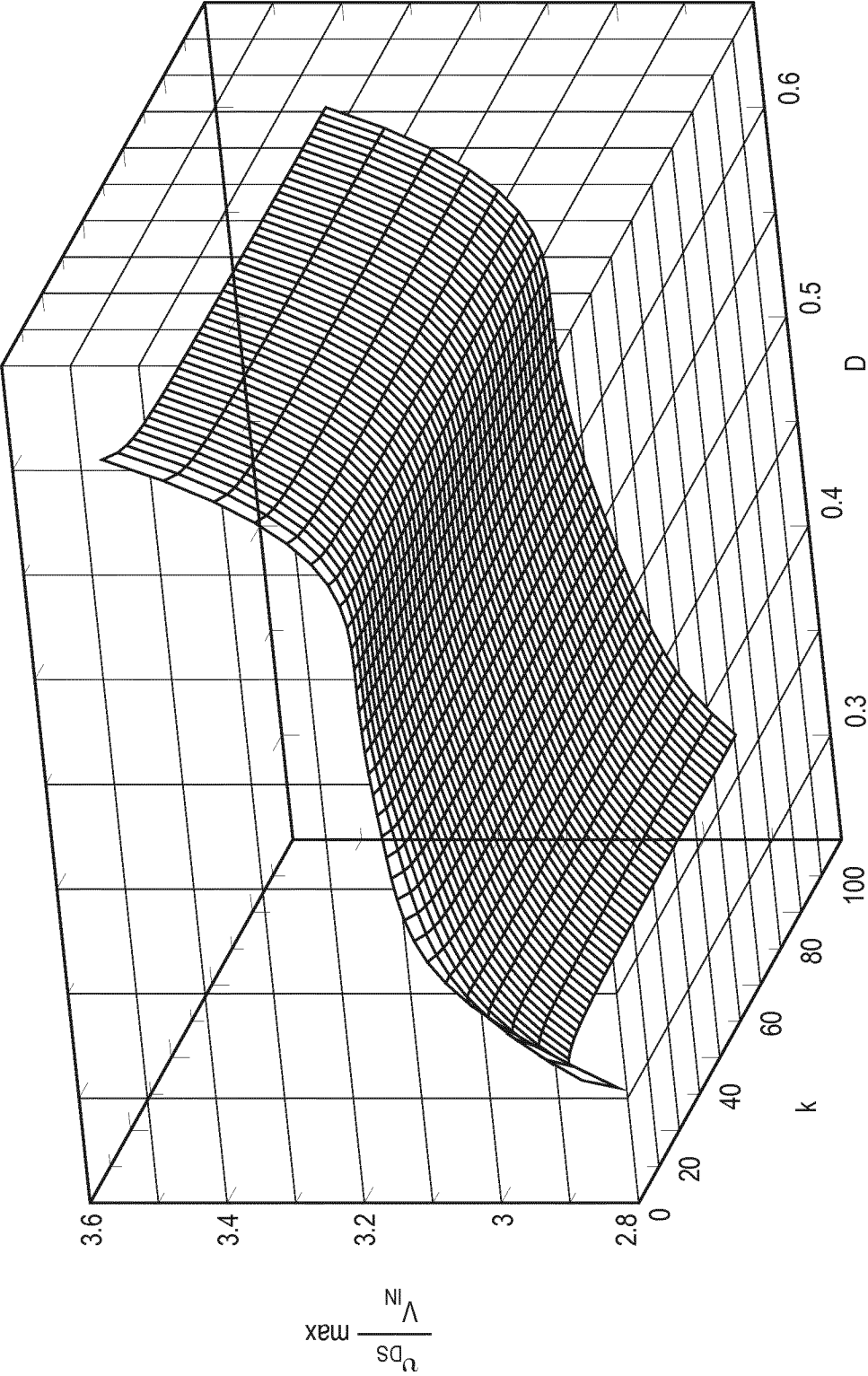


FIG. 16a

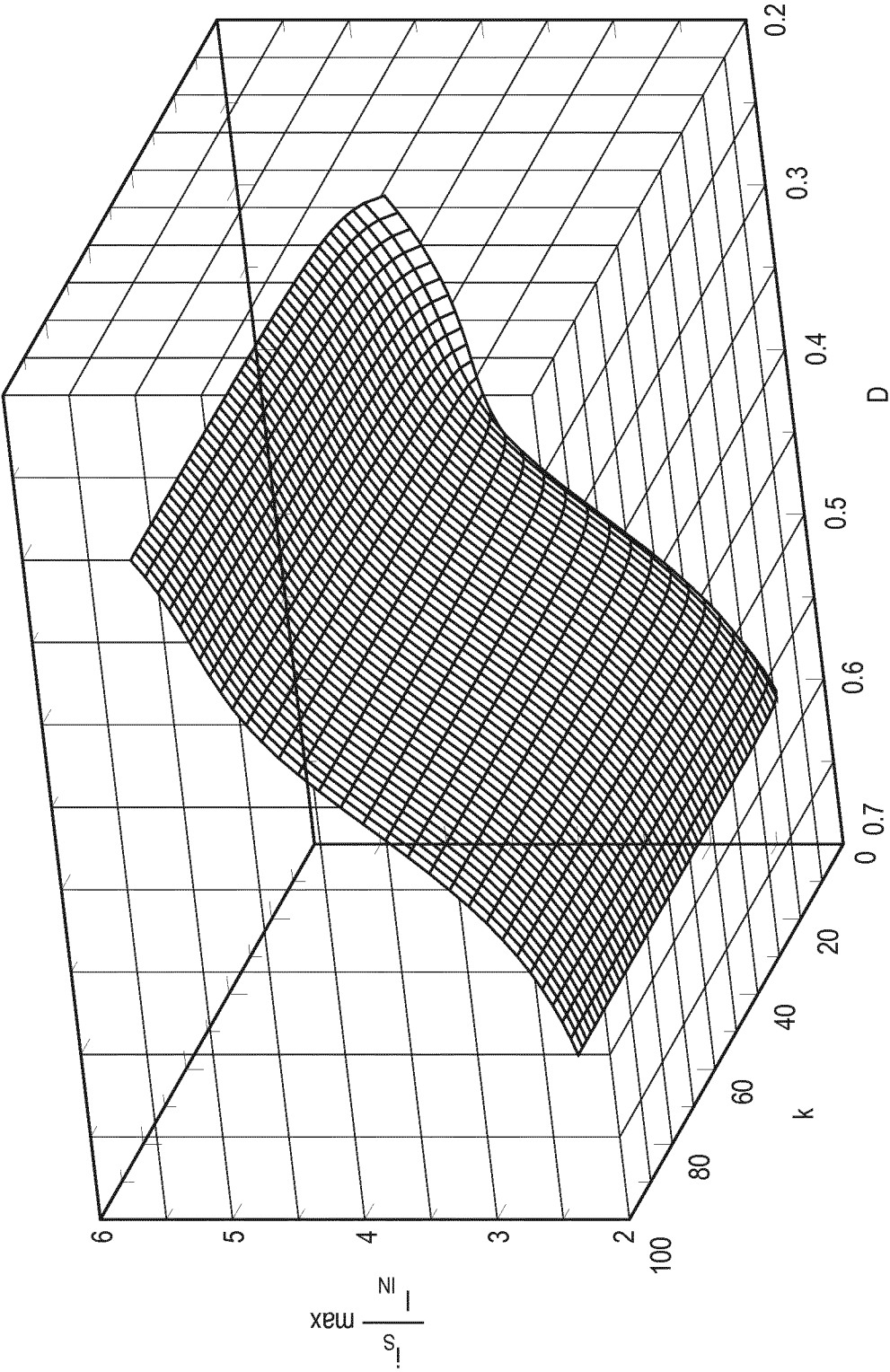


FIG. 16b

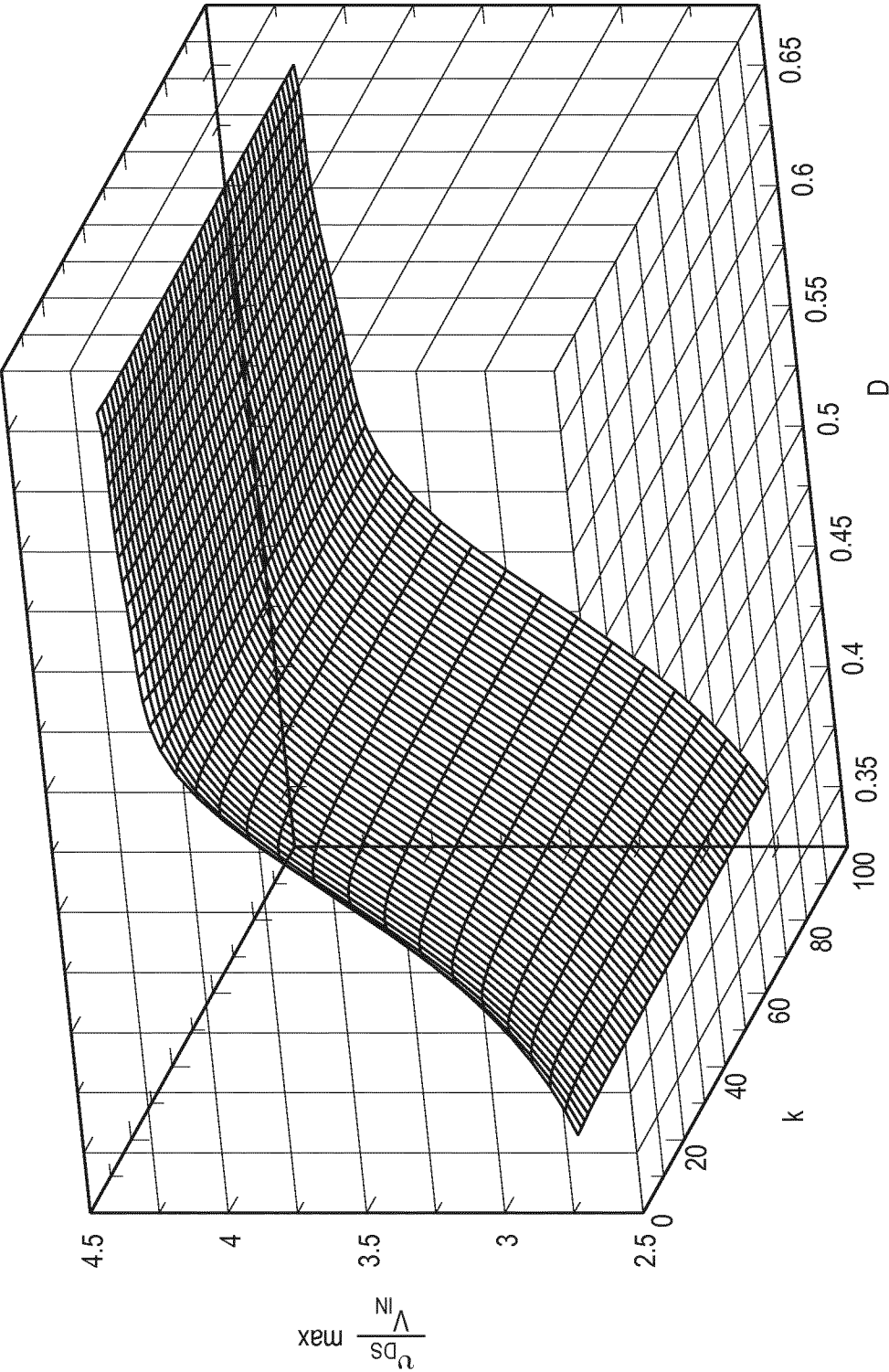


FIG. 17a

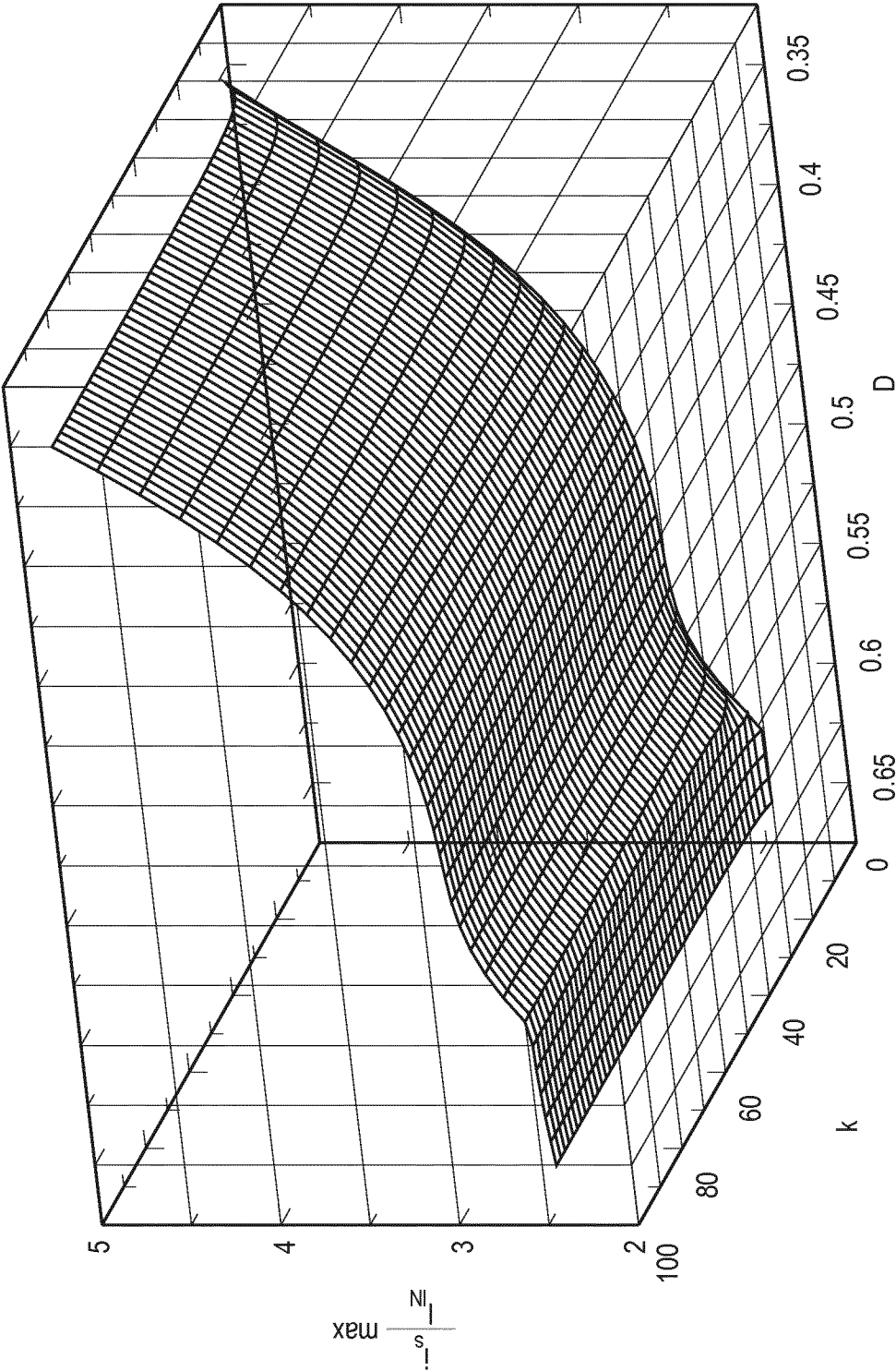


FIG. 17b

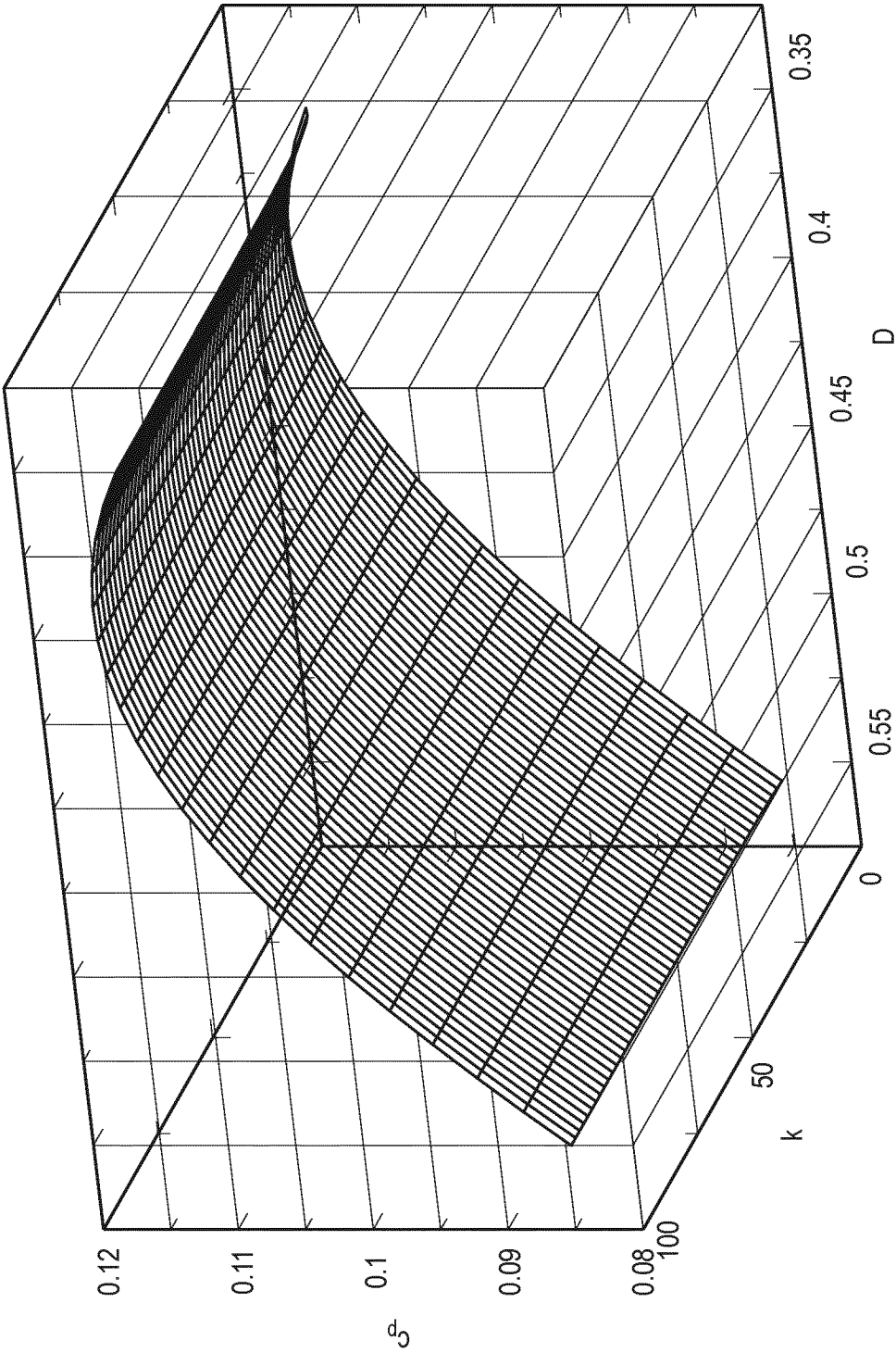


FIG. 18a

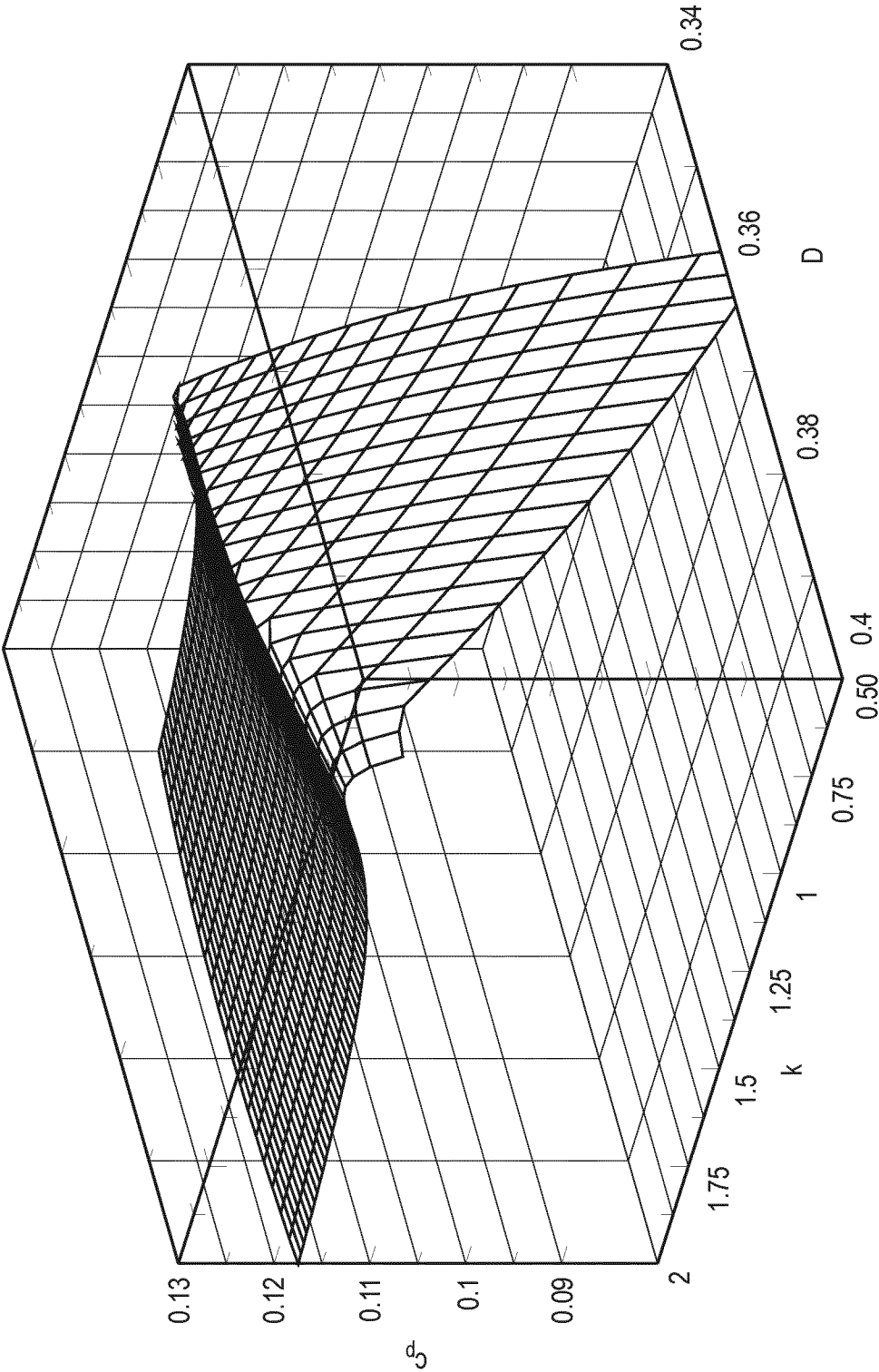


FIG. 18b

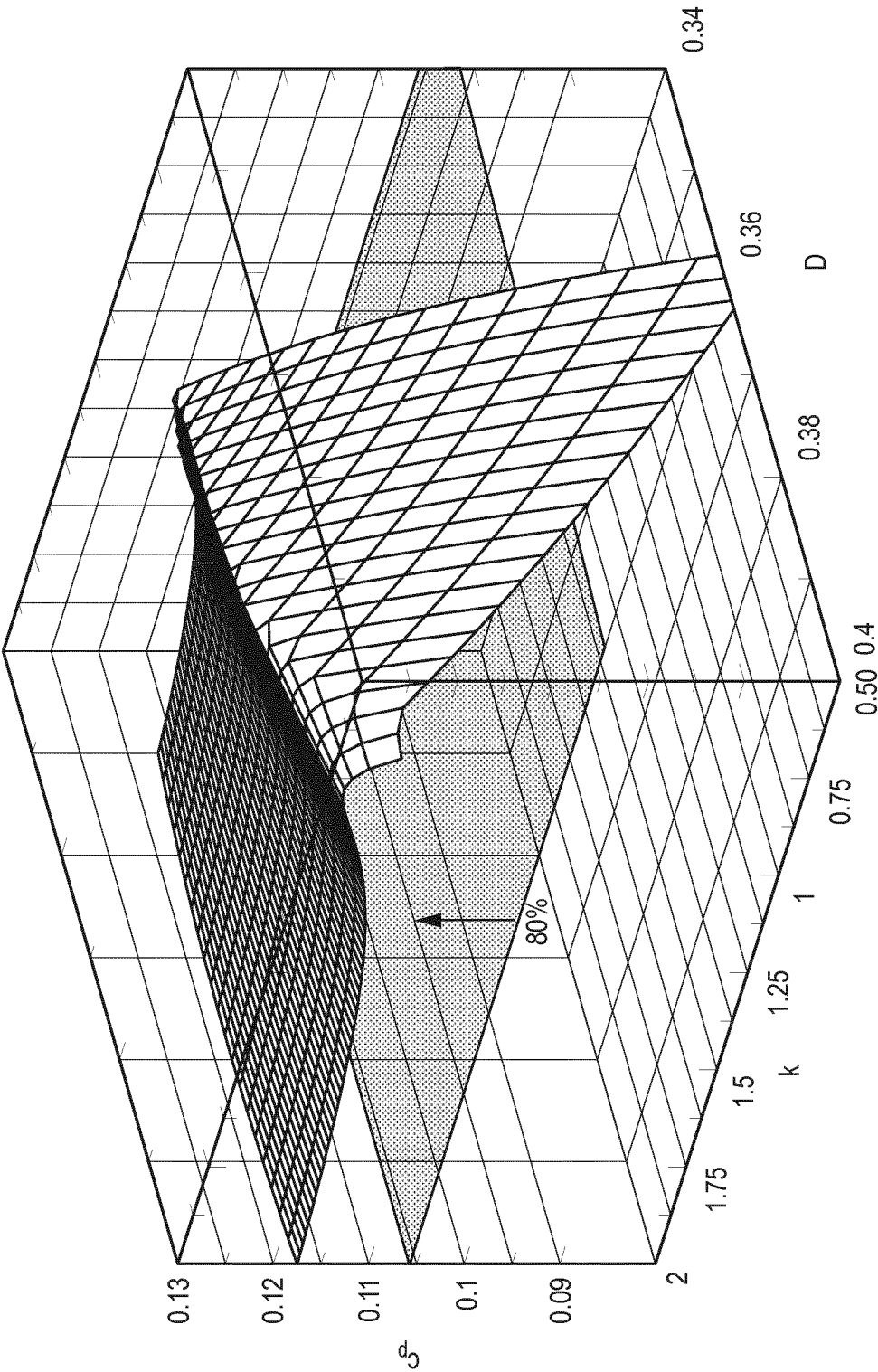


FIG. 18c

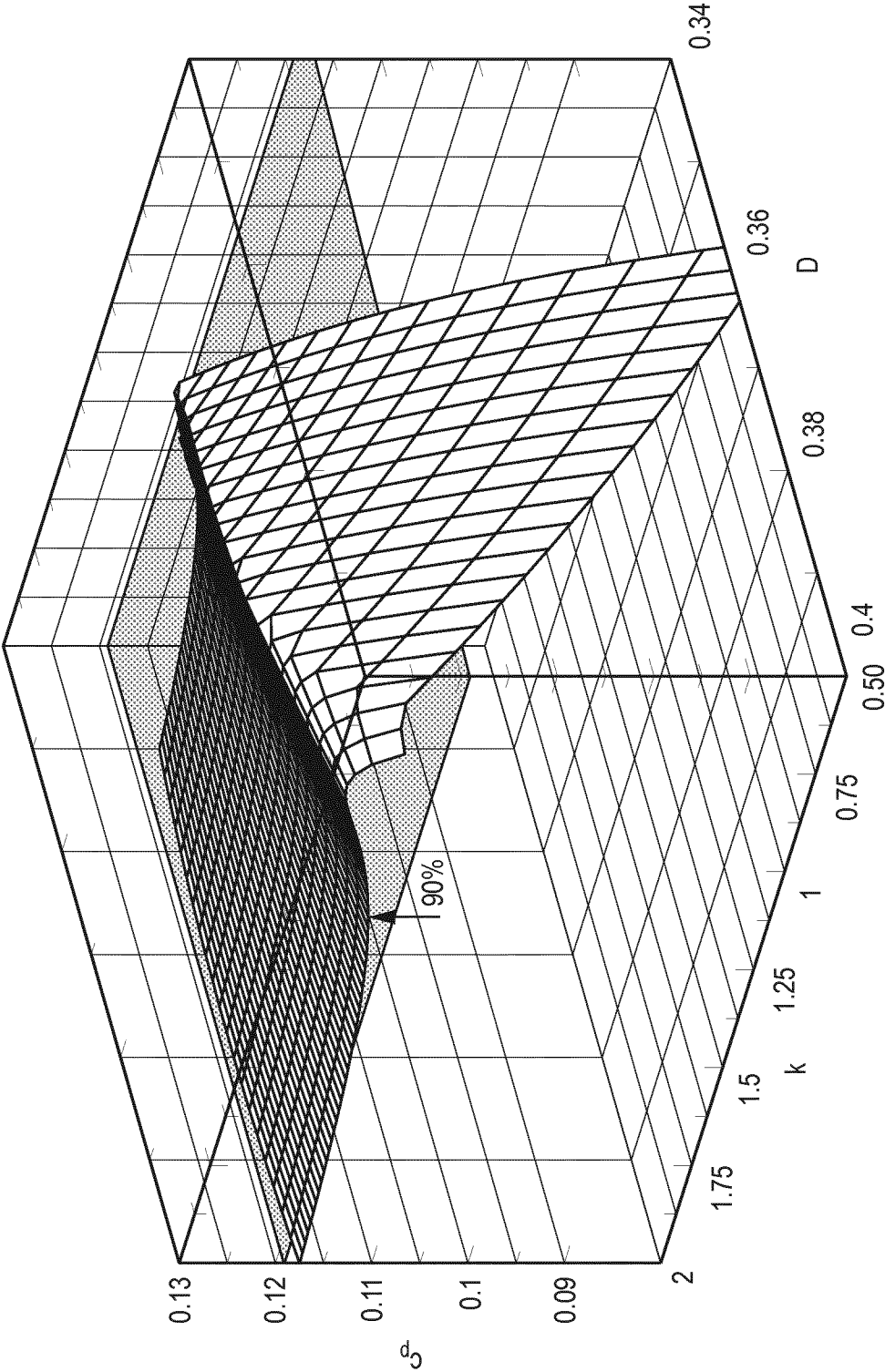


FIG. 18d

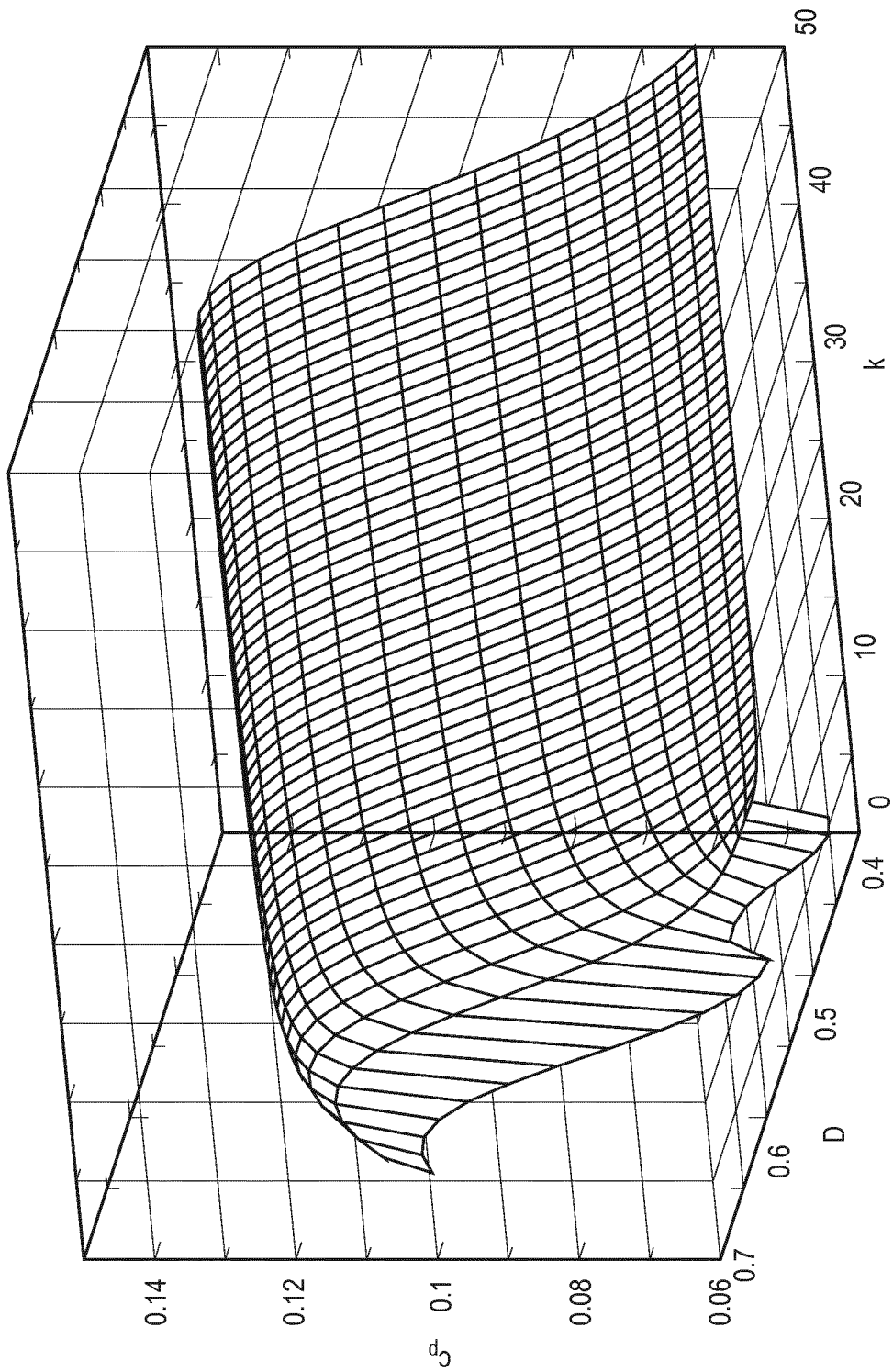


FIG. 19a

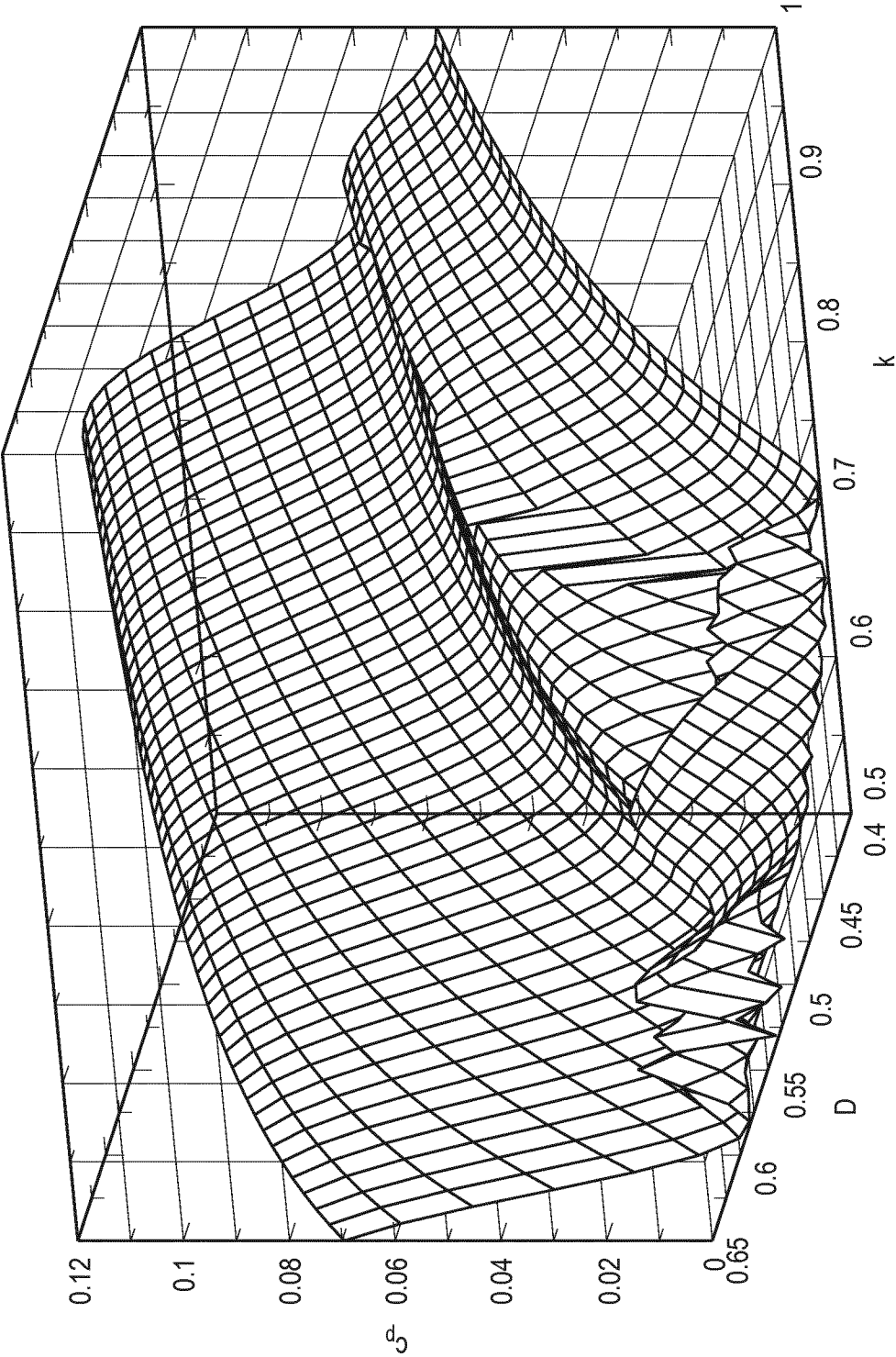


FIG. 19b

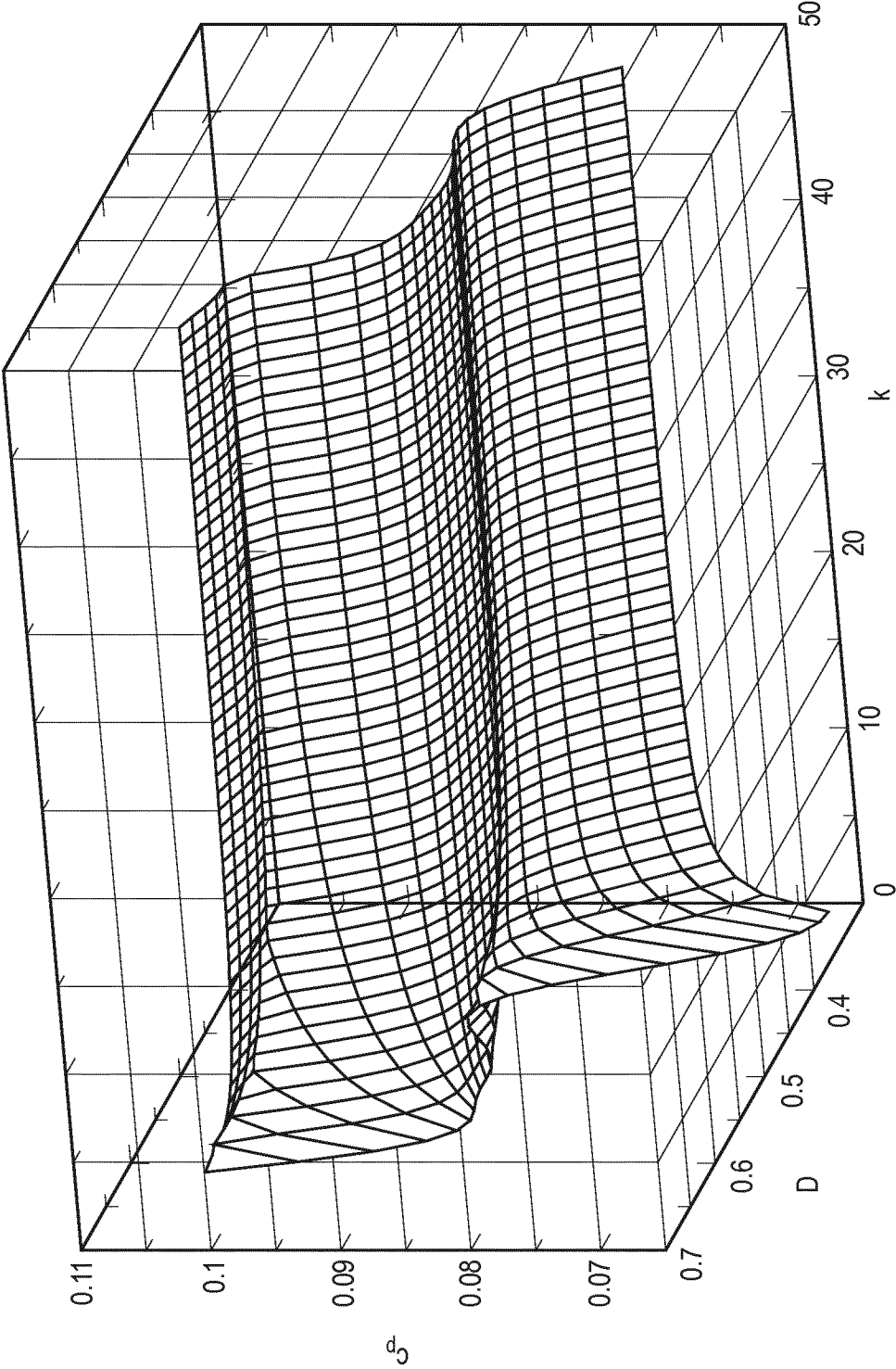


FIG. 20a

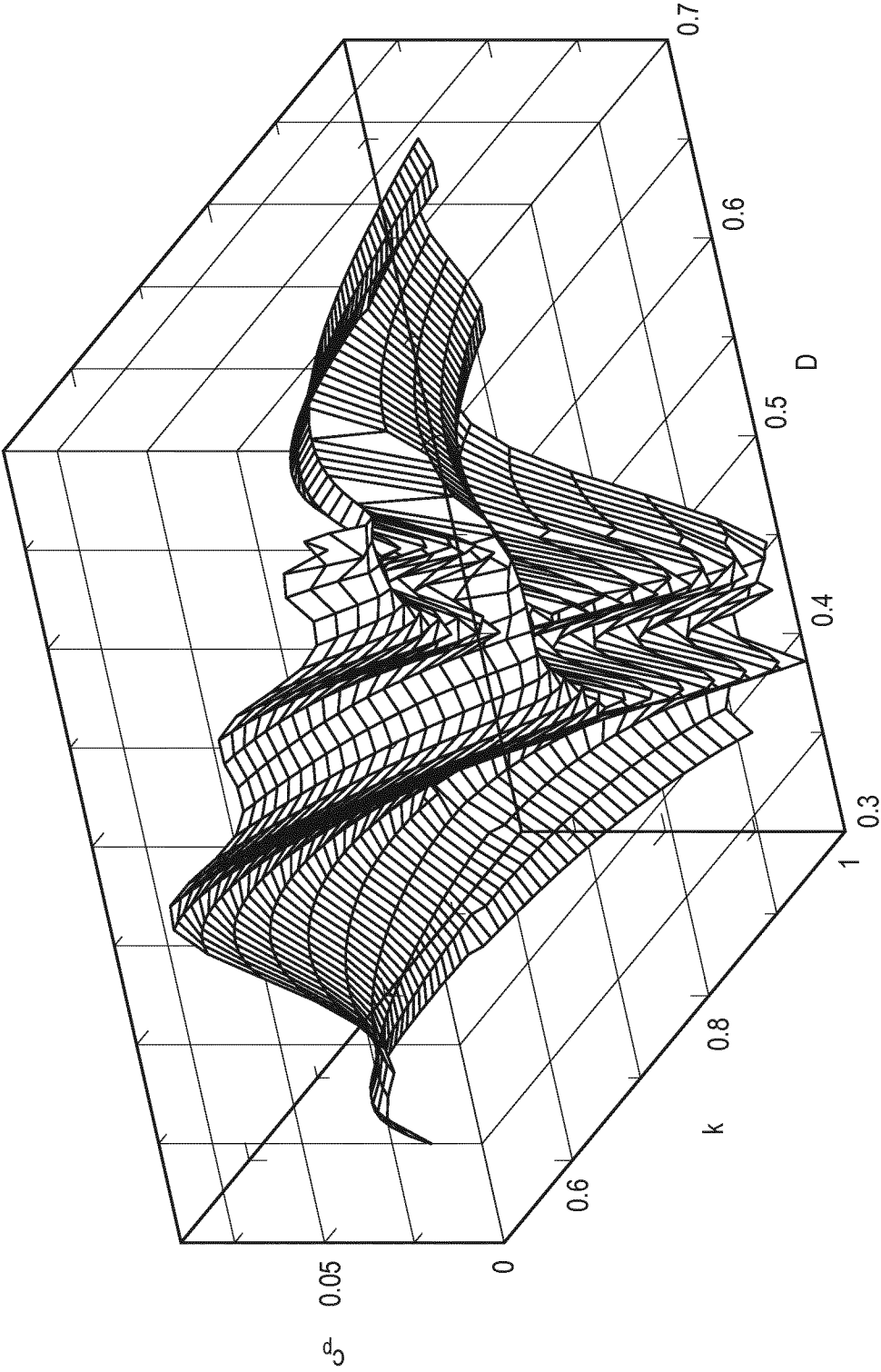


FIG. 20b

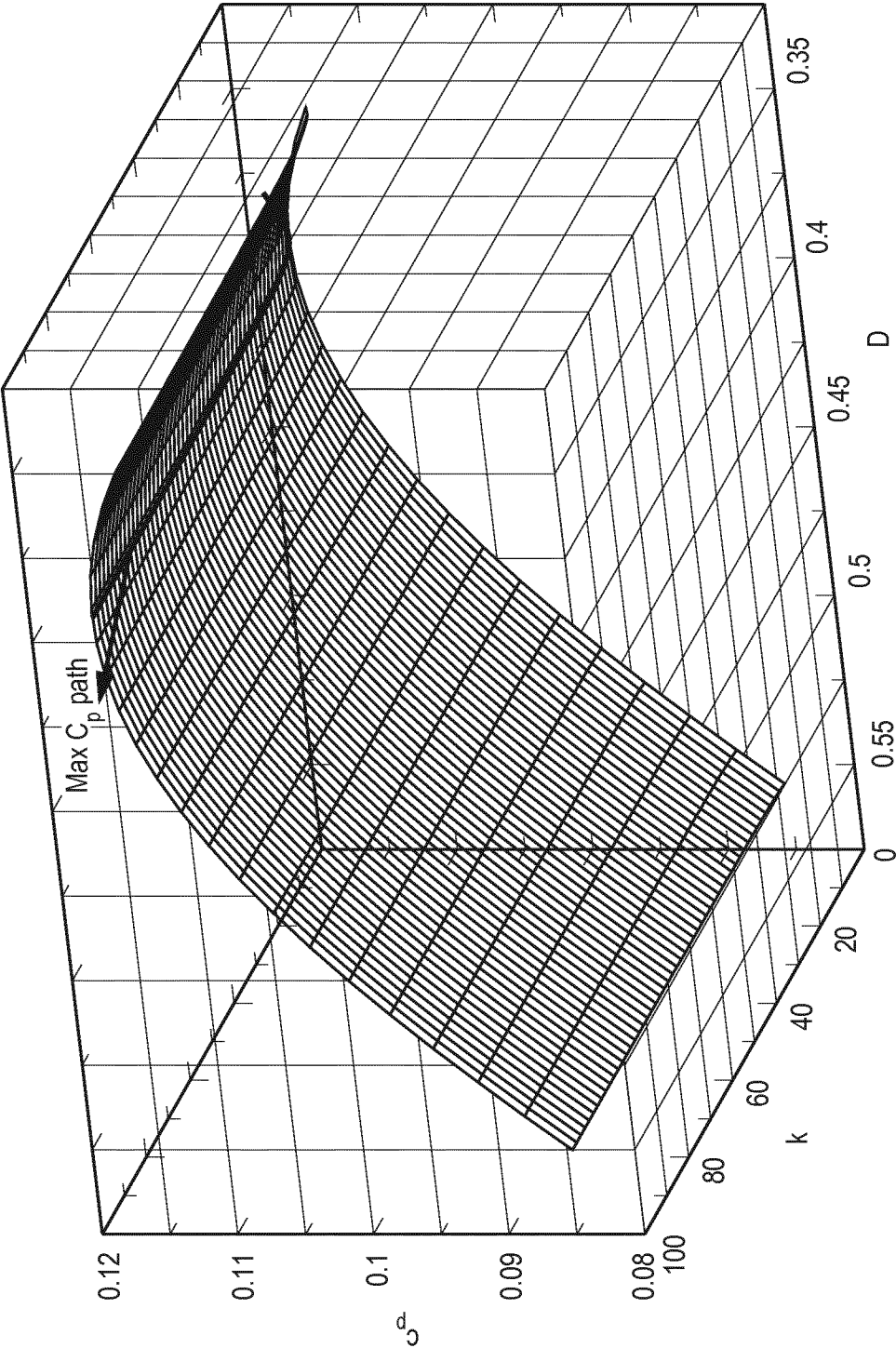


FIG. 21a

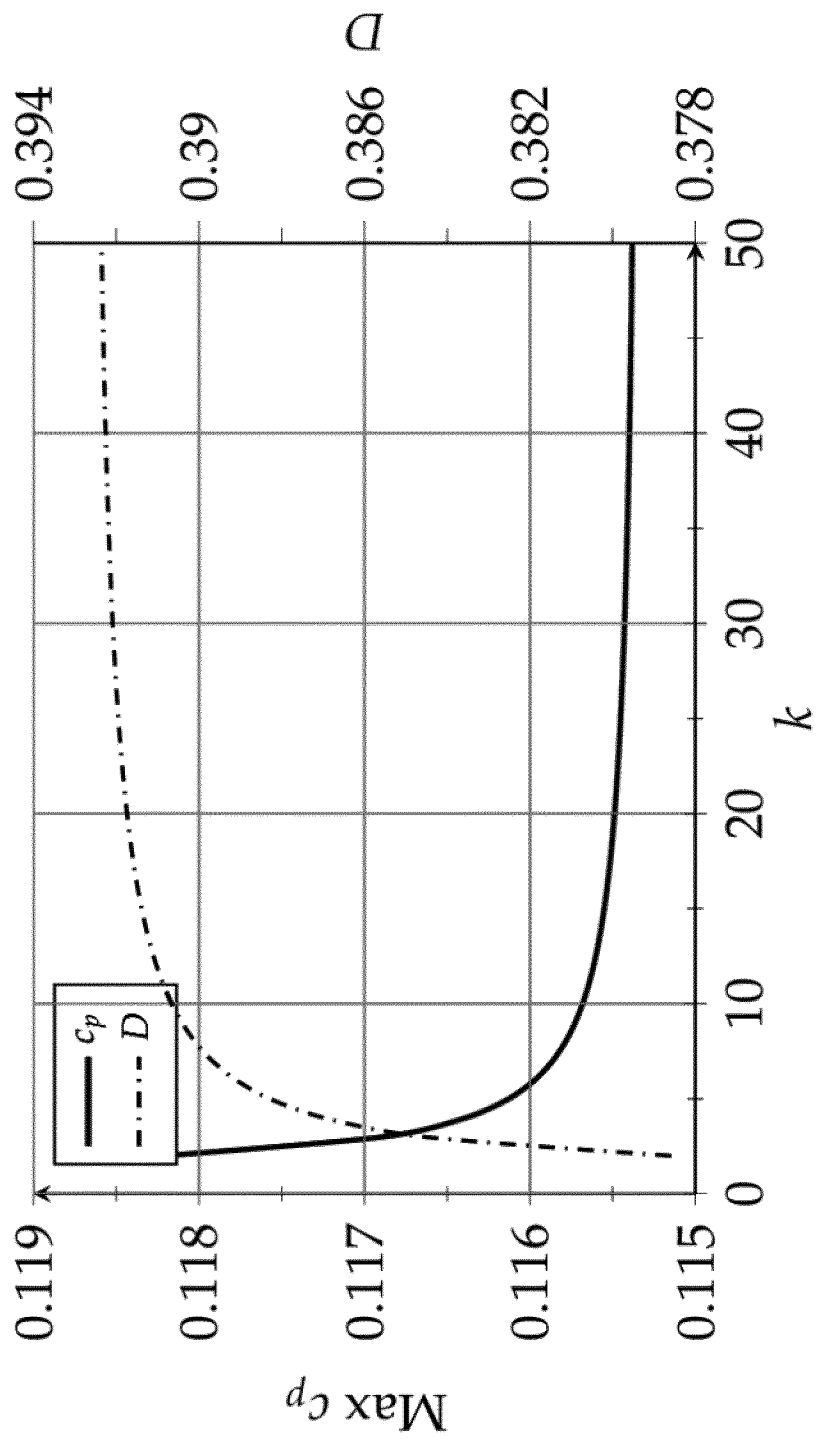


FIG. 21b

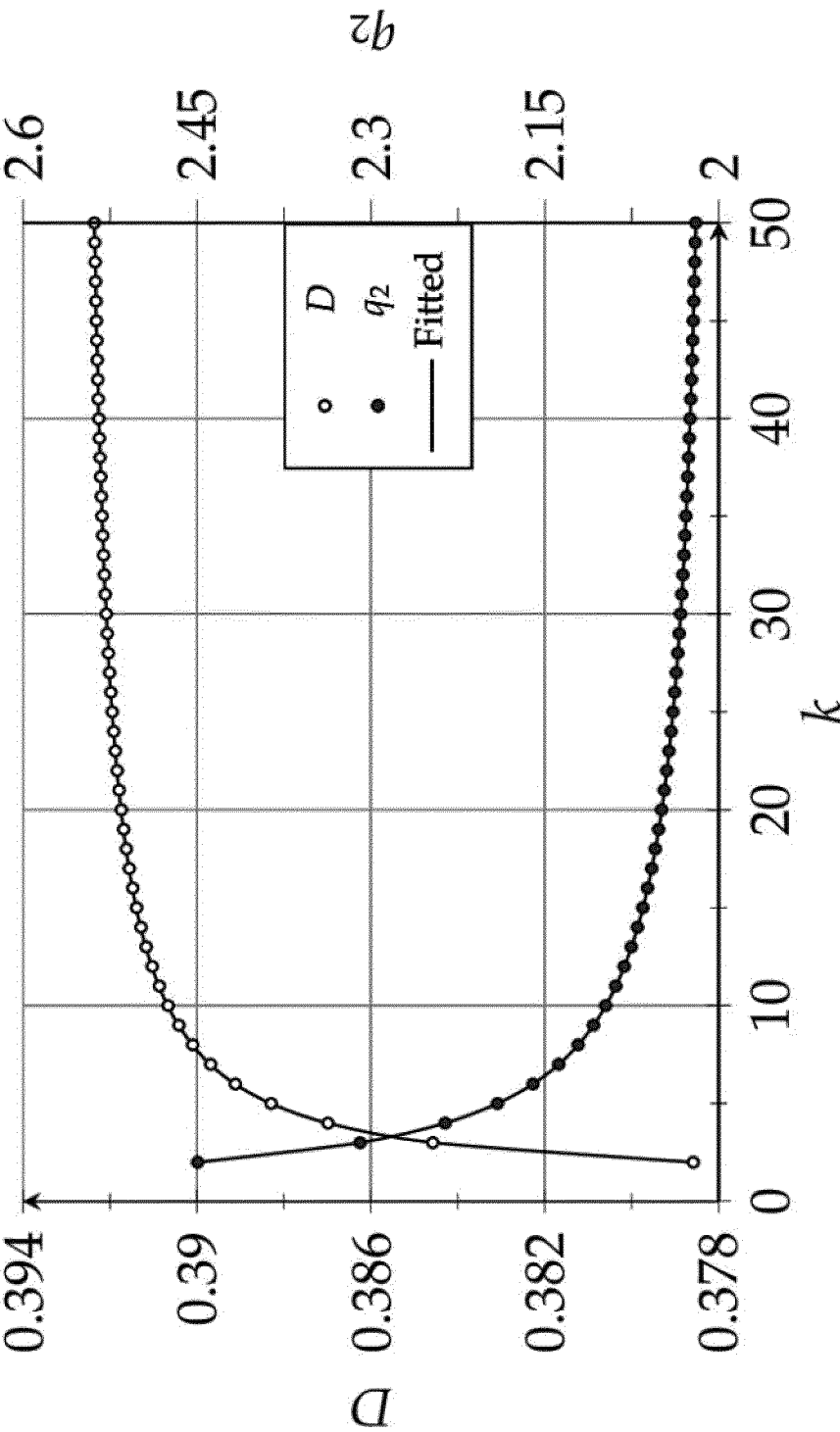


FIG. 22a

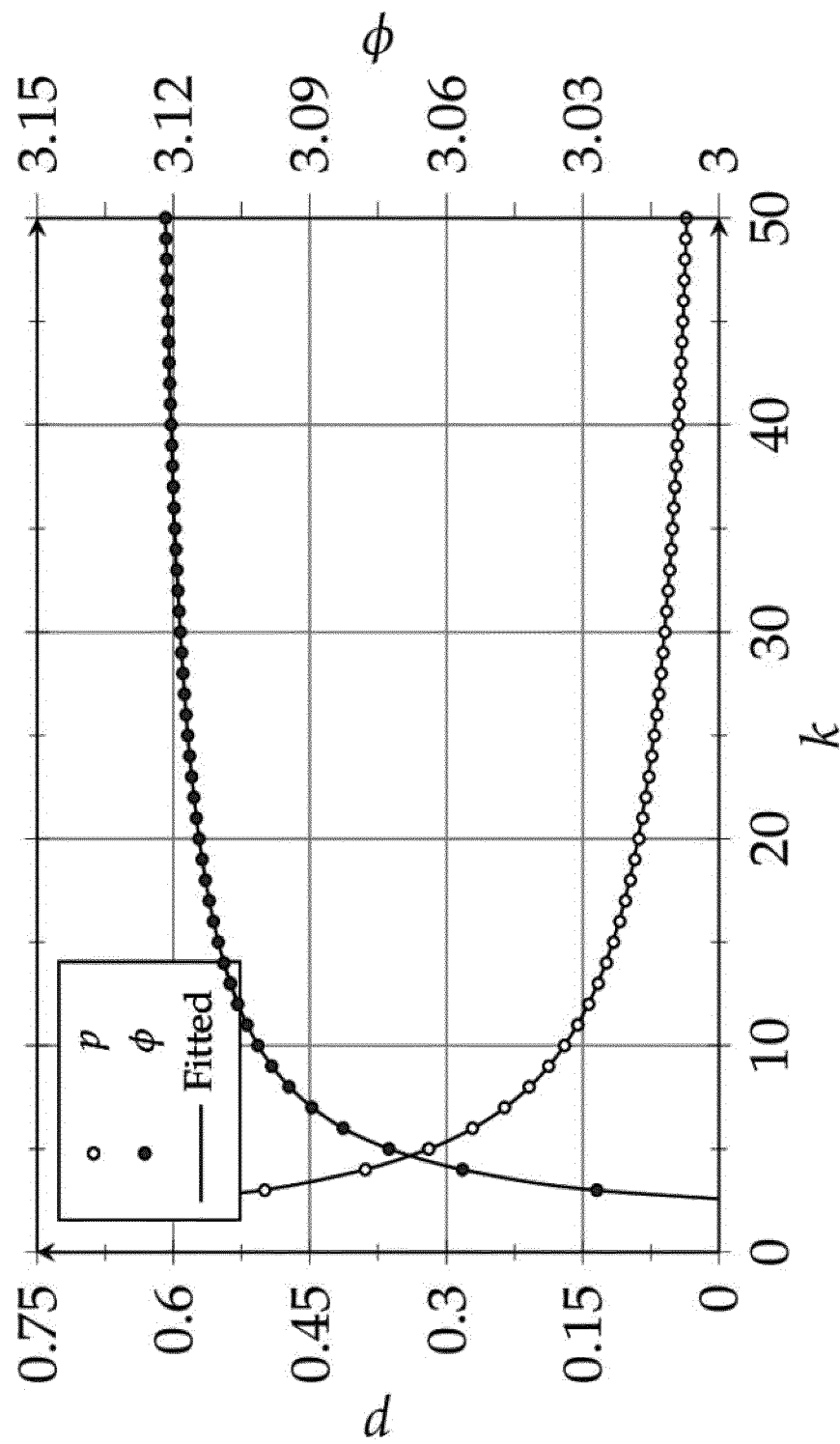


FIG. 22b

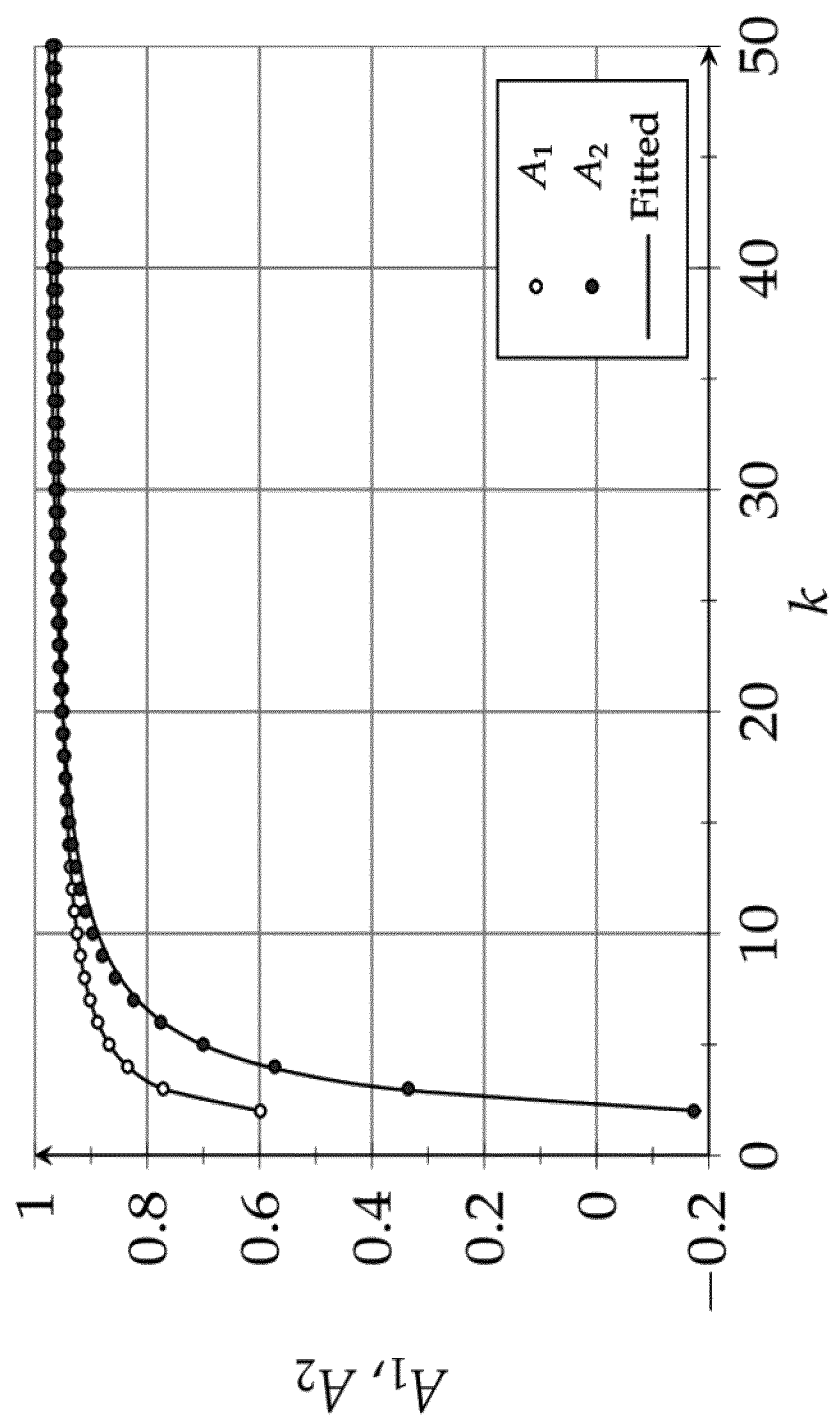


FIG. 22c

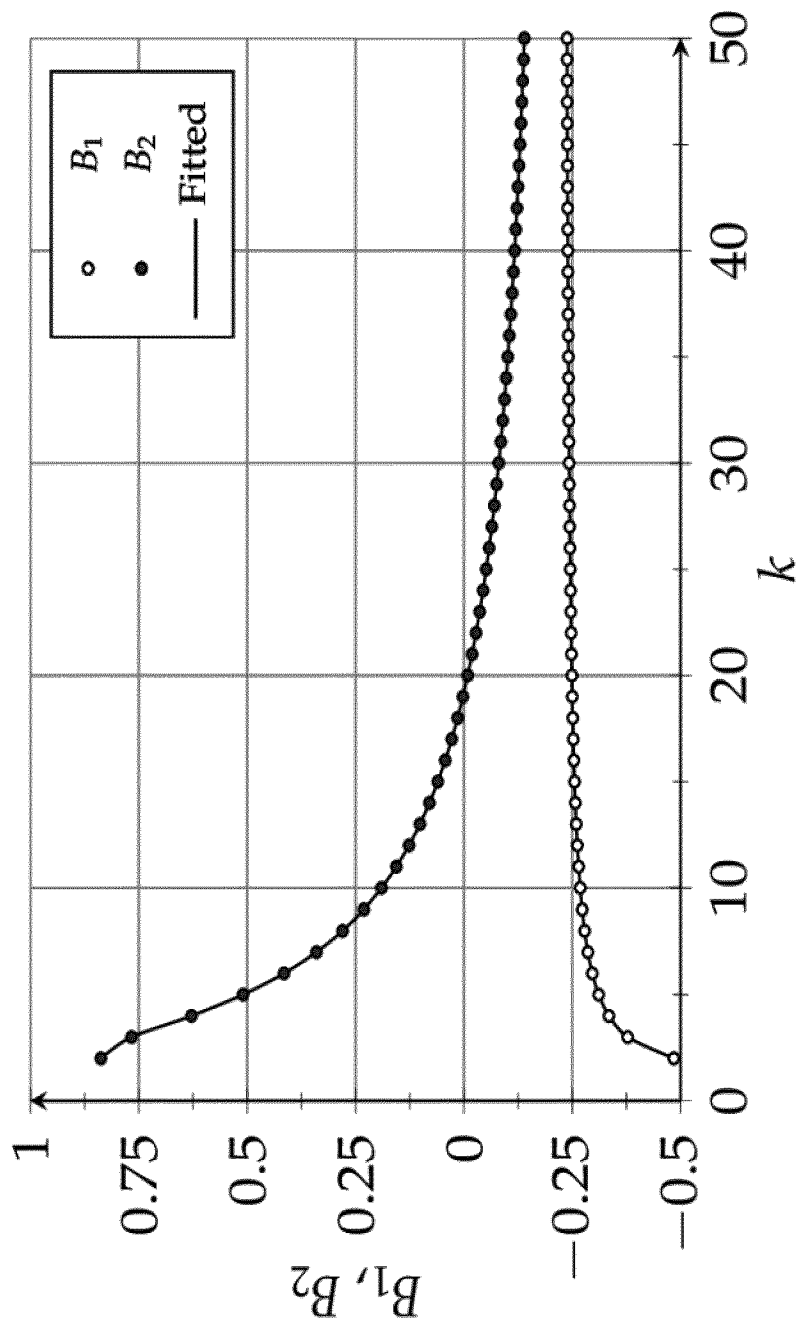


FIG. 22d

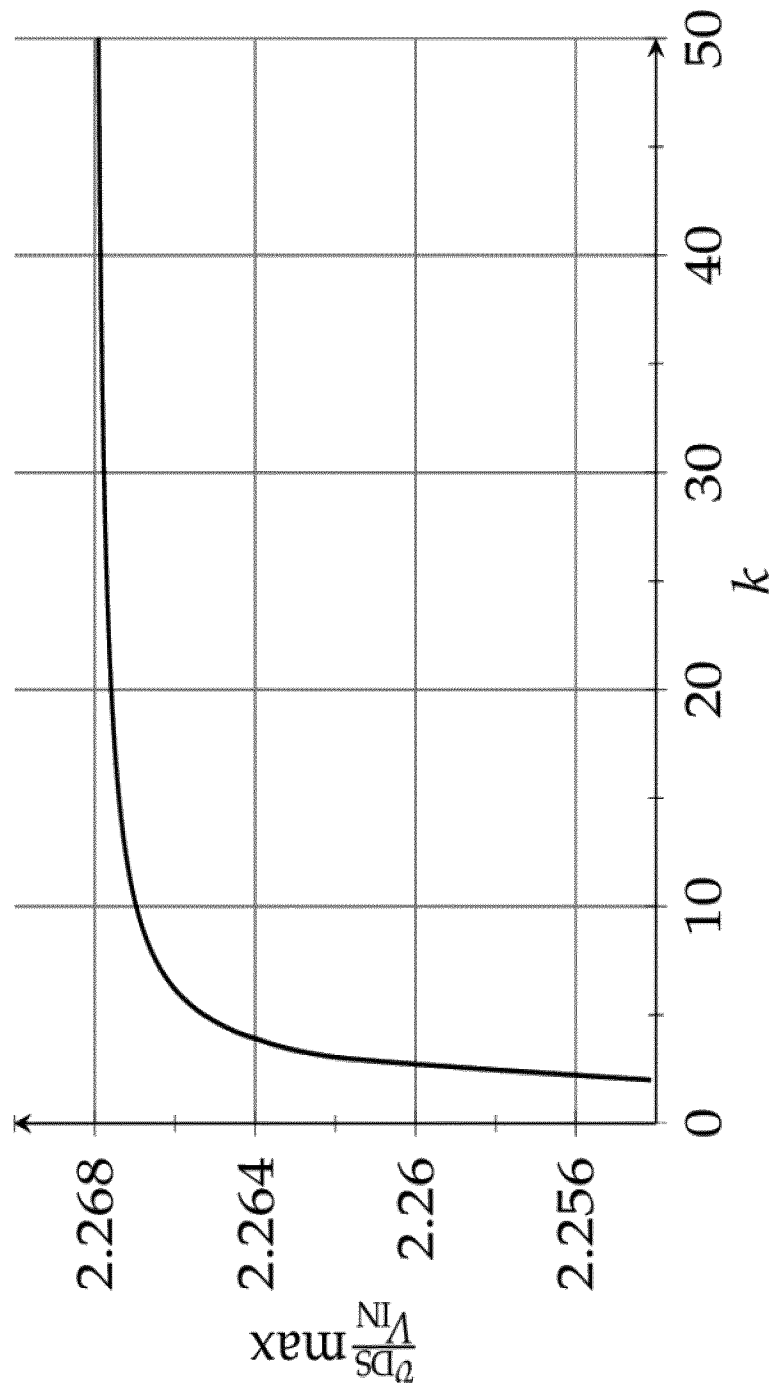


FIG. 23a

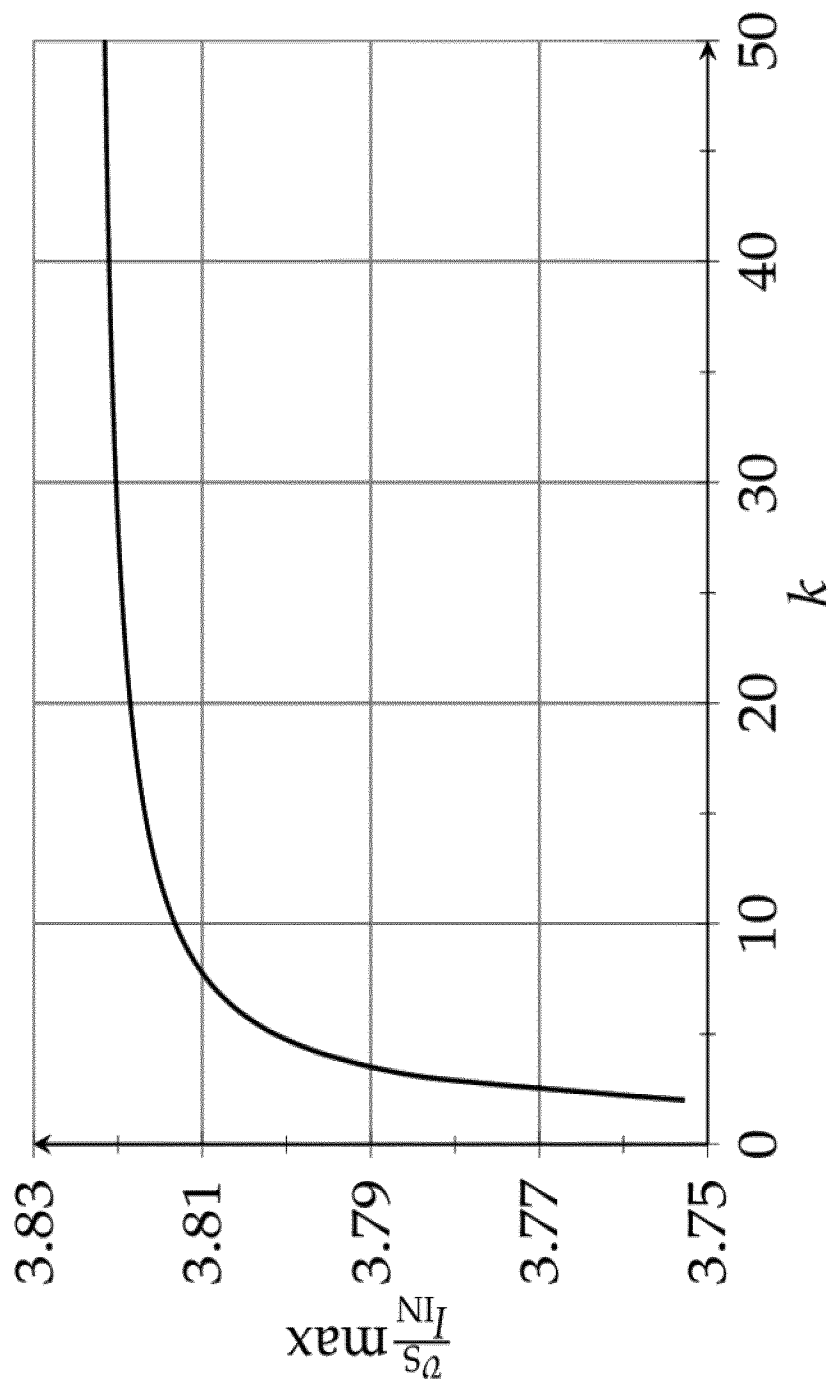


FIG. 23b

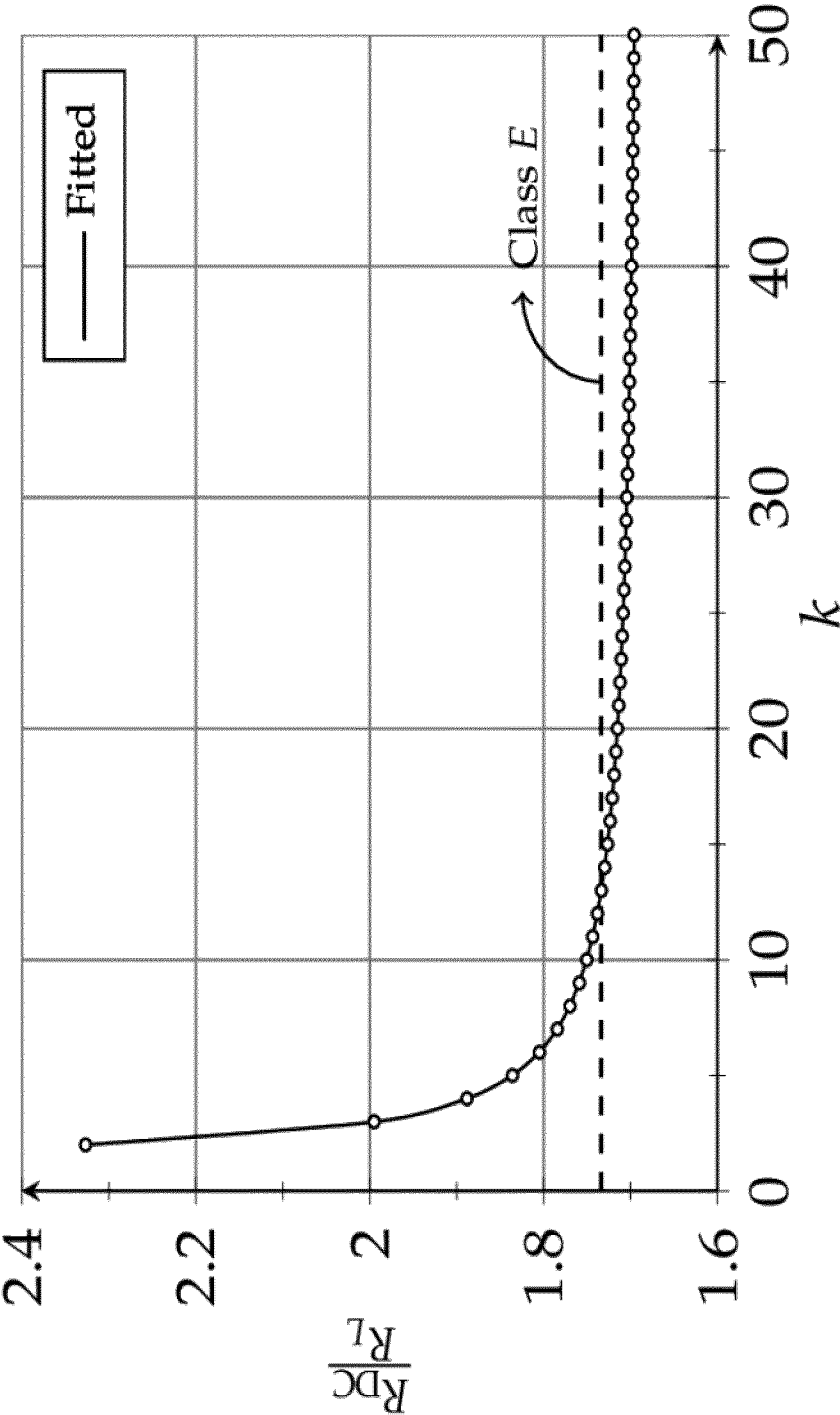


FIG. 24a

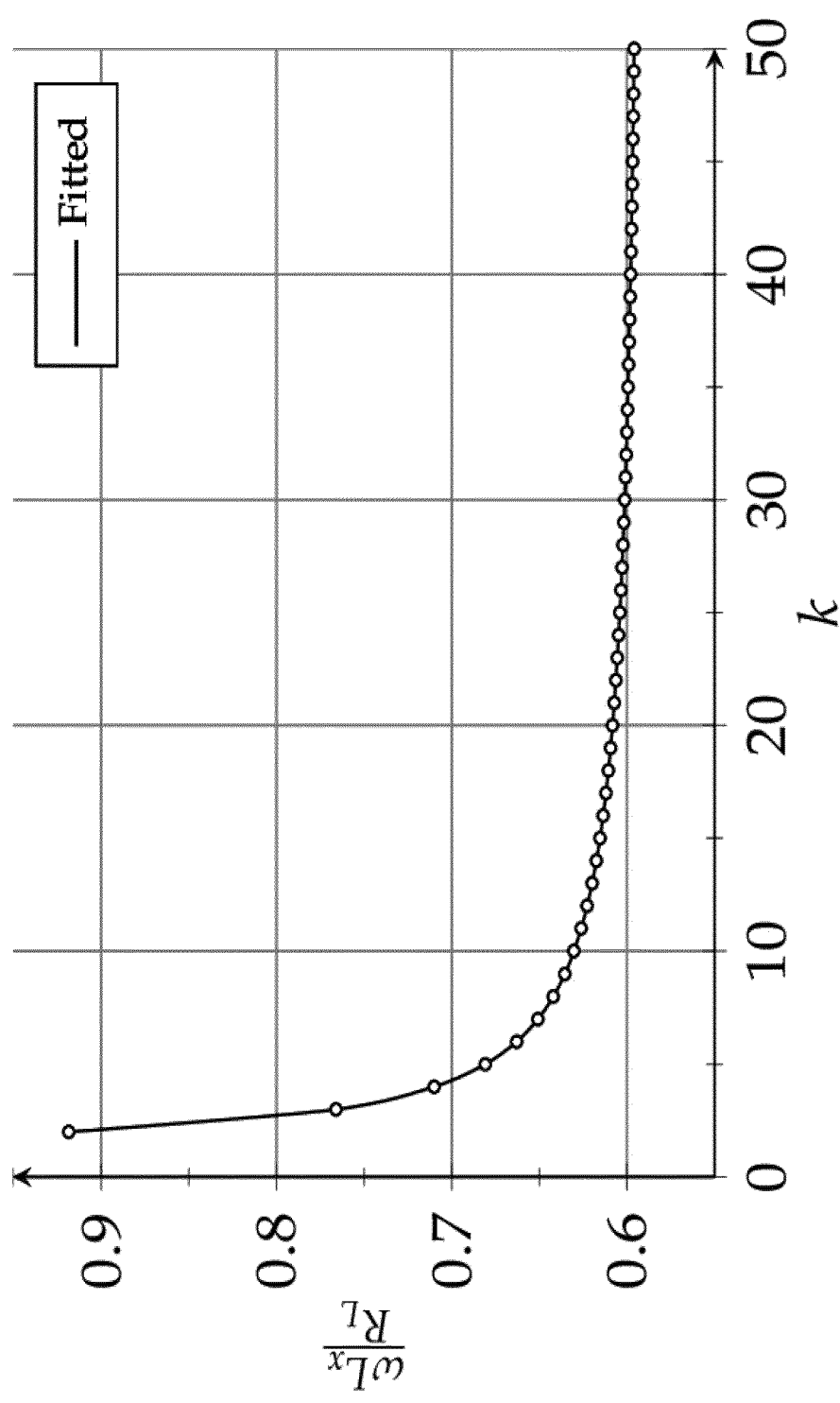


FIG. 24b

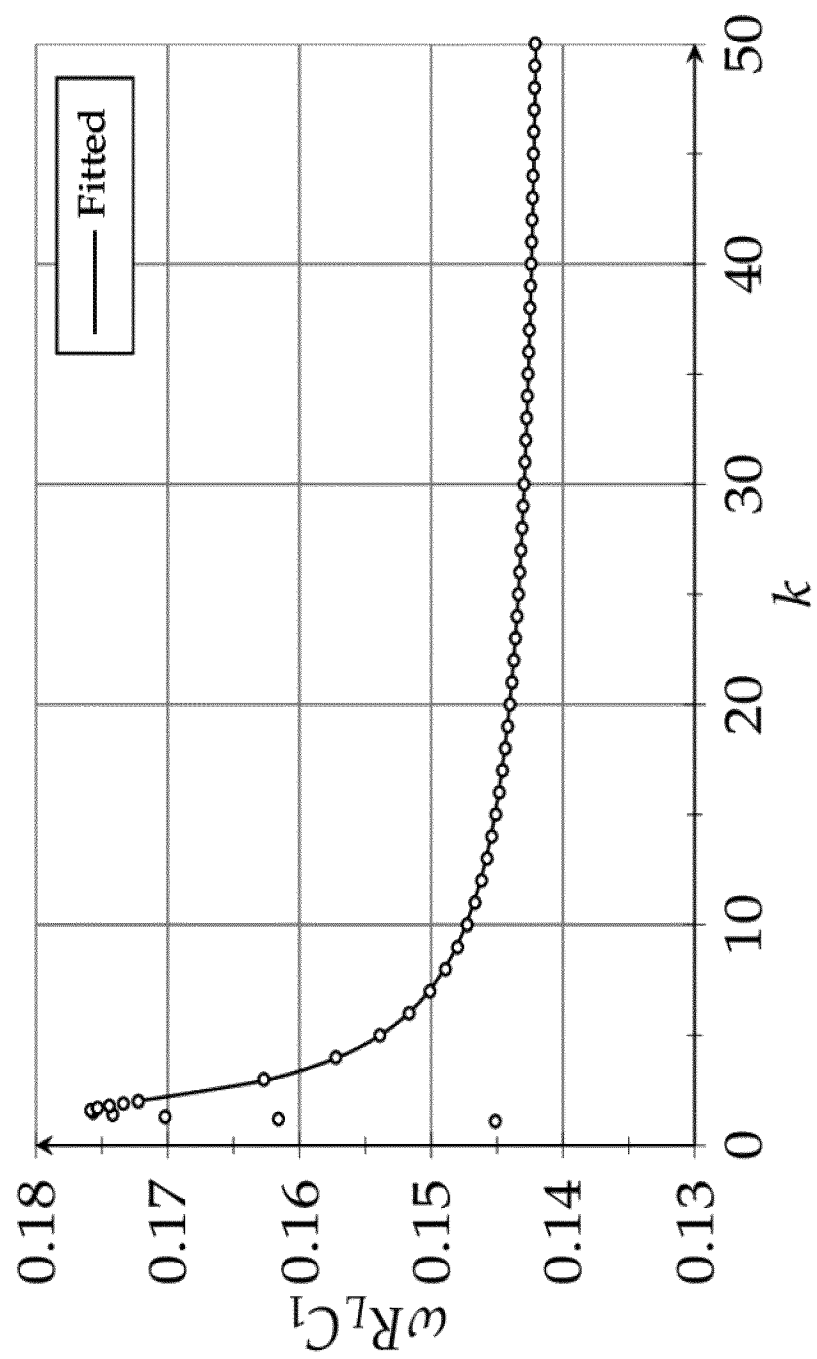


FIG. 24c

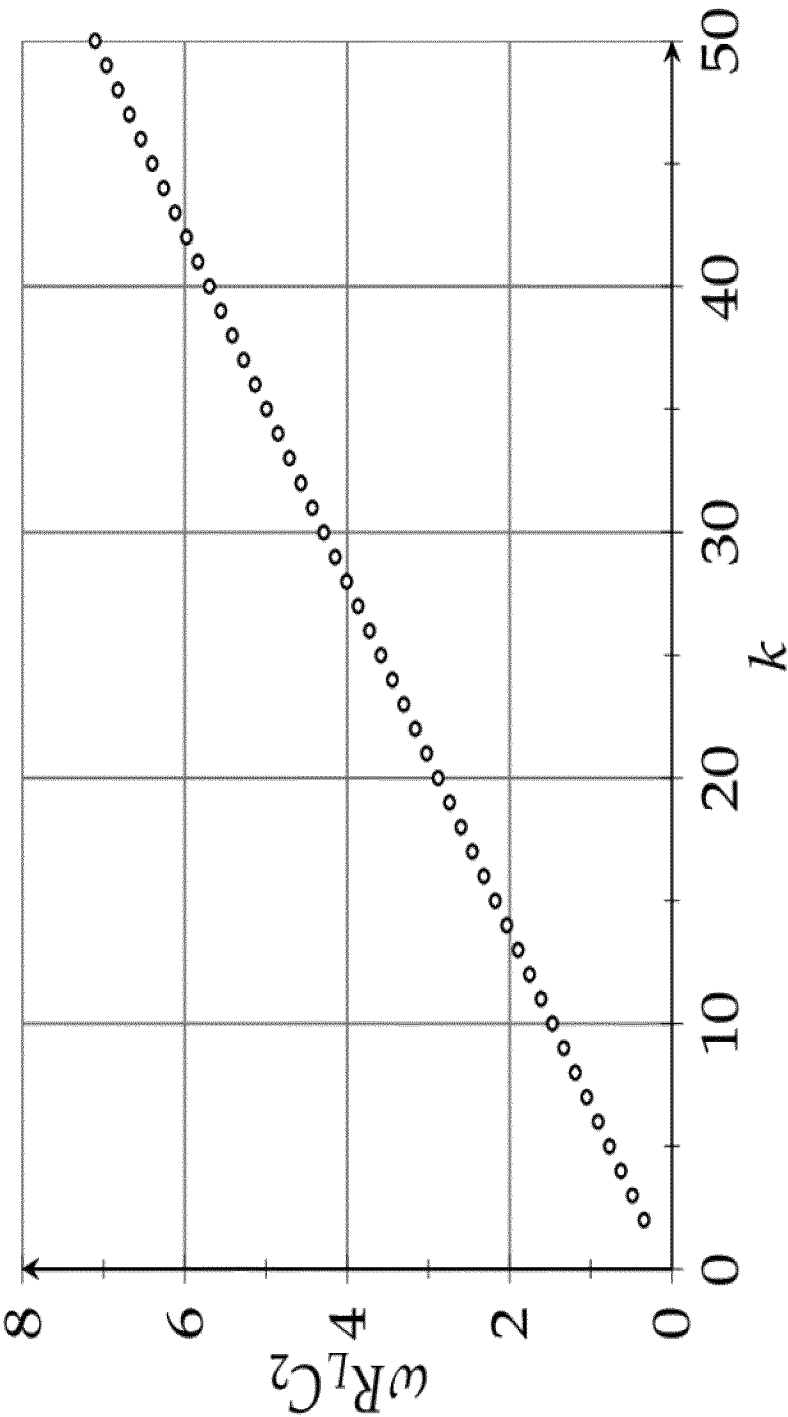


FIG. 24d

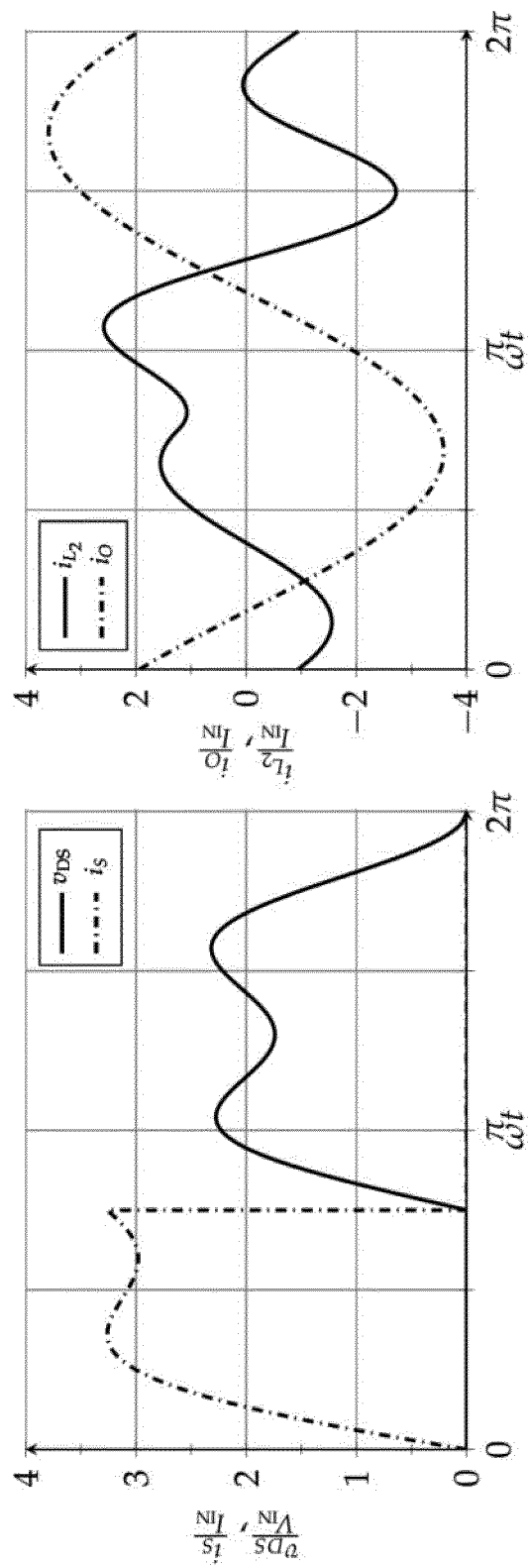


FIG. 25

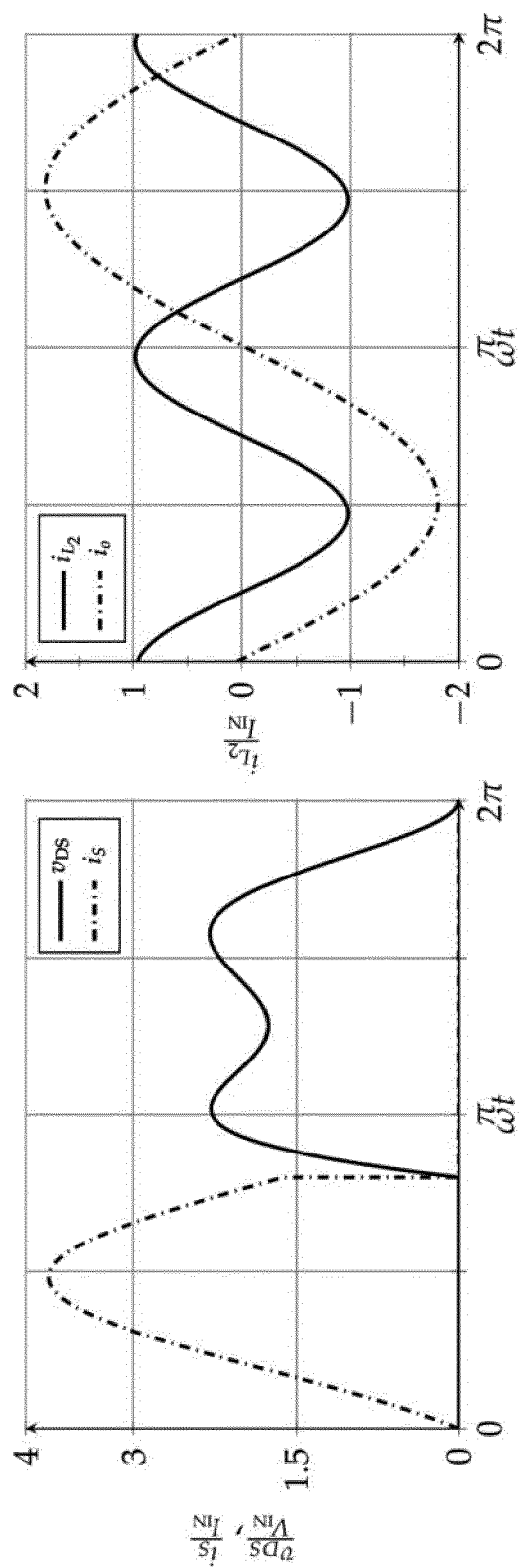


FIG. 26

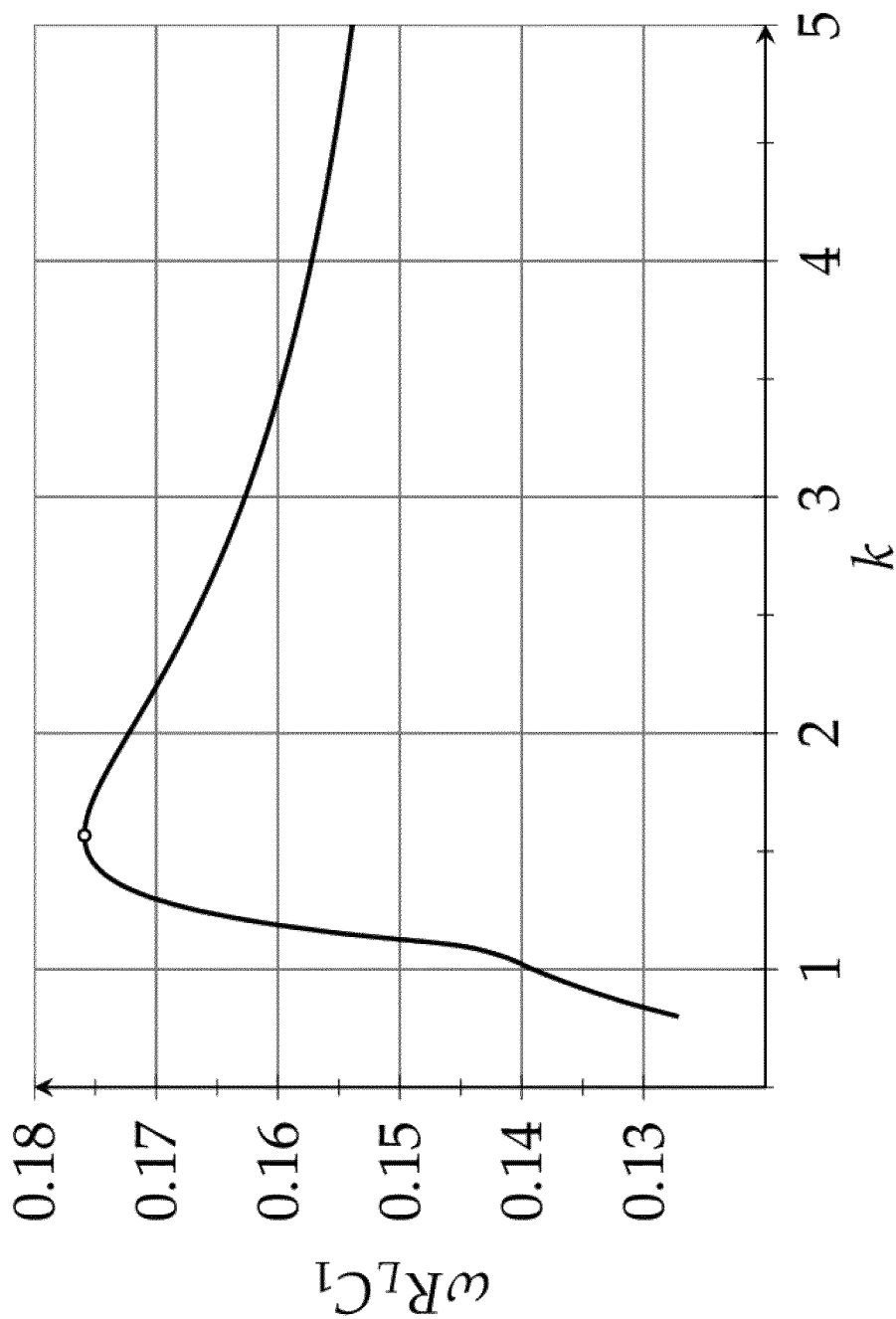


FIG. 27a

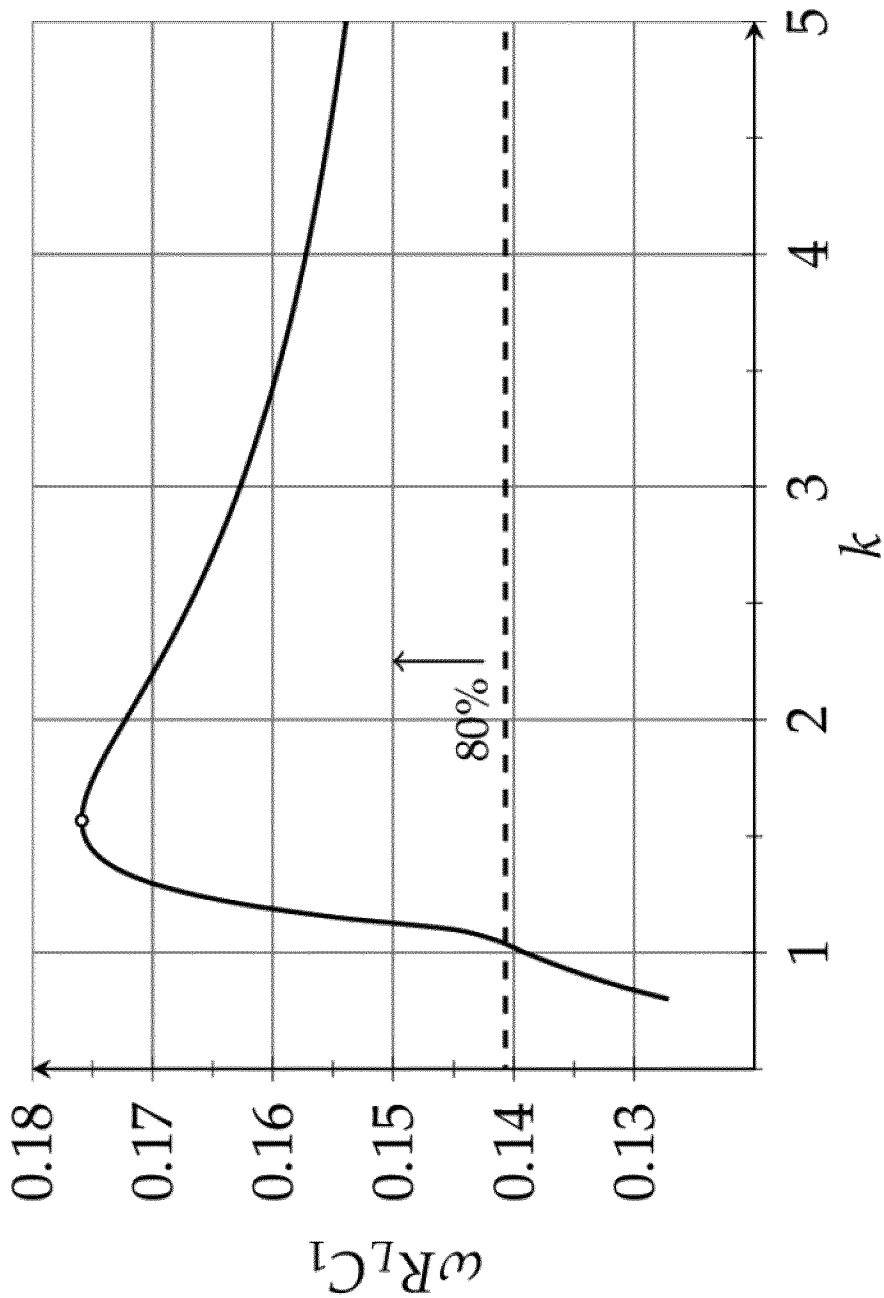


FIG. 27b

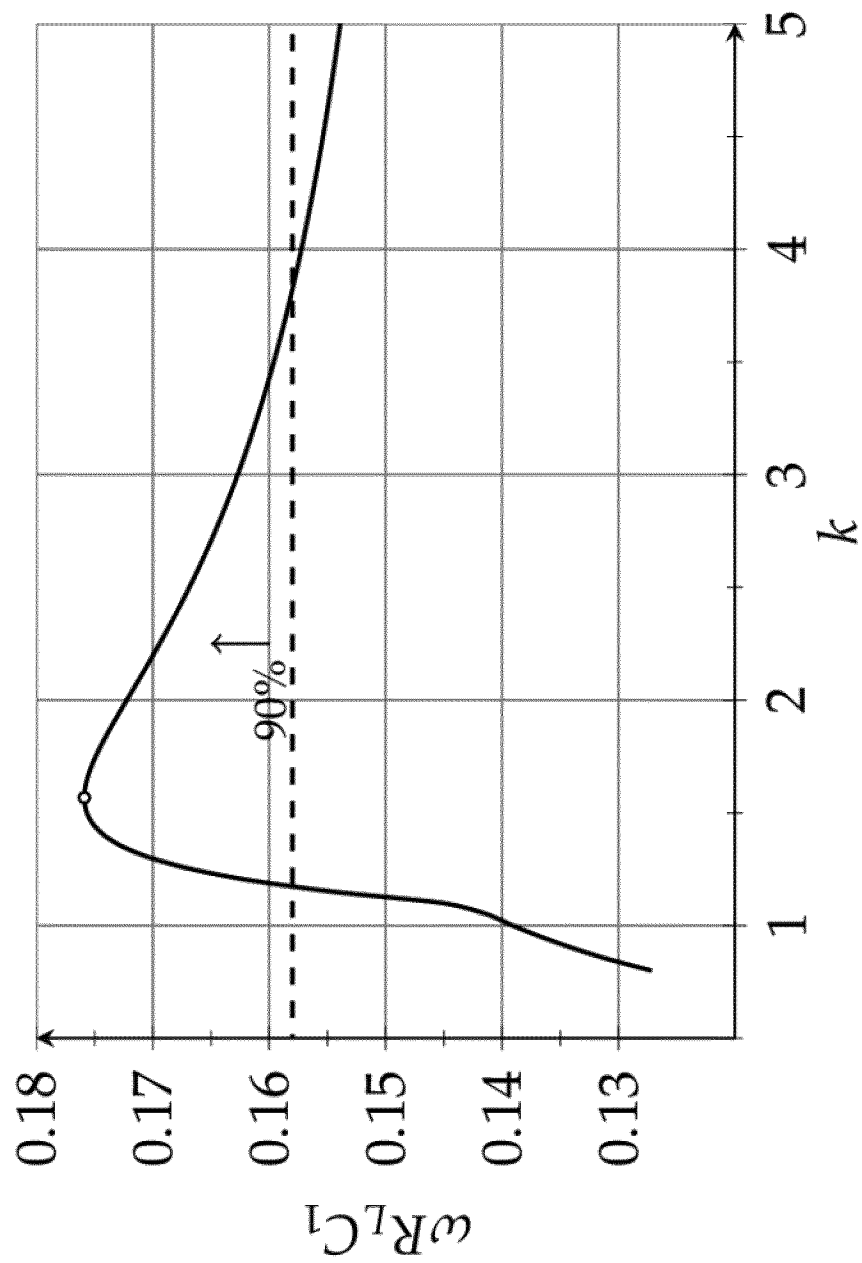


FIG. 27c

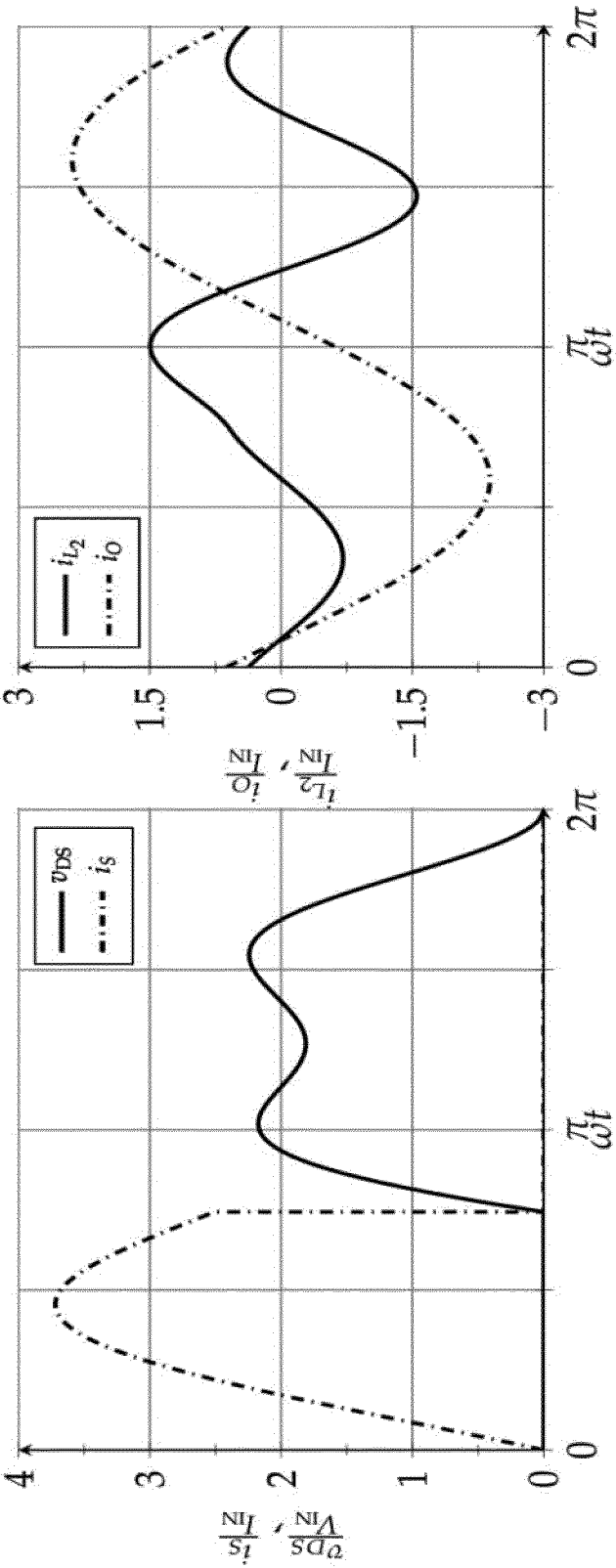


FIG. 28

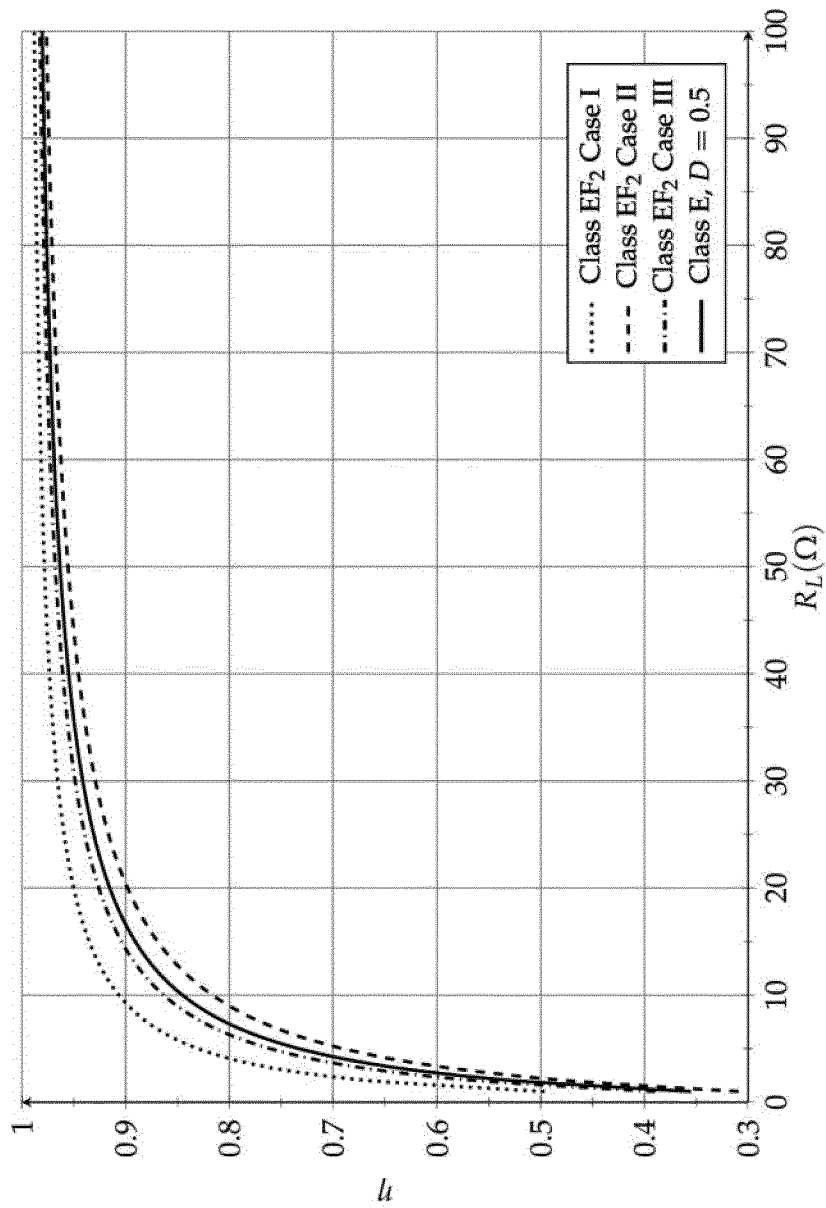


FIG. 29

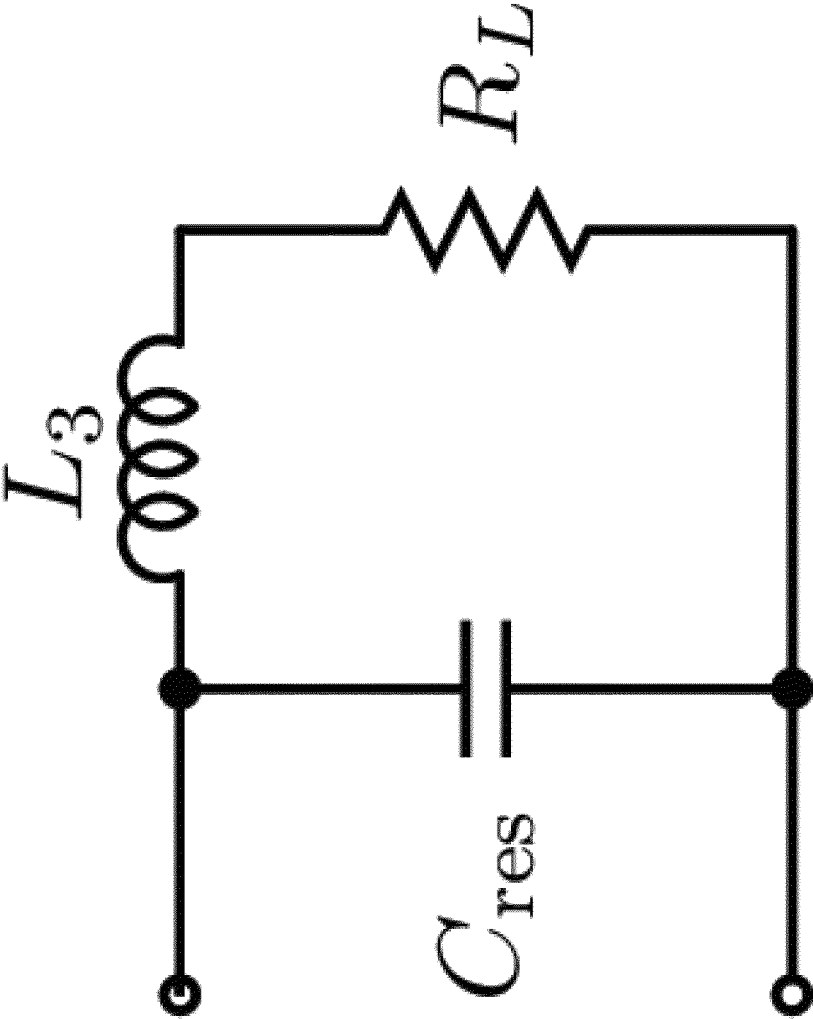
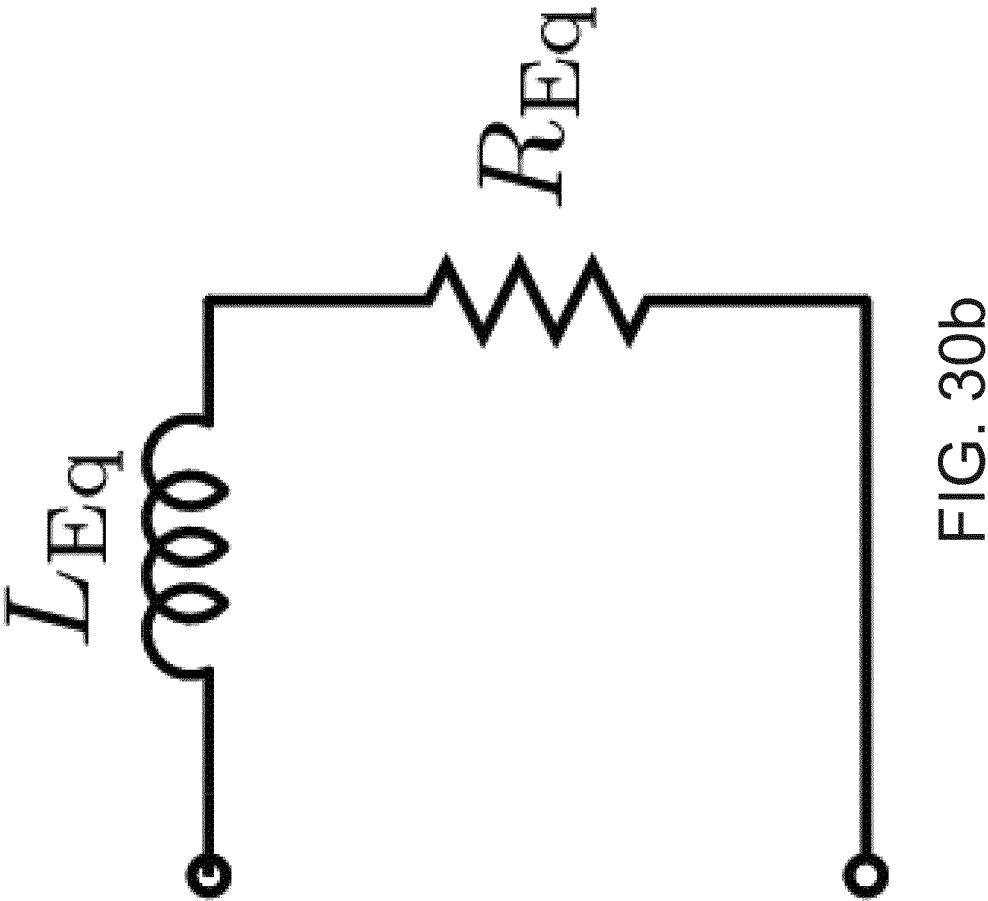


FIG. 30a



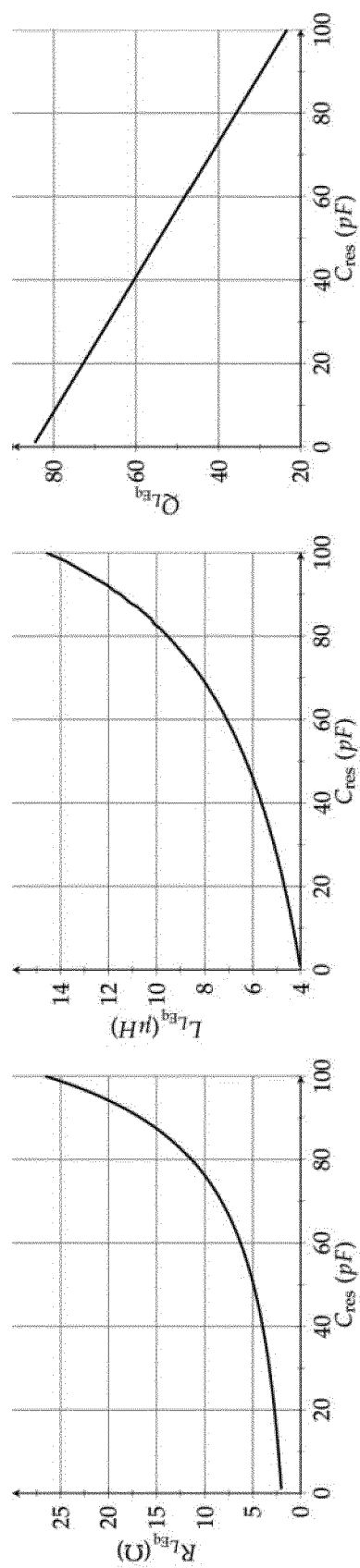


FIG. 31

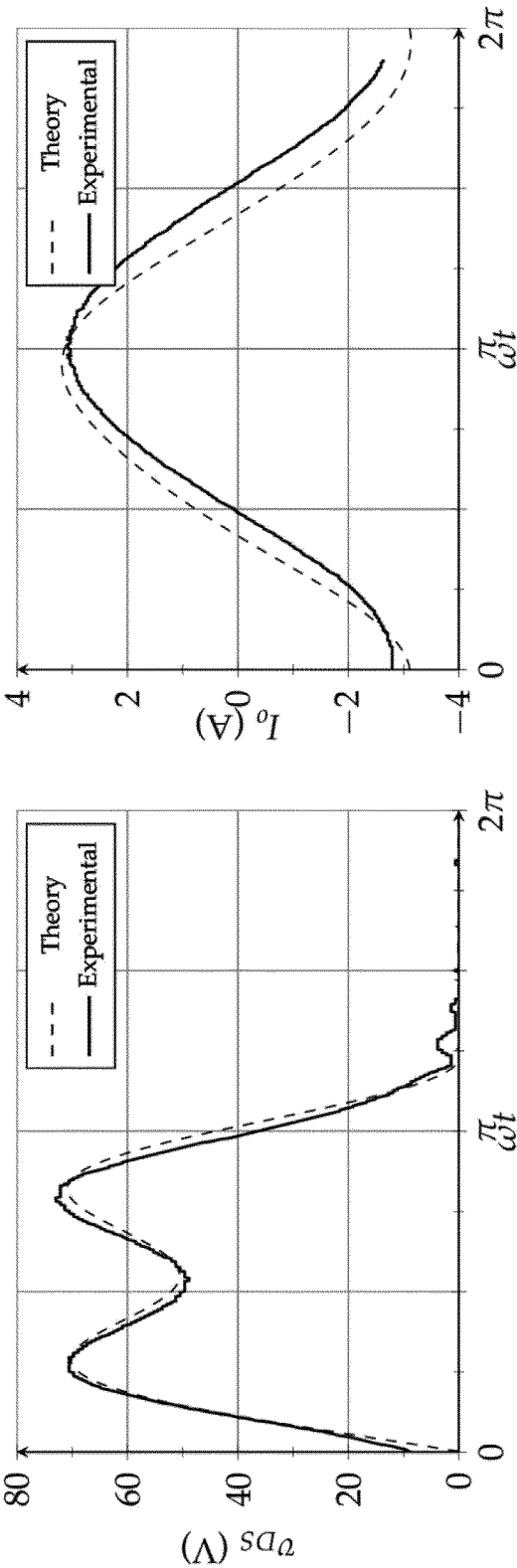


FIG. 32a

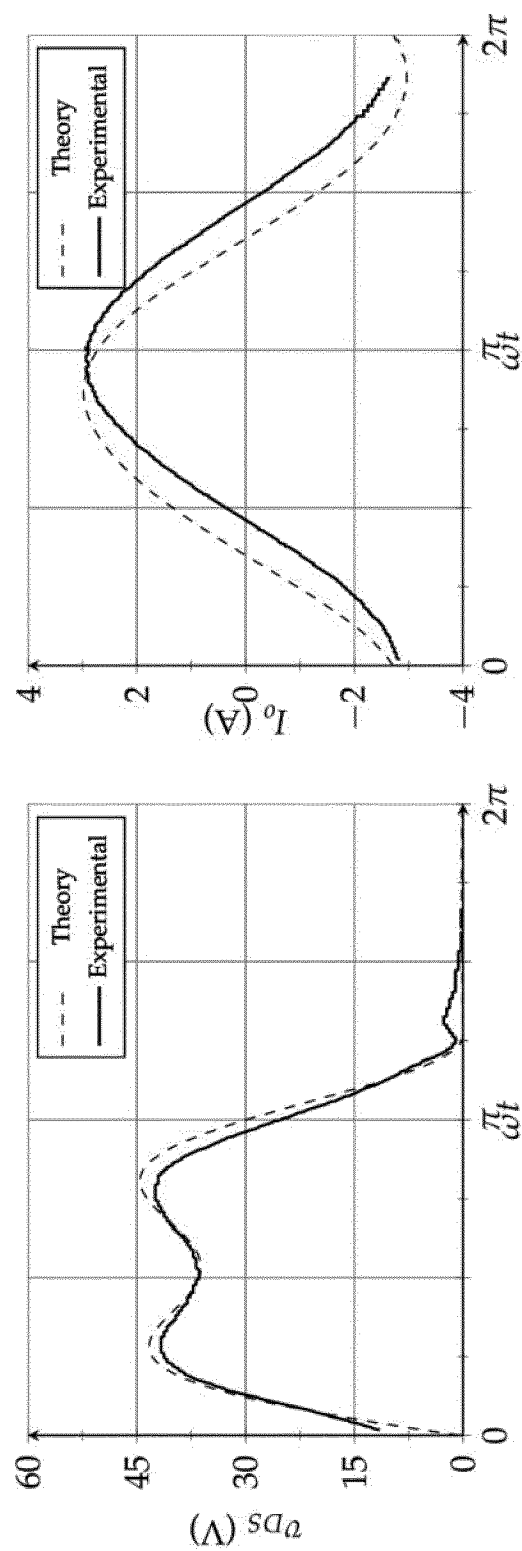


FIG. 32b

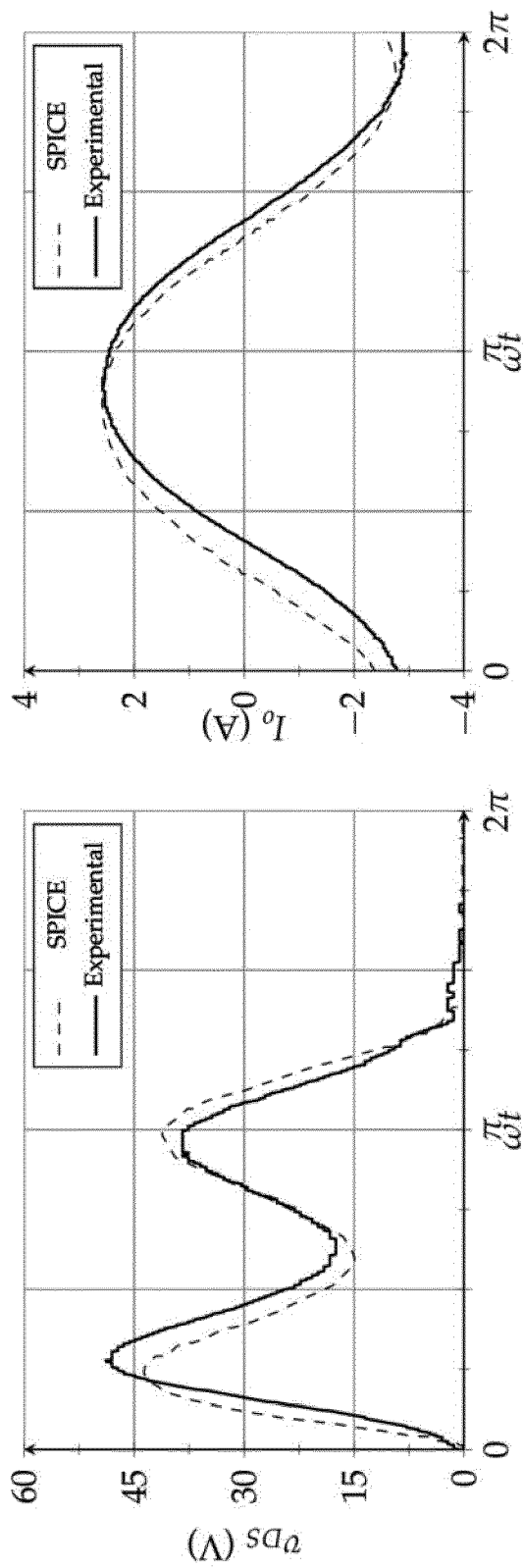


FIG. 32c

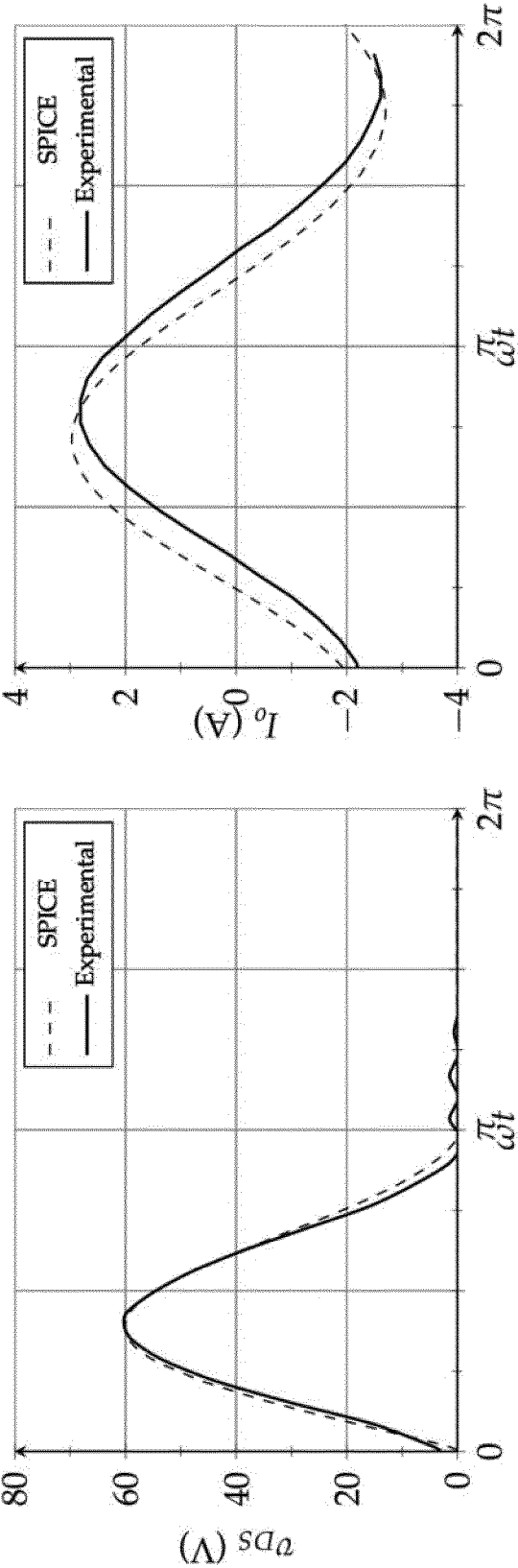


FIG. 32d

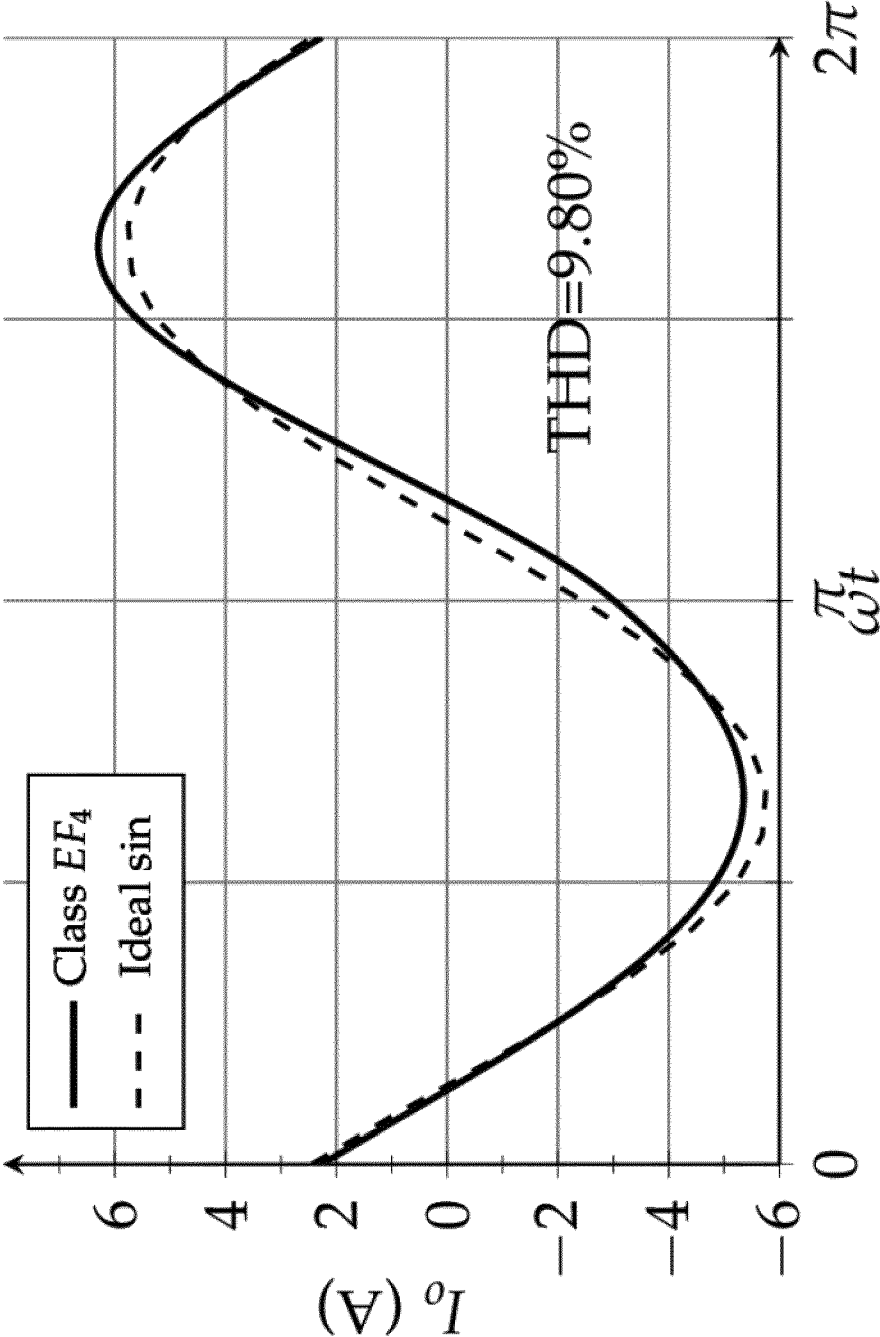


FIG. 33a

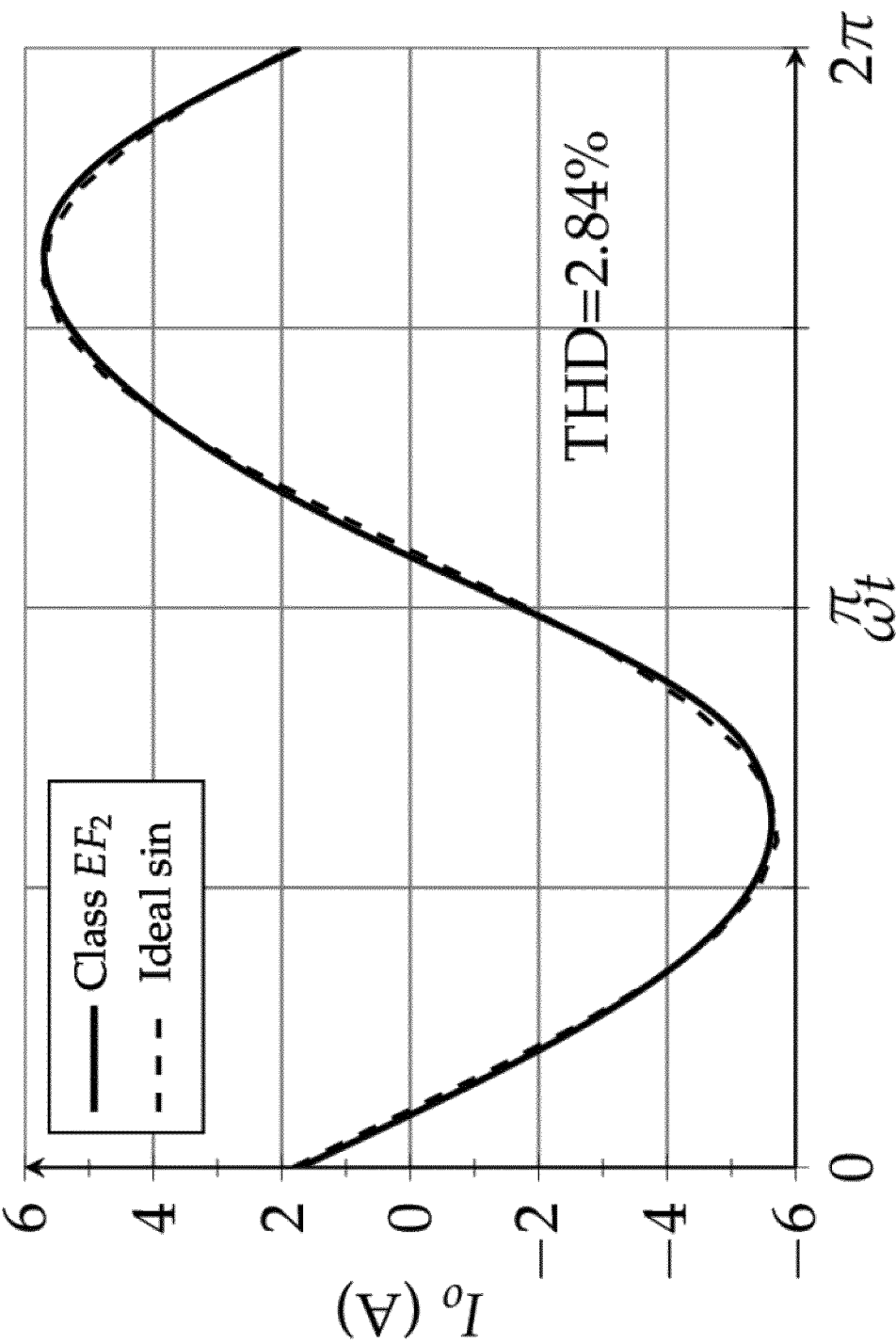


FIG. 33b

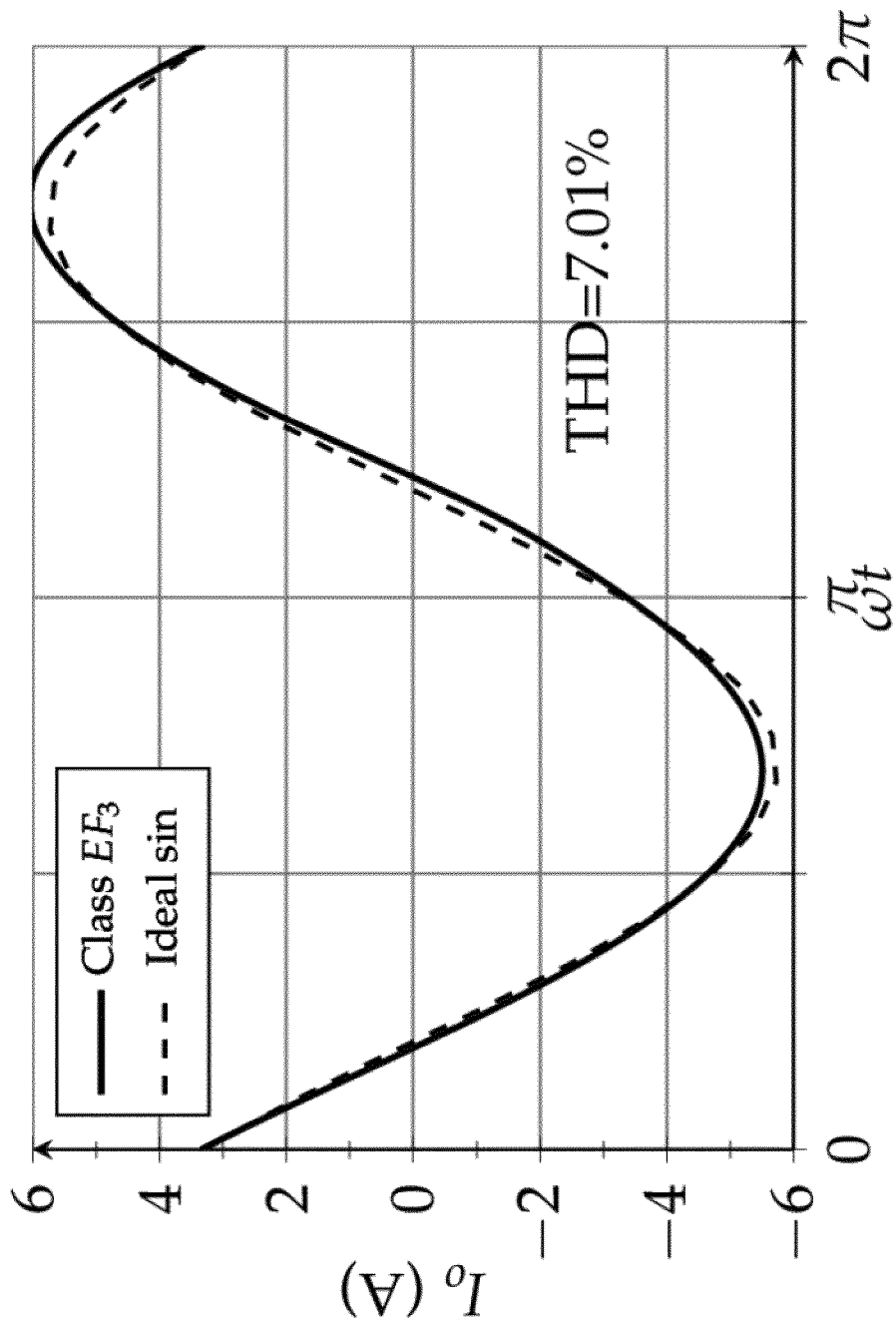


FIG. 33c

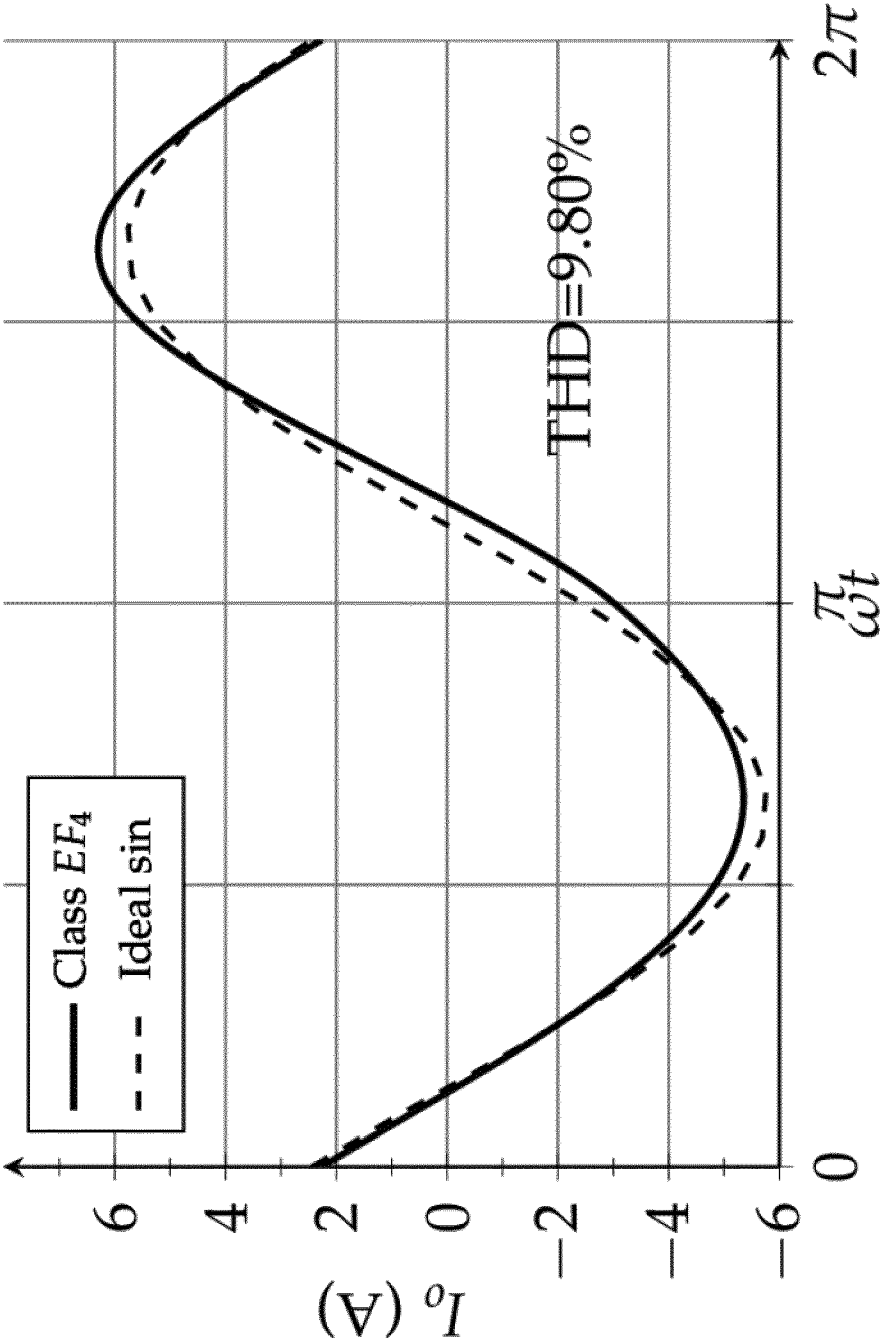


FIG. 33d

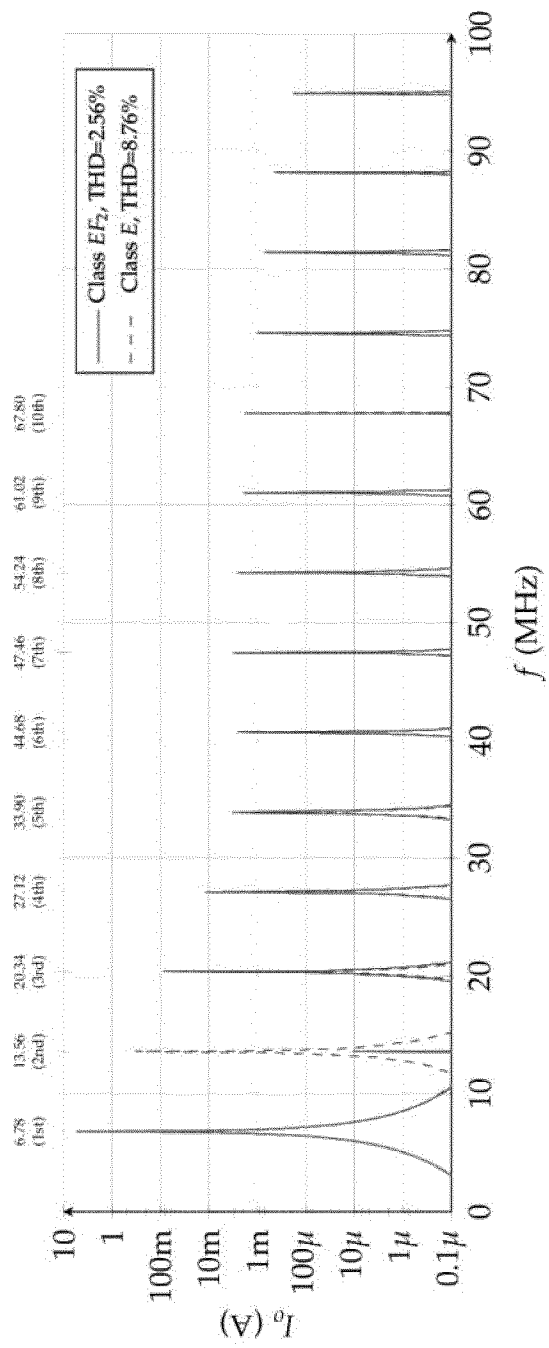


FIG. 34a

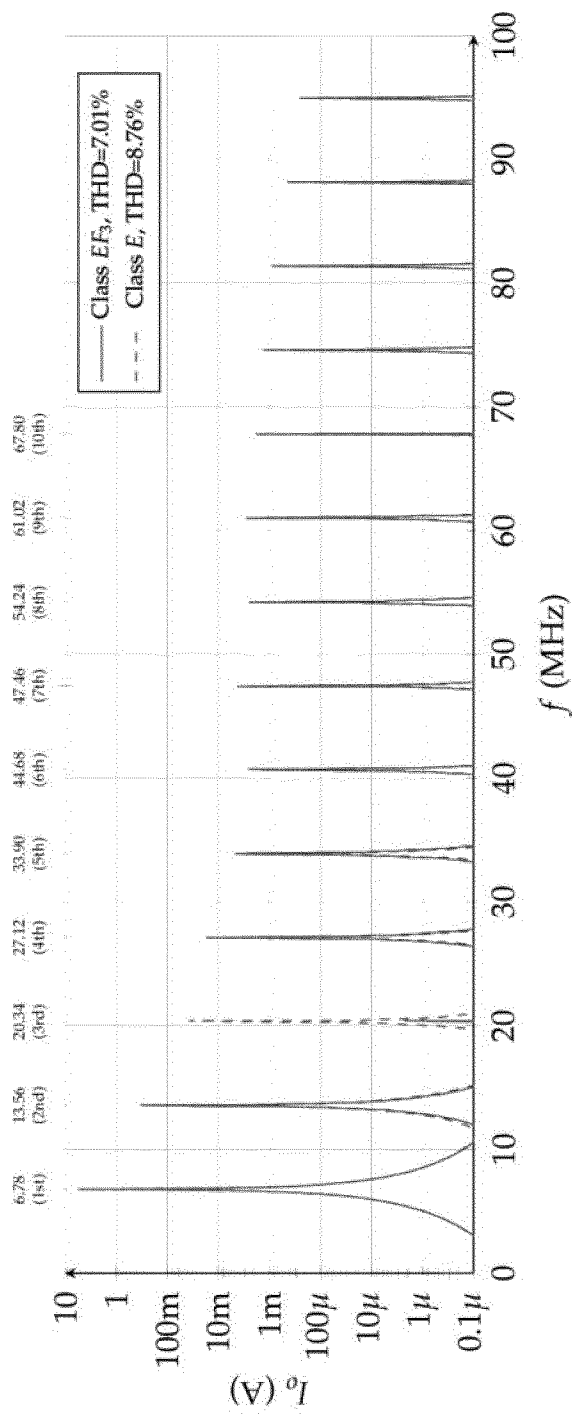


FIG. 34b

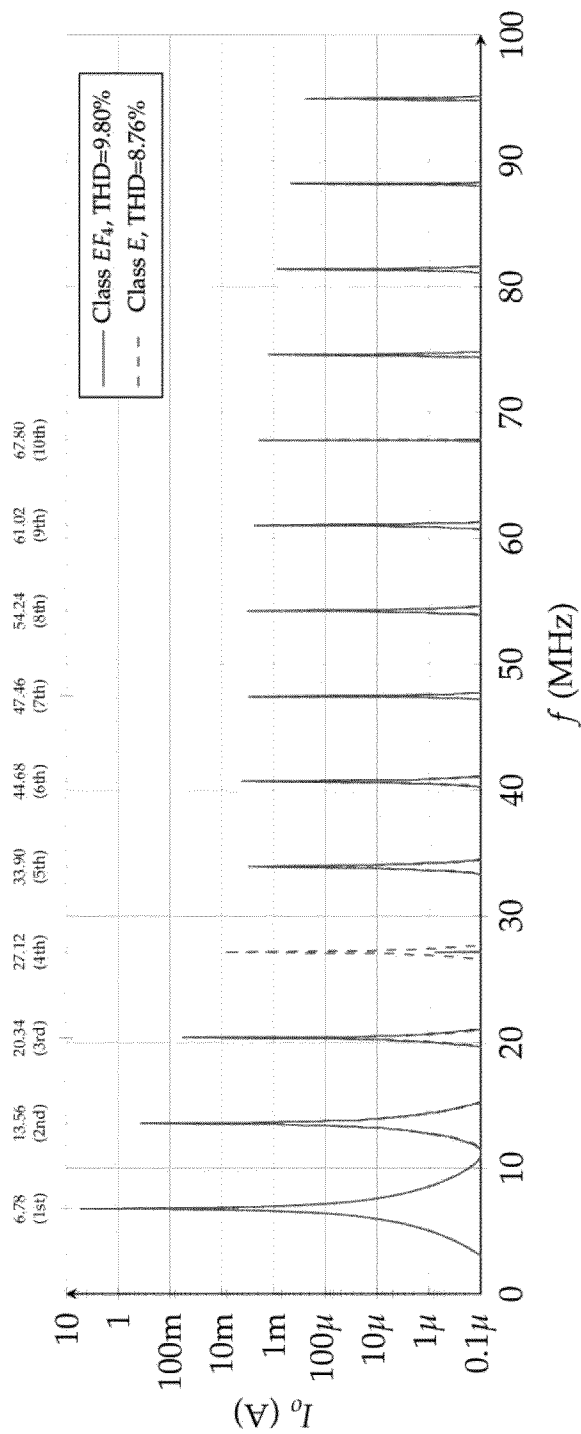


FIG. 34c

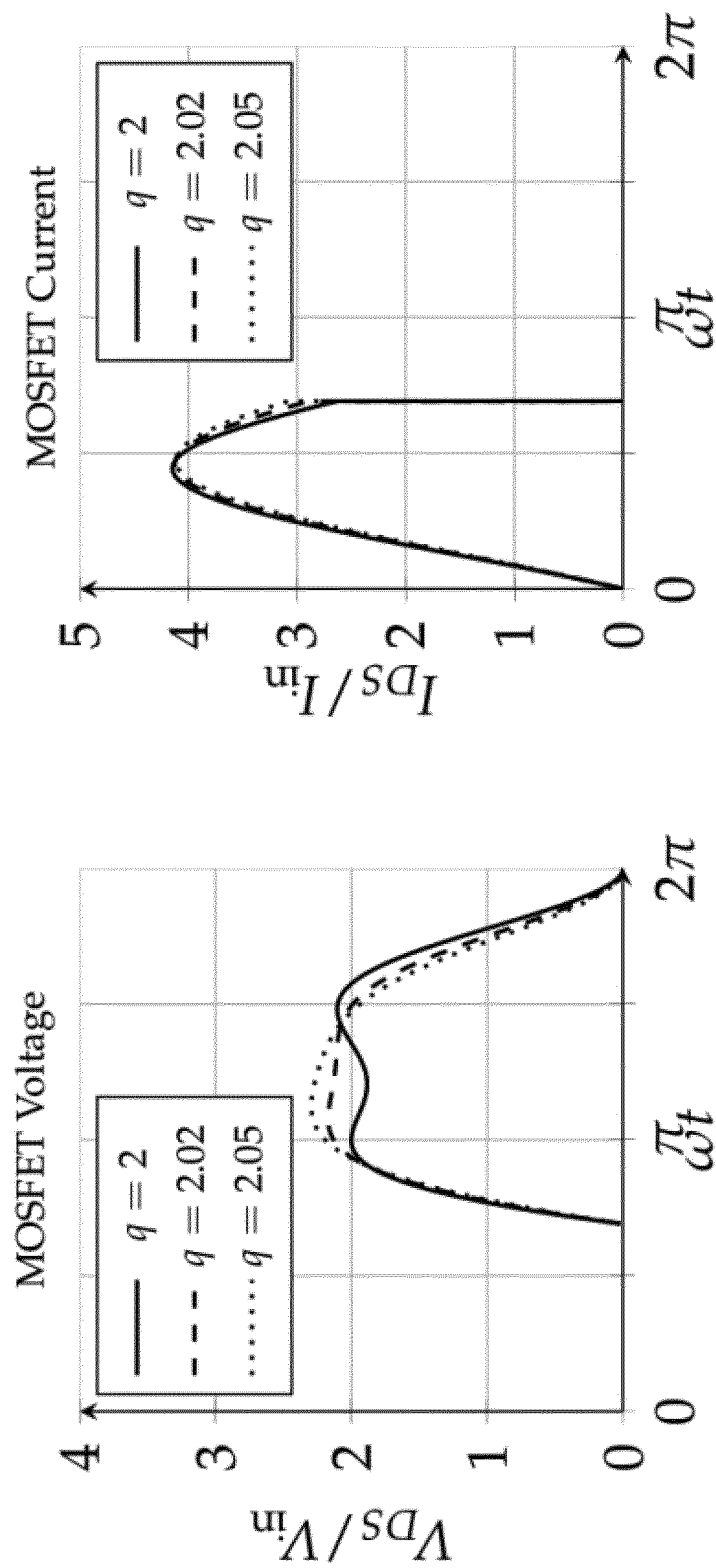


FIG. 35

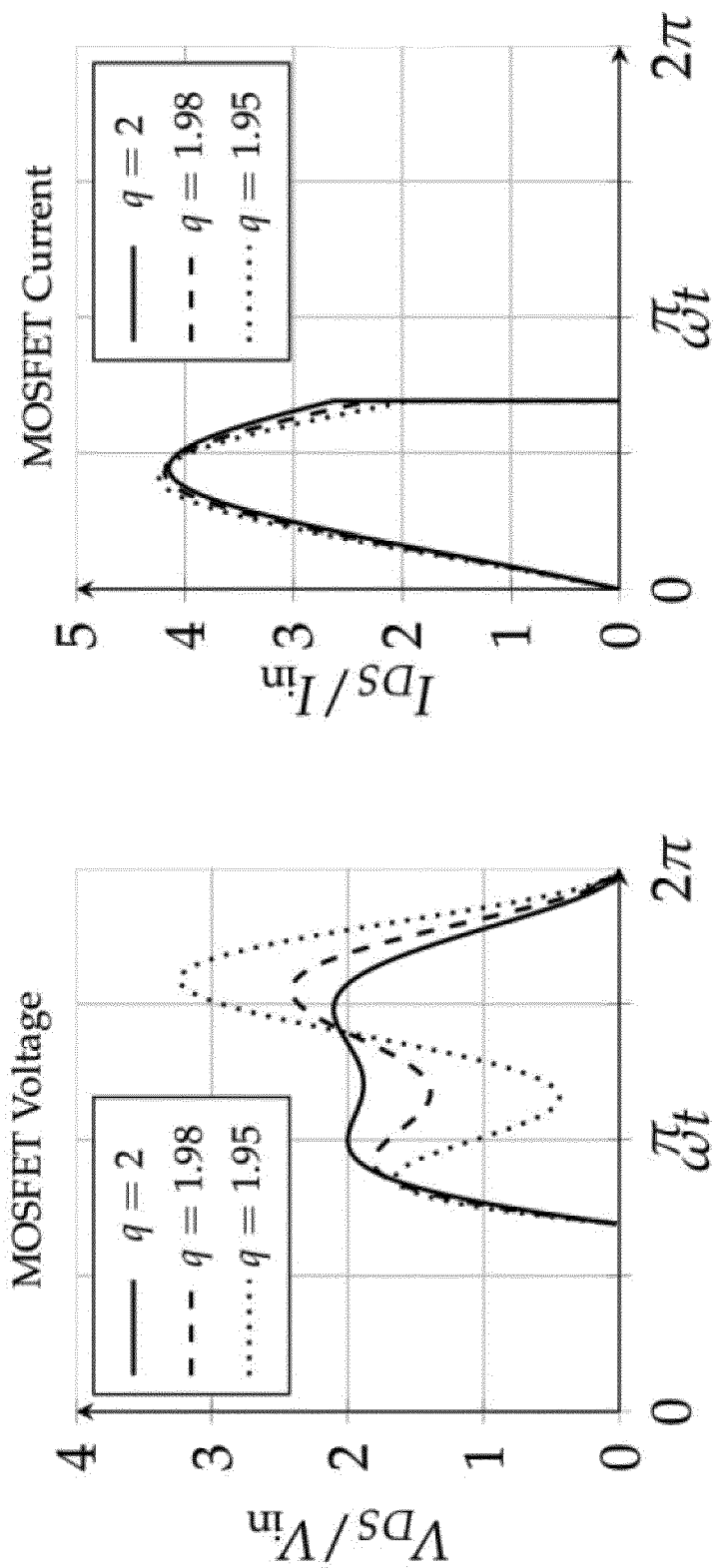


FIG. 36

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/052154

A. CLASSIFICATION OF SUBJECT MATTER INV. H02M7/537 H02M7/5383 H03F3/217 H02M3/335 H02J5/00 H02M7/48 ADD. According to International Patent Classification (IPC) or to both national classification and IPC											
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H02M H02J H03F Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) EPO-Internal, WPI Data											
C. DOCUMENTS CONSIDERED TO BE RELEVANT <table border="1"> <thead> <tr> <th>Category*</th> <th>Citation of document, with indication, where appropriate, of the relevant passages</th> <th>Relevant to claim No.</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>GB 2 505 278 A (IMP INNOVATIONS LTD [GB]) 26 February 2014 (2014-02-26) abstract paragraphs [0036], [0037]; figure 8 -----</td> <td>1-25</td> </tr> <tr> <td>A</td> <td>WO 2013/014521 A1 (TOYOTA MOTOR CO LTD [JP]; NIPPON SOKEN [JP]; SAKAKIBARA HIROYUKI [JP];) 31 January 2013 (2013-01-31) paragraphs [0050] - [0062]; figure 3 -----</td> <td>1-25</td> </tr> </tbody> </table>			Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	A	GB 2 505 278 A (IMP INNOVATIONS LTD [GB]) 26 February 2014 (2014-02-26) abstract paragraphs [0036], [0037]; figure 8 -----	1-25	A	WO 2013/014521 A1 (TOYOTA MOTOR CO LTD [JP]; NIPPON SOKEN [JP]; SAKAKIBARA HIROYUKI [JP];) 31 January 2013 (2013-01-31) paragraphs [0050] - [0062]; figure 3 -----	1-25
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.									
A	GB 2 505 278 A (IMP INNOVATIONS LTD [GB]) 26 February 2014 (2014-02-26) abstract paragraphs [0036], [0037]; figure 8 -----	1-25									
A	WO 2013/014521 A1 (TOYOTA MOTOR CO LTD [JP]; NIPPON SOKEN [JP]; SAKAKIBARA HIROYUKI [JP];) 31 January 2013 (2013-01-31) paragraphs [0050] - [0062]; figure 3 -----	1-25									
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2016/052154

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