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(56) Documents Cited:
US 6440810 B **US 20050073026 A**
US 20040082135 A

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Other: **EPODOC, WPI**

(54) Abstract Title: **Improvements in transistor manufacture**

(57) An oxide layer is formed on material defining and surrounding an emitter window. The technique comprises depositing a non-conformal oxide layer on the surrounding material and in the emitter window, whereby the thickness of at least a portion of the oxide layer in the emitter window is smaller than the thickness of the oxide layer on the surrounding material outside the emitter window; and removing at least a portion of the oxide layer in the emitter window so as to reveal at least a portion of the bottom of the emitter window whilst permitting at least a portion of the oxide layer to remain on the surrounding material. The technique can be used in the manufacture of a self aligned epitaxial base BJT (bipolar junction transistor) or SiGe HBT (hetero junction bipolar transistor).

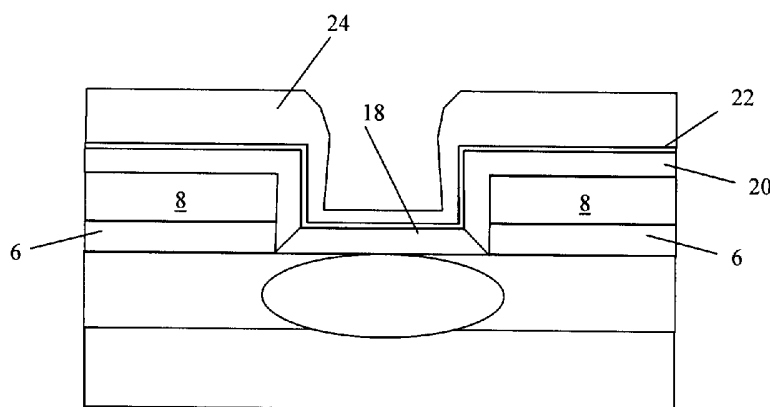


Fig. 6

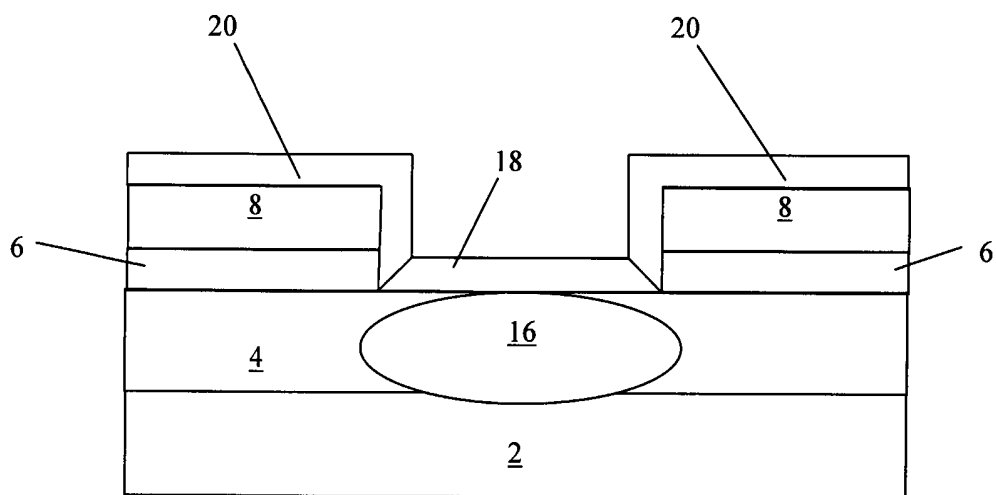


Fig. 4

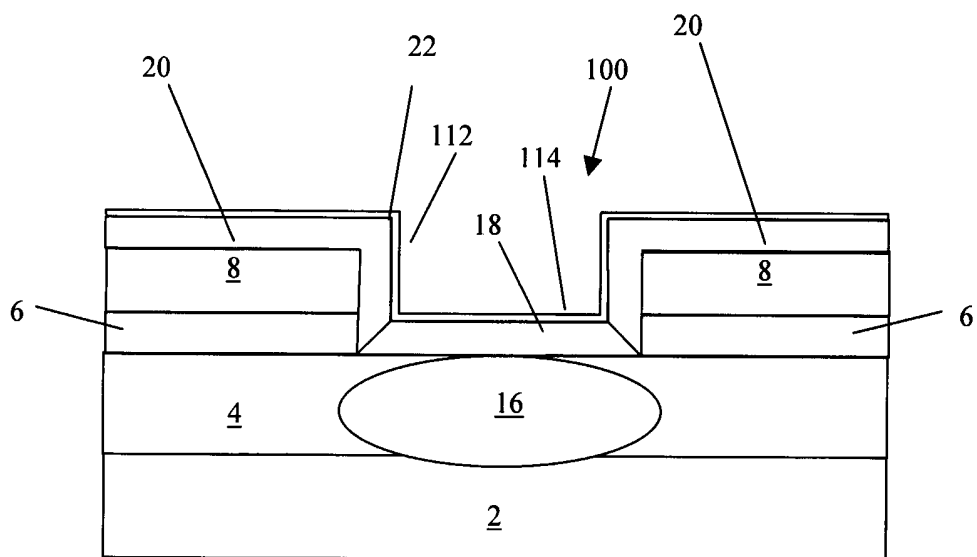


Fig. 5

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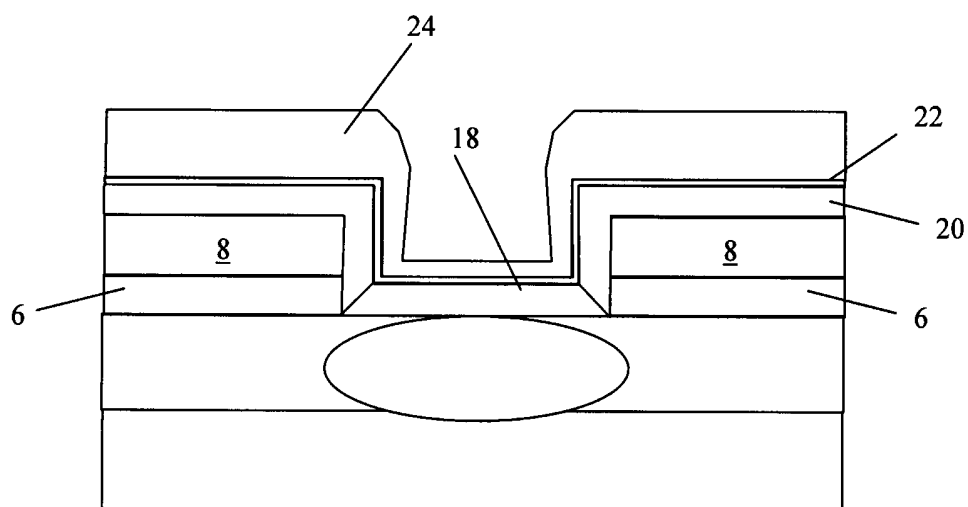


Fig. 6

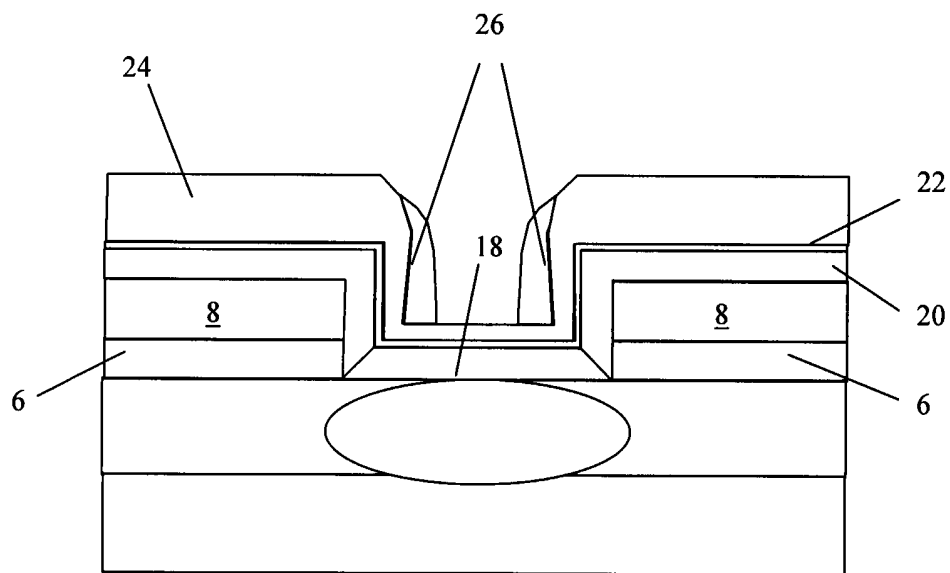


Fig. 7

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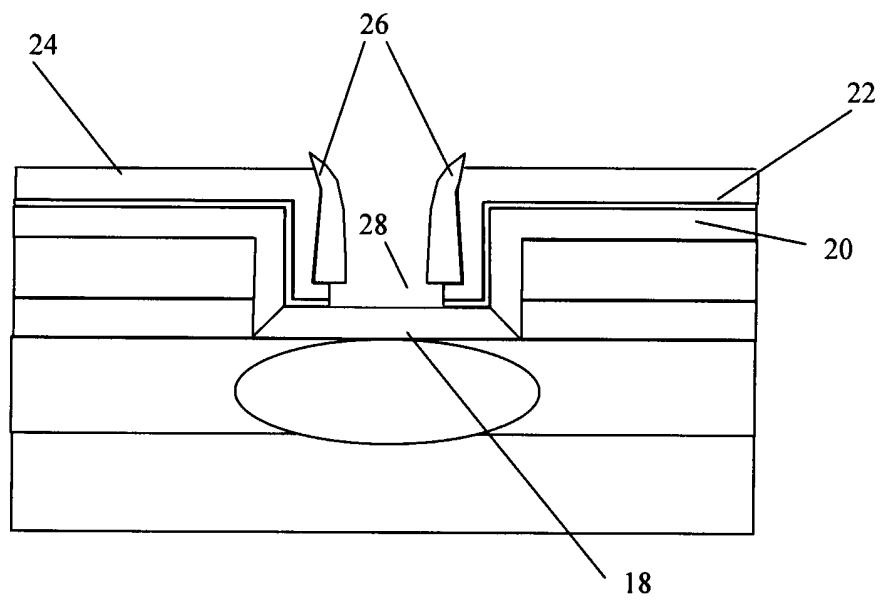


Fig. 8

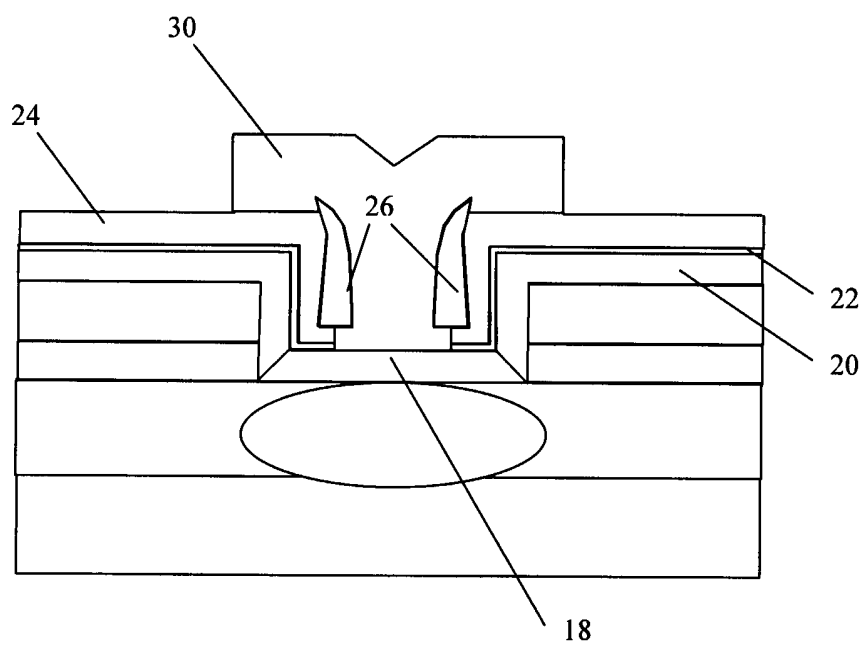


Fig. 9

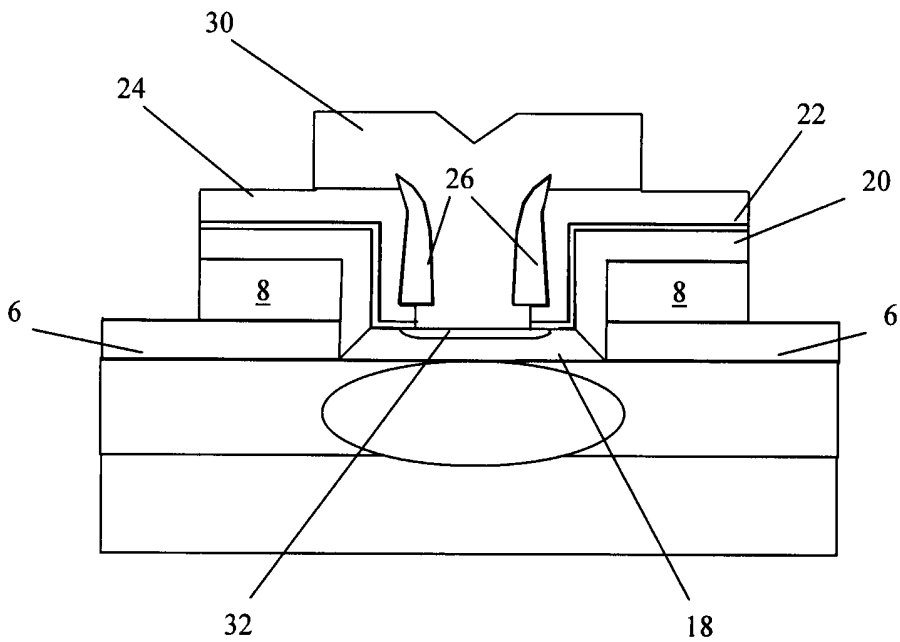


Fig. 10

Improvements in Transistor Manufacture

The present invention relates to improvements in transistor manufacture. The invention finds particular application in the manufacture of a bipolar junction transistor (BJT) or a hetero junction bipolar transistor (HBT). Whilst not limited thereto, the invention is particularly useful in the manufacture of a self-aligned epitaxial base BJT or SiGe HBT.

In some transistor manufacturing processes an emitter window is formed, and it is then desired to form an oxide layer on material surrounding the emitter window, whilst it is also desired that the bottom of the emitter window is not covered by the oxide layer. Complicated processes are known in the art which aim to achieve this.

The present inventor has devised a novel method of providing an oxide layer on material surrounding an emitter window whilst ensuring that at least a portion of the bottom of the emitter window is not covered by the oxide layer.

One or more aspect(s) is/are set out in the independent claim(s).

A preferred embodiment of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1 shows a first step of a processing sequence according to an embodiment of the invention.

Figure 2 shows a second step of a processing sequence according to an embodiment of the invention.

Figure 3 shows a third step of a processing sequence according to an embodiment of the invention.

Figure 4 shows a fourth step of a processing sequence according to an embodiment of the invention.

Figure 5 shows a fifth step of a processing sequence according to an embodiment of the invention.

Figure 6 shows a sixth step of a processing sequence according to an embodiment of the invention.

Figure 7 shows a seventh step of a processing sequence according to an embodiment of the invention.

Figure 8 shows an eighth step of a processing sequence according to an embodiment of the invention.

5 Figure 9 shows a ninth step of a processing sequence according to an embodiment of the invention.

Figure 10 shows a tenth step of a processing sequence according to an embodiment of the invention.

10 The principle of the present invention will now be illustrated with reference to the manufacture of a self-aligned epitaxial base BJT, but it will be understood that the invention is not limited thereto.

As shown in figure 1, a heavily doped n+ buried layer 2, which serves as the sub-collector, is provided. A n-type Si epitaxial layer 4, which acts as a collector, is grown
15 on the heavily doped n+ buried layer 2.

As shown in figure 2, silicon oxide is deposited so as to form a pad oxide layer 6 on the n-type Si epitaxial layer 4. Subsequently a poly Si layer 8 is deposited on pad oxide
20 layer 6, which poly Si layer 8 is then p-type heavily doped by high dose ion implantation.

As shown in figure 3, an opening 10 is etched into the p+ poly Si layer 8 and pad oxide layer 6. The opening 10 can be generally of rectangular cross section as shown in figure
25 3, with side walls 12 and bottom portion 14. Other geometries are also possible. A SIC 16 (selectively ion-implanted collector) is then formed primarily in n-type Si-epitaxial layer 4 by ion implantation through the opening 10.

As shown in figure 4, a Si epitaxial layer 18 is then grown on the bottom portion 14 of
30 the opening 10 so as to form a base material. A corresponding polycrystalline layer 20 is also deposited on top of poly Si layer 8 and on side wall 12 formed by the poly Si layer 8 and the pad oxide layer 6. As a result of subsequent thermal cycles, the

polycrystalline layer 20 will be p-type heavily doped by dopant-diffusion from poly Si layer 8. Eventually, layers 20 and 8 will constitute an extrinsic base layer.

As shown in figure 5, a thin silicon oxide layer 22 is then thermally grown on Si epitaxial layer 18 and extrinsic base layer 20 so as to form a surface passivation layer.

The opening resulting after the forming of oxide layer 22 will be referred to as emitter window 100. This has a bottom portion 114 and side walls 112, as shown in figure 5.

As shown in figure 6, an intentionally non-conformal silicon oxide cap layer 24 is then deposited on surface passivation layer 22 so as to form a dielectric layer inside the emitter window 100 and on the material surrounding the emitter window. This dielectric layer 24 is thinner inside the emitter window than outside the emitter window. Preferably, at least over a portion of the bottom 114 of the emitter window 100 the dielectric layer is thinner than outside the emitter window. Preferably, the dielectric layer 24 is thinner substantially over the entire bottom portion 114 of the emitter window than over the material (immediately) surrounding the emitter window.

A technique of non-conformal coverage of a step with an SiO₂ film has been disclosed on pages 185 – 187 of “Silicon Processing for the VLSI Era”, Volume 1: Process Technology, by S. Wolf and R. N. Tauber, Lattice Press, Post Office Box 340, Sunset Beach, California 90742, USA. This technique can be applied to the present invention, subject to any necessary modifications, which will be clear to one skilled in the art.

Preferably, the oxide cap layer 24 is about 50 to 300% thicker outside the emitter window than inside the emitter window. More preferably, the oxide cap layer 24 is about 100 to 200% thicker outside the emitter window than inside the emitter window. For example, the thickness of oxide cap layer 24 at the bottom of the emitter window may be 100nm and outside the emitter window the thickness may be 200-300nm when cap layer 24 has been deposited.

As shown in figure 7, nitride side wall spacers 26 are then created along the side walls 112 of the emitter window 100. This can be achieved by depositing a nitride layer and subsequently performing an etch-back.

- 5 As shown in figure 8, a HF wet etch is then carried out. This removes the cap oxide layer 24 and surface passivation layer 22 at least at a central portion 28 of the emitter window 100, i.e. where, due to the non-conformality, the silicon oxide cap layer 24 is thinner than in other regions. During this HF wet etch the silicon oxide cap layer 24 is also etched outside the emitter window, i.e. on the material surrounding the emitter
- 10 window, but a sufficiently thick portion of the cap oxide layer 24 remains on top of the p⁺ polycrystalline layer 20. Preferably the HF wet etch is stopped as soon as substantially all of the silicon oxide cap layer 24 and surface passivation layer 22 has been removed between the nitride side wall spacers, although the HF wet etch may also continue until a small portion of surface passivation layer 22 and silicon oxide cap layer
- 15 24 has been removed from “under” the nitride side wall spacers. As shown in figure 8, a structure results which has the Si epitaxial layer 18 exposed (at least partially) and which is formed with a sufficiently thick cap oxide layer 24 and surface passivation layer 22 outside the emitter window 100. Preferably, the combined thickness of cap oxide layer 24 and passivation layer 22 remaining outside the emitter window 100 is at
- 20 least 50nm, preferably 50-150nm, more preferably 80-120nm and most preferably about 100nm.

Preferably, the etch rate in the emitter window 100 is the same as outside the emitter window.

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- As shown in figure 9, the emitter poly 30 is then deposited, doped (in this example it is heavily n⁺ doped in situ during deposition) and patterned. The doping could alternatively be carried out by ion implant. Due to the oxide/nitride side wall spacers (note that now part of oxide layer 24 and passivation layer 22 can be regarded as
- 30 forming part of the (oxide/nitride) side wall spacers) and the sufficiently thick cap oxide layer 24 remaining between the emitter poly material 30 and the extrinsic base poly material 20 and 8 it is possible to keep the emitter-base capacitances sufficiently low.

As shown in figure 10, the p⁺ extrinsic base poly layer 8 is patterned, and this is followed by an emitter drive-in anneal. This results in dopant out-diffusion from the emitter poly 30, which in turn results in the formation of an intrinsic emitter 32, at the bottom portion of emitter window 100. The p⁺ extrinsic base 20 and 8 is spaced from the emitter edge by means of the oxide/nitride side wall spacer in a self-aligned manner. The spacing is preferably chosen relatively small so that extrinsic base resistances are kept small. However, the spacing is preferably chosen large enough so that breakdown and leakage between emitter and extrinsic base is avoided.

- 10 Finally, the manufacture of the self-aligned epitaxial base BJT is completed by conventional backend processes, including the forming of contacts and vias, and metallisation steps.

The invention is also applicable to the manufacture of a HBT, such as a SiGe HBT. In this case the epitaxial layer 18 which is grown as base material (see figure 4) is a Si/SiGe/Si epitaxial stack layer.

Whilst in the specific description reference has been made to a NPN BJT, the invention is also applicable to a PNP BJT. Any necessary modifications will be clear to one skilled in the art.

Whilst in the above detailed description of a preferred embodiment it is stated that the opening shown in figure 5 is an emitter window it will be appreciated that an emitter window can be formed by processes other than the technique described with reference to figures 1 to 5. It will further be appreciated that during the wet etch shown in figure 8 the emitter window 100 changes in form. Nevertheless, the opening shown in figure 8 is still to be regarded as an emitter window, and it is intended that the term "emitter window" as used in the claims will be interpreted in a similarly "flexible" manner.

30 Although the invention has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure which are

contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

CLAIMS:

1. A method of forming an oxide layer on material defining and surrounding an emitter window, comprising:
 - 5 depositing a non-conformal oxide layer on said surrounding material and in said emitter window, whereby the thickness of at least a portion of the oxide layer in the emitter window is smaller than the thickness of the oxide layer on said surrounding material outside said emitter window; and
 - removing at least a portion of said oxide layer in said emitter window so as to
10 reveal at least a portion of the bottom of said emitter window whilst permitting at least a portion of said oxide layer to remain on said surrounding material.
2. A method according to claim 1, wherein after deposition of the oxide layer the
15 thickness of the oxide layer over at least a portion of the bottom of the emitter window is smaller than the thickness of the oxide layer on said surrounding material.
3. A method according to claim 2, wherein the thickness of the oxide layer over
substantially the entire bottom of the emitter window is smaller than the thickness of the
oxide layer on said surrounding material.
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4. A method according to any of claims 1 to 3, wherein after deposition of the
oxide layer the thickness of the oxide layer on said surrounding material is 50 to 300%,
preferably 100 to 200%, greater than the thickness of the oxide layer over said portion
of the bottom of the emitter window.
25
5. A method according to any of claims 1 to 4, wherein the thickness of the oxide
layer over said portion of the bottom of the emitter window is between 50 and 150nm,
preferably 80 to 120nm and more preferably about 100nm.
- 30 6. A method according to any of claims 1 to 5, wherein after deposition of the
oxide layer the thickness of the oxide layer on said surrounding material is between 200
and 300nm.

7. A method according to any of claims 1 to 6, wherein after removal of said portion of said oxide layer in said emitter window the thickness of the oxide layer remaining on said surrounding material is at least 50nm, preferably 50 to 150nm, more preferably 80 to 120nm and most preferably about 100nm.

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8. A method according to any of claims 1 to 7, wherein removing at least said portion of said oxide layer in the emitter window comprises etching said oxide layer, preferably HF wet etching said oxide layer.

10 9. A method according to any of claims 1 to 8, further comprising forming at least one nitride side wall spacer in said emitter window.

10. A method according to claim 9, comprising forming two nitride side wall spacers in said emitter window, and wherein removing at least said portion of said oxide
15 layer in said emitter window comprises removing substantially all of said oxide layer over an area of said bottom of said emitter window which is not covered by said nitride side wall spacers.

11. A method according to any of claims 1 to 10, further comprising forming at least
20 a portion of an emitter in said emitter window.

12. A method according to any of claims 1 to 11, wherein said oxide layer comprises a silicon oxide layer.

25 13. A method according to any of claims 1 to 12, comprising also removing a portion of the oxide layer on said surrounding material at substantially the same rate at which the oxide layer in said emitter window is removed.

14. Use of a method according to any of claims 1 to 13 in the manufacture of a
30 bipolar junction transistor or a hetero junction bipolar transistor, preferably a self-aligned epitaxial base bipolar junction transistor or SiGe hetero junction bipolar transistor.

15. A method or a use, substantially as herein described, with reference to, or as illustrated in, the accompanying drawings.



INVESTOR IN PEOPLE

Application No: GB0507772.2

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Examiner: Ms Anna Brandon

Claims searched: 1 to 15

Date of search: 16 August 2005

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	none	US2005/073026 A (LOJEK)
A	none	US2004/082135 A (UNITED MICROELECTRONICS)
A	none	US6440810 B (ERICSSON TELEFON)

Categories:

X Document indicating lack of novelty or inventive step	A Document indicating technological background and/or state of the art.
Y Document indicating lack of inventive step if combined with one or more other documents of same category.	P Document published on or after the declared priority date but before the filing date of this invention.
& Member of the same patent family	E Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^X:

H1K

Worldwide search of patent documents classified in the following areas of the IPC⁰⁷

H01L

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI