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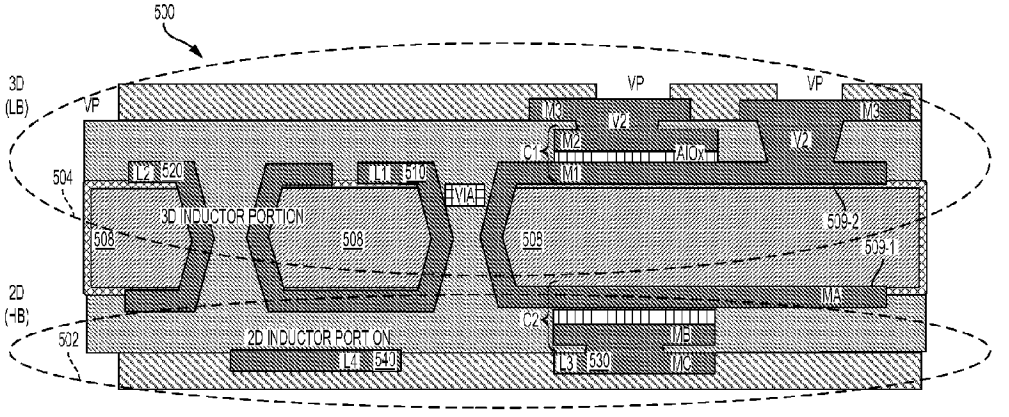

(57) Abrégé/Abstract:
A multiplexer structure (500) includes a passive substrate (508). The multiplexer structure (500) may also include a high band filter (502) on the passive substrate. The high band filter (502) may include a 2D planar spiral inductor(s) (530, 540) on the passive substrate. The multiplexer structure (500) may further include a low band filter (504) on the passive substrate. The low band filter (504) may include a 3D through-substrate inductor (510, 520) and a first capacitor(s) on the passive substrate. The multiplexer structure (500) may also include a through substrate via(s) (VIA) coupling the high band filter (502) and the low band filter (504).

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(54) **Title**: MULTIPLEXER DESIGN USING A 2D PASSIVE ON GLASS FILTER INTEGRATED WITH A 3D THROUGH GLASS VIA FILTER

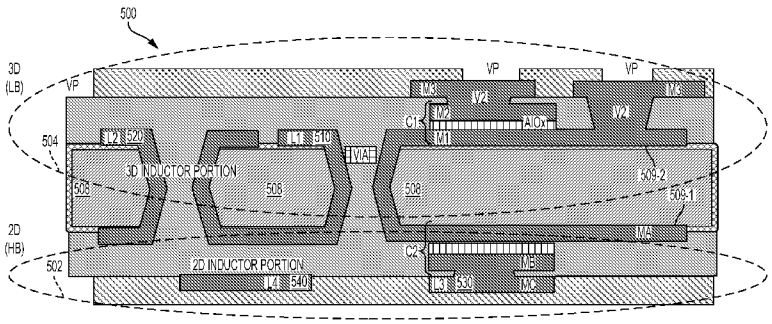

FIG. 5A

(57) **Abstract**: A multiplexer structure (500) includes a passive substrate (508). The multiplexer structure (500) may also include a high band filter (502) on the passive substrate. The high band filter (502) may include a 2D planar spiral inductor(s) (530, 540) on the passive substrate. The multiplexer structure (500) may further include a low band filter (504) on the passive substrate. The low band filter (504) may include a 3D through-substrate inductor (510, 520) and a first capacitor(s) on the passive substrate. The multiplexer structure (500) may also include a through substrate via(s) (VIA) coupling the high band filter (502) and the low band filter (504).

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MULTIPLEXER DESIGN USING A 2D PASSIVE ON GLASS FILTER INTEGRATED WITH A 3D THROUGH GLASS VIA FILTER

[0001]

TECHNICAL FIELD

[0002] The present disclosure generally relates to integrated circuits (ICs). More specifically, the present disclosure relates to multiplexer design using a 2D passive on glass (POG) filter integrated with a 3D through glass via (TGV) filter.

BACKGROUND

[0003] For wireless communication, a diplexer can help process signals carried in a carrier aggregation system. In carrier aggregation systems, signals are communicated with both high band and low band frequencies. In a chipset, the diplexer is usually inserted between an antenna and a tuner (or a radio frequency (RF) switch) to ensure high performance. Usually, a diplexer design includes inductors and capacitors. Diplexers can attain high performance by using inductors and capacitors that have a high quality factor (or high Q-factor). High performance diplexers can also be attained by reducing the electromagnetic coupling between components, which may be achieved through an arrangement of the geometry and direction of the components. Diplexer performance may be quantified by measuring the insertion loss and rejection (e.g., quantities expressed in decibels (dB)) at certain frequencies.

[0004] The diplexer fabrication process may be compatible with standard semiconductor processes, such as processes for fabricating voltage-controlled capacitors (varactors), switched-array capacitors, or other like capacitors. It may be beneficial to fabricate the components of the diplexer design on a single substrate. Fabrication on a single substrate may also enable tunable diplexers that are tuned through a variety of different parameters.

[0005] Fabricating high performance diplexers in an efficient and cost-effective manner is problematic. Increasing the Q of the inductors and the capacitors in the diplexer is also an issue. Reducing the electromagnetic coupling between the various components in the diplexer, while decreasing the size of the diplexer and making the most economical use of resources, would be beneficial.

SUMMARY

[0006] A multiplexer structure includes a passive substrate. The multiplexer structure may also include a high band filter on the passive substrate. The high band filter may include a 2D planar spiral inductor(s) on the passive substrate. The multiplexer structure may further include a low band filter on the passive substrate. The low band filter may include a 3D through-substrate inductor and a first capacitor(s) on the passive substrate. The multiplexer structure may also include a through substrate via(s) coupling the high band filter and the low band filter.

[0007] A method of constructing a multiplexer structure from a passive substrate panel may include fabricating a high band filter on the passive substrate panel. The high band filter may include a 2D planar spiral inductor(s) on the passive substrate panel. The method may also include fabricating a low band filter on the passive substrate panel. The low band filter may include a 3D through-substrate inductor and a first capacitor(s) on the passive substrate panel. The method may further include fabricating a via through the passive substrate panel coupling the high band filter and the low band filter.

[0008] A multiplexer structure includes a passive substrate. The multiplexer structure may also include a high band filter on the passive substrate. The high band filter may include a 2D planar spiral inductor(s) on the passive substrate. The multiplexer structure may further include a low band filter on the passive substrate. The low band filter may include a 3D through-substrate inductor and a first capacitor(s) on the passive substrate. The multiplexer structure may also include means for coupling the high band filter and the low band filter.

[0009] A radio frequency (RF) front end module may include a multiplexer structure. The multiplexer structure may include a high band filter on a passive substrate. The high band filter may include a 2D planar spiral inductor(s) on the passive

substrate. The multiplexer structure may also include a low band filter on the passive substrate. The low band filter may include a 3D through-substrate inductor and a first capacitor(s) on the passive substrate. The multiplexer structure may further include a through substrate via(s) coupling the high band filter and the low band filter. The RF front end module may also include an antenna coupled to an output of the multiplexer structure.

[0010] This has outlined, rather broadly, the features and technical advantages of the present disclosure in order that the detailed description that follows may be better understood. Additional features and advantages of the disclosure will be described below. It should be appreciated by those skilled in the art that this disclosure may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the teachings of the disclosure as set forth in the appended claims. The novel features, which are believed to be characteristic of the disclosure, both as to its organization and method of operation, together with further objects and advantages, will be better understood from the following description when considered in connection with the accompanying figures. It is to be expressly understood, however, that each of the figures is provided for the purpose of illustration and description only and is not intended as a definition of the limits of the present disclosure.

[0010a] According to one aspect of the present invention, there is provided a method of constructing a multiplexer structure from a passive substrate panel, comprising: fabricating a high band filter on the passive substrate panel, the high band filter including at least a 2D planar spiral inductor on a first side of the passive substrate panel; fabricating a low band filter on the passive substrate panel, the low band filter including a 3D through-substrate inductor and at least one first capacitor, the at least one first capacitor being formed on a second side of the passive substrate panel, opposite the first side; and fabricating a via through the passive substrate panel coupling the high band filter and the low band filter through the passive substrate panel.

[0010b] According to another aspect of the present invention, there is provided a multiplexer structure, comprising: a passive substrate; a high band filter on the passive substrate, the high band filter including at least a 2D planar spiral inductor on a first side of the passive substrate; a low band filter on the passive substrate, the low band filter including a 3D through-substrate inductor and at least one first capacitor, the at least one first capacitor being formed on a second side of the passive substrate, opposite the first side; and means for coupling the high band filter and the low band filter through the passive substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] For a more complete understanding of the present disclosure, reference is now made to the following description taken in conjunction with the accompanying drawings.

[0012] FIGURE 1A is a schematic diagram of a radio frequency (RF) front end (RFFE) module employing a diplexer according to an aspect of the present disclosure.

[0013] FIGURE 1B is a schematic diagram of a radio frequency (RF) front end (RFFE) module and a WiFi module employing diplexers for a chipset to provide carrier aggregation according to aspects of the present disclosure.

[0014] FIGURE 2A is a schematic diagram of a diplexer design according to an aspect of the present disclosure.

[0015] FIGURE 2B is a graph illustrating performance of the diplexer design of FIGURE 2A according to an aspect of the present disclosure.

[0016] FIGURE 2C is a diagram further illustrating the diplexer design of FIGURE 2A according to an aspect of the present disclosure.

[0017] FIGURE 3A is a top view of a layout of a diplexer design according to an aspect of the present disclosure.

[0018] FIGURE 3B shows a cross section view of the diplexer design of FIGURE 3A according to aspects of the present disclosure.

[0019] FIGURE 4A is a top view of a layout of a diplexer design according to an aspect of the present disclosure.

[0020] FIGURE 4B shows a cross section view of the diplexer design of FIGURE 4A according to aspects of the present disclosure.

[0021] FIGURE 5A illustrates a multiplexer structure using a 2D filter integrated with a 3D filter for a high quality (Q)-factor radio frequency (RF) application according to aspects of the present disclosure.

[0022] FIGURE 5B illustrates a top view of components of the multiplexer structure of FIGURE 5A, including a 2D filter integrated with a 3D filter for high quality (Q)-factor radio frequency (RF) applications according to aspects of the present disclosure.

[0023] FIGURE 6 is a process flow diagram illustrating a method of making a multiplexer structure according to aspects of the present disclosure.

[0024] FIGURE 7 is a block diagram showing an exemplary wireless communication system in which a configuration of the disclosure may be advantageously employed.

[0025] FIGURE 8 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component according to one configuration.

DETAILED DESCRIPTION

[0026] The detailed description set forth below, in connection with the appended drawings, is intended as a description of various configurations and is not intended to represent the only configurations in which the concepts described herein may be practiced. The detailed description includes specific details for the purpose of providing a thorough understanding of the various concepts. However, it will be apparent to those skilled in the art that these concepts may be practiced without these specific details. In some instances, well-known structures and components are shown in block diagram form in order to avoid obscuring such concepts. As described herein, the use of the term "and/or" is intended to represent an "inclusive OR", and the use of the term "or" is intended to represent an "exclusive OR".

[0027] Mobile radio frequency (RF) chip designs (e.g., mobile RF transceivers) have migrated to a deep sub-micron process node due to cost and power consumption considerations. The design complexity of mobile RF transceivers is further complicated by added circuit functions to support communication enhancements, such as carrier aggregation. Further design challenges for mobile RF transceivers include analog/RF performance considerations, including mismatch, noise and other performance considerations. The design of these mobile RF transceivers includes the use of passive devices, for example, to suppress resonance, and/or to perform filtering, bypassing and coupling.

[0028] Successful fabrication of modern semiconductor chip products involves interplay between the materials and the processes employed. In particular, the formation of conductive material plating for the semiconductor fabrication in the back-end-of-line (BEOL) processes is an increasingly challenging part of the process flow. This is particularly true in terms of maintaining a small feature size. The same challenge of maintaining a small feature size also applies to passive on glass (POG) technology, where high performance components such as inductors and capacitors are built upon a highly insulative substrate that may also have a very low loss.

[0029] Passive on glass devices involve high performance inductor and capacitor components that have a variety of advantages over other technologies, such as surface mount technology or multi-layer ceramic chips. These advantages include being more compact in size and having smaller manufacturing variations. Passive on glass devices also involve a higher quality (Q)-factor value that meets stringent low insertion loss and low power consumption specifications. Devices such as inductors may be implemented as 3D structures with passive on glass technologies. 3D through substrate inductors or other 3D devices may also experience a number of design constraints due to their 3D implementation.

[0030] An inductor is an example of an electrical device used to temporarily store energy in a magnetic field within a wire coil according to an inductance value. This inductance value provides a measure of the ratio of voltage to the rate of change of current passing through the inductor. When the current flowing through an inductor changes, energy is temporarily stored in a magnetic field in the coil. In addition to their magnetic field storing capability, inductors are often used in alternating current (AC) electronic equipment, such as radio equipment. For example, the design of mobile RF transceivers includes the use of inductors with improved inductance density while reducing magnetic loss at high frequency.

[0031] Various aspects of the disclosure provide techniques for fabrication of multiplexers using 2D passive on glass (POG) filters integrated with 3D through glass via (TGV) filters. The process flow for semiconductor fabrication of the multiplexer structure may include front-end-of-line (FEOL) processes, middle-of-line (MOL) processes, and back-end-of-line (BEOL) processes. It will be understood that the term "layer" includes film and is not to be construed as indicating a vertical or horizontal thickness unless otherwise stated. As described herein, the term "substrate" may refer to a substrate of a diced wafer or may refer to a substrate of a wafer that is not diced. Similarly, the terms chip and die may be used interchangeably unless such interchanging would tax credulity.

[0032] As described herein, the back-end-of-line interconnect layers may refer to the conductive interconnect layers (e.g., metal one (M1), metal two (M2), metal three (M3), etc.) for electrically coupling to front-end-of-line active devices of an integrated circuit. The back-end-of-line interconnect layers may electrically couple to middle-of-

line interconnect layers for, for example, connecting M1 to an oxide diffusion (OD) layer of an integrated circuit. A back-end-of-line first via (V2) may connect M2 to M3 or others of the back-end-of-line interconnect layers.

[0033] Aspects of the present disclosure describe multiplexers using 2D passive on glass (POG) filters integrated with 3D through glass via (TGV) filters for high quality (Q)-factor radio frequency (RF) applications. In one arrangement, a multiplexer structure includes a high band (HB) filter on a passive substrate. The high band filter includes a 2D spiral inductor on the passive substrate. The multiplexer structure also includes a low band (LB) filter on the passive substrate. The low band filter includes a 3D inductor and a first capacitor on the passive substrate. The multiplexer structure further includes at least one through substrate via coupling the high band filter and the low band filter. In one aspect of the present disclosure, the high band filter and the low band filter are arranged on opposing surfaces of a glass substrate to provide a two-sided multiplexer structure. In this arrangement, the high band filter includes a second capacitor on a first surface of the passive substrate. Alternatively, the high band filter and the low band filter may share the first capacitor on a second surface of the passive substrate opposite the first surface.

[0034] FIGURE 1A is a schematic diagram of a radio frequency (RF) front end (RFFE) module 100 employing a diplexer 200 according to an aspect of the present disclosure. The RF front end module 100 includes power amplifiers 102, duplexer/filters 104, and a radio frequency (RF) switch module 106. The power amplifiers 102 amplify signal(s) to a certain power level for transmission. The duplexer/filter 104 filters the input/output signals according to a variety of different parameters, including frequency, insertion loss, rejection or other like parameters. In addition, the RF switch module 106 may select certain portions of the input signals to pass on to the rest of the RF front end module 100.

[0035] The RF front end module 100 also includes tuner circuitry 112 (e.g., first tuner circuitry 112A and second tuner circuitry 112B), the diplexer 200, a capacitor 116, an inductor 118, a ground terminal 115 and an antenna 114. The tuner circuitry 112 (e.g., the first tuner circuitry 112A and the second tuner circuitry 112B) includes components such as a tuner, a portable data entry terminal (PDET), and a house keeping analog to digital converter (HKADC). The tuner circuitry 112 may perform impedance

tuning (e.g., a voltage standing wave ratio (VSWR) optimization) for the antenna 114. The RF front end module 100 also includes a passive combiner 108 coupled to a wireless transceiver (WTR) 120. The passive combiner 108 combines the detected power from the first tuner circuitry 112A and the second tuner circuitry 112B. The wireless transceiver 120 processes the information from the passive combiner 108 and provides this information to a modem 130 (e.g., a mobile station modem (MSM)). The modem 130 provides a digital signal to an application processor (AP) 140.

[0036] As shown in FIGURE 1A, the diplexer 200 is between the tuner component of the tuner circuitry 112 and the capacitor 116, the inductor 118, and the antenna 114. The diplexer 200 may be placed between the antenna 114 and the tuner circuitry 112 to provide high system performance from the RF front end module 100 to a chipset including the wireless transceiver 120, the modem 130 and the application processor 140. The diplexer 200 also performs frequency domain multiplexing on both high band frequencies and low band frequencies. After the diplexer 200 performs its frequency multiplexing functions on the input signals, the output of the diplexer 200 is fed to an optional LC (inductor/capacitor) network including the capacitor 116 and the inductor 118. The LC network may provide extra impedance matching components for the antenna 114, when desired. Then a signal with the particular frequency is transmitted or received by the antenna 114. Although a single capacitor and inductor are shown, multiple components are also contemplated.

[0037] FIGURE 1B is a schematic diagram of a WiFi module 170 including a first diplexer 200-1 and an RF front end module 150 including a second diplexer 200-2 for a chipset 160 to provide carrier aggregation according to an aspect of the present disclosure. The WiFi module 170 includes the first diplexer 200-1 communicably coupling an antenna 192 to a wireless local area network module (e.g., WLAN module 172). The RF front end module 150 includes the second diplexer 200-2 communicably coupling an antenna 194 to the wireless transceiver (WTR) 120 through a duplexer 180. The wireless transceiver 120 and the WLAN module 172 of the WiFi module 170 are coupled to a modem (MSM, e.g., baseband modem) 130 that is powered by a power supply 152 through a power management integrated circuit (PMIC) 156. The chipset 160 also includes capacitors 162 and 164, as well as an inductor(s) 166 to provide signal integrity. The PMIC 156, the modem 130, the wireless transceiver 120, and the WLAN

module 172 each include capacitors (e.g., 158, 132, 122, and 174) and operate according to a clock 154. The geometry and arrangement of the various inductor and capacitor components in the chipset 160 may reduce the electromagnetic coupling between the components.

[0038] FIGURE 2A is a schematic diagram of a diplexer 200 according to an aspect of the present disclosure. The diplexer 200 includes a high band (HB) input port 202, a low band (LB) input port 204, and an antenna 206. A high band path of the diplexer 200 includes an input capacitor 218 (C5) and a first parallel coupled capacitor 242 (C2) with a fourth inductor 240 (L4). The high band path also includes a second capacitor 216 (C4) and a second parallel coupled capacitor 232 (C3) with a third inductor 230 (L3), and an output capacitor 228 (C1). A low band path of the diplexer 200 includes an input capacitor 214 (C6) and a first parallel coupled capacitor 222 (C7) with a second inductor 220 (L2). The low band path also includes a second capacitor 212 (C8) and a first inductor 210 (L1). Operation of the diplexer 200 is controlled by the first inductor 210, the second inductor 220, the third inductor 230, and the fourth inductor 240, as shown in the graph 250 of FIGURE 2B.

[0039] FIGURE 2B is a graph 250 illustrating performance of a diplexer design according to an aspect of the present disclosure. The x-axis of the graph 250 reflects the frequency in gigahertz (GHz) and the y-axis of the graph 250 reflects a decibel (dB) rating. A high pass filter curve 252 is a frequency response (transmission in dB) of the third inductor 230 (L3) and the fourth inductor 240 (L4). A low pass filter curve 254 is a frequency response (transmission in dB) of the first inductor 210 (L1) and the second inductor 220 (L2). In the diplexer configuration of FIGURE 2A, an antenna pad (e.g., the antenna 206) is the output for both the high band path and the low band path, whereas the input ports (e.g., the high band input port 202 and the low band input port 204) are separate. According to the graph 250, meeting the low pass filter curve 254 may involve higher performance inductors (e.g., the first inductor 210 (L1) and the second inductor 220 (L2)) than the inductors (e.g., the third inductor 230 (L3) and the fourth inductor 240 (L4)) for meeting the high pass filter curve 252.

[0040] FIGURE 2C is a diagram further illustrating the diplexer 200 of FIGURE 2A according to an aspect of the present disclosure. The diplexer 200 includes a high band (HB) input port 202, a low band (LB) input port 204, and an antenna 206 coupled to an

output port. A high band path of the diplexer 200 includes a high band antenna switch 260-1. A low band path of the diplexer 200 includes a low band antenna switch 260-2. A wireless device including an RF front end module may use the antenna switches 260 and the diplexer 200 to enable a wide range band for an RF input and an RF output of the wireless device. In addition, the antenna 206 may be a multiple input, multiple output (MIMO) antenna. Multiple input, multiple output antennas will be widely used for the RF front end of wireless devices to support features such as carrier aggregation.

[0041] FIGURE 3A is a top view of a layout of a diplexer design 300 according to an aspect of the present disclosure. The layout of the diplexer design 300 corresponds to the schematic diagram of the diplexer 200 from FIGURE 2A according to a 2D configuration. Also, the components are implemented in (or on) a passive substrate 308. As described herein, the term "passive substrate" may refer to a substrate of a diced wafer or panel, or may refer to the substrate of a wafer/panel that is not diced. In one arrangement, the passive substrate is comprised of glass, air, quartz, sapphire, high-resistivity silicon, or other like passive material. The passive substrate may be a coreless substrate.

[0042] The diplexer design 300 includes a high band (HB) input path 302, a low band (LB) input path 304, and an antenna 306. In this arrangement the first inductor 310 (L1) and the second inductor 320 (L2) are arranged using 2D spiral inductors. In addition, the third inductor 330 and the fourth inductor 340 are also arranged using 2D spiral inductors. The various capacitor (e.g., C1 to C8) are also shown and arranged according to the configuration shown in FIGURE 2A. A thickness of the 2D planar inductors may be within a range of ten (10) to thirty (30) micrometers. In addition, the footprint occupied by the diplexer design 300 may be in the range of 2 micrometers by 2.5 micrometers due to the 2D planar spiral configuration of the inductors. While this arrangement may be fabricated using less complicated designs, this arrangement consumes additional space.

[0043] FIGURE 3B shows a cross section view 350 of the diplexer design 300 of FIGURE 3A according to aspects of the present disclosure. For purposes of illustration, only the first inductor 310 (L1) and the second inductor 320 (L2) are shown, as supported by a passive substrate 308.

[0044] FIGURE 4A is a top view of a layout of a diplexer design 400 according to an aspect of the present disclosure. The layout of the diplexer design 400 corresponds to the schematic diagram of the diplexer 200 from FIGURE 2A according to a 3D implementation. Also, the components are implemented in (or on) a passive substrate 408 (see FIGURE 4B), comprised of glass, air, quartz, sapphire, high-resistivity silicon, or other like passive material.

[0045] In the arrangement shown in FIGURE 4A, the diplexer design 400 also includes a high band (HB) input path 402, a low band (LB) input path 404, and an antenna 406. In this arrangement, however, the first inductor 410 (L1) and the second inductor 420 (L2) are arranged using 3D spiral inductors. In addition, the third inductor 430 and the fourth inductor 440 are also arranged using 3D spiral inductors. The various capacitor (e.g., C1 to C8) are also shown and arranged according to the configuration shown in FIGURE 2A. As a result, a reduced footprint is occupied by the diplexer design 400, which is in the range of 2 millimeters by 1.7 millimeters, relative to the diplexer design 300 of FIGURES 3A and 3B.

[0046] FIGURE 4B shows a cross section view 450 of the diplexer design 400 of FIGURE 4A according to aspects of the present disclosure. For purposes of illustration, only the first inductor 410 (L1) and the second inductor 420 (L2) are shown, as supported by a passive substrate 408. The structures of the various inductors and capacitors shown in FIGURES 3A to 4B are not limited to the structures shown and can take on any structure, such that the layout of the diplexer designs 300/400 are possible implementations of the diplexer 200 shown in FIGURE 2A. Furthermore, the geometry and arrangement of the various inductor and capacitor components in the diplexer 200 may be configured to further reduce the electromagnetic coupling between the components.

[0047] In the depicted configuration of FIGURE 4A, the inductors (e.g., the first inductor 410 (L1), the second inductor 420 (L2), the third inductor 430 (L3), and the fourth inductor 440 (L4)) are high performance inductors implemented in a 3D configuration as a series of traces and through substrate vias that are further illustrated in the cross section view of FIGURE 4B. Although the diplexer design 400 of FIGURES 4A and 4B occupies a smaller footprint than the diplexer design 300 of FIGURES 3A and 3B, fabrication of the diplexer design 400 is more complex and

involves additional cost to implement the high performance 3D inductors (e.g., 410, 420, 430, and 440).

[0048] According to aspects of the present disclosure, a 3D implementation of the first inductor 410 and the second inductor 420 (FIGURE 4A) may be integrated with a 2D implementation of the third inductor 330 and the fourth inductor 340 (FIGURE 3A), for example, as shown in FIGURES 5A and 5B. In particular, because meeting the low pass filter curve 254 (FIGURE 2B) may involve higher performance inductors, the first inductor 410 and the second inductor 420 may be implemented using the higher cost 3D arrangement shown in FIGURES 4A and 4B. Conversely, because meeting the high pass filter curve 252 may involve lower performance inductors, the third inductor 230 (L3) and the fourth inductor 240 (L4) may be implemented using the lower cost and simplified 2D arrangement shown in FIGURES 3A and 3B.

[0049] FIGURE 5A illustrates a multiplexer structure 500 using a 2D filter integrated with a 3D filter for a high quality (Q)-factor radio frequency (RF) application according to aspect of the present disclosure. In one arrangement, the multiplexer structure 500 includes a high band (HB) filter 502 on a passive substrate 508. In one aspect of the present disclosure, the passive substrate 508 may be a diced portion of a passive substrate panel (e.g., a glass substrate panel) that supports a dual-sided printing process. The glass substrate panel may, for example, have dimensions including a twenty (20) by twenty (20) inch (20" x 20") length and width, with a panel thickness in the range of three hundred (300) to four hundred (400) microns.

[0050] In this arrangement, the dual-sided printing process enables the printing of conductive interconnect layers (e.g., metal A (MA), metal B (MB), metal C (MC), etc.) on a first surface 509-1 of the passive substrate 508. This dual-sided printing process also enables the printing of back-end-of-line (BEOL) interconnect layers (e.g., metal 1 (M1), metal 2 (M2), metal 3 (M3), etc.) on a second surface 509-2 of the passive substrate 508. According to aspects of the present disclosure, this dual-sided printing process enables a two-sided multiplexer structure, as described in further detail below.

[0051] The high band filter includes 2D spiral inductor(s) (e.g., the third inductor 530 (L3) and the fourth inductor 540 (L4)) on the passive substrate 508. The multiplexer structure 500 also includes a low band (LB) filter 504 on the passive

substrate 508. The low band filter 504 includes 3D inductor(s) (e.g., the first inductor 510 (L1) and the second inductor 520 (L2)) and a first capacitor (C1) on the passive substrate 508. The multiplexer structure 500 further includes a through substrate via(s) (VIA) coupling the high band filter 502 and the low band filter 504.

[0052] In this aspect of the present disclosure, the high band filter 502 and the low band filter 504 are arranged on opposing surfaces of a glass substrate panel to provide a two-sided multiplexer structure. In this arrangement, the high band filter 502 includes a second capacitor (C2) on a first surface 509-1 of the passive substrate 508. Alternatively, the high band filter 502 and the low band filter 504 may share the first capacitor C1 on a second surface 509-2 of the passive substrate 508 opposite the first surface 509-1. In one arrangement, the first surface of the passive substrate is a back-side of the two-sided multiplexer distal from a system board (e.g., a printed circuit board (PCB)).

[0053] In the arrangement shown in FIGURE 5A, the first capacitor C1 is formed from back-end-of-line (BEOL) interconnect layers M1 and M2, separated by a dielectric layer (e.g., aluminum oxide) on the second surface 509-2 of the passive substrate 508. In this arrangement, the first capacitor C1 is coupled to BEOL interconnect layer M3 through a through substrate via V2. In addition, the second capacitor C2 is formed from conductive interconnect layers MA and MB separated by a dielectric on the first surface 509-1 of the passive substrate 508. The third inductor 530 (L3) and the fourth inductor 540 (L4) may be formed from conductive interconnect layer MC, whereas the first inductor 510 (L1) and the second inductor 520 (L2) may be formed from BEOL interconnect layer M1. The multiplexer structure 500 is also surrounded by a final passivation layer VP (e.g., polyimide or solder resist).

[0054] FIGURE 5B illustrates a top view 550 of components of the multiplexer structure 500 of FIGURE 5A, including a 2D filter integrated with a 3D filter for high Q-factor RF applications according to aspects of the present disclosure. In this arrangement, side B of the multiplexer structure 500 includes the high band filter 502 including the third inductor 530 (L3) and the fourth inductor 540 (L4) arranged as 2D spiral inductors within a 1 millimeter by 2.5 millimeter footprint. In addition, side A of the multiplexer structure 500 also includes the low band filter 504 including the first inductor 510 (L1) and the second inductor 520 (L2)) arranged as 3D inductors within a

1 millimeter by 1.7 millimeter footprint. The multiplexer structure 500 further includes a through substrate via(s) (VIA) coupling the high band filter 502 and the low band filter 504.

[0055] FIGURE 6 is a process flow diagram illustrating a method 600 of constructing a multiplexer structure according to an aspect of the present disclosure. In block 602, a high band (HB) filter, including a 2D planar spiral inductor, is fabricated on a passive substrate panel. For example, as shown in FIGURE 5A, the multiplexer structure 500 includes the high band filter 502 on the first surface 509-1 of the passive substrate 508. The high band filter may include 2D planar spiral inductor(s) (e.g., the third inductor 530 (L3) and the fourth inductor 540 (L4)) on the first surface 509-1 of the passive substrate 508.

[0056] As noted above, the passive substrate 508 may be formed by dicing a glass substrate panel along the dicing lines, which may be referred to herein as "dicing streets." The dicing lines indicate where the glass panel substrate is to be broken apart or separated into pieces. The dicing lines may define the outline of the various RF circuits that have been fabricated on the glass panel substrate. This dicing process may be performed using a stealth dicing process that involves a scribing and cracking process along the dicing street without material loss. Stealth dicing may be distinguished from the dicing of silicon, which involves material loss due to grinding of, for example, a saw blade along the dicing street.

[0057] In block 604, a low band (LB) filter, including a 3D through-substrate inductor and a first capacitor, is fabricated on the passive substrate panel. For example, as shown in FIGURE 5A, the multiplexer structure 500 includes the low band filter 504 on the second surface 509-2 of the passive substrate 508. The low band filter may include 3D through-substrate inductor(s) (e.g., the first inductor 510 (L1) and the second inductor 520 (L2)) and a first capacitor (C1), on the second surface 509-2 of the passive substrate 508.

[0058] In block 606, a through substrate via is fabricated through the passive substrate, coupling the high band filter and the low band filter. As shown in FIGURE 5B, the multiplexer structure 500 further includes a through substrate via(s) (VIA) coupling the high band filter 502 and the low band filter 504. The method 600 may also

include fabricating at least one second capacitor on the first surface of the passive substrate. According to aspects of the present disclosure, a dual-sided printing process for a glass panel substrate enables a two-sided multiplexer structure, for example, as shown in FIGURE 5A. Although shown in the noted order, it should be recognized that the method of constructing the multiplexer structure may be performed in any desired order including, but not limited to, performing the method 600 is reverse order beginning with block 606 and terminating with block 602.

[0059] According to a further aspect of the present disclosure, circuitry for multiplexer structures using through glass via or through substrate via technology is described. The multiplexer structure includes high band filters and low band filters on opposing surfaces of a passive substrate. The multiplexer structure further includes means for coupling the high band filter and the low band filter. The coupling means may be the through substrate VIA, shown in FIGURE 5A. In another aspect, the aforementioned means may be any module or any apparatus configured to perform the functions recited by the aforementioned means.

[0060] Various aspects of the disclosure provide techniques for fabrication of multiplexers using 2D passive on glass (POG) filters integrated with 3D through glass via (TGV) filters. Aspects of the present disclosure describe multiplexers using 2D POG filters integrated with 3D TGV filters for high Q-factor RF applications. In one arrangement, a multiplexer structure includes a high band (HB) filter on a passive substrate. The high band filter includes a 2D spiral inductor on the passive substrate. The multiplexer structure also includes a low band (LB) filter on the passive substrate. The low band filter includes a 3D inductor and a first capacitor on the passive substrate. The multiplexer structure further includes at least one through substrate via coupling the high band filter and the low band filter.

[0061] In one aspect of the present disclosure, the high band filter and the low band filter are arranged on opposing surfaces of a glass substrate to provide a two-sided multiplexer structure. In this arrangement, the high band filter includes a second capacitor on a first surface of the passive substrate. Alternatively, the high band filter and the low band filter may share the first capacitor on a second surface of the passive substrate opposite the first surface. In particular, because meeting the low pass filter curve 254 (FIGURE 2B) may involve higher performance inductors, the first inductor

410 and the second inductor 420 may be implemented using the higher cost 3D arrangement shown in FIGURES 4A and 4B. The higher performance inductors may be high-Q, high-density 3D inductors for critical bands (e.g., the low band). Conversely, because meeting the high pass filter curve 252 may involve lower performance inductors, the third inductor 330 (L3) and the fourth inductor 340 (L4) may be implemented using the lower cost and simplified 2D planar arrangement shown in FIGURES 3A and 3B. In addition, placing the 2D filters away from the system board (e.g., PCB) may eliminate customer specific ground plan impact.

[0062] FIGURE 7 is a block diagram showing an exemplary wireless communication system 700 in which an aspect of the disclosure may be advantageously employed. For purposes of illustration, FIGURE 7 shows three remote units 720, 730, and 750 and two base stations 740. It will be recognized that wireless communication systems may have many more remote units and base stations. Remote units 720, 730, and 750 include IC devices 725A, 725C, and 725B that include the disclosed multiplexer structures. It will be recognized that other devices may also include the disclosed multiplexer devices, such as the base stations, switching devices, and network equipment. FIGURE 7 shows forward link signals 780 from the base station 740 to the remote units 720, 730, and 750 and reverse link signals 790 from the remote units 720, 730, and 750 to base stations 740.

[0063] In FIGURE 7, remote unit 720 is shown as a mobile telephone, remote unit 730 is shown as a portable computer, and remote unit 750 is shown as a fixed location remote unit in a wireless local loop system. For example, a remote units may be a mobile phone, a hand-held personal communication systems (PCS) unit, a portable data unit such as a personal digital assistant (PDA), a GPS enabled device, a navigation device, a set top box, a music player, a video player, an entertainment unit, a fixed location data unit such as a meter reading equipment, or other communications device that stores or retrieve data or computer instructions, or combinations thereof. Although FIGURE 7 illustrates remote units according to the aspects of the disclosure, the disclosure is not limited to these exemplary illustrated units. Aspects of the disclosure may be suitably employed in many devices, which include the disclosed multiplexer devices.

[0064] FIGURE 8 is a block diagram illustrating a design workstation used for circuit, layout, and logic design of a semiconductor component, such as the multiplexer devices disclosed above. A design workstation 800 includes a hard disk 801 containing operating system software, support files, and design software such as Cadence or OrCAD. The design workstation 800 also includes a display 802 to facilitate design of a circuit 810 or a semiconductor component 812 such as a multiplexer device. A storage medium 804 is provided for tangibly storing the circuit design 810 or the semiconductor component 812. The circuit design 810 or the semiconductor component 812 may be stored on the storage medium 804 in a file format such as GDSII or GERBER. The storage medium 804 may be a CD-ROM, DVD, hard disk, flash memory, or other appropriate device. Furthermore, the design workstation 800 includes a drive apparatus 803 for accepting input from or writing output to the storage medium 804.

[0065] Data recorded on the storage medium 804 may specify logic circuit configurations, pattern data for photolithography masks, or mask pattern data for serial write tools such as electron beam lithography. The data may further include logic verification data such as timing diagrams or net circuits associated with logic simulations. Providing data on the storage medium 804 facilitates the design of the circuit design 810 or the semiconductor component 812 by decreasing the number of processes for designing semiconductor wafers.

[0066] For a firmware and/or software implementation, the methodologies may be implemented with modules (e.g., procedures, functions, and so on) that perform the functions described herein. A machine-readable medium tangibly embodying instructions may be used in implementing the methodologies described herein. For example, software codes may be stored in a memory and executed by a processor unit. Memory may be implemented within the processor unit or external to the processor unit. As used herein, the term "memory" refers to types of long term, short term, volatile, nonvolatile, or other memory and is not to be limited to a particular type of memory or number of memories, or type of media upon which memory is stored.

[0067] If implemented in firmware and/or software, the functions may be stored as one or more instructions or code on a computer-readable medium. Examples include computer-readable media encoded with a data structure and computer-readable media

encoded with a computer program. Computer-readable media includes physical computer storage media. A storage medium may be an available medium that can be accessed by a computer. By way of example, and not limitation, such computer-readable media can include RAM, ROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or other medium that can be used to store desired program code in the form of instructions or data structures and that can be accessed by a computer; disk and disc, as used herein, includes compact disc (CD), laser disc, optical disc, digital versatile disc (DVD), floppy disk and Blu-ray disc where disks usually reproduce data magnetically, while discs reproduce data optically with lasers. Combinations of the above should also be included within the scope of computer-readable media.

[0068] In addition to storage on computer readable medium, instructions and/or data may be provided as signals on transmission media included in a communication apparatus. For example, a communication apparatus may include a transceiver having signals indicative of instructions and data. The instructions and data are configured to cause one or more processors to implement the functions outlined in the claims.

[0069] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the technology of the disclosure as defined by the appended claims. For example, relational terms, such as "above" and "below" are used with respect to a substrate or electronic device. Of course, if the substrate or electronic device is inverted, above becomes below, and vice versa. Additionally, if oriented sideways, above and below may refer to sides of a substrate or electronic device. Moreover, the scope of the present application is not intended to be limited to the particular configurations of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed that perform substantially the same function or achieve substantially the same result as the corresponding configurations described herein may be utilized according to the present disclosure. Accordingly, the appended claims are

intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS:

1. A method of constructing a multiplexer structure from a passive substrate panel, comprising: fabricating a high band filter on the passive substrate panel, the high band filter including at least a 2D planar spiral inductor on a first side of the passive substrate panel; fabricating a low band filter on the passive substrate panel, the low band filter including a 3D through-substrate inductor and at least one first capacitor, the at least one first capacitor being formed on a second side of the passive substrate panel, opposite the first side; and fabricating a via through the passive substrate panel coupling the high band filter and the low band filter through the passive substrate panel.

2. The method of claim 1, in which the multiplexer structure comprises a two-sided multiplexer using a dual-sided printing process.

3. The method of claim 1, in which the passive substrate comprises a glass substrate panel and in which fabricating the via further comprises fabricating a through glass via coupling the high band filter on the first side of the glass substrate panel and the low band filter on the second side of the glass substrate panel.

4. The method of claim 1, in which fabricating the high band filter further comprises fabricating at least one second capacitor on the first side of the passive substrate panel.

5. The method of claim 1, further comprising separating the passive substrate panel along a dicing street using a stealth dicing process.

6. A multiplexer structure, comprising: a passive substrate; a high band filter on the passive substrate, the high band filter including at least a 2D planar spiral inductor on a first side of the passive substrate; a low band filter on the passive substrate, the low band filter including a 3D through-substrate inductor and at least one first capacitor, the at least one first capacitor being formed on a second side of the passive substrate, opposite the first side; and means for coupling the high band filter and the low band filter through the passive substrate.

7. The multiplexer structure of claim 6, in which the multiplexer structure comprises a two-sided multiplexer structure.

8. The multiplexer structure of claim 6, in which the passive substrate comprises a glass substrate.

9. The multiplexer structure of claim 8, in which the means for coupling the high band filter and the low band filter comprises at least one through substrate via and, preferably, wherein the through substrate via comprises a through glass via.

10. The multiplexer structure of claim 6, in which the high band filter comprises at least one second capacitor on the first side of the passive substrate.

11. The multiplexer structure of claim 7, in which the first side of the passive substrate is a back-side of the two-sided multiplexer structure that is distal from a system board.

12. The multiplexer structure of claim 6, in which a thickness of the 2D inductor is within a range of ten, 10, to thirty, 30, micrometers.

13. The multiplexer structure of claim 6, integrated into a radio frequency, RF, front end module, the RF front end module incorporated into at least one of a music player, a video player, an entertainment unit, a navigation device, a communications device, a personal digital assistant, PDA, a fixed location data unit, a mobile phone, and a portable computer.

14. A radio frequency, RF, front end module, comprising: a multiplexer structure as set out in any of claims 6 to 13; and an antenna coupled to an output of the multiplexer structure.

15. The RF front end module of claim 14, further comprising: a high band antenna switch coupled to the high band filter through a high band input port of the multiplexer structure; and a low band antenna switch coupled to the low band filter through a low band input port of the multiplexer structure.

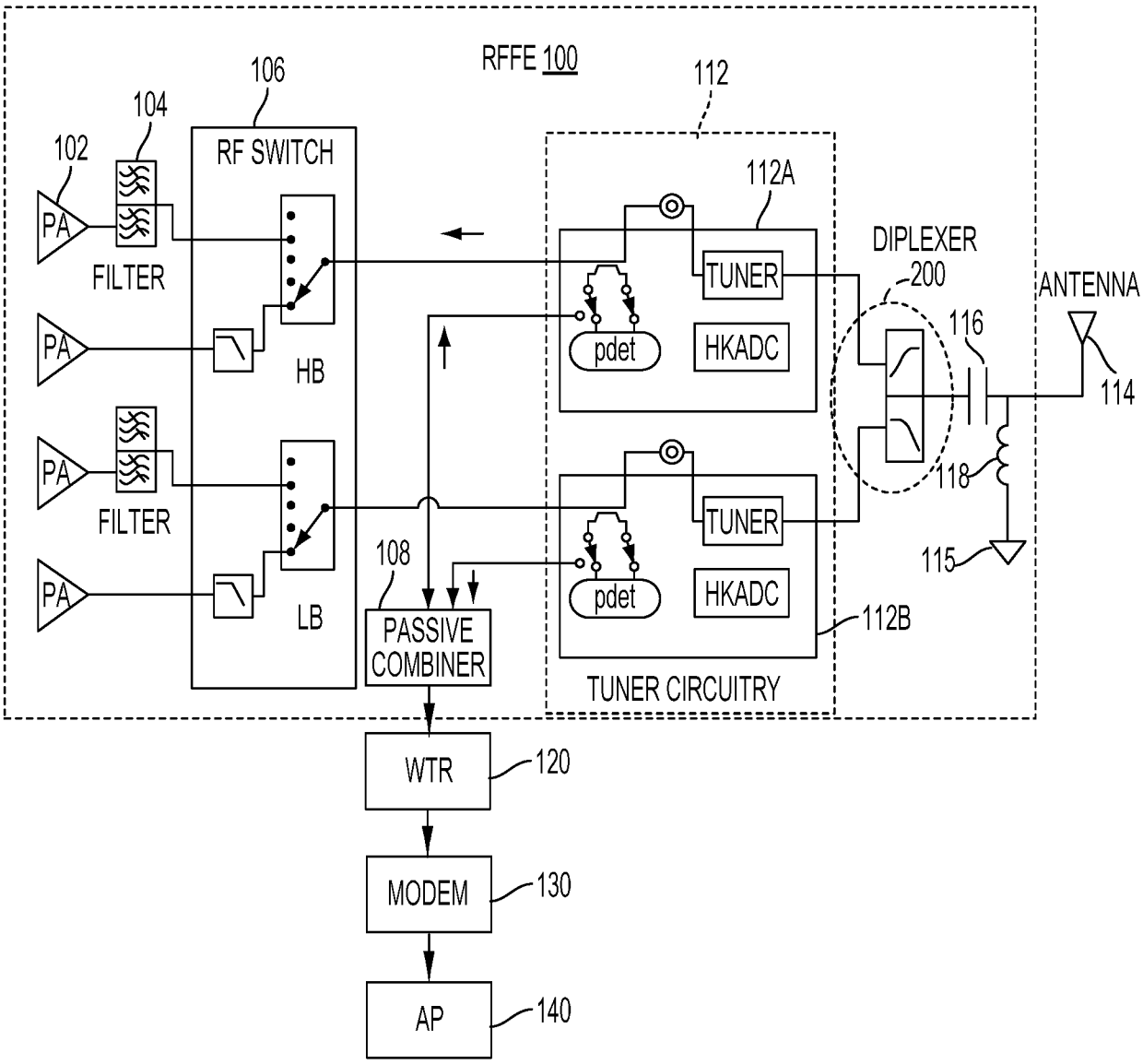

RFFE 100
106
RF SWITCH
104
102
PA
FILTER
PA
HB
PA
FILTER
PA
LB
108
PASSIVE COMBINER
112
112A
TUNER
pdet
HKADC
TUNER
pdet
HKADC
112B
TUNER CIRCUITRY
DIPLEXER
200
116
118
115
ANTENNA
114
WTR
120
MODEM
130
AP
140

FIG. 1A

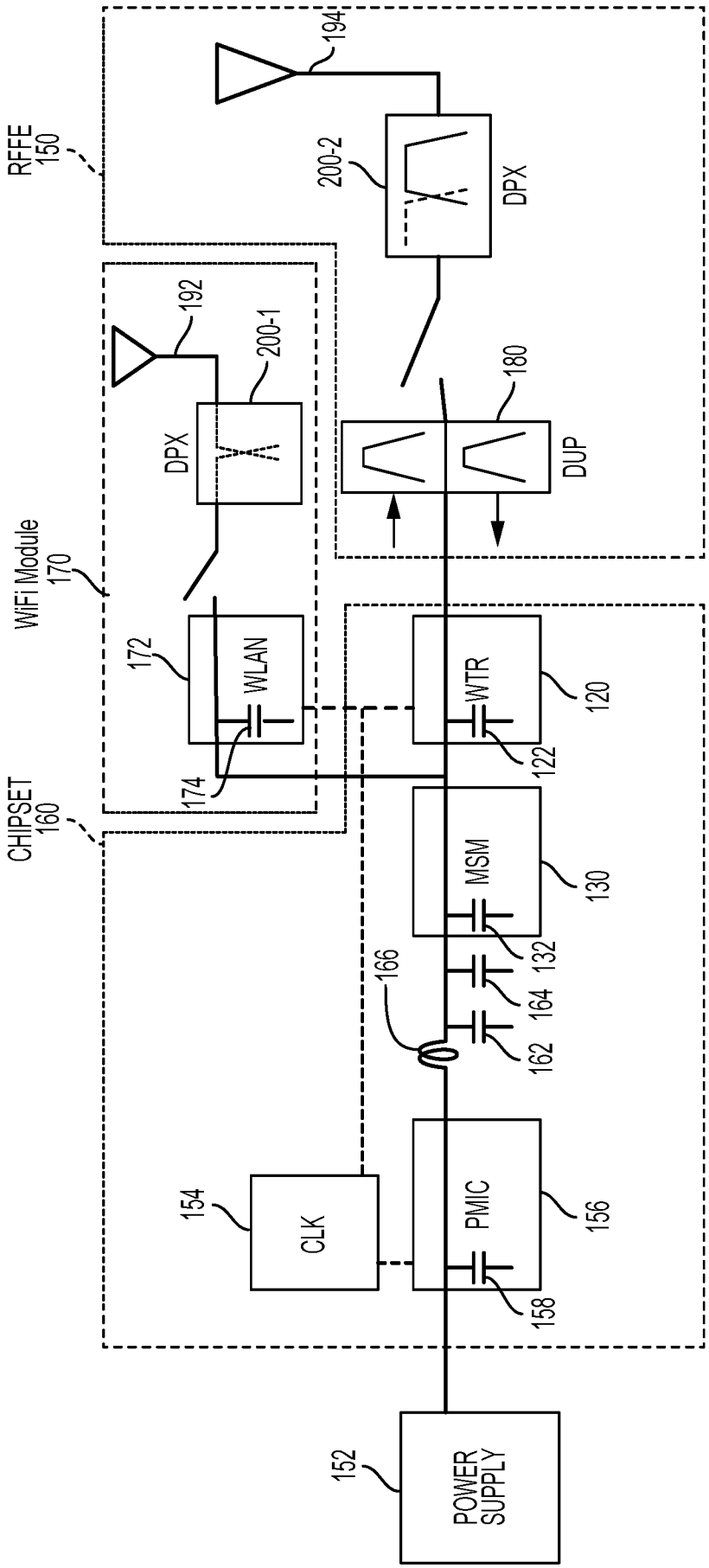

RFFE
150
194
200-2
DPX
192
200-1
DPX
180
DUP
WiFi Module
170
172
WLAN
WTR
120
122
174
CHIPSET
160
MSM
130
132
166
164
162
154
CLK
PMIC
156
158
152
POWER SUPPLY

FIG. 1B

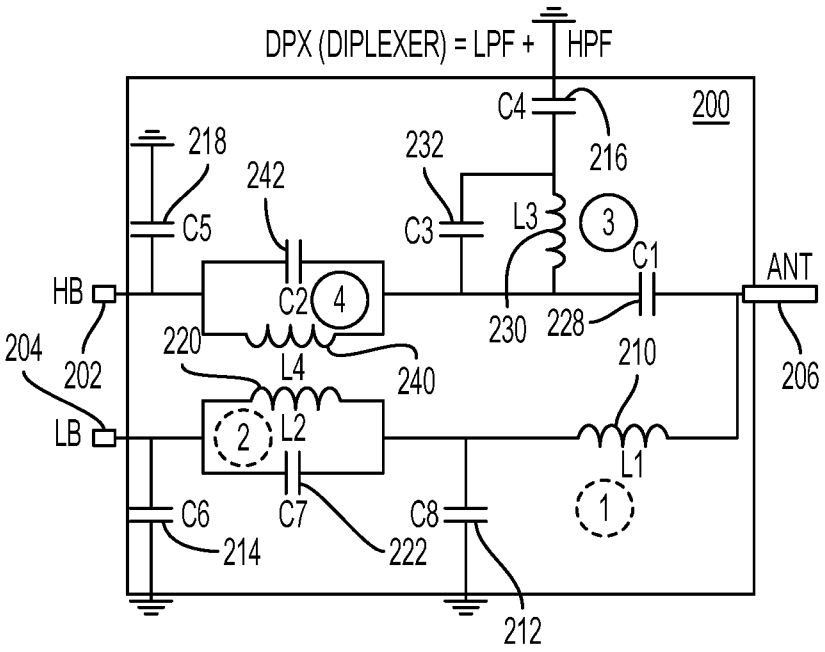

DPX (DIPLEXER) = LPF + HPF
200
C4
216
218
C5
242
232
C3
L3
3
C1
ANT
HB
C2
4
230
228
204
202
220
L4
240
210
206
LB
2
L2
L1
1
C6
C7
C8
214
222
212

FIG. 2A

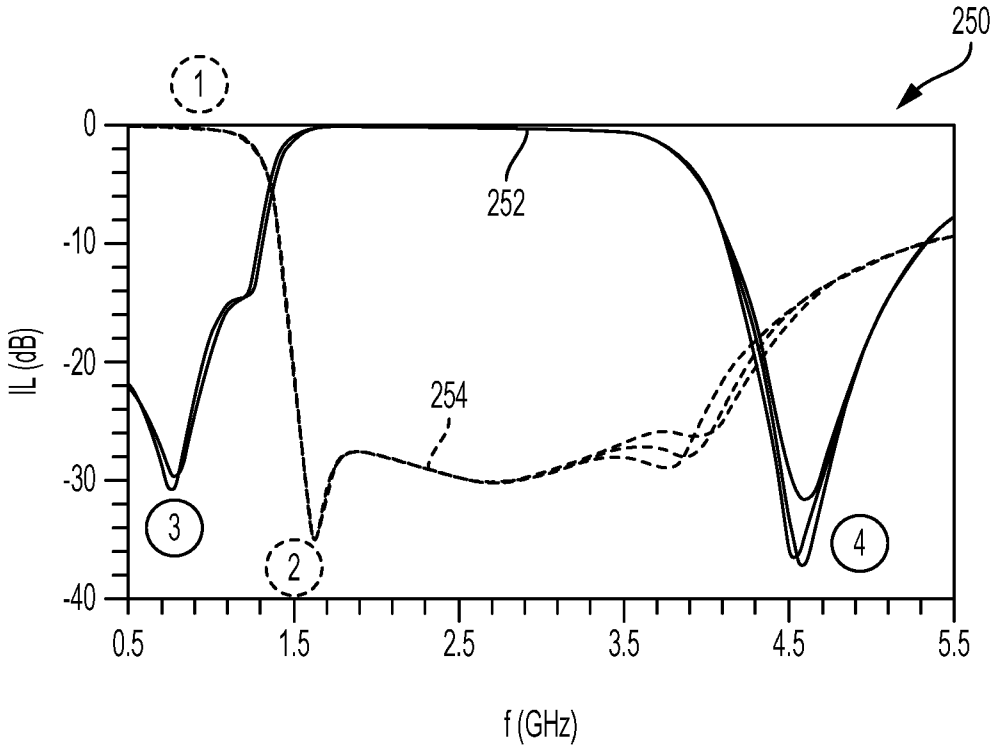

250
1
0
-10
-20
-30
-40
IL (dB)
252
254
3
2
4
0.5
1.5
2.5
3.5
4.5
5.5
f (GHz)

FIG. 2B

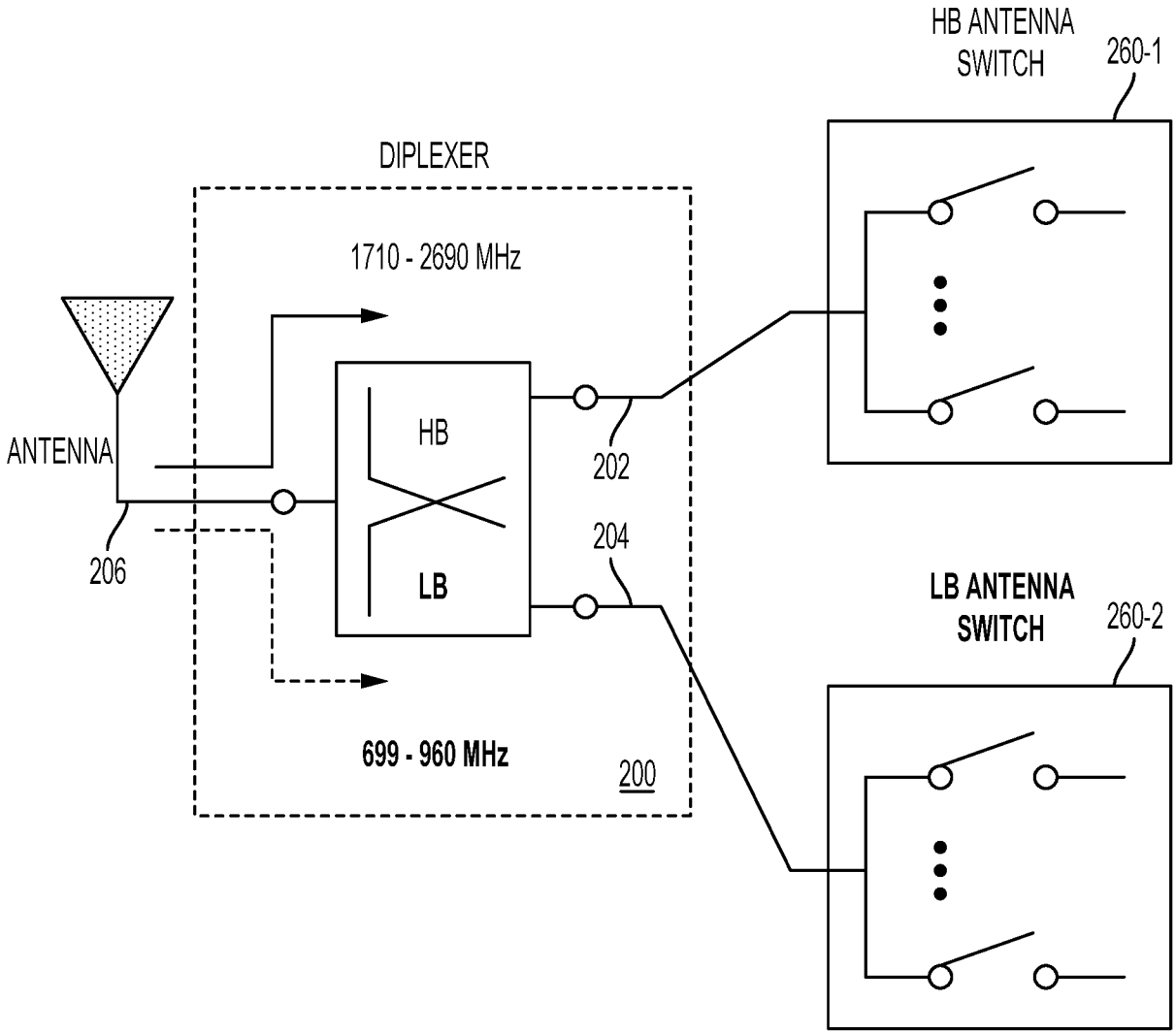

HB ANTENNA SWITCH
260-1
DIPLEXER
1710 - 2690 MHz
ANTENNA
HB
LB
202
204
206
LB ANTENNA SWITCH
260-2
699 - 960 MHz
200

FIG. 2C

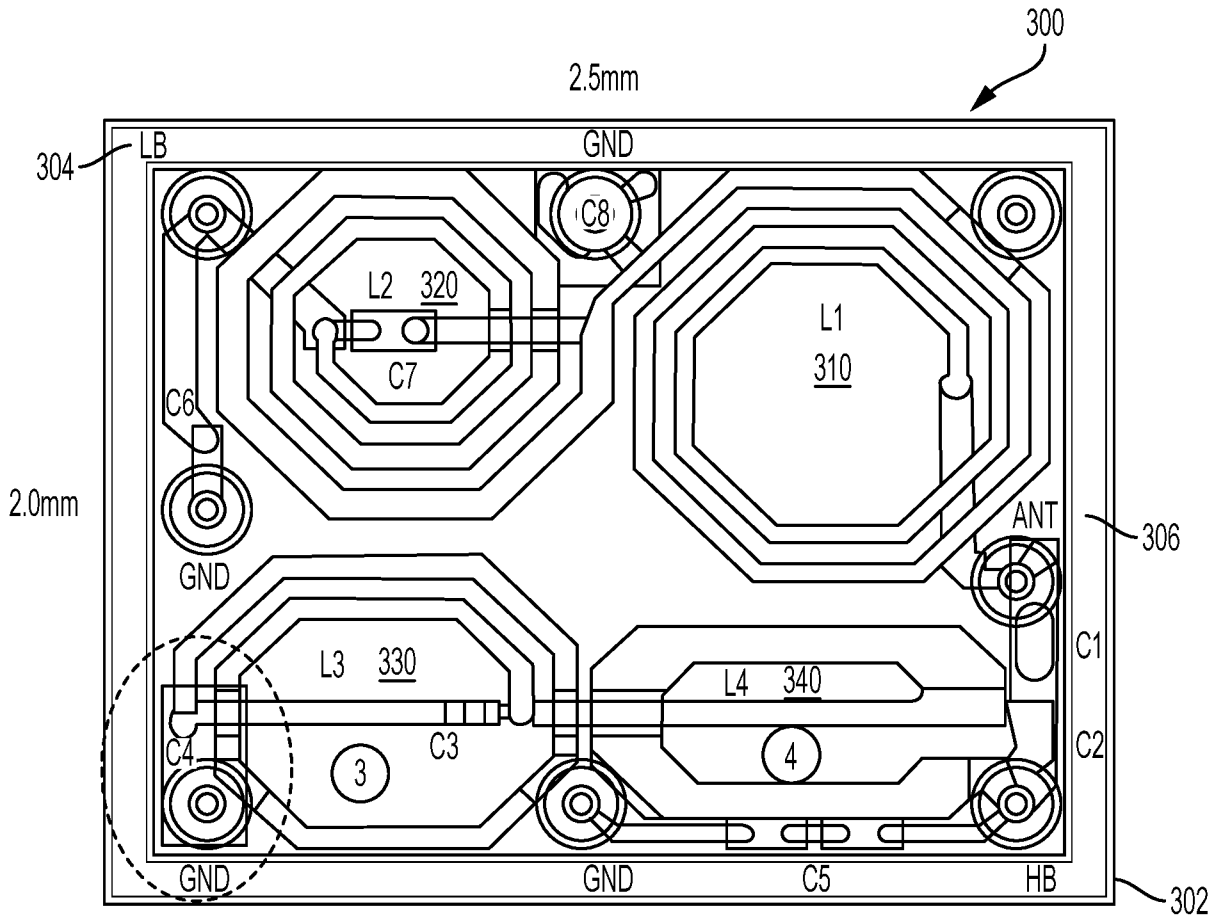

300
2.5mm
304
LB
GND
C8
L2 320
C7
L1
310
C6
2.0mm
GND
ANT
306
C1
L3 330
L4 340
C3
C4
3
4
C2
GND
GND
C5
HB
302

FIG. 3A

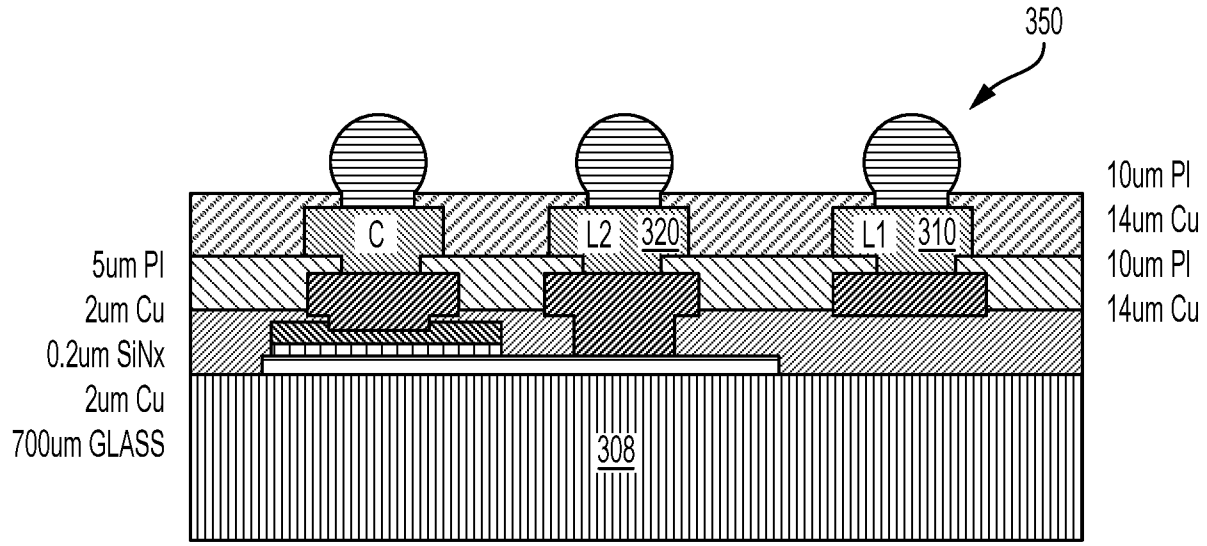

350
C
L2 320
L1 310
10um PI
14um Cu
10um PI
14um Cu
5um PI
2um Cu
0.2um SiNx
2um Cu
700um GLASS
308

FIG. 3B

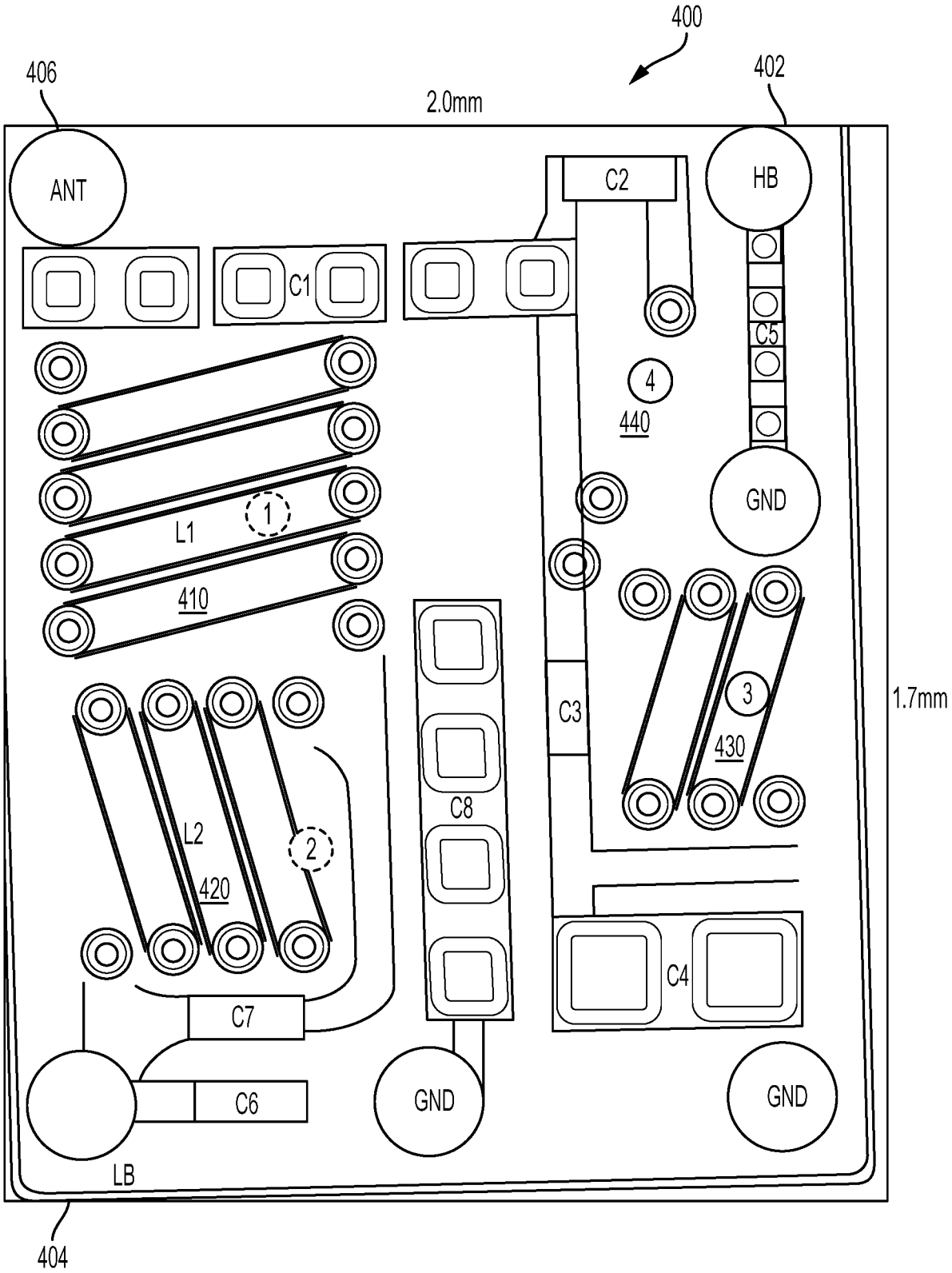

400
406
402
2.0mm
ANT
HB
C2
C1
C5
4
440
GND
L1
1
410
C3
3
430
1.7mm
C8
L2
2
420
C4
C7
C6
GND
GND
LB
404

FIG. 4A

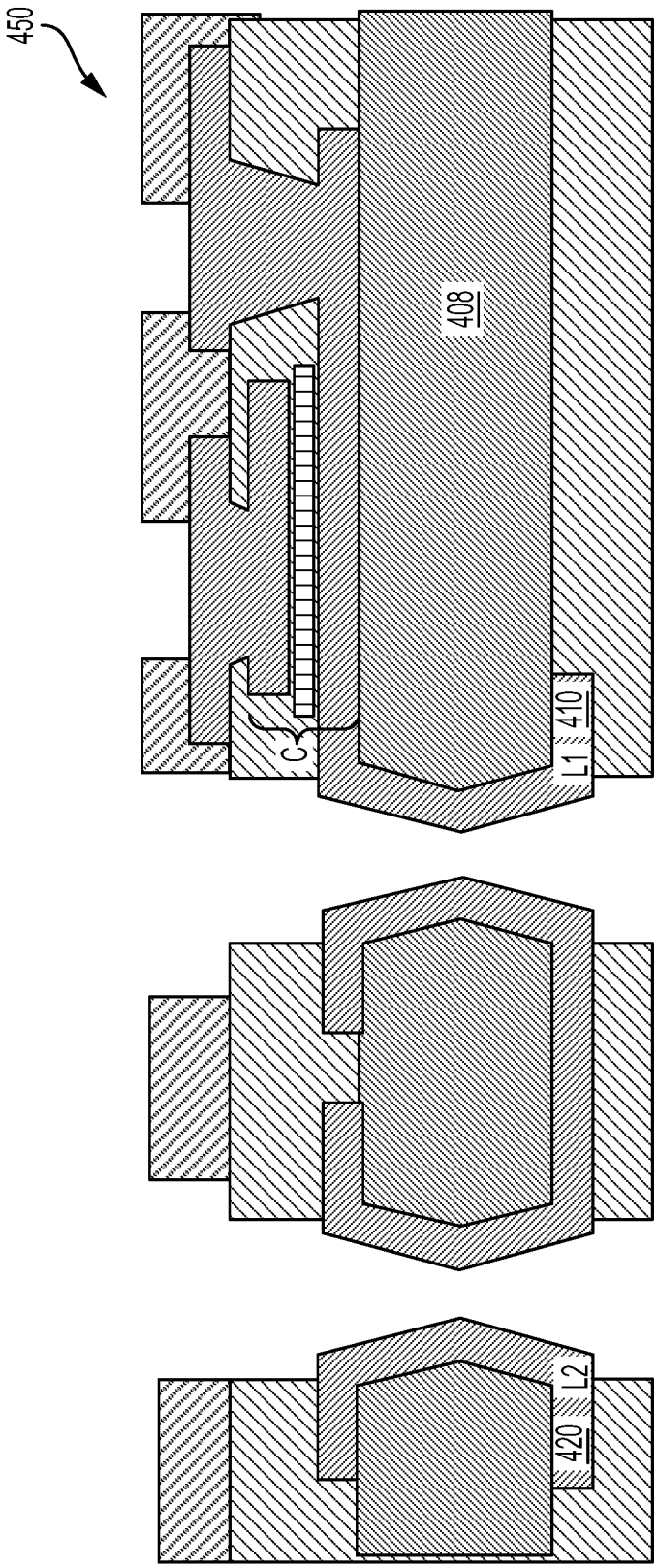


FIG. 4B

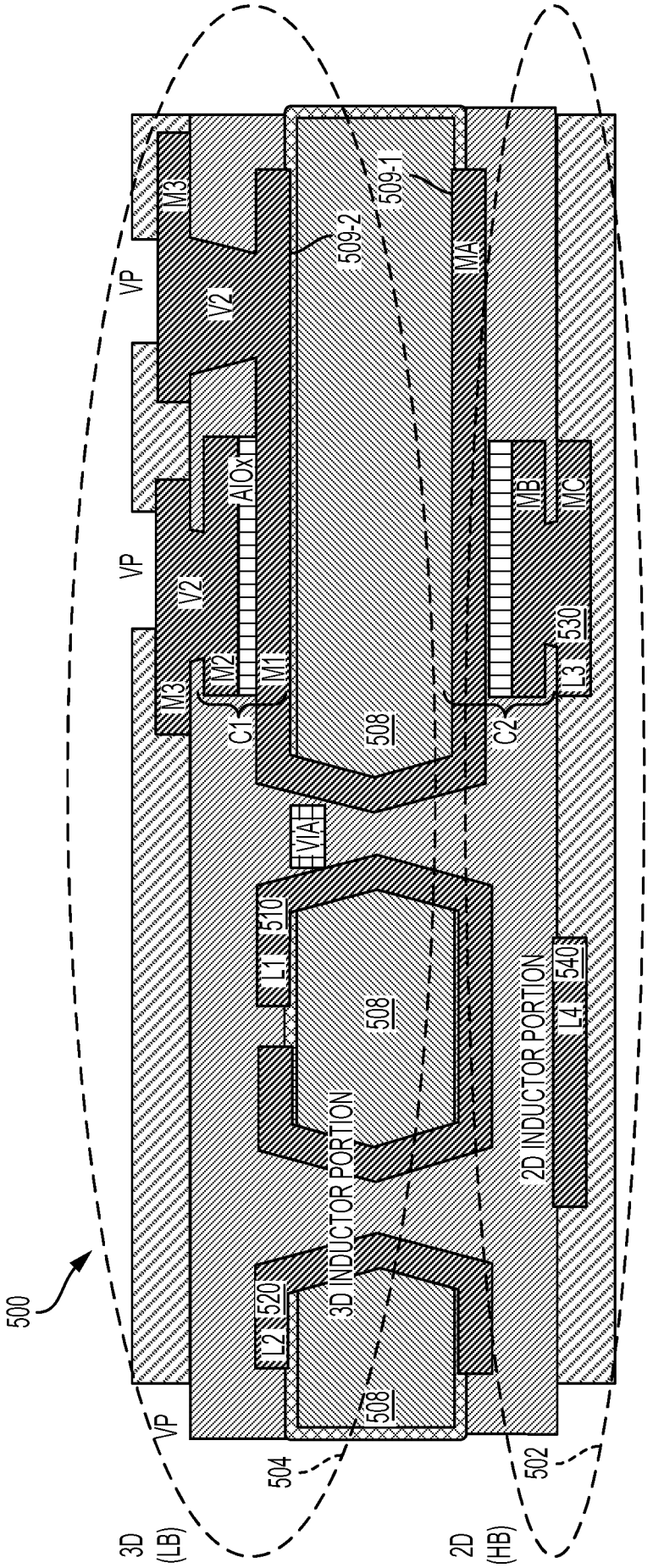

500
3D (LB)
2D (HB)
504
502
VP
M3
V2
AlOx
M2
M1
C1
508
509-1
509-2
MA
MB
MC
C2
L3
530
VIA
L1
510
L2
520
3D INDUCTOR PORTION
2D INDUCTOR PORTION
L4
540

FIG. 5A

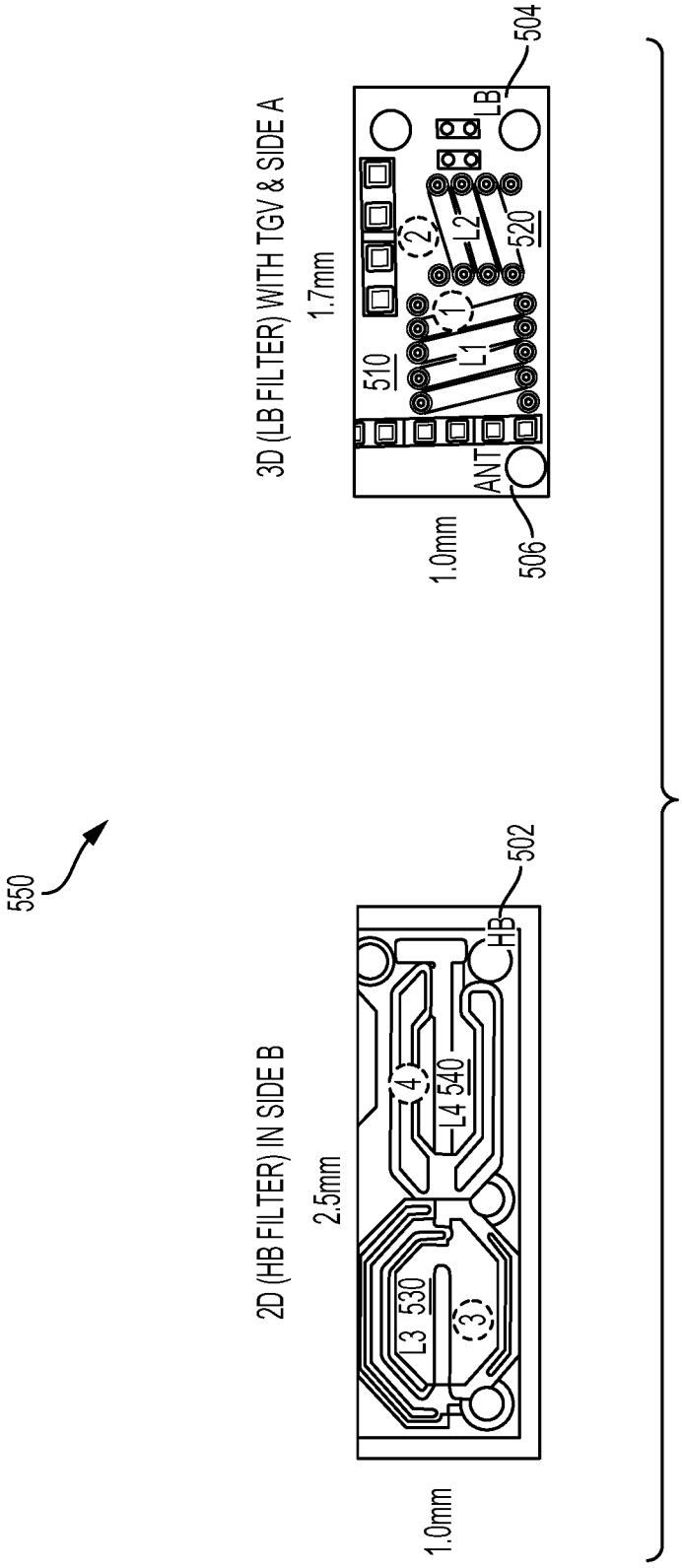

550
2D (HB FILTER) IN SIDE B
2.5mm
1.0mm
502
HB
4
L4 540
L3 530
3
3D (LB FILTER) WITH TGV & SIDE A
1.7mm
1.0mm
504
LB
2
L2
520
1
L1
510
ANT
506

FIG. 5B

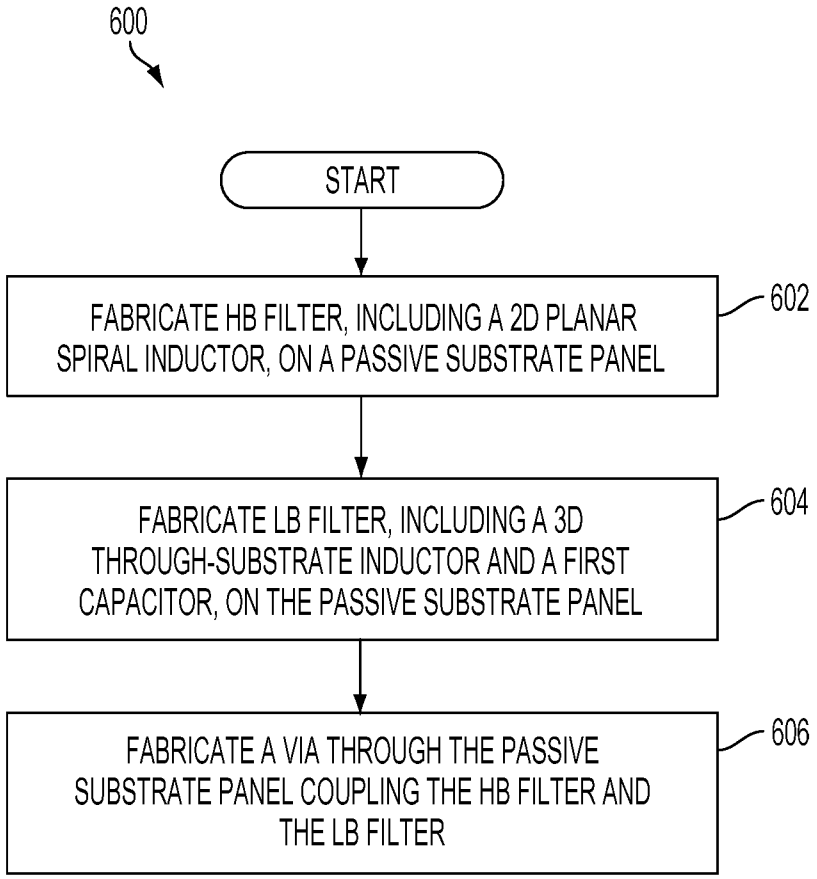

600
START
FABRICATE HB FILTER, INCLUDING A 2D PLANAR SPIRAL INDUCTOR, ON A PASSIVE SUBSTRATE PANEL
602
FABRICATE LB FILTER, INCLUDING A 3D THROUGH-SUBSTRATE INDUCTOR AND A FIRST CAPACITOR, ON THE PASSIVE SUBSTRATE PANEL
604
FABRICATE A VIA THROUGH THE PASSIVE SUBSTRATE PANEL COUPLING THE HB FILTER AND THE LB FILTER
606

FIG. 6

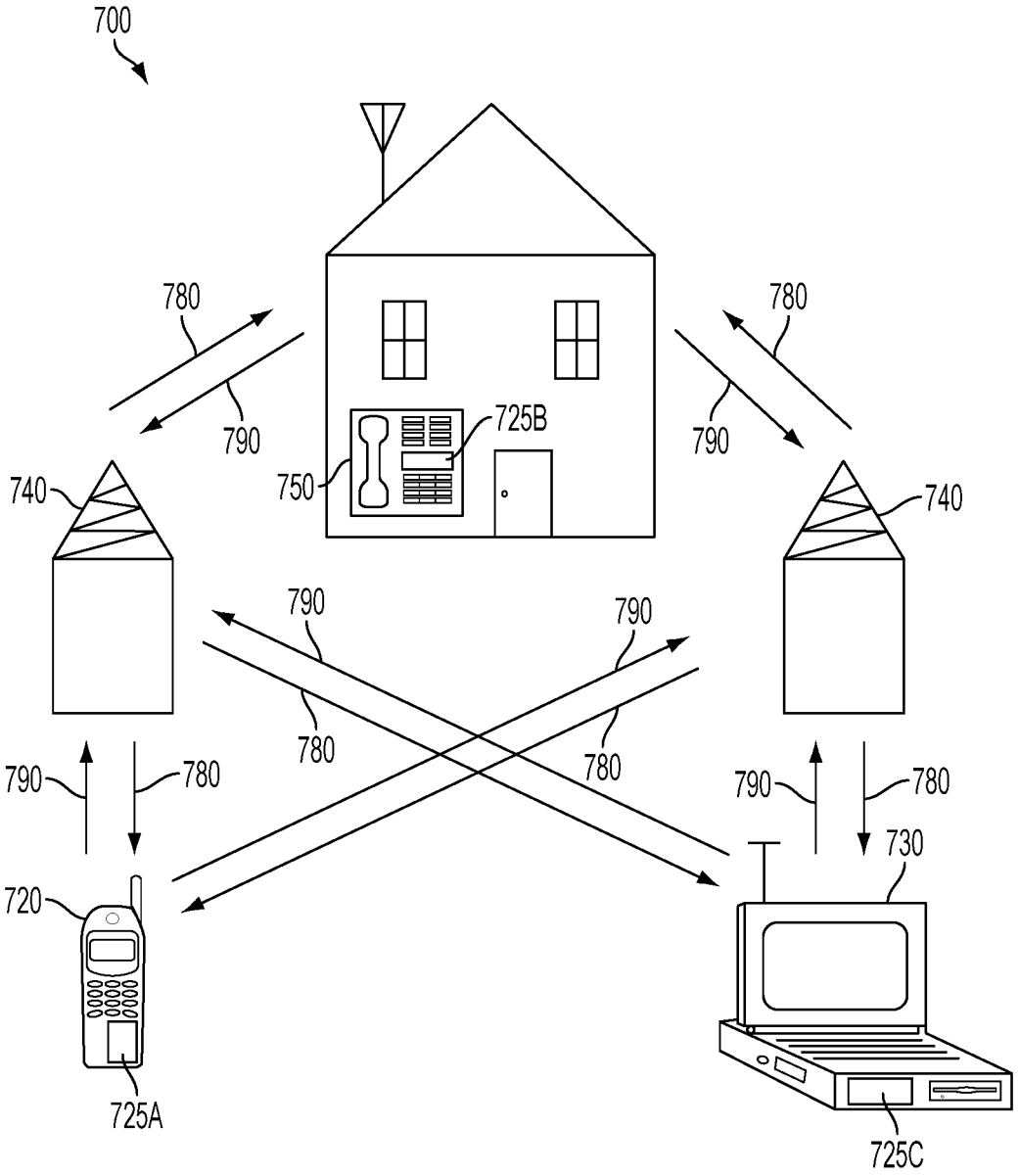

700
780
790
725B
750
740
740
790
790
780
780
790
780
790
780
730
720
725A
725C

FIG. 7

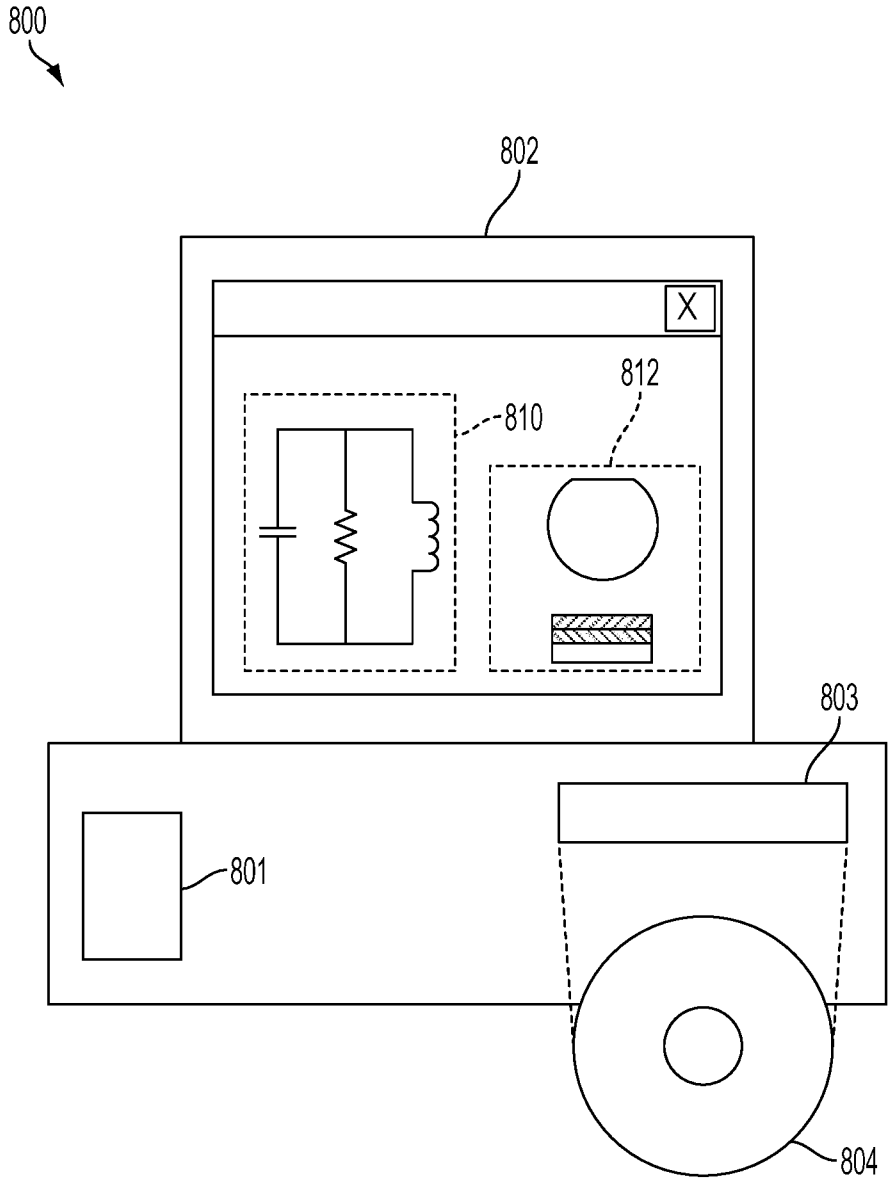
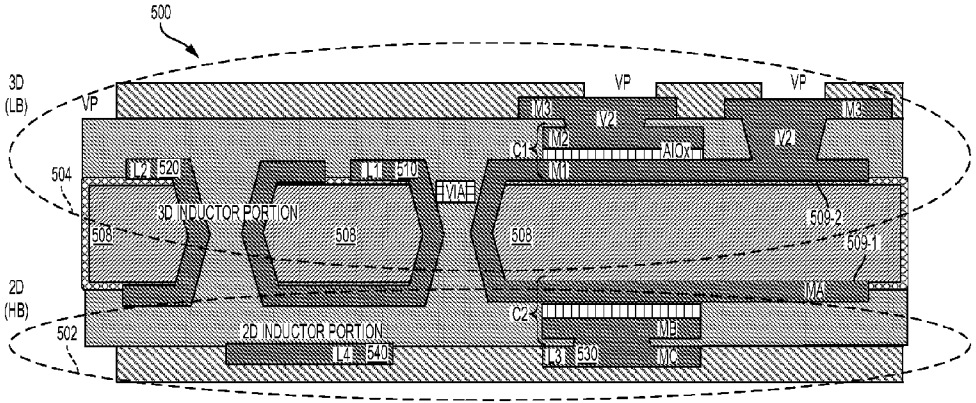


FIG. 8


500
3D
(LB)
VP
VP
VP
M3
V2
M3
M2
V2
C1
AlOx
M1
L2
520
L1
510
V1AE
504
3D INDUCTOR PORTION
508
508
508
509-2
509-1
2D
(HB)
M2
C2
M3
2D INDUCTOR PORTION
502
L4
540
L3
530
M2