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(54) IMPROVEMENTS IN PATTERN RECOGNITION SYSTEMS

(71) We, HITACHI, LTD. of 1-5-1 Marunouchi, Chiyoda-ku, Tokyo, Japan, a body corporate organized according to the laws of Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to a pattern recognition system, and in particular, to a pattern recognition system which can recognize an object having a complicated pattern.

Up to now, systems for recognizing a specified pattern contained in a binary signal have usually included a store for holding the specific pattern as a reference. The input signal and the stored reference pattern are compared.

This prior art system however, has a disadvantage which will now be explained in detail. By way of example, consider how the unidimensional input signal pattern shown in Figure 1*a* of the accompanying drawing is recognized with the prior art system. In order to recognize a specified pattern *a* within a binary signal indicated by "O" and "1" in Figure 1*a*, a reference pattern *b* which is shown in Figure 1*b* of the accompanying drawing, and which corresponds to the specified pattern *a* to be recognized, is employed, and each bit of the input signal shown in Figure 1*a* is compared to a bit of the reference pattern *b*. Considering the relative positions of the reference pattern *b* and the input signal; if the regions *a* and *b* enclosed with broken lines in Figures 1*a* and 1*b* are aligned as shown, the fact that they are identical can be immediately detected. However, if the reference pattern *b* is shifted to the right or left, relative to the portion *a* of the input signal, the input signal and the reference pattern must be repeatedly compared while shifting the reference pattern a little at a time until the portion *a* and the reference pattern *b* coincide. Alternatively, it is possible to have a plurality of reference patterns whose positions are slightly different, and to simultaneously compare the plurality of reference patterns with the input signal.

In the above example, the first method requires a long processing time. The second method involves the storage of a plurality of reference patterns, so that a memory of large capacity is necessary.

The disadvantages of the prior art will now be described with reference to the recognition of a two-dimensional specific pattern in the signal from an image pick-up device, e.g. an industrial television camera.

The pattern to be recognized is the rectangular hatched portion shown in Figure 2*a* of the accompanying drawings. To recognize such a rectangular pattern with the prior art system, four features enclosed with broken lines A to D, which are characteristic of the rectangular pattern are found, and their positional relationship is investigated.

In order to recognize the specified pattern using such a system, the reference pattern R*c1*, shown in Figure 2*b* of the accompanying drawings (the figure shows only the reference pattern which is employed to recognize the partial pattern C) is stored beforehand, and the part of the object which looks most like the reference pattern R*c1* is found.

In practice, it is sometimes the case that the object to be recognized is at the wrong angle relative to the image pick-up device. In such a case, even if the feature C is present in the object, it cannot be recognized by using only the reference pattern Rc1. In order to make recognition possible, even with such a rotation of the object, reference patterns Rc2 and Rc3, shown in Figures 2*c* and 2*d* of the accompanying drawings, respectively formed by rotating the pattern Rc1 by different amounts, must be employed.

Prior art systems which need to store such reference patterns as Rc1 to Rc3 in advance

require memories of large capacity. which result in high cost and complicated processing.

It is an object of the present invention to obviate partially or wholly the above disadvantages.

According to the present invention, there is provided a pattern recognition system for detecting the presence of a specified pattern in a binary signal pattern, the specified pattern including two portions which have logic values opposite to each other in corresponding bits comprising:

first means arranged to derive from the binary signal pattern a pair of partial patterns having a predetermined position relative to each other;

second means connected to said first means and including a plurality of Exclusive-OR gates, each of which receives a respective pair of the corresponding bits of the pair of partial patterns; and

third means connected to the second means and arranged to generate a coincidence signal indicating the presence of the specified pattern when a given number of said exclusive-OR gates produces a predetermined output signal thus indicating the presence of a pattern.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:-

Figures 1a and *1b* are diagrams showing a unidimensional pattern and a corresponding reference pattern;

Figure 2a and *Figures 2b* to *2d* are diagrams showing a two-dimensional pattern and corresponding reference patterns;

Figure 3 is a diagram for illustrating the principle of operation of embodiments of the present invention;

Figure 4 is a block diagram showing the basic elements of the first embodiment which can recognize a unidimensional pattern;

Figures 5a to *5c* are diagrams showing the first embodiment of a pattern recognition system of the invention and modifications thereof;

Figures 6a and *6b* show judging circuits for use in the circuits of Figures 5*a* to 5*c*;

Figures 7a to *7c* illustrate the principle operation of the second and third embodiments of the invention for recognizing a two-dimensional pattern;

Figure 8a illustrates more particularly the principle of operation of the second embodiment;

Figure 8b shows a typical shape which could be recognized by the second embodiment;

Figure 9 is a block diagram showing the second embodiment of a pattern recognition system;

Figure 10 is a block diagram of a possible timing signal generator for use in the second embodiment;

Figure 11 is a block diagram showing a possible pattern cutting-out circuit for use in the second embodiment, and also in the third embodiment;

Figure 12 is a block diagram showing an EXCLUSIVE OR gate and a judging circuit;

Figure 13 is a block diagram showing an example of the logic circuit, the gate circuits, the memory circuit and the co-ordinate computing circuit shown in Figure 9; and

Figure 14 is a block diagram showing the third embodiment of a pattern recognition system.

A specified pattern intended to be recognized by the first embodiment must have portions which are complementary to each other.

Take as an example the unidimensional pattern shown in Figure 1*a*. This includes a signal pattern formed by the eight bits within the region enclosed by the broken line *a*. The signal pattern has complementary portions with a boundary at the fourth and fifth bits. The first embodiment will recognize such a pattern. In the example given, the first four bits and the last four bits are completely complementary. Generally speaking, however, if the complementary portions form only part of the whole specific pattern, the first embodiment of the invention can still effect recognition.

The principle of operation of the first and second embodiments of the present invention will now be explained.

Assume that the partial patterns of a specified pattern to be sampled are patterns $g_1(x)$ and $g_2(x)$ in which, as illustrated in Figure 3, the level "1" continues over k bits. That is,

$$g_1(x) = \begin{cases} \text{"1"} & (0 \leqslant x < k) \\ \text{"0"} & (x < 0,\ x \geqslant k) \end{cases} \quad \ldots(1)$$

When a region from $x = 0$ to $x = 2k$ is considered, the partial patterns $g_1(x)$ and $g_2(x)$ are complementary, with a boundary at $x = k$.

Therefore, the partial pattern $g_2(x)$ whose logic level is complementary to that of $g_1(x)$ in a range $0 \leqslant x \leqslant 2k$ is given by:

$$g_2(x) = g_1 (x - k) \quad \text{....(2)}$$

An EXCLUSIVE OR operation on $g_1(x)$ and $g_2(x)$ of equations (1) and (2) (the operation is denoted by $g_1(x) \oplus g_2(x)$ gives:

$$g_1(x) \oplus g_2 (x) = \begin{cases} 1 & 0 \leqslant \times < 2k \\ 0 & x < 0,\ x \geqslant 2 \end{cases} \quad \text{....(3)}$$

This is illustrated in Figure 3.

The partial patterns $g_1(x)$ and $g_2(x)$ are respectively "seen" through a first cutting out "window" having a length of k bits and a second cutting out "window" shifted by k bits therefrom, and having the same length. EXCLUSIVE OR operations are performed on corresponding pairs of bits. If the partial patterns $g_1(x)$ and $g_2(x$ are seen through the first and second cutting out windows, all results of the EXCLUSIVE OR operations on the respective bits from 0 to $2k$ are "1" (in the case of positive logic) so that the presence of the partial patterns $g_1(x)$ and $g_2(x)$ can be detected.

The method of recognition of the pattern shown in Figure 1*a* by the first embodiment of the present invention will now be described.

The pattern of "1" and "0" levels in the region enclosed by the broken line *a*, i.e. the pattern "00111100", is a bilaterally complementary pattern with a boundary between the fourth and fifth bits. Let us assume that the specific pattern to be recognized is "1111." The first four bits are assumed to be the partial pattern $g_1(x)$ previously described, and the bits after the fourth bit are assumed to be the partial pattern $g_2(x)$. When the EXCLUSIVE OR operator is applied to corresponding bits of the partial patterns $g_1(x)$ and $g_2(x)$, the results are all "1" in the region $0 \leqslant x < 2k$, and the specific pattern "1111" can be detected. Even if, in this example, the pattern "00111100" is shifted to the left or right by two bits with respect to the region enclosed by the broken line *a*, i.e. it becomes "11110000" or "00001111", an EXCLUSIVE OR operation between the first four bits and the following four bits gives "1" for all the bits. Therefore, even if the specific pattern shifts to the right or left relative to the partial pattern cutting out windows (in the case of this example, the initial four bits and the final four bits correspond to the first and second windows, respectively) the specific pattern can be recognized.

Figure 4 shows schematically the principal elements of the first embodiment.

A binary input signal is fed to an input terminal 1 on a pattern cutting out circuit 2 for cutting out the partial patterns $g_1(x)$ and $g_2(x)$ described above. An EXCLUSIVE OR circuit 3 operates between corresponding bits of the partial patterns $g_1(x)$ and $g_2(x)$. A judging circuit 4 decides if an output of the EXCLUSIVE OR circuit 3 coincides with a reference corresponding to a logic output which is obtained from the EXCLUSIVE OR circuit 3 when a specific pattern is previously entered to the input terminal 31. An output terminal 5 gives a "1" (in the case of positive logic) when the input signal is the specific pattern.

Figure 5*a* shows the construction of the first embodiment. An input terminal 1 receives the binary signal. A partial pattern cutting out circuit 50, consists of an eight bit shift register having stages S_1 to S_8. EXCLUSIVE OR circuits 51 to 54 operate on respectively the pairs of bits output from the states S_4 and S_8, S_3 and S_7, S_2 and S_6, and S_1 and S_5 of the partial pattern cutting out circuit 50. The circuits 51 to 54 perform an EXCLUSIVE OR function between the bits of the first partial pattern S_1 to S_4, and those of the second partial pattern S_5 to S_8. Assuming the specific pattern to be "00111100" when it is fed to the input terminal 1, "00111100" is stored in the respective stages S_1 to S_8 of the partial pattern cutting out circuit 50, i.e. the shift register. Therefore, all the outputs of the EXCLUSIVE OR circuits 50 to 54 go to "1" (in the case of positive logic).

A judging circuit 55 receives the outputs from the EXCLUSIVE OR circuits 51 to 54, and is constructed as shown in Figure 6*a* or Figure 6*b*. In the example shown in Figure 6*a*, the output signals from the EXCLUSIVE OR circuits 51 to 54 are fed to respective input terminals 60 to 63, and are summed by an adder 64. The output of the adder 64 is compared in a comparator 65 with a reference signal derived from a reference input terminal 66. When the output of the adder 64 and the reference signal are the same the comparator 65 delivers a pulse to an output terminal 5. When "00111100" (assuming this to be the specific pattern as in the foregoing example) is fed to the input terminal 1 (in Figure 5*a*), all the outputs of the EXCLUSIVE OR circuits 51 to 54 becomes "1" as described previously, and hence, the output of the adder 64 goes to "4". However, a value "4" has previously been

fed to the reference input terminal 66. Consequently, when the output of the adder 64 and the reference signal derived from the terminal 66 are compared by the comparator 65, the output which indicates that the two are the same appears as a pulse at the output terminal 5.

The judging circuit 55 can also be constructed as in Figure 6*b*, in which the arrangement of Figure 6*a* is further simplified. An AND circuit 67 has input terminals 60 to 63 to which the output signals of the EXCLUSIVE OR circuits 51 to 54 are respectively applied. As in the preceding example, when the specified pattern is applied to the input terminal 1 in Figure 5*a*, a pulse signal is obtained on an output terminal 5 of the AND circuit 67.

The partial pattern cutting out circuit 50 shown in Figure 5α is suitable when, for instance, "00111100" is the specified pattern. It is a characteristic of the pattern that the logic level "1" is maintained over four bits. Consider the case where the specified pattern is "0011001100". In this pattern, the logic level "1" is present at the third and fourth bits and at the seventh and eighth bits. When the first four bits and the last four bits are considered as partial patterns, these two partial patterns are complementary to each other. Thus, the characteristic parts of the specified pattern are non-consecutive in contrast to the previous example. For such a specified pattern, a modified partial pattern cutting out circuit may be constructed as shown in Figure 5*b*. More specifically, a partial pattern cutting out circuit 50' comprises a shift register, so as to provide outputs S_1 to S_4 corresponding to the first four bits of the specified pattern "0011001100" and outputs S_5 to S_8 corresponding to the last four bits. The fifth and sixth stages of the shift register have no output. The signals respectively stored in stages S_1 to S_8 of the shift register are fed to the EXCLUSIVE OR circuits as shown in Figure 5*a*. Thus, recognition of the specified pattern can be effected.

Another modification of the first embodiment will now be described, which is used for the recognition of a specified pattern, such as "001110001", in which partial patterns complementary to each other overlap.

In the case of the present example, the first six bits and the last six bits are "001110" and "110001" respectively. The patterns of "0" and "1" are completely complementary and overlap at the fourth to sixth bits.

A possible partial pattern cutting out circuit 50" for recognizing such a pattern is shown in Figure 5*c*. A shift register, consisting of nine stages S_1 to S_9, has twin outputs from the fourth to sixth stages S_4 to S_6. Thus, the outputs are derived so that EXCLUSIVE OR operations between the outputs of the stages S_1 to S_6 corresponding to the first partial pattern $g_1(x)$ and the outputs of the stages S_4 to S_9 corresponding to the second partial pattern $g_2(x)$ can be executed. The outputs of the partial pattern cutting out circuit 50" are applied to the EXCLUSIVE OR circuits in the same way as in Figure 5*a*, the required number of the EXCLUSIVE OR circuits being six in the case of this example. Where the arrangement shown in Figure 6*a* is adopted for the judging circuit 55, "6" is the reference signal which must be fed to the reference input terminal 66. Thus, the specified pattern "001110001" can be recognized.

The second embodiment of the present invention will now be described, which is capable of recognizing a two-dimensional pattern.

The principle of operation of this embodiment has been explained previously with reference to Figure 3. The application of the principle to a two-dimensional pattern will be described in greater detail, with reference to Figures 7*a* to 7*c*.

In Figure 7*a*, a hatched portion indicates a specified pattern. In the case of this example, it is a right-angled pattern POR whose vertex is $\overline{O}$

In order to recognize such a pattern, partial patterns are cut out, and EXCLUSIVE OR functions between brightness levels of corresponding image elements are taken (in the present case, the brightness level corresponding to the hatched portion is "1" and that corresponding to the other area is "0").

Consider the brightness levels of the image elements on a circumference whose centre is the vertex $\overline{O}$ and whose radius is r_1. Let a_1 - a_8 denote the brightness levels of the image elements on the circumference of a sector which extends by an angle θ_1 about the vertex $\overline{O}$, whose radius is r_1, and whose centre line is OP.

The image elements lie within two curves k_1 and k_2. For the sake of clarity, the relative size of the image elements has been exaggerated in Figure 7*a*. In fact, the image elements can almost be considered as points on a single curve.

The image elements a_1 to a_8 form the partial pattern $g_1(x)$, while the partial pattern $g_2(x)$ is formed by image elements b_1 to b_8 respectively. The elements b_1 to b_8 subtend an angle θ_1 at the point O, as do the elements a_1 to a_8. As can be seen from Figure 7*b*, the taking of the image elements b_1 to b_8 instead of the elements a_1 to a_8 is equivalent to rotating the object from a position POR to a position P'OR' (c.f. Eqn.2) but it is of course more practical to examine the elements a_1 to a_8 and b_1 to b_8 simultaneously, rather than physicaly rotate the object. The example shown produces a $g_2(\chi)$ and a $g_2(\chi)$ of "00001111" and "11110000", respectively.

So far, only the method of cutting out the partial patterns in the case of recognition of a right-angled pattern has been described. To recognize a specific pattern, however, it is sometimes necessary to determine the shape of the hatched portion POR in Figure 7*a* or, for example, the shape of a hatched portion E, as shown in Figure 7*c*. Distinguishing between the shapes of the specific pattern POR and the hatched portion E in the case of the present example is achieved thus. A pair of partial patterns is cut out through the windows in the sector of radius r_1 as previously described. Simultaneously, windows in a sector of radius r_2, are also used and partial patterns comprising the elements c_1 to c_4 and d_1 to d_4 are obtained. An EXCLUSIVE OR operation is carried out between c and d.

A modification will now be described of the way of cutting out partial patterns, reference being made to Figure 8*a*. The example shown in Figure 8*a* corresponds to the recognizing of the right-hand part of a pattern 80, as shown in Figure 8*b*. In the methods so far described, image elements on the circumferences of sectors corresponding to regions, in which the characteristic parts of the specified pattern are complementary have been considered, and partial patterns cut out. In contrast, in the example shown in Figure 8*a*, note is taken of the brightness levels of image elements in a certain specific region of the pattern. That is to say, note is taken of the fact that for the patterns of brightness levels on the right-hand side of the pattern 80 in Figure 8*b* shown by a hatched portion and the surrounding region, the portions within sectors UOV and U'OV' ($<UOV = <U'OV' = \theta_2$) are complementary. Image elements a_1 - a_{64} within the sector UOV form the partial pattern $g_1(x)$, while image elements b_1 - b_{64} within the sector U'OV' form the partial pattern $g_2(x)$. Cutting out the partial patterns by noting all the picture elements within a certain region in this manner is the limiting case of searching for partial patterns by changing the radius r to r_1 and r_2, as illustrated in Figure 7*c*. The processing after cutting out the partial patterns is the same as before.

Figure 9 is a diagram showing the second embodiment of the present invention in which a two-dimensional pattern is recognized by the use of an image pick-up device, such as an industrial television camera.

An image pick-up device 90, such as an industrial television camera, serves to convert light from an object into a single electrical signal varying with time, obtained by scanning the object at a fixed rate, as in a conventional television camera. The output signal from the image pick-up device 90 is fed into an analogue-to-digital converter 91 and is binary-encoded therein. The binary-encoded signal is subsequently fed into a pattern cutting-out circuit 92. A possible construction for the pattern cutting-out circuit 92 is shown in Figure 11.

The pattern cutting-out circuit shown in Figure 11 is a device for achieving the method of cutting out partial patterns, which is shown in Figure 8*a*. The pattern cutting-out circuit 92 consists of shift registers 111 to 113 connected in series, which have the capacity for storing all the elements of the image of the object and sixteen 12-bit shift registers 114 to 117, which have the capacity for storing all the elements of regions intended to be cut out from the respective shift registers 111 to 113, and which are respectively connected in series with the shift registers 111 to 113. The shift registers 111 to 113 and 114 to 117 are operated in synchronizm by timing pulses, which are received at a timing pulse input terminal 118. The timing pulses are produced by a timing signal generator 900 (Figure 9) and a possible construction thereof is shown in Figure 10.

Clock pulses are provided by a clock pulse generator 100. The clock pulses are applied to a counter 101, and are directly supplied to the timing pulse input terminal 118 in Figure 11 via an output terminal 103. Outputs of the counter 101 are connected to a counter 102, which counts down. The clock pulse generator 100 produces a 6 MHz signal. The counter 101 is so constructed as to provide one pulse when it has counted 382 input pulses, and the counter 102 is so constructed as to provide one pulse when it has counted 262 input pulses.

The operation of the counter 101 is such that it counts the output pulses of the clock pulse generator 100, oscillating at 6 MHz and that when it has counted 382 pulses, it produces a pulse to reset itself, and to simultaneously enter the pulse into the counter 102. In addition, the output signal from the counter 101 is employed to control the horizontal direction of the image pick-up device 90. The counter 102 counts the output pulses from the counter 101, and when it has counted 262 pulses, it resets itself and simultaneously delivers a pulse to one of a pair of output terminals 104, the output of the counter 101 being connected to the other one of the pair for the driving in a vertical direction of the image pick-up device. On the other hand, when the counter 101 and/or the counter 102 are/is counting the count values are fed to output terminals 105, and delivered to gate circuits 96 and 96', which will be described later.

Referring back to Figure 11, the operation of the partial pattern cutting-out circuit will be explained. As previously stated, the shift registers 114 to 117 have sufficient memory capacity to store the elements of the image of regions of the object corresponding to the

partial patterns to be cut out. They are so constructed that the bits of the shift registers 114 to 117 correspond to the inner elements a_1 - a_{64} and b_1 - b_{64} (In Figure 8*a*) in the manner shown, and provide logic levels indicating the brightness of each element. The stages of the shift registers correspond to the elements of the sector UOV in Figure 8*a*, for example, the stage S_{13} corresponds to the element a_1 and the stage S_{14} to the element a_2, and the same applies to the sector U'OV'. Thus, the partial pattern cutting-out windows are constructed. The terminals which provide the a_1 - a_{64} outputs constitute the second window. By adopting the construction just described, the partial patterns can be cut out by using as windows the two sectors UOV and U'OV' shown in Figure 8*a*, and while shifting the object in succession. When the object pattern stored in the shift registers 114 to 117 within the partial pattern cutting-out circuit coincides with the hatched portion in Figure 8*a* the presence of the specific pattern can be detected by carrying out the following operation.

Referring to Figure 9, f_1 and f_2 denote signals from the two groups a_1 - a_{64} and b_1 - b_{64}, which correspond to the sectors UOV and U'OV' obtained from the pattern cutting-out circuit 92. The signals f and f_2 are fed to an EXCLUSIVE OR gate 93, in order to perform EXCLUSIVE OR functions between image elements whose logic levels would be complementary if the specified pattern were present (for example, between a_1 and b_1, a_2 and b_2, ..., a_{64} and b_{64}). Thus, an EXCLUSIVE OR function is operated between the signals f_1 and f_2. A judging circuit 94 determines whether or not the partial pattern cut out corresponds to the specific pattern.

Possible constructions for the EXCLUSIVE OR gate 93 and the judging circuit 94 are shown in Figure 12.

In Figure 12, the signal f_1 corresponding to elements a_1 - a_{64}, and the signal f_2 corresponding to elements b_1 - b_{64} are fed into EXCLUSIVE OR gates 120 to 122 in such a manner that corresponding bits are fed to the same gate. By way of example, assume that the signals f_1 and f_2 are such that, as shown in Figure 8*a*, they are identical to the characteristic parts of the specified pattern. Then, all the outputs of the EXCLUSIVE OR gates 120 to 122 go to "1" (in the case of positive logic). The output signals are counted by a counter 123, whose output is compared in comparator 124 with a reference signal fed into a reference signal input terminal 125. Then, a coincidence output is provided from an output terminal 126 of the comparator 124. As the reference signal, "64" is entered in the case of the present example. As illustrated in Figure 6*b*, just as the judging circuit used in the recognition of the unidimensional pattern could be constructed of an "AND" circuit, so can the judging circuit 94.

By observing the output of the judging circuit 94, a pattern having an angle of 120°, as shown in Figure 8*a*, can be detected. However, patterns in which, as in the pattern shown in Figure 8*b*, the right-hand side and left-hand side are opposite in brightness levels cannot be detected by the methods so far described. Therefore, in order to recognize the specified pattern 80, the right and left of the pattern need to be further distinguished, and subsequent circuit stages after the judging circuit 94 in Figure 9 are necessary.

More specifically, in order to distinguish in the output of the judging circuit 94 whether the right side or left side of the specified pattern 80 is being viewed, a third partial pattern corresponding to a region F or F' in Figure 8*b* is cut out, and a signal f_3 is produced by the partial pattern cutting-out circuit 92.

Generally speaking, the third partial patterns F and F' may correspond to regions which lie in the vicinity of the partial patterns corresponding to two characteristic parts of the specified pattern, which are opposite in brightness level, and whose brightness levels differ from each other in the specified pattern. Signals are cut out from the stages of the shift registers 114 to 117 of Figure 11 corresponding to, for example, the position F or F' in Figure 8*b*.

The circuit arrangement for the second embodiment also includes a logic circuit 95, gate circuits 96 and 96', a memory circuit 97 and a co-ordinate computing circuit 98.

As shown in Figure 13, the logic circuit 95 has an input terminal 130, into which the logic level of the third partial pattern f_3 is entered, and an input terminal 131 into which the output of the judging circuit 94 is fed. The signals respectively delivered to the input terminals 130 and 131 are fed to an AND gate 132 and an "INHIBIT GATE" circuit 133. The "INHIBIT GATE" circuit 133 has an inverted input terminal 134. Assume that the partial patterns f_1 and f_2 cut out by the partial pattern cutting-out circuit correspond to the right side of Figure 8*b*, the signal f_3 of logic level "1", corresponding to the third partial pattern F', is fed to the input terminal 130. Therefore, the output of the AND gate 132 becomes "1", whilst that of the "INHIBIT GATE" circuit 133 goes to "0".

The circuit 96 and 96' are both AND gates. One input terminal of each of the AND gates 96 and 96' receives the corresponding one of the output signals from the AND gate 132 and the "INHIBIT GATE" circuit 133, while the other input terminal 139 receives the address in the horizontal (x-direction) from the timing signal generator 900, i.e. the output of the

counter 101 in Figure 10. Since the specified pattern 80 in the present example has characteristic parts which present opposite patterns in the horizontal direction, only the count of the counter 101 in the x-direction may be fed to the input terminal 139 in Figure 13. Where the specific pattern rotates by 90° and is situated longitudinally in the vertical direction, the address in the y direction or the count value of the counter 102 may be entered at the input terminal 139.

Assume that in Figure 13, the count of the counter 101 of the timing signal generator 900 appearing at terminal 105 in Figure 10 is received at the terminal 139, i.e. the count of the counter 102 is ignored.

Consider the case where, as previously described, the right side of the specified pattern 80, i.e. the side with the third partial pattern F' is cut out. Then, the AND gate 96 allows the signal from the terminal 139 to pass through, whereas the AND circuit 96' blocks it. Thus, the AND gate 96 operates so as to supply the register 135 of the memory circuit 97 with the count of the counter 101 when the AND gate 132 has its output at "1", i.e. with the horizontal x-direction address value existing at that time.

On the other hand, suppose that the object cut out corresponds to the left side of the specified pattern 80, i.e. the side on which the third partial pattern F is present. Then, conversely to the foregoing, the "INHIBIT GATE" circuit 133 has an output of "1", and the count of the counter 101, i.e. the x-direction address value is supplied to the register 136 through the AND gate 96'. The co-ordinate computing circuit 98 has a substractor 137, which evaluates the difference between the values stored in the registers 135 and 136 equal to the difference in address values or the distance in the x-direction between the third partial patterns F and F'. The value found by the subtractor 137 is compared in a comparator 138 with a reference signal which represents the distance between the third partial patterns F and F' of the pattern 80 originally specified. When they are equal, a pulse is produced at an output terminal 142. The actual count of the counter 101 when the third partial pattern is cut out may, in fact, be slightly in error. Therefore, the use of a single absolute value as a reference may introduce difficulties. Therefore, in the device shown in Figure 13, an error margin $\triangle L$ is allowed in the matching of the distance L between the third partial patterns F and F', with the reference value L':-

$$L' = L \pm \triangle L \quad \text{....(4)}$$

Thus, an upper limit and a lower limit are set, and upper and lower limit signals are fed into respective reference signal input terminals 140 and 141 on the comparator 138:-

$$\left.\begin{array}{l} \text{upper limit} = L + \triangle L \\ \\ \text{lower limit} = L - \triangle L \end{array}\right) \quad \text{....(5)}$$

If the value of the input to the comparator 138 lies between the upper limit and the lower limit of equation (5), a pulse is provided at the output terminal 142.

The operation of the system shown in Figure 9 has so far been described with reference to an object positioned at a particular angle relative to the image pick-up device 90. The system can still recognize the object if it is at other angles to the pick-up device 90, provided certain conditions are met.

Consider the right-hand side of the specified pattern 80. Even if the pattern is rotated by up to ± 60° about the point $\overline{O}$ in Figure 8a, the partial patterns cut out corresponding to the two sectors UOV and U'OV' are still complementary. Therefore, such a pattern can be recognized by the system, provided the condition regarding the value of L is satisfied. If the pattern is still to be recognized when rotated through up to ± θ°, then equation (5) must be replaced by:-

$$\left.\begin{array}{l} \text{upper limit} = (L + \triangle L)\cos\theta \\ \\ \text{lower limit} = (L - \triangle L)\cos\theta \end{array}\right) \quad \text{...(6)}$$

The third embodiment of the present invention (which employs the method illustrated by Figure 7c) will now be described. The embodiment is a combination of the circuit shown in Figure 11, and the circuit illustrated in Figure 14. The system shown in Figure 14 processes the four partial patterns a_1 - a_8, b_1 - b_8, c_1 - c_4 and d_1 - d_4 of radii r_1 and r_2, lying between the curves k_1 and d_2, and the curves k_3 and k_4 in Figure 7c, which are cut out by the shift registers 114 to 117 of the pattern cutting-out circuit shown in Figure 11, through windows corresponding to the four partial patterns.

The four partial patterns are fed to the input terminals 143 to 146. Sets of EXCLUSIVE

OR gates 930 and 931 operate between the partial patterns a_1 to a_8 and b_1 to b_8, and between the patterns c_1 to c_4 and d_1 to d_4 respectively. Judging circuits 940 and 941 constructed as shown in Figure 6*a* or *b* decide whether or not the cut out patterns are identical to the partial patterns of the specified pattern, which excludes the hatched portion E shown in Figure 7*c*. Assuming that partial patterns identical to those of the specified pattern are cut out, then the judging circuits 940 and 941 each deliver pulses to an AND gate 147, and a coincidence output is produced at an output terminal 148. If the cut out partial patterns include a part corresponding to the hatched portion E shown in Figure 7c, a pulse is produced by the judging circuit 940, but not by the judging circuit 941. Therefore, no pulse appears at the output terminal 148, and the situation can be distinguished from the previous case where the partial patterns identical to those of the specified pattern are cut out.

WHAT WE CLAIM IS:-

1. A pattern recognition system for detecting the presence of a specified pattern in a binary signal pattern, the specified pattern including two portions which have logic values opposite to each other in corresponding bits comprising:

first means arranged to derive from the binary signal pattern a pair of partial patterns having a predetermined position relative to each other;

second means connected to said first means and including a plurality of Exclusive-OR gates, each of which receives a respective pair of the corresponding bits of the pair of partial patterns; and

third means connected to the second means and arranged to generate a coincidence signal indicating the presence of the specified pattern when a given number of said Exclusive-OR gates produces a predetermined output signal thus indicating the presence of a pattern.

2. A pattern recognition system according to claim 1, wherein said first means comprises a memory for storing signals representative of said plurality of partial patterns.

3. A pattern recognition system according to claim 1 or 2, wherein said third means comprises an adder for adding the output signals from said second means, and a comparator connected to said adder for comparing an output from said adder to a reference value.

4. A pattern recognition system according to claim 1 or 2, wherein said third means comprises an AND circuit for performing an AND function on the output of said EXCLUSIVE OR circuit.

5. A pattern recognition system according to any one of the preceding claims, further including fourth means connected to said third means and for distinguishing between two complementary characteristic portions of said binary signal pattern.

6. A pattern recognition system according to claim 5, wherein said fourth means includes an AND circuit and an "INHIBIT" circuit for receiving signals corresponding to a further partial pattern extracted by said means circuit, and signals obtained from said third means.

7. A pattern recognition system according to claim 5, further comprising fifth means connected to said fourth means for calculating a distance between said two characteristic portions from co-ordinates of the partial patterns at the time when a output signal is obtained from said fourth means and for judging if the calculated distance is within predetermined limits.

8. A pattern recognition system according to claim 7, wherein said fifth means comprises two gates for gating signals representative of co-ordinates of the partial patterns derived with two output signals of said fourth means, two memories for storing output signals of said two gates, subtraction means for evaluating the difference between the signals representative of the co-ordinates stored in said two memories, and a comparator for comparing a value of the output signal of said subtraction means to a reference value.

9. A pattern recognition system substantially as herein described with reference to and as illustrated in Figure 5*a*, or any one of Figures 5*a* to 5*c* in combination with either Figure 6*a* or 6*b*, or Figure 9, or Figure 9 in combination with any one of Figures 10 to 13, or Figure 14 in combination with Figure 11 of the accompanying drawings.

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FIG. 1a

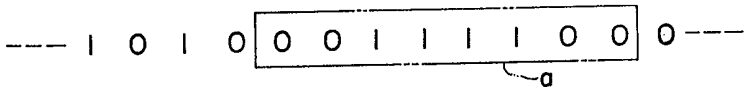


FIG. 1b

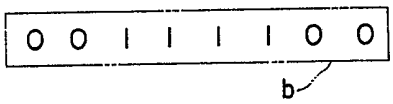


FIG. 2a

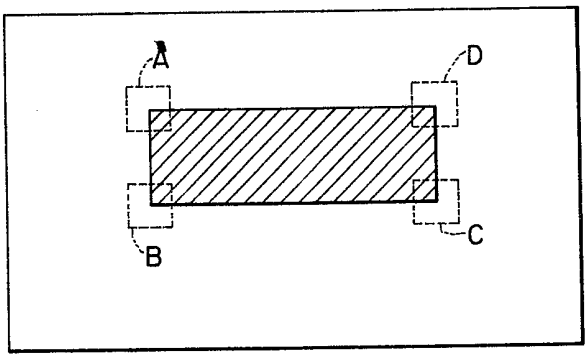


FIG. 2b

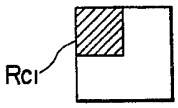


FIG. 2c

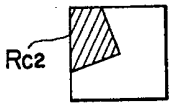


FIG. 2d

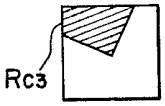


FIG. 3

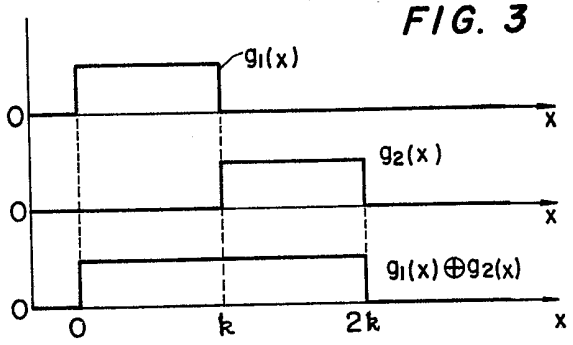


FIG. 4

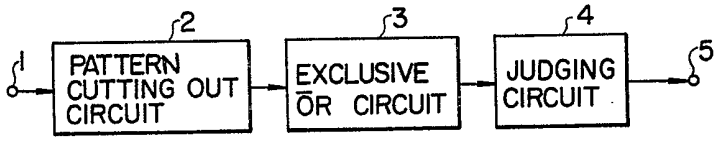


FIG. 5a

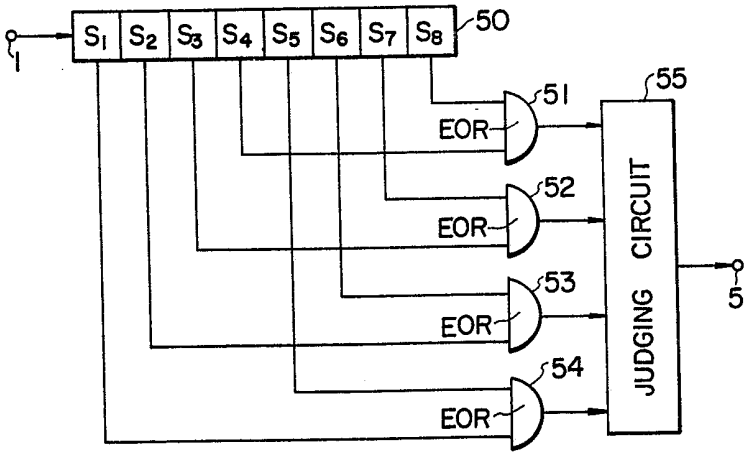


FIG. 5b

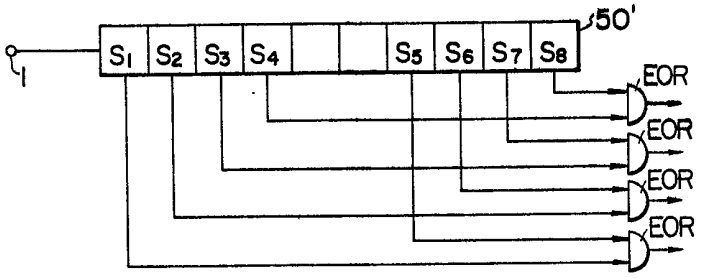


FIG. 5c

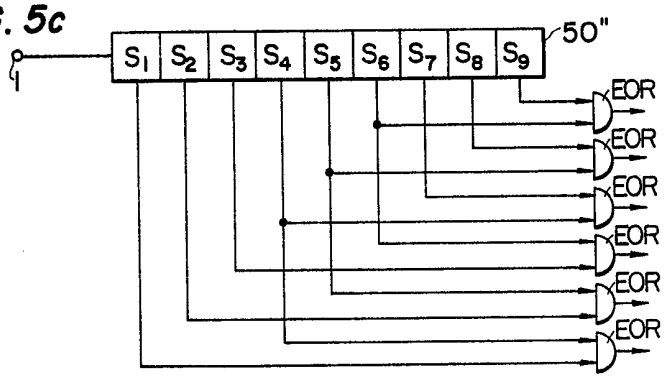


FIG. 6a

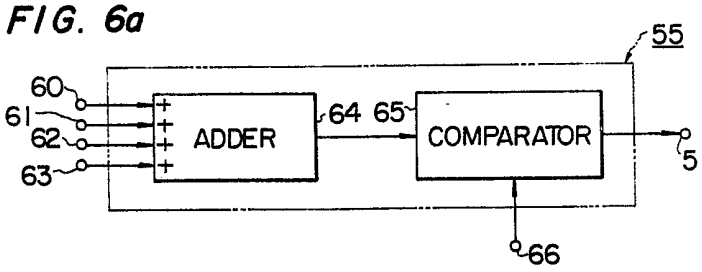


FIG. 6b

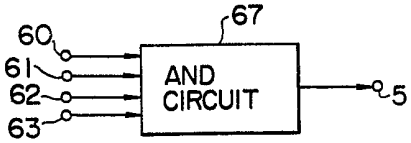


FIG. 7a

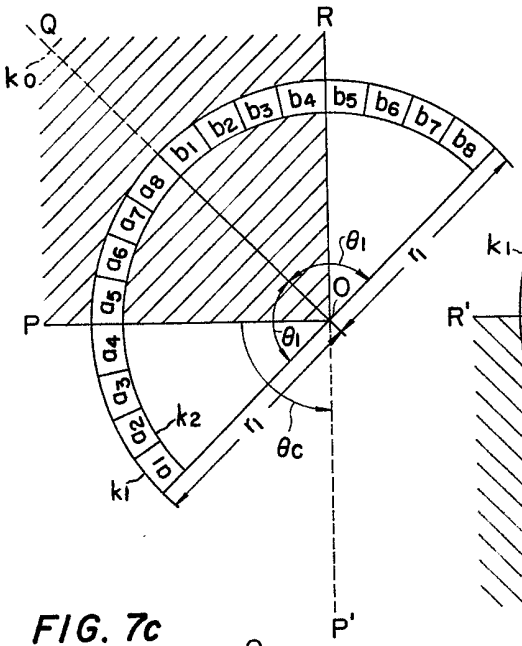


FIG. 7b

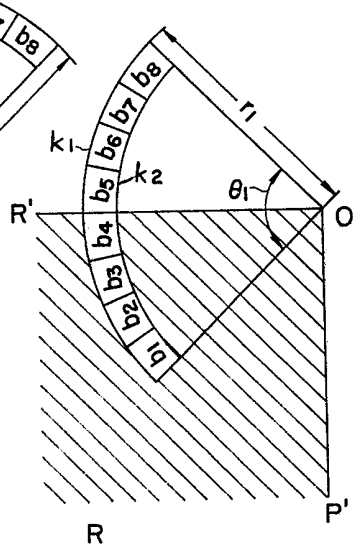


FIG. 7c

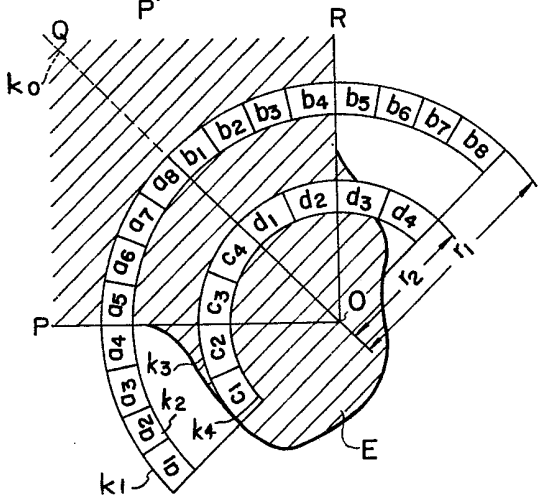


FIG. 8a

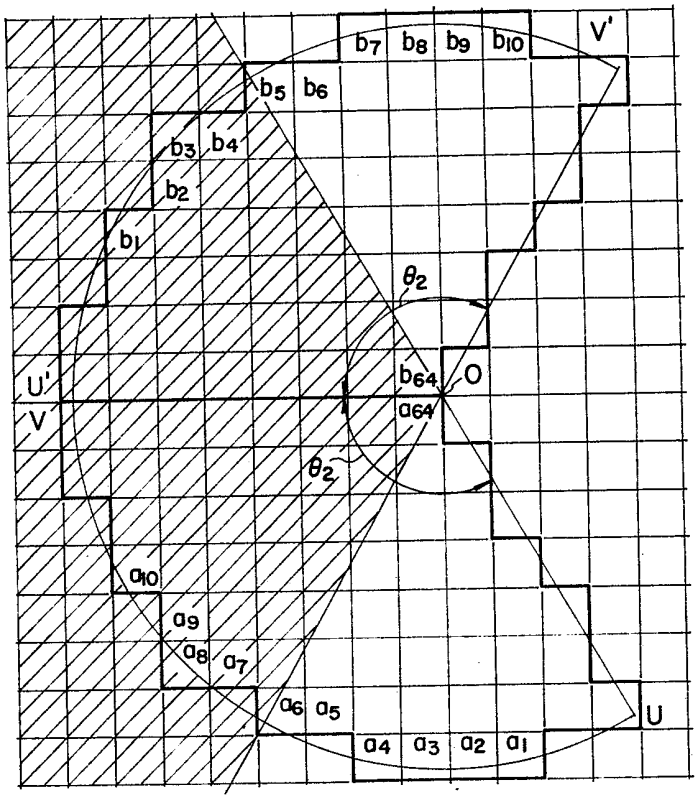

b7
b8
b9
b10
V'
b5
b6
b3
b4
b2
b1
θ2
U'
V
b64
O
a64
θ2
a10
a9
a8
a7
a6
a5
U
a4
a3
a2
a1

FIG. 8b

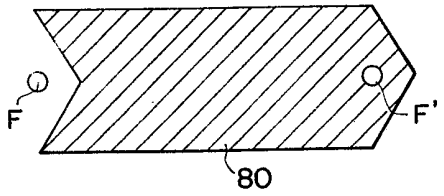

F
F'
80

FIG. 9

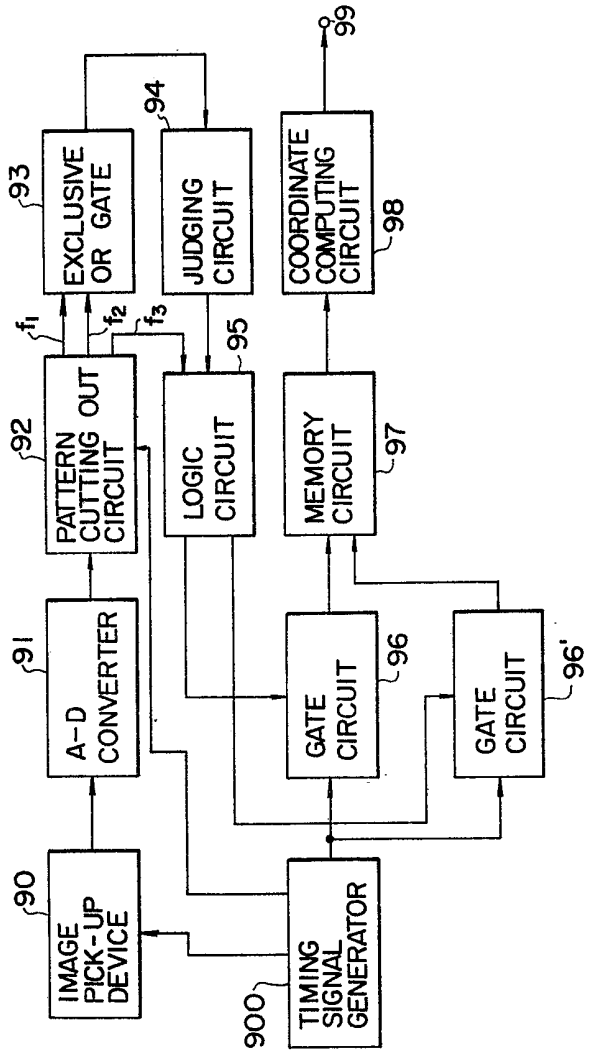

90
IMAGE PICK-UP DEVICE
91
A-D CONVERTER
92
PATTERN CUTTING OUT CIRCUIT
93
EXCLUSIVE OR GATE
94
JUDGING CIRCUIT
95
LOGIC CIRCUIT
96
GATE CIRCUIT
96'
GATE CIRCUIT
97
MEMORY CIRCUIT
98
COORDINATE COMPUTING CIRCUIT
99
900
TIMING SIGNAL GENERATOR
f1
f2
f3

FIG. 10

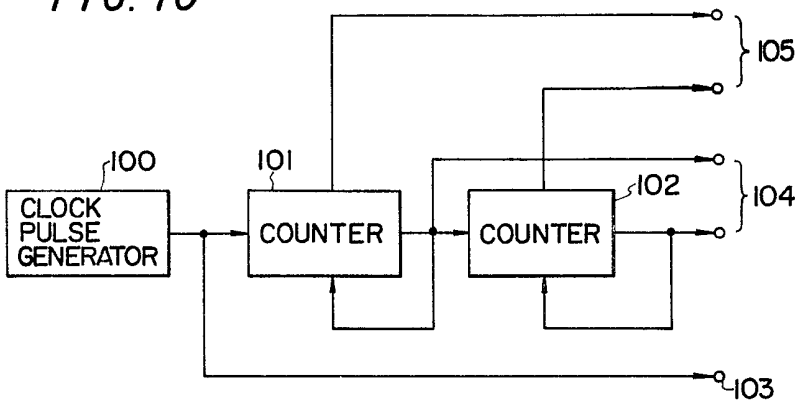
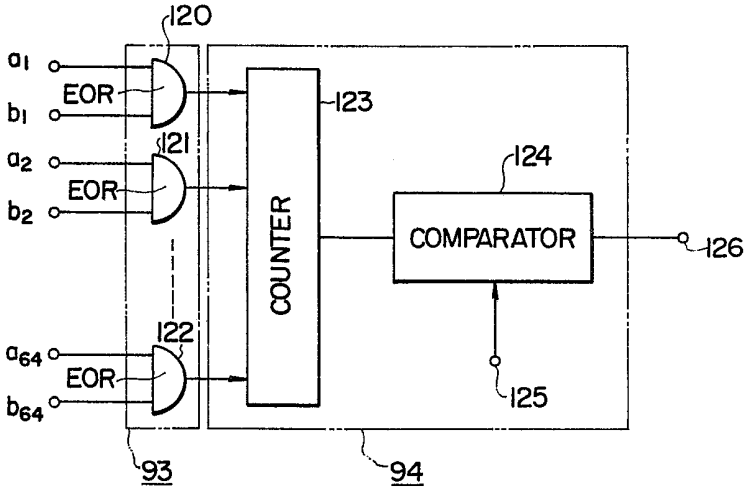

100
CLOCK PULSE GENERATOR
101
COUNTER
102
COUNTER
105
104
103

FIG. 12


120
a_1
EOR
b_1
121
a_2
EOR
b_2
122
a_{64}
EOR
b_{64}
123
COUNTER
124
COMPARATOR
125
126
93
94

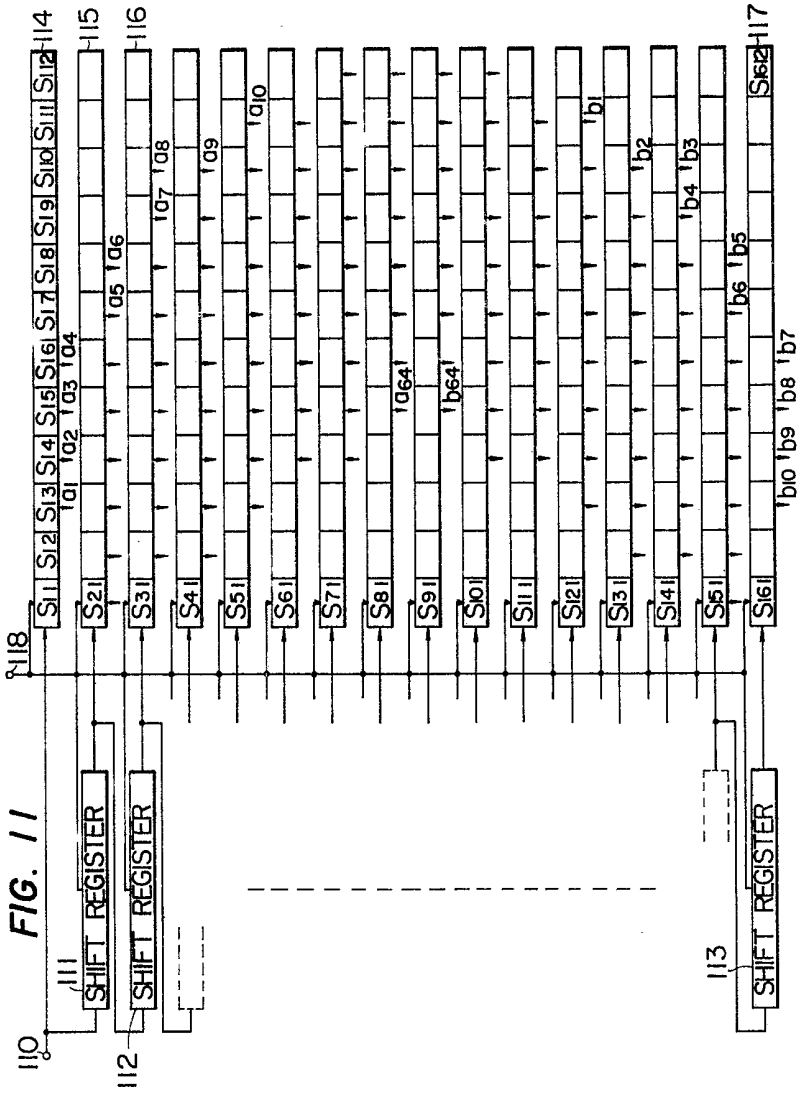


FIG. 11

1563616 COMPLETE SPECIFICATION
9 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 9

FIG. 13

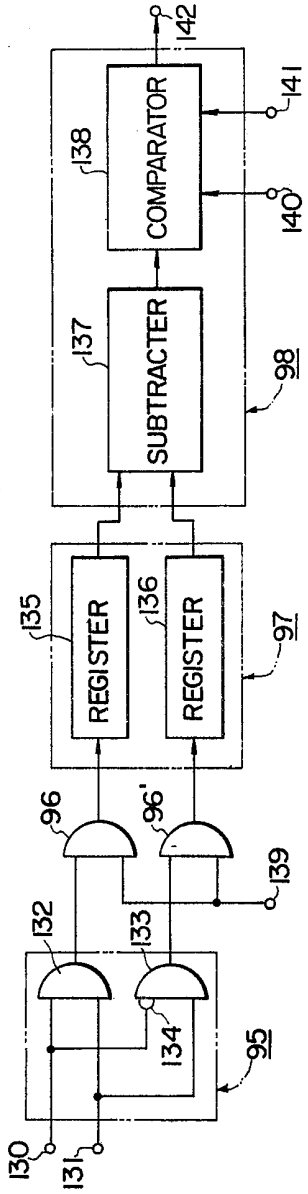


FIG. 14