(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 September 2010 (30.09.2010)

PCT

(10) International Publication Number
WO 2010/110951 A1

(51) International Patent Classification:
H05B 41/392 (2006.01) *H05B 41/36* (2006.01)
H05B 41/28 (2006.01) *H05B 41/38* (2006.01)

(21) International Application Number:
PCT/US2010/024288

(22) International Filing Date:
16 February 2010 (16.02.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/410,846 25 March 2009 (25.03.2009) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: DIMMING INTERFACE FOR POWER LINE

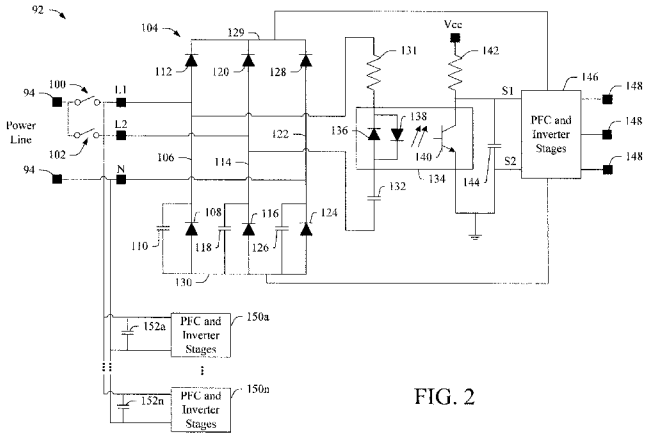


FIG. 2

(57) **Abstract**: An interface circuit for a lamp ballast includes first and second input power lines, L 1 and. L2, with first and second respective switches, and a neutral power line N, all coupled to a diode bridge. Closing one of the first or second input power lines L1 or L2 causes a photodiode in an opto-isolator coupled to the diode bridge to turn ON. which in turn causes a MOSFET in a control circuit to be in an open state. When in the open state, a first resistor coupled to the source of the MOSFET is included in the control circuit and causes a lamp attached thereto to operate in a dimmed state. When both input power line switches are closed. L 1 and L2 are both coupled to the diode bridge and thereby cause the phototransistor to be in an OFF state, which causes the MOSFET to close, thereby including a second resistor, coupled to the drain of the MOSFET. in the control circuit in parallel with the first resistor. This in turn causes the lamp to operate at full intensity.

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DIMMING INTERFACE FOR POWER LINE

BACKGROUND OF THE INVENTION

[0001] The present application relates to electronic lighting. More specifically, it relates to a dimming interface for a power line and will be described with particular reference thereto. It is to be appreciated that the present interface can also be used in other lighting applications and/or other power line applications, and is not limited to the aforementioned application.

[0002] In the past, dimmable ballast systems have typically been composed of multiple discrete ballasts. In order to achieve a lower light output, one or more of the ballasts would be shut off. Conversely, when greater light output is desired, more ballasts are activated. This approach has the drawback of only being able to produce discrete levels of light output. With each ballast only able to produce a single light output, the aggregate output is limited to what the various combinations of the ballasts present can produce. Moreover, this setup also requires multiple lamps for the same space to be lighted, resulting in an inefficient use of space.

[0003] Another approach in dimmable lighting applications has been to dim a single ballast by varying the operating voltage of the ballast, that is, by varying the voltage of the high frequency signal used to power the lamp. One drawback in such a system is that as the voltage of the high frequency signal is diminished, the lamp cathodes cool down. This can lead to the lamp extinguishing, and unnecessary damage to the cathodes. To avoid this problem, such systems apply an external cathode heating. While this solves the problem of premature extinguishing, the ballast is drawing power that is not being used to power the lamp. This decreases the overall efficiency of the ballast.

[0004] Another option is to reduce the range from full light output to a lower light output, but not low enough that external cathode heating is required. In T8 lamps, this amounts to a ballast that can change the lamp current from a high ballast factor level (typically 265mA of arc current) to a low ballast factor level of only 140mA. This provides a dimming range where a considerable amount of energy can be saved without sacrificing too much light. Associated with this high-low ballast factor approach is the

interface between the power line and the ballast control input, which determines the light level. Conventional dimming interfaces have 2 output levels: a high ballast factor at which full power is output, and a low ballast factor at which less than full power is output. A drawback of conventional dimming interfaces is that they are subject to capacitive loading by non-dimming ballasts coupled to the circuit, which can cause the dimming interface to malfunction.

[0005] The following description provides new systems and methods that overcome the above referenced problem caused by capacitive loading by other dimming or non-dimming ballasts.

BRIEF DESCRIPTION OF THE INVENTION

[0006] A first input power line L1 with a first switch, a second input power line L2 with a second switch, and a neutral input power line N comprise the external power source to which the ballast is connected. The interface circuit comprises a diode bridge to which the first input power line is coupled via the first switch; to which the second input power line is coupled via the second switch; and to which the neutral power line is directly coupled. The interface circuit further comprises a phototransistor that is in an OFF state when the first and second switches are closed so that the first and second input lines are connected to the diode bridge, and is in an ON state when only one of the first and second switches are closed.

[0007] According to another aspect, a control circuit for a dimming interface circuit for controlling an electric device comprises a MOSFET that has a source coupled to a first resistor and a drain coupled to a second resistor, wherein the second resistor is excluded from the circuit when the MOSFET is open, and wherein the second resistor is included in the circuit, in parallel with the first resistor, when the MOSFET is closed.

[0008] According to yet another aspect, a method of dimming one or more lamps comprises providing first and second switchable input power lines L1 and L2, and a neutral power line N, and closing one of the switchable input power lines L1 or L2 to cause a phototransistor in an interface circuit to turn ON, which causes a MOSFET in a

control circuit to be in an open state during which at least one lamp coupled to the control circuit is in a dimmed state. The method further comprises closing both of the switchable input power lines L1 and L2 to cause a phototransistor to turn OFF, which causes the MOSFET to be in a closed state during which the at least one lamp is in a non-dimmed state.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGURE 1 a ballast circuit, such as an instant start ballast or the like, which may be employed in conjunction with the herein-described dimming interface circuit.

[0010] FIGURE 2 illustrates the dimming interface circuit, which is insensitive to capacitive load caused by one or more non-dimming ballasts coupled to common power lines.

[0011] FIGURE 3 illustrates a simplified view of a control circuit in the PFC and inverter circuitry that is affected by the interface circuit, in accordance with one or more aspects described herein.

DETAILED DESCRIPTION OF THE INVENTION

[0012] The following relates to a dimming interface or ballast for a power line. The dimming ballast mitigates capacitive loading caused by non-dimming interfaces or ballasts coupled to the same power line. The described dimming ballast is insensitive to the capacitive loading caused by non-dimming ballasts.

[0013] With reference to FIGURE 1, a ballast circuit **10**, such as an instant start ballast or the like, which may be employed in conjunction with the herein-described dimming interface circuit **92**.The ballast circuit includes an inverter circuit **12** resonant circuit or network **14**, and a clamping circuit **16**. A DC voltage is supplied to the inverter **12** via a positive bus rail **18** running from a positive voltage terminal **20**. DC voltage is derived from the PFC stage. The circuit **10** completes at a common conductor **22** connected to a

ground or common terminal **24**. A high frequency bus **26** is generated by the resonant circuit **14** as described in more detail below. First, second, third, through n^{th} lamps **28, 30, 32, 34** are coupled to the high frequency bus **26** via first, second, third, and n^{th} ballasting capacitors **36, 38, 40, 42**. Thus, if one lamp is removed, the others continue to operate. It is contemplated that any number of lamps can be connected to the high frequency bus **26**. E.g., lamps **28, 30, 32, 34** are coupled to the high frequency bus **26** via an associated ballasting capacitor **36, 38, 40, 42**.

[0014] The inverter **12** includes analogous upper and lower, that is, first and second switches **44** and **46**, for example, two n-channel MOSFET devices (as shown), serially connected between conductors **18** and **22**, to excite the resonant circuit **14**. It is to be understood that other types of transistors, such as p-channel MOSFETs, other field effect transistors, or bipolar junction transistors may also be so configured. The high frequency bus **26** is generated by the inverter **12** and the resonant circuit **14** and includes a resonant inductor **48** and an equivalent resonant capacitance that includes the equivalence of first, second, and third capacitors **50, 52, 54** and ballasting capacitors **36, 38, 40, 42** which also prevent DC current from flowing through the lamps **28, 30, 32, 34**. Although they do contribute to the resonant circuit, the ballasting capacitors **36, 38, 40, 42** are primarily used as ballasting capacitors. The switches **44** and **46** cooperate to provide a square wave at a common first node **56** to excite the resonant circuit **14**.

[0015] First and second gate drive circuits, generally designated **60** and **62**, respectively, include first and second driving inductors **64, 66** that are secondary windings mutually coupled to the resonant inductor **48** to induce a voltage in the driving inductors **64, 66** proportional to the instantaneous rate of change of current in the resonant circuit **14**. First and second secondary inductors **68, 70** are serially connected to the first and second driving inductors **64, 66** and the gates of switches **44** and **46**. The gate drive circuits **60, 62** are used to control the operation of the respective upper and lower switches **44, 46**. More particularly, the gate drive circuits **60, 62** maintain the upper switch **44** "on" for a first half cycle and the lower switch **46** "on" for a second half cycle. The square wave is generated at the node **56** and is used to excite the resonant circuit. First and second bi-directional voltage clamps **71, 73** are connected in parallel to the secondary inductors **68, 70**, respectively, each including a pair of back-to-back Zener diodes. The bi-directional

voltage clamps **71, 73** act to clamp positive and negative excursions of gate-to-source voltage to respective limits determined by the voltage ratings of the back-to-back Zener diodes. Each bi-directional voltage clamp **71, 73** cooperates with the respective first or second secondary inductor **68, 70** so that the phase angle between the fundamental frequency component of voltage across the resonant circuit **14** and the AC current in the resonant inductor **48** approaches zero during ignition of the lamps.

[0016] Upper and lower capacitors **72, 74** are connected in series with the respective first and second secondary inductors **68, 70**. In the starting process, the capacitor **72** is charged from the voltage terminal **18**. The voltage across the capacitor **72** is initially zero, and during the starting process, the serially connected inductors **64** and **68** act essentially as a short circuit, due to the relatively long time constant for charging the capacitor **72**. When the capacitor **72** is charged to the threshold voltage of the gate-to-source voltage of the switch **44** (e.g. 2-3 Volts), the switch **44** turns ON, which results in a small bias current flowing through the switch **44**. The resulting current biases the switch **44** in a common drain, Class A amplifier configuration. This produces an amplifier of sufficient gain such that the combination of the resonant circuit **14** and the gate control circuit **60** produces a regenerative action that starts the inverter into oscillation, near the resonant frequency of the network including the capacitor **72** and the inductor **68**. The generated frequency is above the resonant frequency of the resonant circuit **14**. This produces a resonant current that lags the fundamental of the voltage produced at the common node **56**, allowing the inverter **12** to operate in the soft-switching mode prior to igniting the lamps. Thus, the inverter **12** starts operating in the linear mode and transitions into the switching Class D mode. Then, as the current builds up through the resonant circuit **14**, the voltage of the high frequency bus **26** increases to ignite the lamps, while maintaining the soft-switching mode, through ignition and into the conducting, arc mode of the lamps.

[0017] During steady state operation of the ballast circuit **10**, the voltage at the common node **56**, being a square wave, is approximately one-half of the voltage of the positive terminal **20**. The bias voltage that once existed on the capacitor **72** diminishes. The frequency of operation is such that a first network **76** including the capacitor **72** and the inductor **68** and a second network **78** that includes the capacitor **74** and the inductor **70**

are equivalently inductive. That is, the frequency of operation is above the resonant frequency of the identical first and second networks **76, 78**. This results in the proper phase shift of the gate circuit to allow the current flowing through the inductor **48** to lag the fundamental frequency of the voltage produced at the common node **56**. Thus, soft-switching of the inverter **12** is maintained during the steady-state operation.

[0018] The output voltage of the inverter **12** is clamped by serially connected clamping diodes **80, 82** of the clamping circuit **16** to limit high voltage generated to start the lamps **28, 30, 32, 34**. The clamping circuit **16** further includes the second and third capacitors **52, 54**, which are essentially connected in parallel to each other. Each clamping diode **80, 82** is connected across an associated second or third capacitor **52, 54**. Prior to the lamps starting, the lamps' circuits are open, since impedance of each lamp **28, 30, 32, 34** is seen as very high impedance. The resonant circuit **14** is composed of the capacitors **36, 38, 40, 42, 50, 52,** and **54** and the resonant inductor **48**. The resonant circuit **14** is driven near resonance. As the output voltage at the common node **56** increases, the clamping diodes **80, 82** start to clamp, preventing the voltage across the second and third capacitors **52, 54** from changing sign and limiting the output voltage to a value that does not cause overheating of the inverter **12** components. When the clamping diodes **80, 82** are clamping the second and third capacitors **52, 54** the resonant circuit **14** becomes composed of the ballast capacitors **36, 38, 40, 42** and the resonant inductor **48**. That is, the resonance is achieved when the clamping diodes **80, 82** are not conducting. When the lamps ignite, the impedance decreases quickly. The voltage at the common node **52** decreases accordingly. The clamping diodes **80, 82** discontinue clamping the second and third capacitors **52, 54** as the ballast **10** enters steady state operation. The resonance is dictated again by the capacitors **36, 38, 40, 42, 50, 52,** and **54** and the resonant inductor **48**.

[0019] In the manner described above, the inverter **12** provides a high frequency bus **26** at the common node **56** while maintaining the soft switching condition for switches **44, 46**. The inverter **12** is able to start a single lamp when the rest of the lamps are lit because there is sufficient voltage at the high frequency bus to allow for ignition. An interface inductor **90** is coupled to the inductors **68** and **70**. The interface inductor **90**

provides an interface between an interface circuit **92** and the inverter **12**. The dimming interface circuit **92** is coupled to control leads **94** (e.g., power lines).

[0020] FIGURE 2 illustrates the dimming interface circuit **92**, which is insensitive to capacitive load caused by one or more non-dimming ballasts coupled to common power lines. As is known, an instant start ballasts may have interfaces to a power line that control light output. The interface described herein has three input wires, one of which is a neutral wire, **N**. The other two input lines, **L1** and **L2**, control the state of dimming. If either **L1** or **L2** is connected to the power line, (e.g., by respective switches **100** or **102**), then the ballast circuit **10** lights the lamps to a less-than-full intensity (e.g., 50-60%, or some other predetermined intensity level). When both switches **100**, **102** are closed, both **L1** and **L2** are connected to the power line, and the ballast drives the lamps to full intensity. Thus, the ballast sheds the lighting load to a dimming level (e.g., 50-60%, or some other predetermined intensity level) when only one of lines **L1** and **L2** are connected to power, and drives the lamps to full intensity when both of lines **L1** and **L2** are connected to power. It will be understood that **L1**, **L2** and the external switches are external to the ballast. In one example, the switches **100**, **102** are wall switches. **L1** and **L2** are a connection to the power line.

[0021] If other ballasts (e.g. non-dimming ballasts) are connected to the switches **100**, **102**, they do not inhibit the operation of the interface circuit **92** due to the bridge network **104**. The bridge **104** comprises a bus **106** that is coupled to **L1** and to a cathode of a diode **108**, which is coupled in parallel with a capacitor **110** to the bus **106**. The bus **106** is further coupled to an anode of a diode **112**. The bridge **104** further comprises a bus **114** that is coupled in similar fashion to **L2**, and to a cathode of a diode **116** that is coupled to the bus **114** in parallel with a capacitor **118**. The bus **114** is further coupled to an anode of a diode **120**. The bridge **104** further comprises a bus **122** that is coupled in similar fashion to the neutral line N, and to a cathode of a diode **124** that is coupled to the bus **122** in parallel with a capacitor **126**. The bus **122** is further coupled to an anode of a diode **128**. The cathodes of diodes **112**, **120**, and **128** are coupled to a common bus **129**. The anodes of diodes **108**, **116**, and **124** are coupled to a common bus **130** in addition to the respective capacitors **110**, **118**, and **126**, which are also coupled to the bus **130**.

[0022] Bus **106** is coupled to a resistor **131**, and bus **114** is coupled to a capacitor **132**. The resistor **131** and capacitor **132** are coupled to an opto-isolator **134** that includes two light-emitting diodes (LED) **136** and **138**, as well as a phototransistor **140**. The resistor **131** is coupled to a cathode of the diode **136** and to an anode of the LED **138**, and the capacitor is coupled to an anode of the diode **136** and to a cathode of the LED **138**. The LEDs **136** and **138** are connected in an anti-parallel connection, anode to cathode. As the power line voltage changes polarity, each half-cycle, current can flow through each LED, thereby doubling the frequency of the signal that appears across the capacitor **144**. Thus both halves of the power line can turn the phototransistor **140** on.

[0023] The phototransistor **140** is coupled line **S1**, and to a resistor **142** that is further coupled to Vcc. The emitter of the phototransistor **140** is coupled to ground. A capacitor **144** is coupled between lines **S1** and **S2**, which in turn are coupled to a power factor correction (PFC) and inverter circuitry **146**. The PFC an inverter circuitry **146** is coupled to one or more lamps **148**. In one example, the PFC and inverter circuitry **146** includes the ballast **10** of Figure 1, although it is not limited thereto and may comprise additional PFC circuitry as described with regard to Figure 3.

[0024] One or more non-dimming ballasts **150a-150n** may be coupled to the lines **L1**, **L2**, and **N**, as illustrated, each non-dimming ballast **150** has a respective capacitor **152** coupled between the connection to the neutral line N and the connection to lines **L1** and **L2**. It is the capacitor(s) **150** that contribute a capacitive load that can cause conventional dimming interfaces or ballasts to fail. However, the bridge **104** and the opto-isolator **134** of the herein-described interface **92** make the interface insensitive to such capacitive loading, thereby permitting the dimming interface to function properly even when such non-dimming ballasts are also coupled to the lines **L1**, **L2** and **N**.

[0025] In one example, the diodes **108**, **112**, **116**, **120**, **124**, and **128** are S2J (General Semiconductor) diodes. The capacitors **110**, **118**, **126**, and **132** may be 100nf capacitors. The resistor **131** may be a 5kΩ resistor. The resistor **142** may be a 100kΩ resistor. The opto-isolator **134** may be a Fairchild Semiconductor FOD814. It is to be appreciated that the foregoing example(s) is/are provided for illustrative purposes and that the subject innovation is not limited to the specific values or ranges of values presented therein.

Rather, the subject innovation may employ or otherwise comprise any suitable values or ranges of values, as will be appreciated by those of skill in the art.

[0026] With continued reference to Figure 2, FIGURE 3 illustrates a simplified view of a ballast control circuit **158** in the PFC and inverter circuitry **146** that is affected by the interface circuit **92**, in accordance with one or more aspects described herein. The control circuit **158** includes a capacitor **160**, a resistor **162**, and a resistor **164** coupled in series, wherein the capacitor **160** is further coupled to the bus **26** of Figure 1. The resistor **164** is coupled to a resistor **166** and a resistor **168**. The resistor **168** is coupled to drain of a gate such as a MOSFET **170** (or any other suitable type of switch), while the resistor **166** is coupled to a source of the MOSFET **170**. The gate of the MOSFET **170** is coupled to an anode of a Zener diode **172**, to a capacitor **173**, and to a resistor **174**. The capacitor **173** and resistor **174** in turn are coupled to the source of the MOSFET **170**, to the resistor **166**, and to a switch **S2**. The switch **S1** is coupled to the cathode of the Zener diode **172**.

[0027] The control circuit **158** further includes a resistor **176** that is coupled to each of the resistors **164**, **166**, and **168**, as well as to a gate of a MOSFET **178** and a capacitor **180**. A cathode of a Zener diode **182** is coupled to a source of the MOSFET **178**, and the anode of the Zener diode **182** is coupled to the resistor **166**, the source of the MOSFET **170**, the capacitor **173**, and the resistor **174**, all of which are coupled to **S2**. The anode of the Zener diode **182** is further coupled to the anodes of diodes **184** and **186**. The drain of the MOSFET **178** is coupled to the capacitor **180** and to cathodes of diodes **188** and **190**. The anode of diode **188** and the cathode of diode **184** are coupled to each other and to **C1** (Figure 1), which the anode of diode **190** and the cathode of diode **186** are coupled to each other and to **C2** (Figure 1).

[0028] When **L1** or **L2** is connected, the phototransistor **140** of Figure 2 is in an ON state, and low dimming is achieved. When the phototransistor **140** is ON, the MOSFET is OFF (e.g., open), and resistor **168** is taken out of the control circuit. However, when both **L1** and **L2** are connected (when switches **100** and **102** are both closed), current to the opto-isolator goes to zero, and the phototransistor **140** turns OFF. This causes the MOSFET **170** to turn ON (e.g., closed), which puts resistor **168** in parallel with resistor **166**, causing the lamps coupled to the PFC and inverter circuitry **156** to go high (e.g., to

output light at full intensity). When **L1** or **L2** is disconnected again, the phototransistor **140** turns back ON and the MOSFET **170** turns OFF, removing resistor **168** from the circuit and causing the lamps to dim.

[0029] In one example, the capacitor(s) **160,** may be a 100pF capacitor. The resistors **162**, **164** may be 1MΩ resistors, and the resistor **166** may be a 200kΩ resistor. The MOSFETs **170**, **178** may be BSS138 MOSFETs, and the Zener diodes **172**, **182** may be 1N5232 Zener diodes. To further this example, the capacitor **173** may have a value of 1μF, the resistor **174** may be a 100kΩ resistor, and the resistor **174** may have a value of 10kΩ. The capacitor **180** may be a 10nF capacitor, and the diodes **184**, **186**, **188**, and **190** may be 1N4148 diodes.

[0030] It is to be appreciated that the foregoing example(s) is/are provided for illustrative purposes and that the subject innovation is not limited to the specific values or ranges of values presented therein. Rather, the subject innovation may employ or otherwise comprise any suitable values or ranges of values, as will be appreciated by those of skill in the art.

[0031] The invention has been described with reference to the preferred embodiments. Obviously, modifications and alterations will occur to others upon reading and understanding the preceding detailed description. It is intended that the invention be construed as including all such modifications and alterations.

WHAT IS CLAIMED IS:

1. A dimming interface circuit, comprising:

a first input power line L1 with a first switch;

a second input power line L2 with a second switch;

a neutral input power line N;

a diode bridge:

to which the first input power line is coupled via the first switch;

to which the second input power line is coupled via the second switch; and

to which the neutral power line is directly coupled; and

a phototransistor that is in an OFF state when the first and second switches are closed so that the first and second input lines are connected to the diode bridge, and is in an ON state when only one of the first and second switches are closed.

2. The interface circuit as set forth in claim 1, coupled to a control circuit that includes a first resistor and a second resistor, coupled to a gate, wherein the gate is open when the phototransistor is in an ON state, causing at least one lamp coupled to the control circuit to be in dimmed state, and wherein the gate is closed when the phototransistor is in an OFF state, causing the at least one lamp to be in a full-intensity state.

3. The interface circuit as set forth in claim 2, wherein the gate is a MOSFET.

4. The interface circuit as set forth in claim 3, wherein closing one of the first switch and the second switch causes the phototransistor to enter the ON state.

5. The interface circuit as set forth in claim 3, wherein closing both of the first switch and the second switch causes the phototransistor to enter the OFF state.

6. The interface circuit as set forth in claim 2, wherein the second resistor is excluded from the control circuit when the gate is open.

7. The interface circuit as set forth in claim 1, wherein the second resistor is included the control circuit, in parallel with the first resistor when the gate is closed.

8. The interface circuit as set forth in claim 1, wherein the phototransistor is included in an opto-isolator.

9. The interface circuit as set forth in claim 8, wherein the diode bridge includes a first bus that is coupled to first and second diodes, to the first input power line L1, and to the opto-isolator via a resistor.

10. The interface circuit as set forth in claim 9, wherein the diode bridge includes a second bus that is coupled to third and fourth diodes, to the second input power line L2, and to the opto-isolator via a capacitor.

11. The interface circuit as set forth in claim 10, wherein the diode bridge includes a third bus that is coupled to fifth and sixth diodes, and to the neutral power line N.

12. A control circuit for a dimming interface circuit for controlling an electric device, comprising:

a MOSFET that has a source coupled to a first resistor, a first capacitor, and a switch S2, and a drain coupled to a second resistor;

wherein the second resistor is excluded from the circuit when the gate is open; and

wherein the second resistor is included in the circuit, in parallel with the first resistor, when the MOSFET is closed.

13. The control circuit as set forth in claim 12, coupled to an interface circuit with a photo transistor, wherein the gate is open when the phototransistor is in an ON state, and closed when the phototransistor is in an OFF state.

14. The control circuit as set forth in claim 13, wherein the phototransistor is included in an opto-isolator that is coupled to a diode bridge and to the control circuit.

15. The control circuit as set forth in claim 14, wherein the diode bridge comprises:

a first bus that is coupled to first and second diodes, to a first input power line L1, and to the opto-isolator via a resistor;

a second bus that is coupled to third and fourth diodes, to a second input power line L2, and to the opto-isolator via a capacitor; and

a third bus that is coupled to fifth and sixth diodes, and to a neutral power line N.

16. The control circuit as set forth in claim 15, wherein the first and second input power lines are coupled to a power source by first and second switches, respectively, and wherein the phototransistor is in the ON state when one of the first and seconds switches is closed and in the OFF state when both of the first and second switches are closed.

17. The control circuit as set forth in claim 12, wherein the gate is a MOSFET

18. A method of dimming one or more lamps, comprising:

providing first and second switchable input power lines L1 and L2, and a neutral power line N;

closing one of the switchable input power lines L1 or L2 to cause a phototransistor in an interface circuit to turn ON, which causes a MOSFET in a control circuit to be in an open state during which at least one lamp coupled to the control circuit is in a dimmed state; and

closing both of the switchable input power lines L1 and L2 to cause a phototransistor to turn OFF, which causes the MOSFET to be in a closed state during which the at least one lamp is in a full-intensity state.

19. The method according to claim 18, wherein closing the MOSFET causes a second resistor to be included in the control circuit in a parallel configuration with a first resistor, thereby reducing resistance in the control circuit and permitting the at least one lamp to operate at full intensity.

20. The method according to claim 19, further including coupling one or more non-dimming ballast circuits input power lines L1 and L2, and to the input neutral power line N.

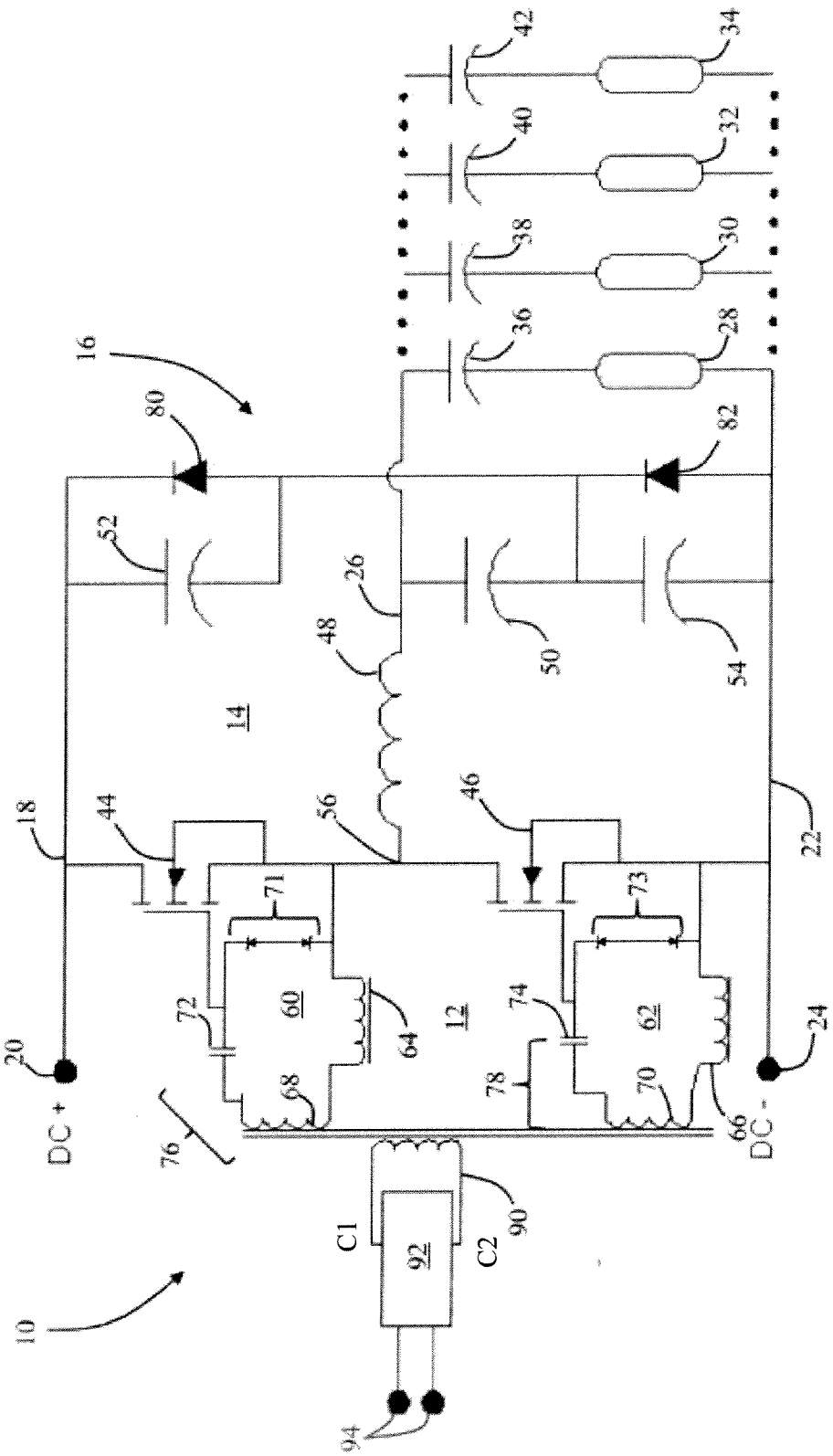

16
80
82
52
26
48
50
54
14
18
44
56
46
22
71
73
72
60
64
12
74
62
24
20
DC +
68
78
70
66
DC -
76
C1
92
C2
90
10
94
42
34
40
32
38
30
36
28

FIG. 1

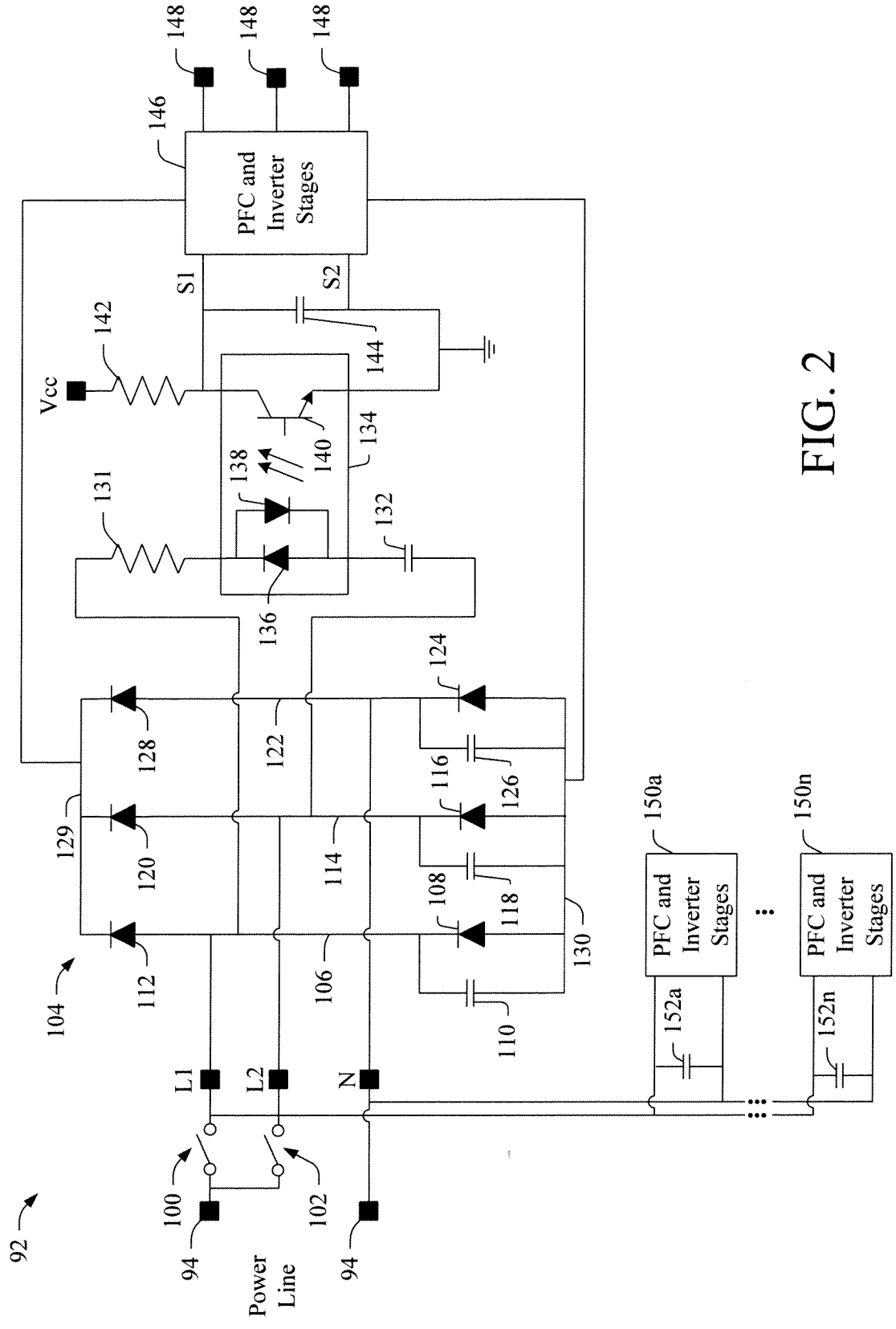

92
94
100
102
94
Power Line
L1
L2
N
104
106
108
110
112
114
116
118
120
122
124
126
128
129
130
131
132
134
136
138
140
142
144
146
148
148
148
PFC and Inverter Stages
S1
S2
Vcc
150a
152a
150n
152n
PFC and Inverter Stages
PFC and Inverter Stages

FIG. 2

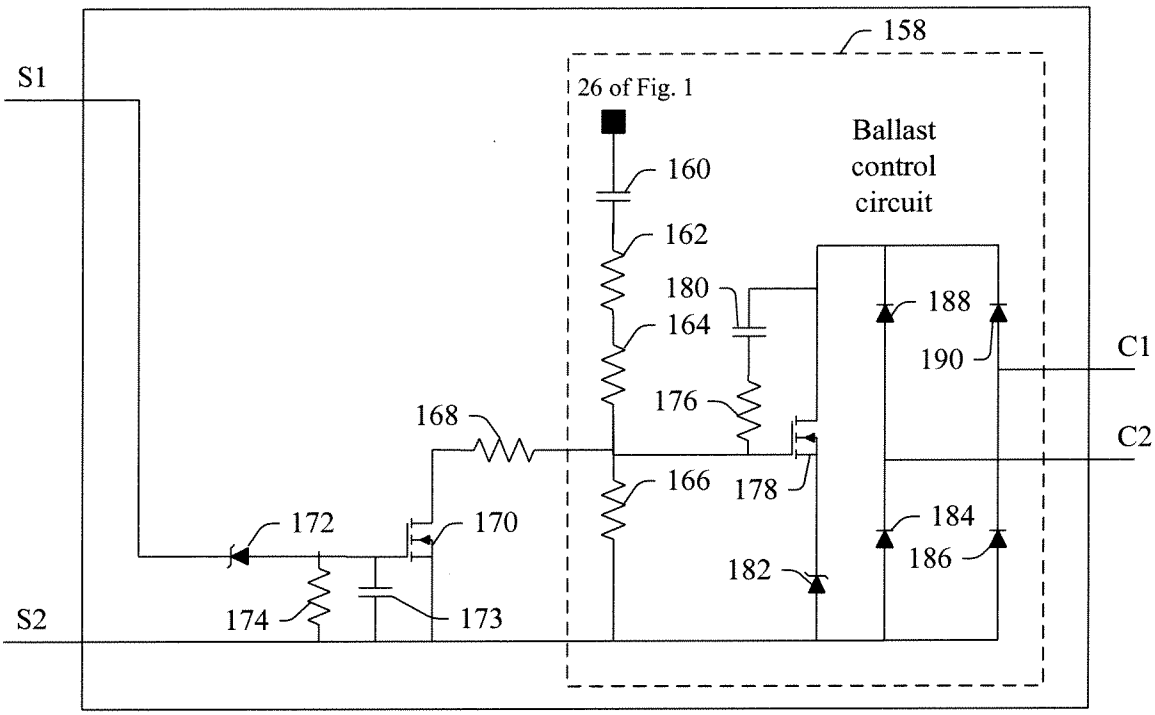

158
S1
26 of Fig. 1
Ballast
control
circuit
160
162
180
164
176
168
166
178
188
190
C1
C2
172
170
184
186
182
174
173
S2

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/024288

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05B41/392 H05B41/28 H05B41/36 H05B41/38
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2004/135523 A1 (TAKAHASHI KENICHIRO [JP] ET AL) 15 July 2004 (2004-07-15) paragraphs [0001] - [0010], [0 13] - [0015], [0 20], [0 36], [0 43] - [0048], [0 56]; figures 1-6	1-11, 18-20 12-17
X A	WO 2009/013656 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; WU MINGLIANG [US]) 29 January 2009 (2009-01-29) pages 1-5, 8; figures 1-3	1-11, 18-20 12-17
X A	US 6 329 767 B1 (SIEVERS RICHARD L [US]) 11 December 2001 (2001-12-11) column 5, line 35 - column 6, line 50; figures 1-5A1, 6	1-11, 18-20 12-17

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 June 2010	09/06/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hagan, Colm

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2010/024288

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 982 111 A (MOISIN MIHAIL S [US]) 9 November 1999 (1999-11-09) the whole document	1-11, 18-20 12-17
X A	US 2004/100205 A1 (TAKAHASHI KENICHIROU [JP] ET AL) 27 May 2004 (2004-05-27) the whole document	1-11, 18-20 12-17
X,P	US 2009/218953 A1 (NERONE LOUIS R [US] ET AL) 3 September 2009 (2009-09-03) paragraph [0022]; figure 3	12-17
X	US 2007/176564 A1 (NERONE LOUIS R [US] ET AL NERONE LOUIS R [US] ET AL) 2 August 2007 (2007-08-02) the whole document	12-17
X	EP 1 435 764 A1 (MATSUSHITA ELECTRIC IND CO LTD [JP]) 7 July 2004 (2004-07-07) paragraphs [0063] - [0069]; figure 6	12-17
X	US 2004/113564 A1 (GLASER JOHN STANLEY [US] ET AL) 17 June 2004 (2004-06-17) the whole document	12-17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2010/024288

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004135523 A1	15-07-2004	CN 1579115 A	09-02-2005
		EP 1478213 A1	17-11-2004
		WO 03071836 A1	28-08-2003
WO 2009013656 A1	29-01-2009	CN 101690414 A	31-03-2010
US 6329767 B1	11-12-2001	NONE	
US 5982111 A	09-11-1999	AU 3998095 A	26-04-1996
		WO 9610898 A2	11-04-1996
US 2004100205 A1	27-05-2004	AU 2003254959 A1	30-04-2004
		CN 1653863 A	10-08-2005
		EP 1538881 A1	08-06-2005
		WO 2004026005 A1	25-03-2004
		JP 4134037 B2	13-08-2008
US 2009218953 A1	03-09-2009	WO 2009108441 A1	03-09-2009
US 2007176564 A1	02-08-2007	CN 101375643 A	25-02-2009
		EP 1987705 A1	05-11-2008
		JP 2009525567 T	09-07-2009
		WO 2007089407 A1	09-08-2007
EP 1435764 A1	07-07-2004	AU 2003242026 A1	22-12-2003
		CN 1596566 A	16-03-2005
		WO 03105542 A1	18-12-2003
		US 2005017656 A1	27-01-2005
US 2004113564 A1	17-06-2004	NONE	