An electronic assembly is provided, having a capacitor interconnected between BGA solder balls. The capacitor is placed on a motherboard and soldered to the BGA solder balls when the BGA solder balls are soldered to electric lands on the motherboard.
CONSTRUCTING OF AN ELECTRONIC ASSEMBLY HAVING A DECOUPLING CAPACITOR

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to an electronic assembly having a decoupling capacitor and to a method according to which it is constructed.

2. Discussion of Related Art

Integrated circuits are generally manufactured in and on semiconductor wafers that are subsequently diced or singulated into individual microelectronic dies. Such a microelectronic die is usually mounted to a package substrate for purposes of providing rigidity thereto and through which signals can be provided to and from the integrated circuit. Such a package substrate often has an array of solder ball interconnection members, also referred to as a ball grid array (BGA), on an opposing surface that are placed on electric lands of a motherboard and, by a thermal reflow process, soldered thereto.

Such a motherboard usually includes a carrier substrate with a power plane and a ground plane therein. A power source is connected to the power plane, and the ground plane is connected to ground. The power and ground planes are connected to separate ones of the electric lands. In addition, input and output (IO) signal sources are connected to other ones of the electric lands. Power, ground, and IO signals can thus be provided through the motherboard, the solder ball interconnection members, and the package substrate to and from the integrated circuit in the microelectronic die.

In order to reduce inductive-capacitance delay, it is usually advantageous to include one or more decoupling capacitors having opposing terminals connected to the power and ground planes. An existing technique is to connect a capacitor between two of the solder ball interconnection members before the solder ball interconnection members are located on the electric lands of the motherboard. Such a process is expensive because it requires additional manufacturing steps, including the placement of the capacitor, and controlled heating and cooling of the solder ball interconnection members so that they reflow over capacitor terminals of the capacitor. These steps have to be carried out before the package (i.e., the combination of the package substrate, the microelectronic die, the solder ball interconnection members, and the capacitor) are shipped to an entity that does the final assembly on the motherboard.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is described by way of example with reference to the accompanying drawings, wherein:

FIG. 1 is a cross-sectional side view illustrating an electronic assembly, according to an embodiment of the invention, having a decoupling capacitor between a semiconductor package and a motherboard of the assembly;

FIG. 2A is a cross-sectional side view illustrating a portion of the semiconductor package and a portion of the motherboard after the capacitor is located on the motherboard;

FIG. 2B is a view similar to FIG. 2A after the semiconductor package is positioned on the motherboard;

FIG. 2C is a view similar to FIG. 2B after reflow of solder ball interconnection members of the semiconductor package;

FIG. 3 is a top plan view illustrating a layout of electric lands, and power and ground planes of the motherboard; and

FIG. 4 is a top plan view illustrating more ground and power planes that are interconnected with additional decoupling capacitors.

DETAILED DESCRIPTION OF THE INVENTION

An electronic assembly is provided, having a capacitor interconnected between BGA solder balls. The capacitor is placed on a motherboard and soldered to the BGA solder balls when the BGA solder balls are soldered to electric lands on the motherboard.

The motherboard includes a carrier substrate which is made of a nonconductive dielectric material. The motherboard further has a plurality of electric lands that are formed near an upper surface of the carrier substrate. The motherboard further has power and ground planes that are formed below an upper surface of a solder mask or upper dielectric layer and are formed in the upper dielectric layer through which portions of the power and ground planes are exposed to leave additional electric lands on the power and ground planes. The motherboards are connected to some of the electric lands to input and output (IO) signals. One of the lines connects the power plane to a power source, and another one of the lines connects the ground plane to ground.

The semiconductor package includes a package substrate, a microelectronic die, a plurality of contact pads, and a plurality of solder ball interconnection members.

The microelectronic die is typically a semiconductor die having an integrated circuit formed therein. The microelectronic die is mounted on an upper surface of the package substrate. A plurality of controlled collapse chip connect (C4) interconnection members are formed in an array on a lower surface of the microelectronic die, and are used to connect the microelectronic die structurally and electrically to terminals on the package substrate. The contact pads on a lower surface of the package substrate. Metal lines in the package substrate interconnect the terminals on the upper surface thereof with the contact pads. Each solder ball interconnection member is attached to a respective contact pads, typically before the microelectronic die is mounted on the package substrate.
FIGS. 2A, 2B, and 2C illustrate how the solder ball interconnection members 42 are attached to the electric lands 18. FIGS. 2A, 2B, and 2C also illustrate how the capacitor 14 is connected between two of the solder ball interconnection members 42 and through the solder ball interconnection members 42 to the power and ground planes 20 and 22 shown in FIG. 1.

As illustrated in FIG. 2A, a layer of solder paste 46 is first applied to each electric land 18. The capacitor 14 has a capacitor body 47 and capacitor terminals 50 and 52 at each respective end of the capacitor body 48. The capacitor 14 is positioned above the carrier substrate 16 with each capacitor terminal 50 or 52 resting on a respective one of the electric lands 18. The layers of solder paste 46 provide a tackiness that retains the capacitor terminals 50 and 52 in position. What can be noted is that the capacitor 14 is not permanently attached to the electric lands 18 or the solder ball interconnection members 42 at this stage, and that the package substrate 36 and solder ball interconnection members 42 are still distant from the capacitor 14 and the electric lands 18.

Next, as illustrated in FIG. 2B, the package substrate 36 (with the microelectronic die 38 thereon) is lowered down to the motherboard 10 until each one of the solder ball interconnection members 42 inserts itself into a respective layer of solder paste 46. The arrangement of the solder ball interconnection members 42 thus matches the layout of the electric lands 18. The solder ball interconnection members 42 are at all stages still solid (not softened or melted), and the capacitor terminals 52 fit in between two of the solder ball interconnection members 42A and 42B. The capacitor 14 is now between the package substrate 36 and the motherboard 10, and covered by the package substrate 36.

FIG. 2C illustrates the assembly of FIG. 2B after the entire assembly is heated and subsequently allowed to cool. Heating softens, melts, and reflows the solder ball interconnection members 42, and the reflow is assisted by the layers of solder paste 46. Each solder ball interconnection member 42 reflows onto the respective electric land 18 on which it is located and, after cooling down and again solidifying, is structurally and electrically connected to the respective electric land 18. The package substrate 36 is now mounted at a spaced location above and to the motherboard 10. In addition, the solder ball interconnection members 42A and 42B reflow onto upper end and side surfaces of the capacitor terminals 50 and 52 respectively. After being cooled down, the capacitor terminal 50 is connected through the solder ball interconnection member 42A to the electric land 18 to which the solder ball interconnection member 42A is attached. Similarly, the capacitor terminal 52 is connected through the solder ball interconnection member 42B to the electric land 18 to which it is attached.

Referring again to FIG. 1, it can be seen that the capacitor 14 connects the power and ground planes 20 and 22 to one another, to reduce resistive-capacitive delay. An advantage of having the capacitor 14 between the motherboard 10 and the semiconductor package 12 is that decoupling capacitance can be provided closer to the semiconductor package 12, and to the microelectronic die 38.

The manner in which the electronic assembly 8 is assembled is that the capacitor 14 does not have to be pre-mounted to the semiconductor package 12 at great cost. A subcontractor may, accordingly, simply locate the capacitor 14 on the motherboard 10 and connect the capacitor 14 during normal BGA reflow.

FIG. 3 illustrates the layout of the electric lands 18 in order to accommodate the capacitor 14. Three of the electric lands 18A, 18B, and 18C are in a first row. Two more of the electric lands 18D and 18E are in a second row parallel to the first row. Two more of the electric lands 18F and 18G are in a third row parallel to the second row, with the second row between the first and third rows.

The electric land 18A is in a first column, and portions of the electric lands 18D and 18F are in the same column as the electric land 18A. Similarly, the electric land 18C is in a second column, and portions of the electric lands 18E and 18G are in the second column of the electric land 18C. The electric land 18B is in a third column between the first and second columns. There is no electric land in the second row (which includes the electric lands 18D and 18E) having a center point in the third column of the electric land 18B. Similarly, there is no electric land in the third row (of the electric lands 18F and 18G) having a center point in the second column of the electric land 18B. The second and third rows are thus "depopulated" when compared with the first row.

The electric lands 18A, 18D, and 18F are all connected to the power plane 20. The electric lands 18C, 18D, and 18G are all connected to the ground plane 22. The power and ground planes 20 and 22 have a gap between them which is larger in the first row (of the electric lands 18A, 18B, and 18C) than in the second and third rows (of the electric lands 18D, 18E, 18F, and 18G). The extra width of the spacing between the power and ground planes 20 and 22 at the first row allows for placement of the electric land 18B without being connected to either the power or ground plane 20 or 22. Depopulation of the third column of the electric land 18B at the second and third rows simultaneously allows for placement of the capacitor 14 across the third column of the electric land 18B. Although the capacitor illustrated in FIG. 3 is relatively short, a larger capacitor can be used because such a larger capacitor would be connected to electric lands 18F and 18G in columns that are relatively far apart.

As illustrated in FIG. 4, multiple power or ground planes may be provided, in the present example one power plane 20 and two ground planes 22A and 22B. The power and ground planes 20, 22A, and 22B can be interconnected with multiple capacitors 14A, 14B, and 14C. The power plane 20 can also be connected to the ground plane 22A with two capacitors 14A and 14B. The design thus allows for placement of capacitors according to the requirements for decoupling capacitors in a particular area.

The capacitor terminals 50 and 52A are each located on a respective one of the electric lands 18.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art.
17. A method of constructing an electronic assembly, comprising:

positioning a capacitor on a first substrate;

positioning a second substrate adjacent the first substrate with solid interconnection members between respective electric lands on the first substrate and respective contact pads on the second substrate and with the capacitor between the substrates;

heating the interconnection members to reflow the interconnection members, two of the interconnection members reflowing onto terminals of the capacitor located between the substrates; and

allowing the interconnection members to cool and solidify.

18. The method of claim 17, wherein the capacitor is not attached through the interconnection members to either substrate when the second substrate is positioned adjacent the first substrate.

19. The method of claim 17, wherein the capacitor and the interconnection members are on the first substrate before the second substrate is located on the first substrate, and wherein a microelectronic die is mounted to the second substrate.

20. A method of constructing an electronic assembly, comprising:

attaching solder ball interconnection members to contact pads on a package substrate;

mounting a microelectronic die to the package substrate;

locating a capacitor on a carrier substrate;

positioning the package substrate above the carrier substrate, with each solder ball interconnection member on a respective one of a plurality of electric lands on the carrier substrate, and the package substrate covering the capacitor;

heating the solder ball interconnection members so that at least some of the solder ball interconnection members reflow onto the electric lands, and at least first and second ones of the solder ball interconnection members reflow onto first and second capacitor terminals, respectively, of the capacitor; and

allowing the solder ball interconnection members to cool and solidify.

21. The method of claim 20, wherein the first solder ball interconnection member is connected to a ground plane carried by the carrier substrate, and the second solder ball interconnection member is connected to a power plane carried by the carrier substrate.

22. The method of claim 20, further comprising:

applying solder paste to the electric lands, the first and second terminals of the capacitor being located on the solder paste.