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(71) Applicant: **APPLIED MATERIALS, INC.** [US/US]; 3050 Bowers Avenue, Santa Clara, California 95054 (US).

(72) Inventors: **NEMANI, Srinivas D.**; 504 Fern Ridge Court, Sunnyvale, California 94087 (US). **PENDER, Jeremiah T.**; 1565 Fuchsia Drive, San Jose, California 95125 (US). **ZHOU, Qingjun**; 6350 Vegas Drive, San Jose, California 95120 (US). **LUBOMIRSKY, Dmitry**; 862 Bette Avenue, Cupertino, California 95014 (US). **BELOSTOTSKIY, Sergey G.**; 592 Lynxwood Court, Sunnyvale, California 94086 (US).

(74) Agents: **BERNADICOU, Michael A.** et al.; Blakely Sokoloff Taylor & Zafman LLP, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

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(54) **Title**: METHOD OF PATTERNING A LOW-K DIELECTRIC FILM

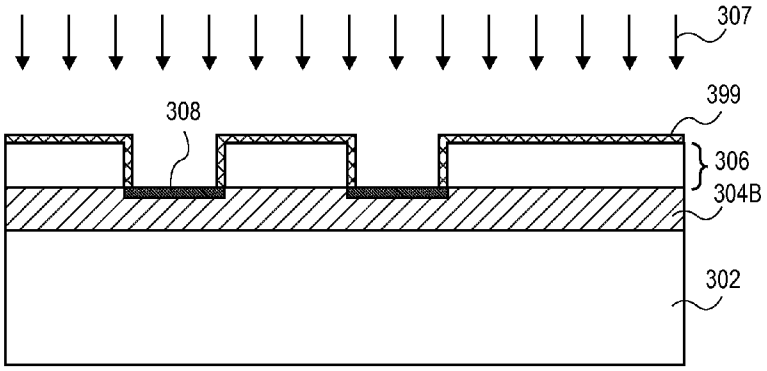


FIG. 3C

(57) **Abstract**: Methods of patterning low-k dielectric films are described. In an example, a method of patterning a low-k dielectric film involves forming and patterning a mask layer above a low-k dielectric layer. The low-k dielectric layer is disposed above a substrate. The method also involves modifying exposed portions of the low-k dielectric layer with a plasma process. The method also involves, in the same operation, removing, with a remote plasma process, the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer.

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Method of Patterning a Low-k Dielectric Film

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/669,824, filed July 10, 2012, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND

1) FIELD

[0002] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of patterning low-k dielectric films.

2) DESCRIPTION OF RELATED ART

[0003] In semiconductor manufacturing, a low-k dielectric is a material with a small dielectric constant relative to silicon dioxide. Low-k dielectric material implementation is one of several strategies used to allow continued scaling of microelectronic devices. In digital circuits, insulating dielectrics separate the conducting parts (e.g., wire interconnects and transistors) from one another. As components have scaled and transistors have moved closer together, the insulating dielectrics have thinned to the point where charge build-up and crosstalk adversely affect the performance of the device. Replacing the silicon dioxide with a low-k dielectric of the same thickness reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation.

[0004] However, significant improvements are needed in the evolution of low-k dielectric processing technology.

SUMMARY

[0005] One or more embodiments of the present invention are directed to methods of patterning low-k dielectric films.

[0006] In an embodiment, a method of patterning a low-k dielectric film involves forming and patterning a mask layer above a low-k dielectric layer. The low-k dielectric layer is disposed above a substrate. The method also involves modifying exposed portions of the low-k dielectric layer with a plasma process. The method also involves, in the same operation, removing, with a remote plasma process, the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer.

[0007] In an embodiment, a method of patterning a low-k dielectric film involves forming and patterning a mask layer above a low-k dielectric layer. The low-k dielectric layer is disposed above a substrate. The method also involves modifying exposed portions of the low-k dielectric layer with an $SiF_4/N_2/Ar$-based plasma process in a chamber. The method also involves, in the same chamber, removing the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer with a remote plasma process based on a plasma selected from the group consisting of an $NF_3/O_2/N_2$, a $CF_4/O_2/N_2$, and an NF_3/NH_3 plasma remote plasma.

[0008] In an embodiment, a method of patterning a low-k dielectric film involves forming and patterning a mask layer above a low-k dielectric layer. The low-k dielectric layer is disposed above a substrate. The method also involves modifying exposed portions of the low-k dielectric layer and forming a protective material layer on the mask layer with a plasma process in a chamber. The method also involves, in the same chamber, removing, with a remote plasma process, the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 illustrates mechanisms through which a low-k dielectric layer may be damages or impacted under conventional oxidizing plasma conditions used to remove polymer formed in a conventions fluorocarbon-based etching process.

[0010] Figure 2 is a Flowchart representing operations in a method of patterning a low-k dielectric film, in accordance with an embodiment of the present invention.

[0011] Figures 3A-3F illustrate cross-sectional views representing various operations in a method of patterning a low-k dielectric film, corresponding to the Flowchart of Figure 2, in accordance with an embodiment of the present invention.

[0012] Figures 4A and 4B illustrate cross-sectional views representing various operations in a method of patterning a low-k dielectric film, and corresponding chamber configurations, in accordance with an embodiment of the present invention.

[0013] Figure 5A illustrates a system in which a method of low-k dielectric film patterning is performed, in accordance with an embodiment of the present invention.

[0014] Figure 5B illustrates a schematic of a possible configuration for chamber 502 of Figure 5A, in accordance with an embodiment of the present invention.

[0015] Figure 6 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0016] Methods of patterning low-k dielectric films are described. In the following description, numerous specific details are set forth, such as specific plasma treatments and effects for modifying portions of low-k dielectric films, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as photolithography patterning and development techniques for mask formation, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0017] Porous low-k dielectric materials, e.g. porous SiCOH, are typically sensitive to plasma etching. Issues typically arise surrounding damage caused to an $Si\text{-}CH_3$ network in an ultra-low-k (ULK) film during an etch process. Such damage may impact the mechanical integrity of a ULK film. Furthermore, there may be an "F memory effect" resulting from polymer formed during a fluorocarbon-based (C_xF_y-based) etch process. The sensitivity may also arise from a high porosity which allows etching chemistry to diffuse deep into low-k dielectric film.

[0018] One of the key issues with patterning low k dielectric films has been the control on the level of damage caused during the etch process. The plasma parameters and chemistry used typically modify the carbon content of the low-k film causing changes in electrical behavior (k value and leakage). One of the root causes for the damage to the carbon has been during the strip of the C_xF_y polymer that deposits on the low-k surface during the etch process. However, typical dielectric etch processes benefit from C_xF_y-based chemistry as it can provide sidewall protection during plasma etch and increase anisotropic etch capability.

[0019] In accordance with one or more embodiments described herein, fundamental aspects of etching are addressed by using alternative gases for etching. For example, in one embodiment, a combination of Si-based precursors (e.g., SiF_4, $SiCl_4$, other fluorosilanes, chlorosilanes, iodosilanes), a nitriding gas (e.g., N_2, NH_3, etc.) and/or an inert dilution gas (e.g., Ar, He, Xe, Ne) is used. An anisotropic etch is made possible by formation of a Si-based (N-rich) deposition on the sidewall of a trench being etched. This deposition also protects the low-k film from plasma attack.

[0020] In other embodiments, oxygen is used along with or instead of N_2 to form an Si-O based deposition on the sidewall. The following stage or operation in the etch sequence involves

use of a remote plasma or low energy plasma to generate species that can selectively remove such a film from low k. One example is the use of NF_3/NH_3 based remote plasma to form NH_4F that reacts with the sidewall deposition to form a silicate species. The silicate species sublimes at elevated temperatures. In one such embodiment, the above described process is highly selective to low-k material in that low-k material is not etched in the process. In another embodiment, use of an $O_2/N_2/NF_3$ or NO/NF_3 based remote plasma process is employed to etch away Si-N type sidewall deposition. The process is tuned to be highly selective to low-k films. These two aspects of the etch process may be repeated multiple times for profile control.

[0021] One or more embodiments of the present invention are targeted at the fluorocarbon-free etching of low-k dielectric films, such as ULK films. In an embodiment, one or more methods herein are used to provide a patterning approach with reduced damage or detrimental impact to the low k dielectric film, e.g., in an etch patterning process. In one such embodiment, approaches described herein may be particularly useful for C-doped oxide films. Conventional fluorocarbon chemistry-based ULK etching processes inevitably deposit CF polymer on the ULK surfaces. The polymer is subsequently removed with an oxidizing post etch treatment (PET) plasma. However, the PET plasma may oxidize carbon-containing ULK dielectrics. Oxidized carbon-containing ULK dielectrics may be amenable to undesirable moisture absorption, resulting in the dielectric constant (k value) of the ULK dielectrics to increase. In accordance with an embodiment of the present invention, fluorocarbon-free etching of ultra-low k dielectric is described below.

[0022] Figure 1 illustrates mechanisms through which a low-k dielectric layer may be damages or impacted under conventional oxidizing plasma conditions used to remove polymer formed in a conventions fluorocarbon-based etching process. Referring to mechanism (a) of Figure 1, when undergoing an oxidizing ash, an SiO_3-methyl fragment, which makes up approximately 40% of a SiCOH low-k film with a dielectric constant of about 2.5, can undesirably lose its methyl group to a hydroxide group. Referring to mechanism (b) of Figure 1, when undergoing an oxidizing ash, an SiO_2-$(CH_2)_2$ fragment, which makes up approximately 10% of a SiCOH low-k film with a dielectric constant of about 2.5, can undesirably be converted to an SiO_2-$(COH)_2$ fragment. Referring to mechanism (c) of Figure 1, when undergoing a reducing ash, an SiO_3-methyl fragment, which makes up approximately 40% of a SiCOH low-k film with a dielectric constant of about 2.5, can undesirably lose its methyl group to a hydride ligand (H).

[0023] In an embodiment, a fluorocarbon-free etch is used to pattern a low-k dielectric film. Thus, CF polymer doe not form, which would otherwise require removal by an ashing process. In one embodiment, etch processes described herein include two basic functions

performed in the same operation: (1) modification of an exposed portion of a low-k film through treatment with a first plasma etch to convert a portion of the film to a silicon oxide (or low-carbon containing oxide), and (2) removal of the treated layer with a second, remote, plasma etch. Thus, in an embodiment, a ULK film is not exposed to any halogen radicals or O radicals that may otherwise cause damage to a Si-CH_3 network.

[0024] In an aspect of the present invention, a low-k dielectric film is patterned by modification of a portion of the low-k dielectric film and subsequent removal of the modified portion selective to the unmodified portions of the film. For example, Figure 2 is a Flowchart 200 representing operations in a method of patterning a low-k dielectric film, in accordance with an embodiment of the present invention. Figures 3A-3F illustrate cross-sectional views representing operations in a method of patterning a low-k dielectric film, in accordance with an embodiment of the present invention.

[0025] Referring to operation 202 of Flowchart 200 and corresponding Figures 3A and 3B, a method of patterning a low-k dielectric film includes forming (Figure 3A) and patterning (Figure 3B) a mask layer 306 above a low-k dielectric layer 304, the low-k dielectric layer 304 disposed above a substrate 302. In an embodiment, the mask layer 306 is a photoresist layer formed directly on the low-k dielectric layer 304. In another embodiment, a photoresist layer is first formed above a hardmask layer (306 in this embodiment) disposed above the low-k dielectric layer 304.

[0026] In an embodiment, e.g., in the case that mask layer 306 is a hardmask layer that is patterned, forming and patterning the mask layer 306 above the low-k dielectric layer 304 includes forming and patterning a non-oxide mask layer. The non-oxide mask layer may provide selectivity against an oxide etch, as described in greater detail below. In a specific such embodiment, the mask layer 306 is a metal-containing layer such as, but not limited to a layer of titanium nitride or a layer of tantalum nitride. In another specific such embodiment, the mask layer 306 is a layer of non-oxide dielectric material such as, but not limited to, a layer of silicon nitride.

[0027] In another embodiment, e.g., in the case that mask layer 306 is a photoresist layer that is patterned, forming and patterning the mask layer 306 above the low-k dielectric layer 304 includes forming and patterning a photoresist layer. The photoresist layer may be composed of a material suitable for use in a lithographic process. That is, in an embodiment, the photoresist layer is exposed to a light source and subsequently developed. In one embodiment, the portions of the photoresist layer to be exposed to the light source will be removed upon developing the photoresist layer, e.g., the photoresist layer is composed of a positive photoresist material. In a specific embodiment, the photoresist layer is composed of a positive photoresist material such as,

but not limited to, a 248 nanometer node resist, a 193 nanometer node resist, a 157 nanometer node resist, an extreme ultra-violet (EUV) resist, or a phenolic resin matrix with a diazonaphthoquinone sensitizer. In another embodiment, the portions of the photoresist layer to be exposed to the light source will be retained upon developing the photoresist layer, e.g., the photoresist layer is composed of a negative photoresist material. In a specific embodiment, the photoresist layer is composed of a negative photoresist material such as, but not limited to, poly-cis-isoprene and poly-vinyl-cinnamate.

[0028] In an embodiment, the low-k dielectric layer 304 has a permittivity less than that of silicon dioxide, e.g., less than approximately 3.9. In one embodiment, the low-k dielectric layer 304 is a material such as, but not limited to, a fluorine-doped silicon dioxide, a carbon-doped silicon dioxide, a porous silicon dioxide, a porous carbon-doped silicon dioxide, a porous SiLK, a spin-on silicone based polymeric dielectric, or a spin-on organic polymeric dielectric. In accordance with an embodiment of the present invention, the low-k dielectric layer 304 is a porous SiCOH layer having a dielectric constant of less than 2.7.

[0029] Substrate 302 may be composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably reside. In accordance with an embodiment of the present invention, substrate 302 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing substrate 302 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, substrate 302 is composed of a III-V material. In an embodiment, a plurality of semiconductor devices resides on substrate 302, below low-k dielectric layer 304.

[0030] Referring to operation 204 of Flowchart 200 and corresponding Figure 3C, patterning the low-k dielectric film also includes modifying exposed portions of the low-k dielectric layer 304 with a plasma process 307. The exposed portions of the low-k dielectric layer 304 are those portions exposed by the patterned mask 306. Plasma 307 is used to modify the exposed portions to provide modified portions 308 and unmodified portion 304B of the low-k dielectric layer 304. In addition to modifying the low-k material, a protective material layer 399 may also be deposited in the same process, as depicted in Figure 3C. Such a protective material layer 399 is described in greater detail below in association with Figures 4A and 4B. Thus, in an embodiment, deposition of a protective layer and modification of a low-k film are performed in the same process, or at least essentially at the same time.

[0031] In an embodiment, the first plasma process involves an $SiF_4/N_2/Ar$-based plasma. In one such embodiment, the low-k sidewall is protected with an SiON or SiONH layer, where

the oxygen is scavenged or introduced intentionally. In a specific embodiment, the Ar from the plasma is used to bombard only the bottom portion of the trench, selectively and anistropically modifying the low-k material (as shown more clearly in Figures 4A and 4B). In an embodiment, in place of or in addition to SiF4, species such as, but not limited to $SiCl_4$, $Si(CH_3)_3H$, SiH_4, Cl_2SiH_2, Si_2Cl_6 (e.g., essentially species including a Si-Cl bond or Si-F bond) may be used. In a specific embodiment, Ar has a pressure approximately in the range of 5-50 mTorr. In an embodiment, N_2 is used with a power approximately in the range of 10-1000W. In an embodiment, a bias RF frequency approximately in the range of 2MHz – 60MHZ is used. In an embodiment, a combination of two or more frequencies is used for biasing, e.g., 2MHz/60MHz, 13MHz/60MHz, or 27MHz/60MHz combinations. In an embodiment, the electrostatic chuck (ESC) temperature is approximately 10 degrees Celsius. In an embodiment, the above conditions are all used in conjunction together.

[0032] Referring again to operation 204 of Flowchart 200 and now to corresponding Figure 3D, patterning the low-k dielectric film also includes removing the modified portions 308 of the low-k dielectric layer 304B. In an embodiment, the removal is selective to the mask layer 306 and to the unmodified portions 304B of the low-k dielectric layer 304. Since carbon may be removed during the modification of the low-k dielectric layer 304, the modified portions 308 may be more oxide-like in nature. Accordingly, in an embodiment, an oxide removal process is used to remove the modified portions 308, examples of which are provided below.

[0033] In an embodiment, the second, remote, plasma is used to essentially clean the surfaces by removing the modified low-k material and the protective layer 399. In one such embodiment, an $NF_3/O_2/N_2$ or a $CF_4/O_2/N_2$ or an NF_3/NH_3 plasma is used remotely as the second plasma. Thus, in one embodiment, a first plasma (a plasma that is not remote) is used to form a protecting layer and modify a low-k film at the same time. Then, a second plasma (a remote plasma) is used to remove the protective layer and the modified low-k material layer. An example of a chamber suitable for such a process is described below in association with Figure 5B.

[0034] Thus, in accordance with an embodiment of the present invention, etching of a low-k dielectric film is achieved by partial film conversion of the low-k dielectric layer. In one embodiment, the etching may be referred to as atomic layer etching or molecular level etching (MLE) since only one or a few layers of exposed portions of the low-k dielectric film are converted and subsequently removed per process cycle. As exemplified above, in one embodiment, the etching process includes first selectively modifying the composition of a horizontal ULK surface with a first plasma and then removing the modified portions with a

second, remote, plasma. In one embodiment, approaches described herein represent true film conversion by methyl knock-off from a low-k dielectric film.

[0035] By contrast, conventional chemical etching typically involves deposition of polymer on ULK surfaces, which are removed with an oxidizing PET operation. An aqueous-based clean is used to remove damaged ULK, which may result in line bending and moisture absorption into the ULK. Instead, in an embodiment herein, essentially damage free etching of a ULK material is achieved by completely avoiding CF etching chemistry. An inert plasma is used to remove carbon from a ULK surface. A downstream plasma is then used to remove modified portions of the ULK. The downstream plasma etching may be extremely selective to the ULK due to its nature of pure chemical etching.

[0036] The above method described in association with operation 204 of Flowchart 200 may be repeated as required to achieve a suitable extent of patterning of the low-k dielectric layer 304. For example, referring again to Figure 3D, trenches 310 are formed in the low-k dielectric layer 304, leaving partially patterned, and unmodified, low-k dielectric layer 304B. The depth of trenches 310 may not be deep enough for suitable patterning of the low-k dielectric layer 304, especially since the modification and removal process described above may only remove one or several molecular layers at a time.

[0037] Accordingly, in an embodiment, the low-k dielectric layer 304 is subjected to multiple modification and removal processes of exposed portions thereof until a depth of trenches 310 suitable for subsequent processing requirements is achieved. In one such embodiment, the modifications and removal is repeated until partial trenches are formed in, but not entirely through, the low-k dielectric layer 304. In another such embodiment, the modifications and removal is repeated until complete trenches are formed entirely through the low-k dielectric layer 304.

[0038] As an example of a cyclic process, Figures 3E and 3F illustrate an embodiment in which, in conjunction with Figures 3A-3D, a total of two cycles are performed to pattern a low-k dielectric layer. It is to be understood that many more than two modification and removal cycles may need to be performed to suitably pattern a low-k dielectric film.

[0039] Referring to Figure 3E, exposed portions of the low-k dielectric layer 304B, e.g., exposed surfaces of trenches 310, are modified and etched with a second modification plasma process involving first and second remote plasma processes in a same operation. The exposed portions of the low-k dielectric layer 304B are those portions exposed by the patterned mask 306 as well as exposed sidewalls of the low-k dielectric layer 304B. The second iteration of the modification and etch cycle of Figure 3E formed deeper trenches 310' and hence a patterned low-k film 304C.

[0040] Referring to Figure 3F, once a desired depth for trenches 310' is achieved, which may involve numerous cycles of the above described modification and removal process, the mask 306 may be removed. However, in an embodiment, care must be taken upon removal of mask 306 such that the removal is selective against the patterned low-k dielectric layer 304C and does not detrimentally impact (e.g., by raising the dielectric constant) the patterned low-k dielectric layer 304C.

[0041] In an embodiment, the mask layer 306 is composed of a photoresist material and is removed in an ashing process. However, in one embodiment, the ashing plasma is applied in a manner to limit ashing damage to the patterned low-k dielectric layer 304C. In a specific such embodiment, although there may be similarities in the composition of a photoresist-based mask layer 306 and the patterned low-k dielectric layer 304C, the differences are exploited for a selective removal of the mask layer 306. For example, an organic mask may include a hydrocarbon polymer (including the elements C, H, O), where an etch thereof may depend more on neutrals species rather than on ions. Meanwhile, the patterned low-k dielectric layer 304C may include an O-Si-O network with $Si-CH_3$ groups, where an etch thereof may require some ion energy and neutrals to induce damage. Approaches for selective removal of the mask layer 306 may, in an embodiment, include increasing ashing selectivity to the patterned low-k dielectric layer 304C by high ion/neutral ratio which may remove the organic mask on horizontal surfaces while preserving the patterned low-k dielectric layer 304C on vertical surfaces.

[0042] In accordance with another embodiment of the present invention, a cyclic passivation and ashing approach is used to reduce ashing damage typically associated with removal of a photoresist layer from an exposed or partially exposed low-k dielectric layer. In one such embodiment, a process scheme includes alternating steps of passivation and ashing. During each of the passivation operations, a silicon-containing passivation agent is used to selectively react with an ultra low-k (ULK) material to form a thin layer of silicon-containing film on exposed portions of the ULK material. During each of the ashing operations, the thin layer of silicon-containing film acts to protect against an ashing plasma, e.g., which may be used to etch a photoresist layer. The protecting reduces damage that the ashing plasma would otherwise cause to the ULK material. The protecting nature of the passivating layer may be considered to be *in situ*, in the sense that the film may form Si-O linkages upon exposure to the ashing plasma. The Si-O linkages may provide selectivity against the ashing plasma.

[0043] The passivation layer may be removed or at least somewhat compromised during the ashing by chemical reaction or physical sputtering. Accordingly, in one embodiment, cyclic passivation/ashing operations are used. Such cyclic passivation/ashing operations may be repeated until all organic mask material (e.g., an overlying photoresist layer) is removed. Any

remaining portions of the passivation layer may be removed, e.g., in one embodiment, by a diluted hydrofluoric acid (HF) clean.

[0044] In a specific embodiment, in order to form a passivation layer for protecting the patterned low-k dielectric layer 304C during removal of the mask layer 306, a silicon source layer is first formed on the surfaces of the trenches 310' of the patterned low-k dielectric layer 304C. In an embodiment, the silicon source layer is formed from molecular species that react with a hydrolyzed portion of the patterned low-k dielectric layer 304C. In one embodiment, the silicon source layer forms a covalent bond between the silicon source layer and the exposed portions of the patterned low-k dielectric layer 304C. In one embodiment, the silicon source layer is formed from a species such as, but not limited to, silicon tetrachloride ($SiCl_4$), dimethylsilane ($(CH_3)_2SiH_2$), trimethylsilane ($(CH_3)_3SiH$), N-(trimethylsilyl)dimethylamine ($(CH_3)_3SiN(CH_2)_2$), or 1,1,1,3,3,3-hexamethyldisilazane (HMDS). In one embodiment, the substrate 302 is situated on a hot plate during the forming of the silicon source layer.

[0045] Next, the silicon source layer is exposed to an oxygen source to form an Si-O-containing layer on the surfaces of the trenches 310' of the patterned low-k dielectric layer 304C and to remove at least a portion of the photoresist-based mask layer 306. In an embodiment, the Si-O-containing layer protects the patterned low-k dielectric layer 304C during removal of some or all of the mask layer 306. It is to be understood that, in the absence of the Si-O-containing layer, the patterned low-k dielectric layer 304C may otherwise be damaged by the process used to remove the portion of the mask layer 306. In an embodiment, exposing the silicon source layer to an oxygen source includes treating with a plasma. In one embodiment, the plasma is based on an oxygen radical source. The oxygen radical source is a molecule with a dissociation product composed of an oxygen radical. In a specific such embodiment, the oxygen radical source is a source such as, but not limited to, oxygen (O_2), ozone (O_3), carbon dioxide (CO_2), or water (H_2O). In an embodiment, subsequent to the removal of the mask layer 306 the Si-O-containing layer is removed. In one such embodiment, the Si-O-containing layer is removed by a dry etch process. In another embodiment, a wet etch solution including hydrofluoric acid (HF) is used to remove the Si-O-containing layer. However, it is to be understood that no such additional treatment may be needed. For example, in one embodiment, the Si-O-containing layer is removed during the ashing by chemical reaction or physical sputtering.

[0046] As described above, a protection layer may be formed during a low-k modification process. As an example, Figures 4A and 4B illustrate cross-sectional views representing various operations in a method of patterning a low-k dielectric film, and corresponding chamber configurations, in accordance with an embodiment of the present invention.

[0047] Referring to Figure 4A, a material stack 402A such as the stack shown in Figure 3C includes trenches formed (or being formed) in a low-k dielectric layer. A protective layer 499 is formed in a first plasma process while exposed portions of the low-k dielectric layer are modified in the same plasma process. In an embodiment, the first plasma process is performed while the stack 402A is positioned at a first plasma stage location 404A, as is described in greater detail in association with Figure 5B. Thus, in an embodiment, plasma deposition for sidewall protection (and to seal pores to prevent damage) with anisotropic film modification is performed in a same process.

[0048] Referring to Figure 4B, a material stack 402B such as the stack shown in Figure 3D includes cleaned trenches in the low-k dielectric layer. The protective layer 499 and the modified low-k material from Figure 4A are removed in a second plasma process. In an embodiment, the second plasma process is a remote plasma process. In one such embodiment, the second plasma process is performed while the stack 402B is positioned at a second plasma stage location 404B, as is described in greater detail in association with Figure 5B. In a specific embodiment, a Siconi plasma process is used to remove the deposited and modified layers.

[0049] Overall, in an embodiment, a non-carbon based approach is used to selectively remove portions of a low-k film with no k-value shift. In one embodiment, a sequential process is used where, first, a Si-based precursor is used for etching with sidewall protection and, second, a highly selective radical based removal is employed. Advantages may include, but are not limited to, use of a carbon-free process (no ash or post-etch treatment necessarily needed), potentially no wet clean needed, low ion energies used leading to minimal metal hardmask erosion, and self limiting treatment and removal operation leading to good depth and uniformity control.

[0050] In an embodiment, one or more of the above processes is performed in a plasma etch chamber. For example, in one embodiment, one or more of the above processes is performed in an Applied Centura® Enabler dielectric etch system, available from Applied Materials of Sunnyvale, CA, USA. In another embodiment, one or more of the above processes is performed in an Applied Materials™ AdvantEdge G3 etcher, also available from Applied Materials of Sunnyvale, CA, USA.

[0051] Patterning of a low-k dielectric layer may be conducted in processing equipment suitable to provide an etch plasma in proximity to a sample for etching. For example, Figure 5A illustrates a system in which a method of low-k dielectric film patterning is performed, in accordance with an embodiment of the present invention.

[0052] Referring to Figure 5A, a system 500 for conducting a plasma etch process includes a chamber 502 equipped with a sample holder 504. An evacuation device 506, a gas

inlet device 508 and a plasma ignition device 510 are coupled with chamber 502. A computing device 512 is coupled with plasma ignition device 510. System 500 may additionally include a voltage source 514 coupled with sample holder 504 and a detector 516 coupled with chamber 502. Computing device 512 may also be coupled with evacuation device 506, gas inlet device 508, voltage source 514 and detector 516, as depicted in Figure 5A.

[0053] Chamber 502 and sample holder 504 may include a reaction chamber and sample positioning device suitable to contain an ionized gas, i.e. a plasma, and bring a sample in proximity to the ionized gas or charged species ejected there from. Evacuation device 506 may be a device suitable to evacuate and de-pressurize chamber 502. Gas inlet device 508 may be a device suitable to inject a reaction gas into chamber 502. Plasma ignition device 510 may be a device suitable for igniting a plasma derived from the reaction gas injected into chamber 502 by gas inlet device 508. Detection device 516 may be a device suitable to detect an end-point of a processing operation. In one embodiment, system 500 includes a chamber 502, a sample holder 504, an evacuation device 506, a gas inlet device 508, a plasma ignition device 510 and a detector 516 similar to, or the same as, those included in an Applied Centura® Enabler dielectric etch system or an Applied Materials™ AdvantEdge G3 system.

[0054] Figure 5B illustrates a schematic of a possible configuration for chamber 502 of Figure 5A, in accordance with an embodiment of the present invention. Referring to Figure 5B, and in association with the description of Figures 3C and 3D, a chamber 502 has a first stage (plasma stage 1, which may include an in-situ source with bias) for performing a first, non-remote, plasma process. For example, a plasma process involving formation of a protective layer along with modification of a low-k film may be performed at stage 1. The chamber 502 also has a second stage (plasma stage 2) for performing a remote plasma process. For example, a plasma process involving cleaning of a deposited protection layer along with modified low-k material may be performed at stage 2. Such a configuration for chamber 502 may enable fine tuning radicals/ion ratio. Benefits of such a tunable source may include control of etch anisotropy polymer-free treatments. Layer-by-layer removal defined by depth of modified layer may also be performed. Additionally, tunable selectivity based on fine control of metastable species (e.g., NH, F, O, H, Cl, etc) may be achieved.

[0055] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to the present invention. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a

machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[0056] Figure 6 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 600 within which a set of instructions, for causing the machine to perform any one or more of the methodologies discussed herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies discussed herein.

[0057] The exemplary computer system 600 includes a processor 602, a main memory 604 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 606 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 618 (e.g., a data storage device), which communicate with each other via a bus 630.

[0058] Processor 602 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 602 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 602 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 602 is configured to execute the processing logic 626 for performing the operations discussed herein.

[0059] The computer system 600 may further include a network interface device 608. The computer system 600 also may include a video display unit 610 (e.g., a liquid crystal display

(LCD) or a cathode ray tube (CRT)), an alphanumeric input device 612 (e.g., a keyboard), a cursor control device 614 (e.g., a mouse), and a signal generation device 616 (e.g., a speaker).

[0060] The secondary memory 618 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 631 on which is stored one or more sets of instructions (e.g., software 622) embodying any one or more of the methodologies or functions described herein. The software 622 may also reside, completely or at least partially, within the main memory 604 and/or within the processor 602 during execution thereof by the computer system 600, the main memory 604 and the processor 602 also constituting machine-readable storage media. The software 622 may further be transmitted or received over a network 620 via the network interface device 608.

[0061] While the machine-accessible storage medium 631 is shown in an exemplary embodiment to be a single medium, the term "machine-readable storage medium" should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term "machine-readable storage medium" shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term "machine-readable storage medium" shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0062] In accordance with an embodiment of the present invention, a machine-accessible storage medium has instructions stored thereon which cause a data processing system to perform a method of patterning a low-k dielectric layer. The method includes forming and patterning a mask layer above a low-k dielectric layer, the low-k dielectric layer disposed above a substrate. Exposed portions of the low-k dielectric layer are modified with a plasma process. In a same operation, with a remote plasma process, the modified portions of the low-k dielectric layer are removed selective to the mask layer and unmodified portions of the low-k dielectric layer.

[0063] Thus, methods of patterning low-k dielectric films have been disclosed.

CLAIMS

What is claimed is:

1. A method of patterning a low-k dielectric film, the method comprising:
   forming and patterning a mask layer above a low-k dielectric layer, the low-k dielectric layer disposed above a substrate;
   modifying exposed portions of the low-k dielectric layer with a plasma process; and, in the same operation,
   removing, with a remote plasma process, the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer.

2. The method of claim 1, wherein modifying exposed portions of the low-k dielectric layer with the plasma process comprises using an $SiF_4/N_2/Ar$-based plasma.

3. The method of claim 2, wherein the Ar has a pressure approximately in the range of 5-50 mTorr, and the plasma has a power approximately in the range of 10-1000W.

4. The method of claim 1, wherein removing the modified portions of the low-k dielectric layer with the remote plasma process comprises using a plasma selected from the group consisting of an $NF_3/O_2/N_2$, a $CF_4/O_2/N_2$, and an NF_3/NH_3 plasma remote plasma.

5. The method of claim 1, wherein modifying exposed portions of the low-k dielectric layer with the plasma process further comprises forming a protective material layer on the mask layer with the plasma process.

6. The method of claim 1, wherein forming and patterning the mask layer comprises forming and patterning a material selected from the group consisting of titanium nitride and tantalum nitride.

7. The method of claim 1, wherein forming and patterning the mask layer comprises forming and patterning a non-oxide dielectric material.

8. The method of claim 1, wherein forming and patterning the mask layer comprises forming and patterning a photoresist layer.

9. The method of claim 1, wherein forming and patterning the mask layer above the low-k dielectric layer comprises forming and patterning the mask layer above a low-k dielectric material selected from the group consisting of a fluorine-doped silicon dioxide, a carbon-doped silicon dioxide, a porous silicon dioxide, a porous carbon-doped silicon dioxide, a porous SiLK, a spin-on silicone based polymeric dielectric, a spin-on organic polymeric dielectric, and a porous SiCOH layer having a dielectric constant of less than 2.7.

10. A method of patterning a low-k dielectric film, the method comprising:

forming and patterning a mask layer above a low-k dielectric layer, the low-k dielectric layer disposed above a substrate;

modifying exposed portions of the low-k dielectric layer with an $SiF_4/N_2/Ar$-based plasma process in a chamber; and, in the same chamber,

removing the modified portions of the low-k dielectric layer selective to the mask layer and unmodified portions of the low-k dielectric layer with a remote plasma process based on a plasma selected from the group consisting of an $NF_3/O_2/N_2$, a $CF_4/O_2/N_2$, and an NF_3/NH_3 plasma remote plasma.

11. The method of claim 10, wherein the Ar of the $SiF_4/N_2/Ar$-based plasma process has a pressure approximately in the range of 5-50 mTorr, and the $SiF_4/N_2/Ar$-based plasma has a power approximately in the range of 10-1000W.

12. The method of claim 10, wherein modifying exposed portions of the low-k dielectric layer with the plasma process further comprises forming a protective material layer on the mask layer with the plasma process.

13. The method of claim 10, wherein forming and patterning the mask layer comprises forming and patterning a material selected from the group consisting of titanium nitride and tantalum nitride.

14. The method of claim 10, wherein forming and patterning the mask layer comprises forming and patterning a non-oxide dielectric material.

15. The method of claim 10, wherein forming and patterning the mask layer comprises forming and patterning a photoresist layer.

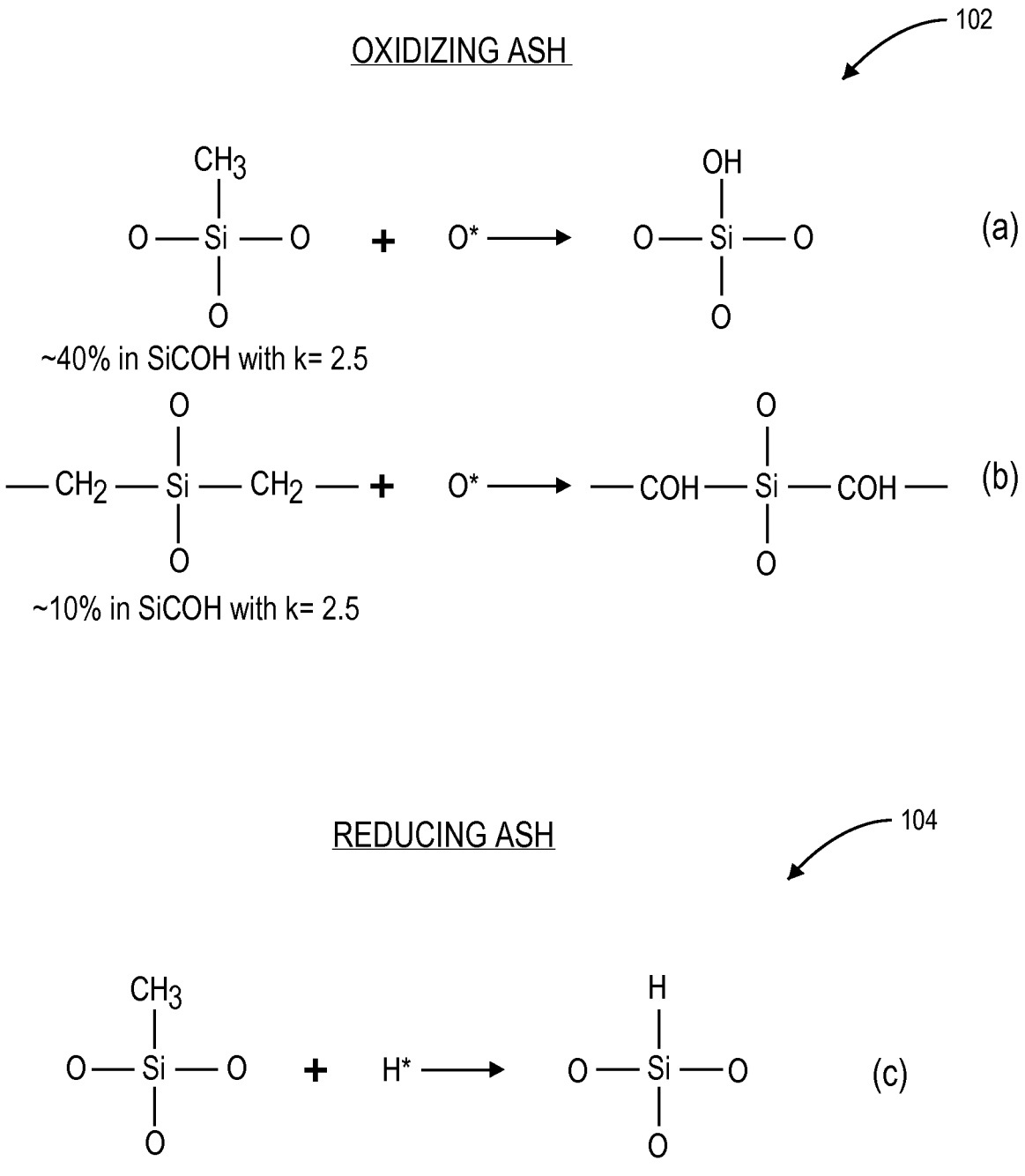

OXIDIZING ASH
102
CH3
O—Si—O
O
+
O*
OH
O—Si—O
O
(a)
~40% in SiCOH with k= 2.5
O
—CH2—Si—CH2—
O
+
O*
O
—COH—Si—COH—
O
(b)
~10% in SiCOH with k= 2.5
REDUCING ASH
104
CH3
O—Si—O
O
+
H*
H
O—Si—O
O
(c)

FIG. 1

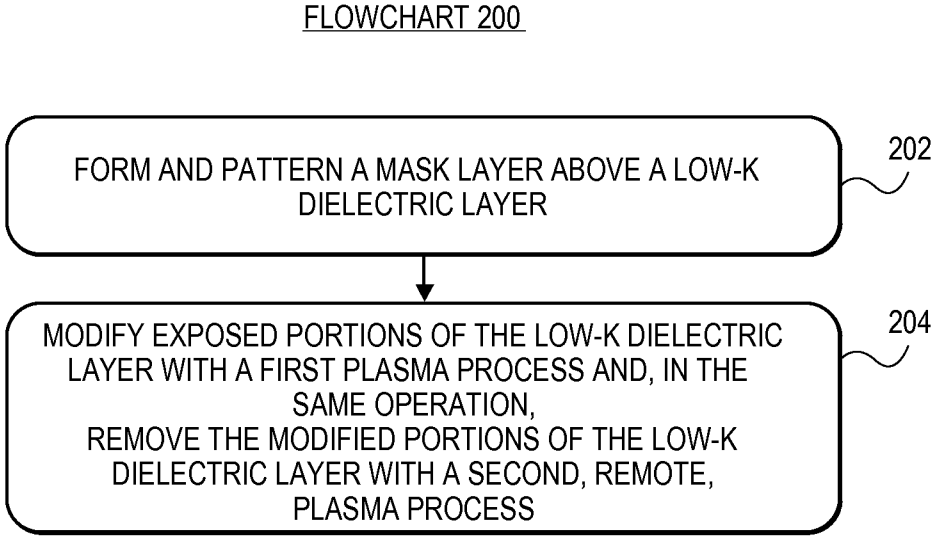

FLOWCHART 200
FORM AND PATTERN A MASK LAYER ABOVE A LOW-K DIELECTRIC LAYER
202
MODIFY EXPOSED PORTIONS OF THE LOW-K DIELECTRIC LAYER WITH A FIRST PLASMA PROCESS AND, IN THE SAME OPERATION,
REMOVE THE MODIFIED PORTIONS OF THE LOW-K DIELECTRIC LAYER WITH A SECOND, REMOTE, PLASMA PROCESS
204

FIG. 2

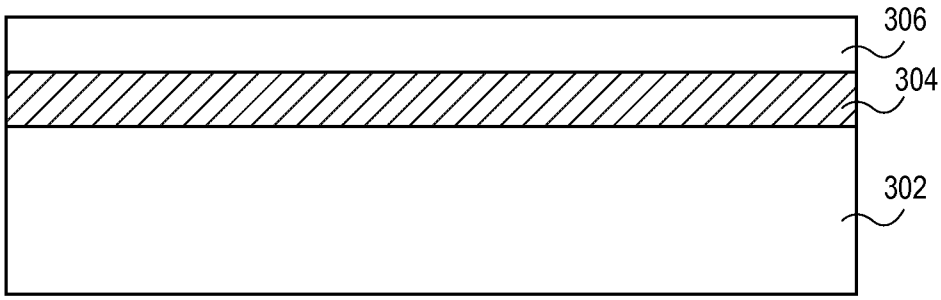


FIG. 3A

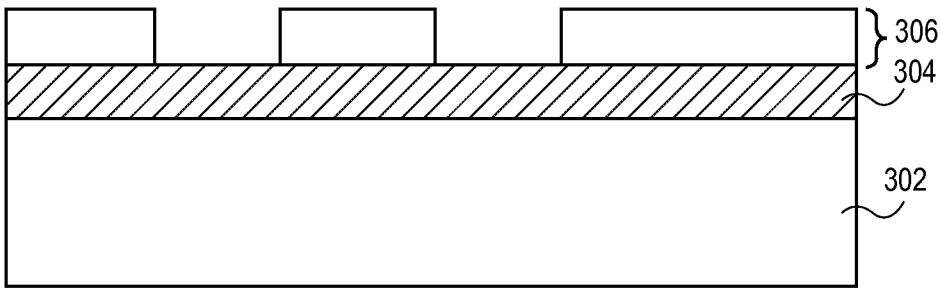


FIG. 3B

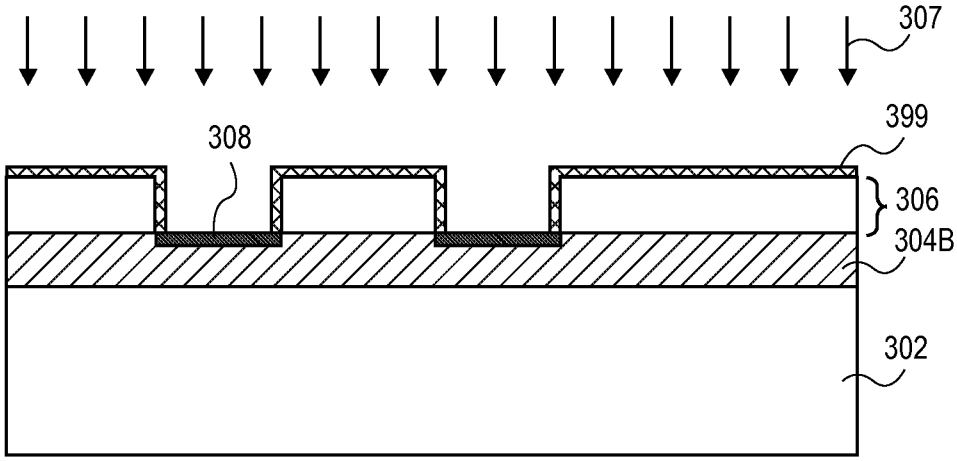


FIG. 3C

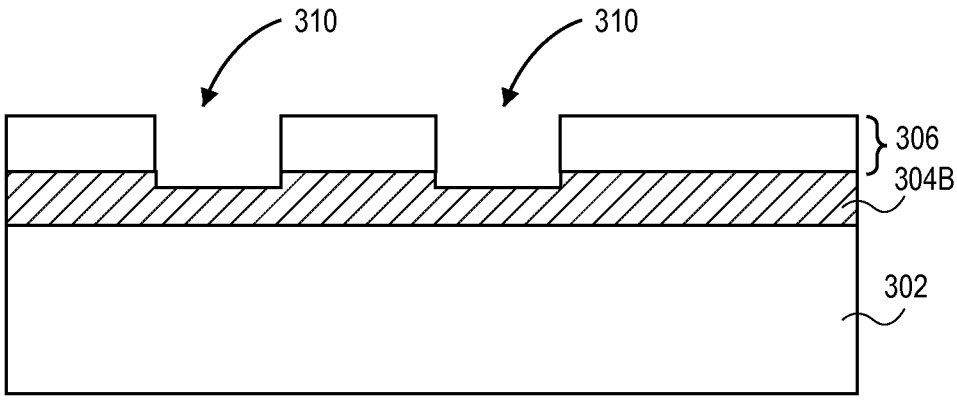


FIG. 3D

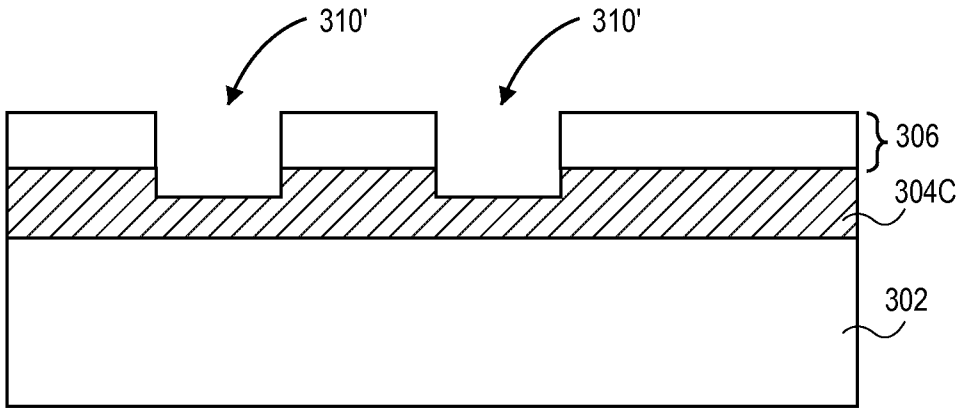


FIG. 3E

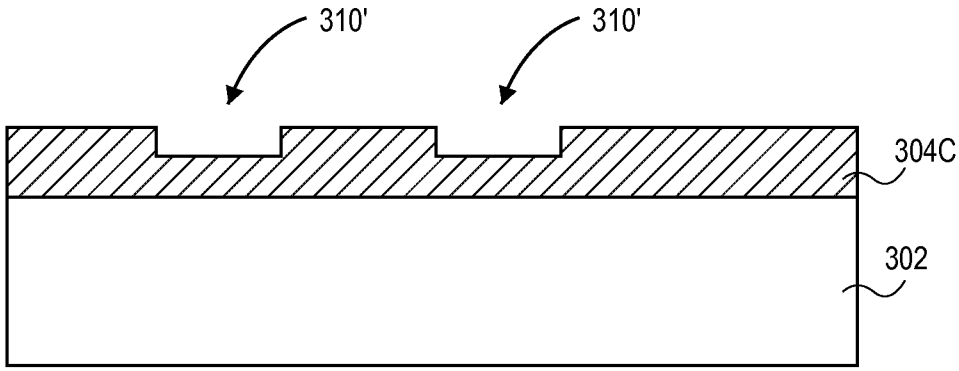


FIG. 3F

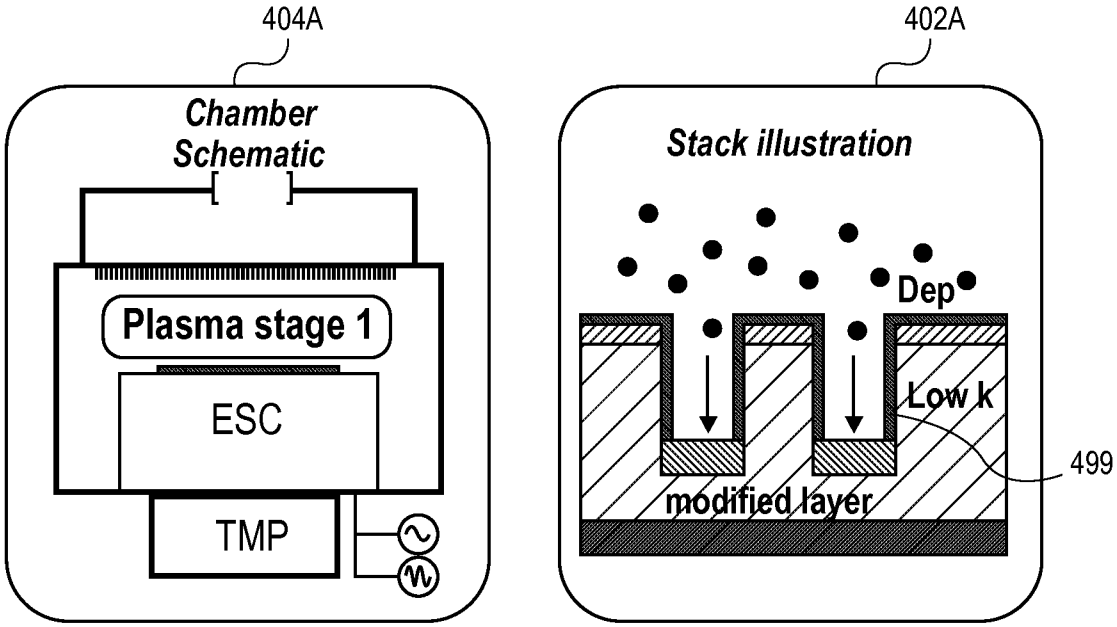

404A
Chamber Schematic
Plasma stage 1
ESC
TMP
402A
Stack illustration
Dep
Low k
499
modified layer

FIG. 4A

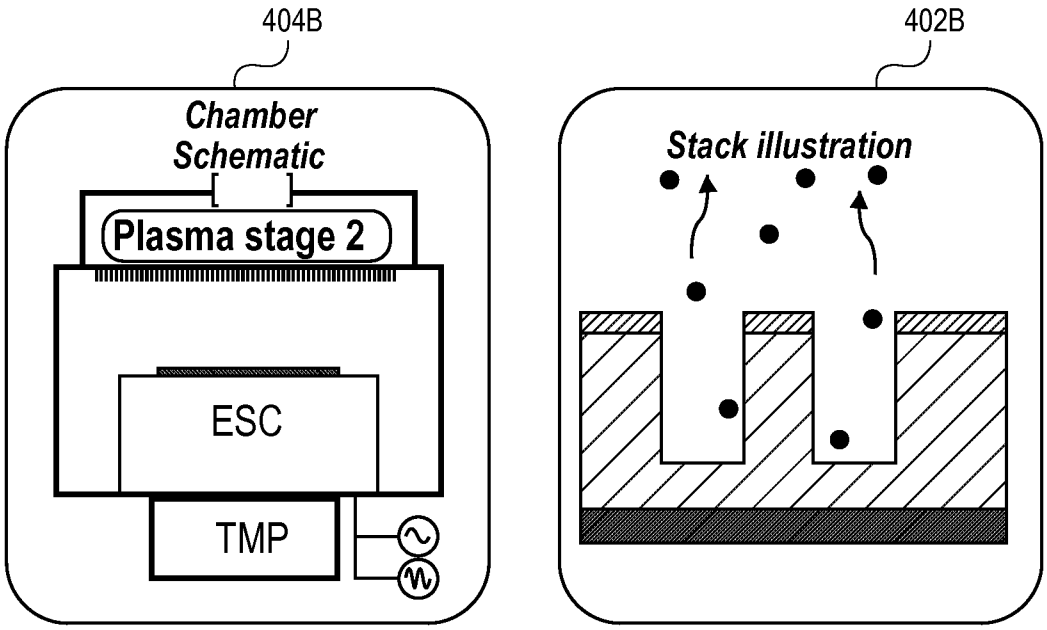

404B
Chamber Schematic
Plasma stage 2
ESC
TMP
402B
Stack illustration

FIG. 4B

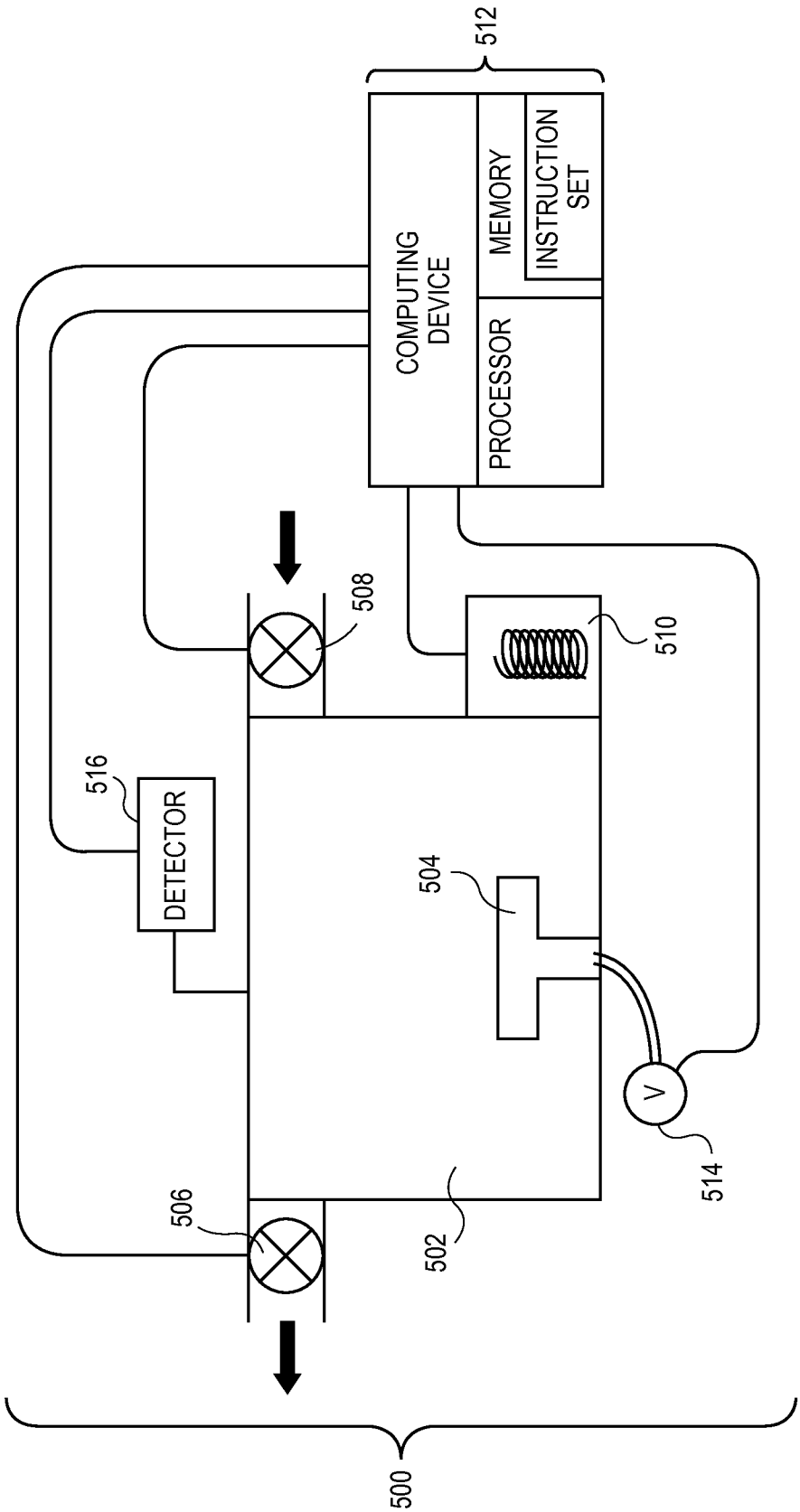

512
COMPUTING DEVICE
MEMORY
INSTRUCTION SET
PROCESSOR
508
510
516
DETECTOR
504
V
514
506
502
500

FIG. 5A

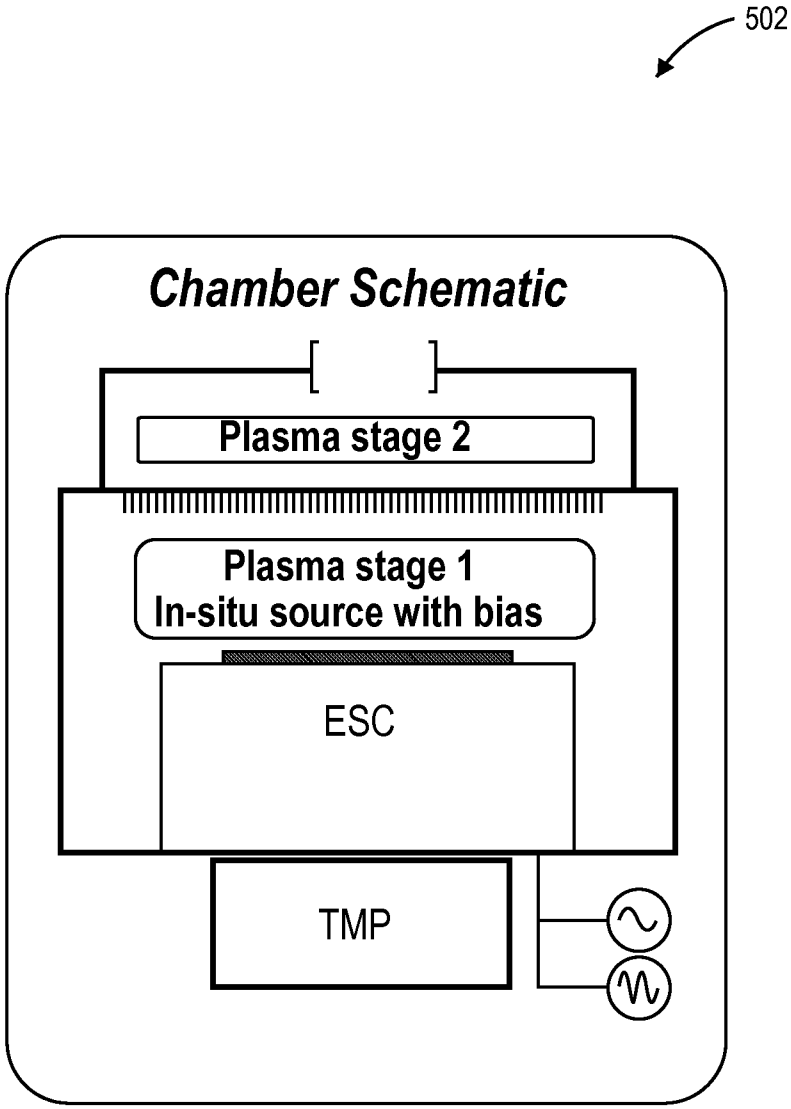

502
Chamber Schematic
Plasma stage 2
Plasma stage 1
In-situ source with bias
ESC
TMP

FIG. 5B

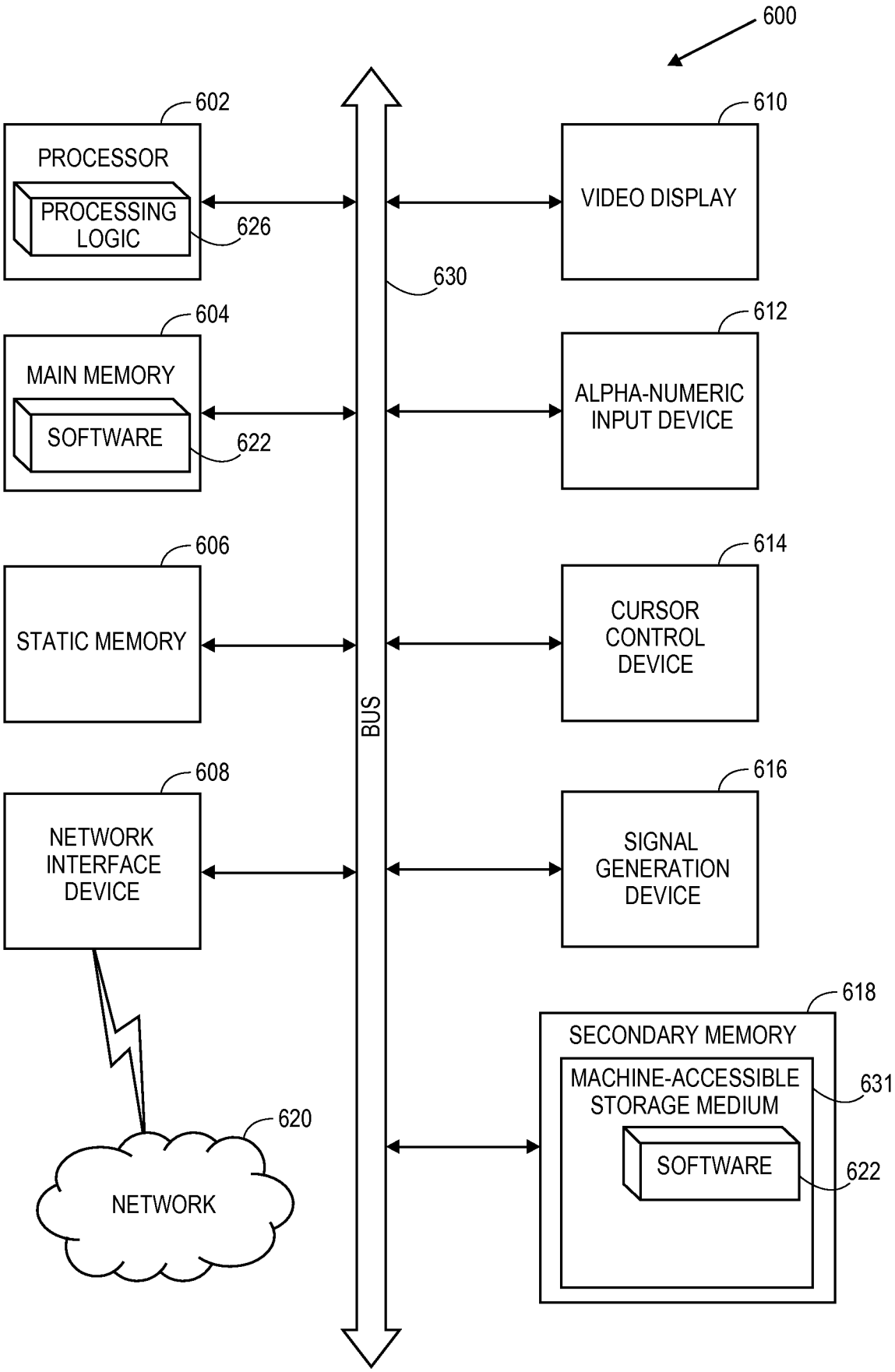

600
602
PROCESSOR
PROCESSING LOGIC
626
604
MAIN MEMORY
SOFTWARE
622
606
STATIC MEMORY
608
NETWORK INTERFACE DEVICE
620
NETWORK
BUS
630
610
VIDEO DISPLAY
612
ALPHA-NUMERIC INPUT DEVICE
614
CURSOR CONTROL DEVICE
616
SIGNAL GENERATION DEVICE
618
SECONDARY MEMORY
MACHINE-ACCESSIBLE STORAGE MEDIUM
631
SOFTWARE
622

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/047164

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/311(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/311; H01L 21/3065; H01L 21/28; H01L 21/31; H01L 21/461

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: low-k, dielectric, pattern, mask, etch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0032087 A1 (MASARU NISHINO et al.) 08 February 2007 See abstract, paragraphs [0016]-[0020] and figures 1A-1C.	1-4,6-11,13-15
A		5,12
Y	US 2008-0311756 A1 (CHIH-HAO CHEN et al.) 18 December 2008 See abstract, paragraphs [0021]-[0025] and figures 1-2.	1-4,6-11,13-15
A	KR 10-2002-0012106 A (SAMSUNG ELECTRONICS CO., LTD. et al.) 15 February 2002 See abstract, page 3 and figures 1e-1g.	1-15
A	KR 10-2012-0009443 A (LAM RESEARCH CORPORATION) 31 January 2012 See abstract, paragraphs [0013]-[0019] and figures 1-3.	1-15
A	KR 10-2010-0121440 A (LAM RESEARCH CORPORATION) 17 November 2010 See abstract, paragraphs [0015]-[0021] and figures 1-3.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 September 2013 (27.09.2013)	**27 September 2013 (27.09.2013)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. +82-42-472-7140

Authorized officer
CHOI Sang Won
Telephone No. +82-42-481-8291

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/047164

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