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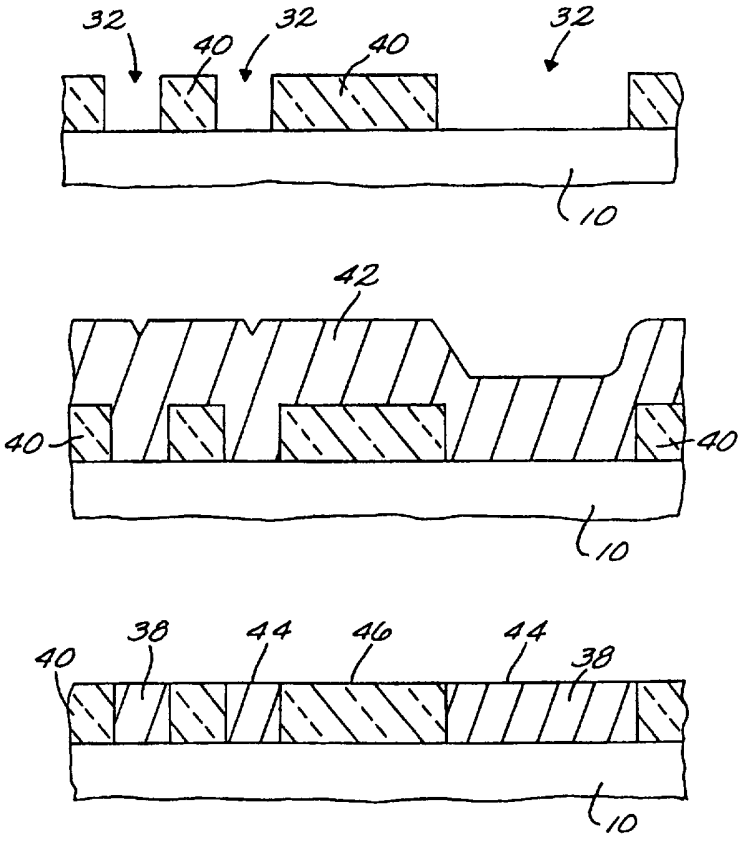
(54) Title: METHOD FOR FORMING CO-PLANAR CONDUCTOR AND INSULATOR FEATURES USING CHEMICAL MECHANICAL PLANARIZATION

(57) **Abstract**

A method is provided for forming conducting interconnects embedded in a layer of dielectric (38) such as an interlevel dielectric layer which resides over an integrated circuit structure (10). The conducting interconnects (38) and the layer of dielectric (40) may comprise, for example, metal and oxide, respectively. A CMP process which polishes both the interconnect material (i.e., the metal) and the dielectric (i.e., the oxide) at the same rate both locally and globally is employed to simultaneously polish the conducting interconnects (38) and the layer of dielectric (40). The CMP process effectively combines two CMP processing steps into one. Thus, the method of the present invention advantageously reduces the cost of manufacturing. Additionally, since both the layer of dielectric (40) and the conducting interconnects (38) are planarized in a single polishing step which polishes the interconnect material and the dielectric (e.g., metal and oxide) at rates which are essentially the same, the surface of the conducting interconnects (44) is level or co-planar with the surface of the layer of dielectric (46). The method of the present invention can be repeated to build multiple levels of conducting interconnects (38).



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METHOD FOR FORMING CO-PLANAR CONDUCTOR AND INSULATOR FEATURES USING CHEMICAL MECHANICAL PLANARIZATION

TECHNICAL FIELD

The present invention relates generally to chemical mechanical polishing or chemical mechanical planarization (CMP). More particularly, the present invention relates to polishing adjacent conductor and insulator surfaces such that the conductor and insulator surfaces are level or co-planar.

BACKGROUND ART

Chemical mechanical polishing is widely accepted for polishing semiconductor wafers. In particular, CMP is used to planarize the surfaces of conducting and insulating layers such as metal and oxide which are supported over a semiconductor wafer.

The main benefit of performing chemical mechanical polishing is to achieve global as well as local planarity. Local planarity corresponds to providing planarization over small regions of the wafer surface less than about 100 micrometers wide, while global planarity corresponds to providing planarization over one stepper field or over the entire wafer surface.

In particular, CMP is employed in the formation of multilayer interconnects, i.e., conducting interconnects used to form electrical connection to integrated circuit devices formed in a semiconductor wafer. Each level of conducting interconnects is supported over the semiconductor wafer by a layer of dielectric. Generally, the semiconductor wafer is coated with the layer of dielectric (e.g., a layer of oxide) and conducting lines (e.g., metal lines) are laid down on the layer of dielectric. Additional levels of conducting lines (i.e., metal lines) are formed over this layer of dielectric, each separated by an additional layer of dielectric, i.e., an interlevel dielectric layer. Contact between each level of metal lines is formed through vias in each of the interlevel dielectric layers. (As used herein, the term conducting interconnects corresponds to conducting lines, contacts, and/or vias. Accordingly, the term metal interconnects corresponds to metal lines, contacts, and/or vias.)

Chemical-mechanical polishing is used to planarize the layers of dielectric which isolate the conducting interconnects. Chemical-mechanical polishing is also employed to form the conducting interconnects using a damascene process, e.g., damascene metallization. (By "damascene metallization" is meant a process in which trenches or contact/via openings are formed and then filled with metal, followed by polishing to remove

any overfilled areas. The term is based on a process developed by goldsmiths in ancient Damascus, comprising crafting a pattern or design on a hard surface and then hammering fine gold wires onto the designed pattern.) A typical damascene metal process is described in, e.g., U.S. Patent 4,944,836.

To form a single level of metal interconnects using damascene metallization, a layer of dielectric such as a layer of oxide is first deposited. Trenches are cut into the oxide using a mask which enables the layer of oxide to be etched to form trenches having a shape and size identical to the shape and size of the metal interconnects to be formed therein. A metal film is deposited thereby filling the trenches with metal. The metal film is polished to remove metal outside the trenches and to form a surface on the metal which is planar. The metal is polished selectively with respect to the surrounding oxide; i.e., the metal is polished at a rate that is larger than the rate at which the oxide is polished. Accordingly, control is maintained over the thickness of the oxide. Ideally, the thickness of the layer of oxide is not reduced or is minimally reduced. Since the rate at which the oxide is polished is smaller than the rate at which the metal is polished, the oxide effectively serves as a polish stop which assists in and eases the requirements for endpoint detection.

Disadvantageously, the metal in the trenches which are wider is dished out due to polishing. (Metal dishing results from the relative softness of the metal in comparison to the relatively hard oxide as well as from the physical nature of the polishing pad employed in polishing.) Dishing is characterized by the recessed surface of the metal and thus causes steps or undulations to be formed in the surface of the metal.

Next, an insulator film comprising, e.g., an additional layer of oxide, is formed over the metal and oxide in order to electrically isolate the metal interconnects. This additional layer of oxide conforms to the shape of the layer of metal thereunder. Thus, the steps or undulations in the surface of the metal are typically replicated in the insulator film deposited thereon. It is conventional, consequently, to polish the additional layer of oxide to produce an insulator film which is planar. This insulator film is polished prior to performing any additional processing steps which are directed to a contact/via mask formation and subsequent etching.

An alternative method for planarizing a layer of oxide is outlined in U.S. Patent 4,954,459. The method described therein involves oxide deposition followed by masking wherein openings in the mask are in registry with raised portions of the oxide. Wet etching is employed to etch the raised portions of the oxide down to approximately the same height as the low portions of the oxide. The mask is stripped and polishing is used to remove any remaining raised portions of the oxide. This process for planarizing a layer of oxide, however, involves additional masking and etching in addition to polishing, and thus, increases process complexity.

What is needed is a method for forming metal interconnects surrounded by oxide which is simpler and does not require additional polishing steps directed to planarizing the oxide.

DISCLOSURE OF INVENTION

In accordance with the invention, a method is provided for forming at least one conducting interconnect embedded in a dielectric which resides over an integrated circuit structure. The method comprises the steps of:

(a) forming a layer of dielectric having a surface which is not polished over the integrated circuit structure;

(b) patterning the layer of dielectric thereby forming openings therein;

(c) depositing a layer of interconnect material filling the openings;

(d) polishing the layer of interconnect material using chemical mechanical polishing to remove a portion thereof such that the surface of the layer of dielectric is exposed and conducting interconnects each having a surface are thereby formed; and

(e) continuing polishing to planarize the layer of dielectric and the conducting interconnects, both the layer of interconnect material and the layer of dielectric being polished at rates which are essentially the same such that the surface of the layer of dielectric which is exposed is level with the surface of the conducting interconnects.

The conducting interconnects may be conducting lines, contacts, and/or vias comprising metal or polysilicon. Examples of metal suitably employed in the method of the present invention include tungsten, aluminum, copper, gold, silver, and alloys thereof. Examples of dielectrics which may be employed in the method of the present invention include undoped oxide, doped oxide, nitride, and low-k dielectric.

It will be appreciated that the above steps can be repeated to build multiple levels of conducting interconnects.

With the method of the present invention, a one-step CMP process which polishes both the interconnect material and the dielectric at the same rate both locally and globally is employed to simultaneously polish the layer of interconnect material and the layer of dielectric. The one-step CMP process effectively combines two CMP processing steps into one. Thus, the method of the present invention advantageously reduces the cost of manufacturing for processes which require CMP processing such as damascene processing.

Additionally, since both the layer of dielectric and the conducting interconnects are planarized in a single polishing step which polishes the dielectric and the interconnect material at rates which are essentially the same, the surface of the conducting interconnects is level or co-planar with the surface of the layer of dielectric.

Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and accompanying drawings, in which like reference designations represent like features throughout the Figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings referred to in this description should be understood as not being drawn to scale except if specifically noted. Moreover, the drawings are intended to illustrate only one portion of an integrated circuit fabricated in accordance with the present invention.

FIGS. 1a-1h are cross-sectional views of an integrated circuit structure depicting various stages of a prior art method for forming metal interconnects which employs conventional damascene processing;

FIGS. 2a-2c are cross-sectional views at various stages in the processing of an integrated circuit structure in accordance with one embodiment of the present invention; and

FIGS. 3a-3e are cross-sectional views at various stages in the processing of an integrated circuit structure in accordance with another embodiment of the present invention.

BEST MODES FOR CARRYING OUT THE INVENTION

Reference is now made in detail to a specific embodiment of the present invention, which illustrates the best mode presently contemplated by the inventors for practicing the invention. Alternative embodiments are also briefly described as applicable.

The method of the present invention is directed to forming conducting interconnects embedded in a layer of dielectric which resides over an integrated circuit structure. The conducting interconnects form electrical connection to integrated circuit devices formed in the integrated circuit structure. (Typically, the integrated circuit devices are formed in a semiconductor wafer from which the integrated circuit structure is built.)

In accordance with the present invention, the conducting interconnects may comprise conducting lines, contacts, and/or vias (i.e., conducting plugs formed in contact and/or via openings).

The method of the present invention comprises the steps of:

(a) forming a layer of dielectric having a surface which is not polished over the integrated circuit structure;

(b) patterning the layer of dielectric thereby forming openings therein;

(c) depositing a layer of interconnect material filling the openings;

(d) polishing the layer of interconnect material using chemical mechanical polishing to remove a portion thereof such that the surface of the layer of dielectric is exposed and conducting interconnects each having a surface are thereby formed; and

(e) continuing polishing to planarize the layer of dielectric and the conducting interconnects, both the layer of interconnect material and the layer of dielectric being polished at rates which are essentially the same such that the surface of the layer of dielectric which is exposed is level with the surface of the conducting interconnects.

The method of the present invention can be repeated to form multiple levels of conducting interconnects, each level of conducting interconnects being electrically isolated by a layer of dielectric.

Preferably, the conducting interconnects comprise metal, however, the conducting interconnects may alternatively comprise polysilicon. Examples of metal suitably employed in the method of the present invention include tungsten, aluminum, copper, gold, silver, and alloys thereof.

Preferably, the layer of dielectric comprises oxide (undoped oxide such as silicon dioxide), however, the layer of dielectric may alternately comprise other dielectrics. Examples of dielectrics which may be employed in the method of the present invention include doped oxide (e.g., boron silane-based glass, phosphorous silane-based glass, boron phosphorous silane-based glass, and boron phosphorous tetra-ethyl orthosilicate), nitride (e.g., silicon nitride), and low-k dielectric (e.g., deposited low-k dielectric or low-k spin-on dielectric). By

"low-k dielectric" is meant a dielectric having a dielectric constant, k, that is less than that of silicon dioxide, or less than about 4.0.

Referring now to FIGS. 1a-1h, wherein like reference numerals designate like elements throughout, a prior art process for forming conducting interconnects (i.e., metal lines and metal plugs) using conventional damascene processing is shown. First, the metal lines which are isolated by a first insulator film are created. Then, the metal plugs which are surrounded by a second insulator film (i.e., an interlevel dielectric layer) are formed. In this prior art process, both the metal lines and the metal plugs are fabricated using a damascene metal process.

FIG. 1a depicts an integrated circuit structure **10** having a first insulator film **12** which is patterned, formed thereon. In forming the first insulator film **12**, a dielectric, e.g., oxide, is deposited and trenches **14** are cut therein using a mask (not shown). The first insulator film **12** is etched to create the trenches **14** which have a shape and size identical to the shape and size of metal lines **16** (shown in FIG. 1c) to be formed therein.

A first metal film **18** (see FIG. 1b) is deposited on the first insulator film **12** thereby filling the trenches **14** with metal. As depicted in FIG. 1b, the first metal film **18** conforms to the shape of the first insulator film **12**. Fluctuations in the surface **20** of the first metal film **18** (such as indicated by arrows **22**) exist above the trenches **14**. The trenches **14** which are wider produce larger fluctuations in the surface **20** of the first metal film **18**. The first metal film **18** is polished to remove metal outside the trenches **14**, thereby forming metal lines **16** as shown in FIG. 1c. Polishing the first metal film **18** also forms a surface **24** on some of the metal lines **16** which is planar.

Conventional metal CMP is used to polish the first metal film **18**. Commercially available polishing slurries and a conventional CMP polish tool are employed. As is conventional in the prior art, the metal comprising the first metal film **18** is polished selectively with respect to the surrounding oxide comprising the first insulator film **12**; that is, the metal is polished at a rate which is larger than the rate at which the oxide is polished. Accordingly, control is maintained over the thickness of the first insulator film **12**. Ideally, the thickness of the first insulator film **12** is not reduced or is minimally reduced. Since the rate at which the oxide is polished is smaller than the rate at which the metal is polished, the first insulator film **12** effectively serves as a polish stop which assists in and eases the requirements for endpoint detection.

Disadvantageously, the metal in the trenches **14** which are wider is dished out due to polishing. Steps or undulations are thus caused to be formed in the surface **24** of some of the metal lines **16** using the prior art process. Arrow **26** points to the recessed surface **24** of one of the metal lines **16** shown in FIG. 1c which is caused by dishing.

A second insulator film **28** (see FIG. 1d) is then formed over the first insulator film **12** and the metal lines **16**. The second insulator film **28** serves as an interlevel dielectric layer which electrically isolates the metal lines **16**. This second insulator film **28** conforms to the shape of the first insulator film **12** and the metal lines **16** which reside thereunder. Thus, the steps or undulations in the surface **24** of some of the metal lines **16** are typically replicated in the second insulator film **28** deposited thereon.

Consequently, it is conventional in the prior art to polish the second insulator film **28** to planarize the surface **30** of the second insulator film. (It will be appreciated that with the method of the present invention,

this polishing step is not required.) In the case where the second insulator film **28** comprises oxide, oxide CMP (which stops on oxide) is typically employed. With oxide CMP, oxide on the surface **30** is removed, producing a planar second insulator film **28** above the metal lines **16** as shown in FIG. 1e. Accordingly, metal deposited on the surface **30** of the second insulator film **28**, will also be have a planar surface. Conventionally, the second insulator film **28** is polished prior to performing any additional processing steps which are directed to contact/via mask formation and subsequent etching.

As depicted in FIG. 1f, the second insulator film **28** is patterned to form openings or vias **32** therein. A second metal film **34** is deposited over the second insulator film **28** and into the openings or vias **32** formed therein; see FIG. 1g. The second metal film **34** is polished to remove a portion of the metal and to expose the second insulator film **28**. Metal plugs **36** are thereby formed in the openings or vias **32** as shown in FIG. 1h.

As describe above, with the prior art process shown in FIGS. 1a-1h, the metal in the trenches **14** which are wider (such as indicated by arrow **26** in FIG. 1c) is dished out due to polishing. With the process of the present invention, however, such metal dishing is minimized.

FIGS. 2a-2c depict one embodiment of the present invention wherein conducting interconnects **38** comprising metal (shown in FIG. 2c) are formed in a layer of dielectric **40**. The conducting interconnects **38** may comprise, for example, conducting lines (metal lines **16**) or conducting plugs (metal plugs **36**) formed in contact or via openings **32**.

FIG. 2a depicts an integrated circuit structure **10** having a layer of dielectric **40** which is patterned, formed thereon. To form the layer of dielectric **40**, a dielectric comprising, e.g., oxide, is deposited and openings or vias **32** are cut therein using a mask (not shown). The layer of dielectric **40** is etched, e.g., using reactive ion etching (RIE) to create the openings or vias **32** which have a shape and size identical to the shape and size of conducting interconnects **38** to be formed therein.

In accordance with the method of the present invention, however, the layer of dielectric **40** is not polished. As depicted in FIG. 2a, the layer of dielectric **40** is instead directly patterned to form openings or vias **32** therein. The openings or vias **32** are patterned in the layer of dielectric **40** using a mask (not shown) and an etching process conventionally employed for etching the dielectric, e.g., oxide. While three openings or vias **32** are shown, it will be readily apparent to those skilled in the art that in fact any number of such openings or vias can be employed.

A layer of interconnect material (layer of metal) **42** is deposited over the layer of dielectric **40** and into the openings or vias **32** formed therein as shown in FIG. 2b. The layer of interconnect material or layer of metal **42** may be deposited using conventional deposition techniques such as chemical vapor deposition, hot metal deposition, physical vapor deposition (PVD) sputtering, electroplating, or electroless depositions. Examples of metals suitably employed as the layer of metal **32** include tungsten, aluminum, copper, gold, silver, and alloys thereof. Other metals may be suitably employed as the layer of metal **42** as well.

The layer of metal **42** is polished to remove a portion of the metal and to expose the layer of dielectric **40**. Metal interconnects (conducting interconnects) **38** are thereby formed in the openings or vias **32**; see FIG. 2c. Each of the metal interconnects **38** which is formed has a surface **44** that is planar as a result of the chemical mechanical polishing of the layer of metal **42**. While three metal interconnects **38** are shown, it will be

readily apparent to those skilled in the art that in fact any number of such metal interconnects can be employed.

Commercially available polishing slurries and a conventional CMP polish tool can be employed in the method of the present invention. It will be appreciated, however, that the method of the present invention does not employ conventional metal CMP which is used in prior art to form metal interconnects **38** via damascene metal processing. With conventional metal CMP, polishing stops partly on metal and partly on dielectric, e.g., oxide. As described above, with metal CMP shown in prior art, the metal is polished selectively with respect to the surrounding dielectric; i.e., the metal is polished at a rate that is larger than the rate at which the dielectric material is polished.

In contrast, with the method of the present invention, a one-step CMP process which polishes both metal and dielectric (e.g., oxide) at the same rate both locally and globally is employed to simultaneously polish the layer of metal **42** and the layer of dielectric **40**. Thus, the layer of dielectric **40** which is exposed is polished as well in this single polishing step. This single polishing step planarizes both the metal interconnects **38** and the layer of dielectric **40**. Accordingly, FIG. 2c depicts the layer of dielectric **40** having a surface **46** which is planar. (It will be appreciated that the rate of polishing of the metal and the dielectric is controlled by the composition of the polishing slurry.)

Since both the layer of dielectric **40** and the metal interconnects **38** are planarized in a single polishing step which polishes the metal and dielectric at rates which are essentially the same, the surface **44** of the metal interconnects **38** is level or co-planar with the surface **46** of the layer of dielectric **40**. In other words, the surface **44** of the metal interconnects **38** is flush with the surface **46** of the surrounding oxide comprising the layer of dielectric **40**.

The one-step CMP process which polishes both metal and dielectric at the same rate and thereby simultaneously planarizes both the metal interconnects **38** and the layer of dielectric **40** effectively combines two CMP processing steps into one. Thus, the method of the present invention advantageously reduces the cost of manufacturing for processes which require CMP processing such as damascene metal processing.

It will be appreciated that the method of the present invention described above can be repeated to build multilayer interconnects comprising additional levels of metal interconnects **38** electrically isolated by layers of dielectric **40** which serve as interlevel dielectric layers.

It will further be appreciated that the conductive interconnects **38** may alternatively comprise polysilicon. For example, the method of the present invention may be employed to form conductive interconnects **38** comprising polysilicon embedded in a layer of dielectric **40** comprising, e.g., oxide.

Additionally, other suitable dielectrics may be employed in the practice of the present invention. Examples of dielectrics suitably employed as the layer of dielectric **40** include doped oxide (e.g., boron silane-based glass, phosphorous silane-based glass, boron phosphorous silane-based glass, and boron phosphorous tetra-ethyl orthosilicate), nitride (e.g., silicon nitride), or low-k dielectric (e.g., deposited low-k dielectric or low-k spin-on dielectric).

In an alternative embodiment, the method of the present invention is employed to form conducting interconnects **38** which contact metal lines **16** wherein the metal lines are formed by patterning metal with a

mask. First, the metal lines **16** which are electrically isolated by a layer of dielectric **40** comprising, e.g., oxide, are created, then the metal interconnects **38** are formed.

Referring now to FIG. 3a, an integrated circuit structure **10** is depicted having metal lines **16** formed thereon. To form the metal lines **16**, metal is deposited over the integrated circuit structure **10** and subsequently patterned using a mask (not shown). While five metal lines **16** are shown, it will be readily apparent to those skilled in the art that in fact any number of such metal lines can be employed.

A layer of oxide (layer of dielectric) **40** is formed over the integrated circuit structure **10** and the metal lines **16** as shown in FIG. 3b. The layer of oxide **40** serves as an interlevel dielectric layer which electrically isolates the metal lines **16**. This layer of oxide **40** conforms to the shape of the integrated circuit structure **10** and the metal lines **16** formed thereon. Fluctuations in the surface **46** of the layer of oxide **40** (such as indicated by arrows **48**) are caused by the non-planar topography produced by the metal lines **16** formed on the integrated circuit structure **10**.

It is conventional in the prior art to polish the layer of oxide **40** using an oxide CMP process to planarize the surface **46** of the layer of dielectric. With oxide CMP, oxide on the surface **46** is removed, producing a planar layer of oxide **40** above the metal lines **16**. Polishing the layer of oxide **40** at this stage, as is conventional, ensures that the surface **48** of the layer of dielectric **40** is planar both locally and globally. Conventionally, the layer of oxide **40** is polished prior to performing the additional processing steps which are directed to a contact/via mask formation and subsequent etching. With prior art approaches, vias **32** are formed in the layer of oxide **40** using a via mask and etch process. Metal plugs **36** are formed in the vias **32** by depositing metal on the layer of oxide **40** and into the openings or vias **32**. The metal is subsequently polished using metal CMP to form the metal plugs **36**. With the prior art approach, the metal is polished selectively with respect to the surrounding oxide; that is, the metal is polished at a rate which is larger than the rate at which the dielectric is polished.

In accordance with the method of the present invention, however, the layer of oxide **40** is not polished. As shown in FIG. 3c, the layer of oxide **40** is instead directly patterned to form openings or vias **32** therein. The openings or vias **32** are patterned in the layer of oxide **40** using a via mask (not shown) and a via etch process conventionally employed for etching oxide. While four openings or vias **32** are shown, it will be readily apparent to those skilled in the art that in fact any number of such openings or vias can be employed.

Since the layer of oxide **40** is not polished, the thickness of the oxide is substantially the same over each of the metal lines **18**. Consequently, via etch control is simplified as variation in the thickness of the dielectric, i.e., the oxide, is minimized or eliminated.

A layer of metal (layer of interconnect material) **42** comprising plug metal is deposited over the layer of oxide **40** and into the openings or vias **32** formed therein as depicted in FIG. 3d. The layer of metal **42** may be deposited using conventional deposition techniques such as chemical vapor deposition, hot metal deposition, physical vapor deposition (PVD) sputtering, electroplating, or electroless depositions. Examples of metals suitably employed as the layer of metal **42** include tungsten, aluminum, copper, gold, silver, and alloys thereof. Other interconnect materials may be suitably employed as the layer of interconnect material **42** as well. (As described above, conducting interconnects **38** may alternatively comprise polysilicon, in which case the layer of

interconnect material **42** also comprises polysilicon.)

The layer of metal **42** is polished to remove a portion of the metal and to expose the layer of oxide **40**; see FIG. 3e. Metal interconnects **38** such as via plugs **16** are thereby formed in the openings or vias **32** in the layer of oxide **40**. Each of the metal interconnects **38** which is formed has a surface **44** which is planar as a result of the chemical mechanical polishing of the layer of metal **42**. While four metal interconnects **38** are shown, it will be readily apparent to those skilled in the art that in fact any number of such metal interconnects can be employed.

Commercially available polishing slurries and a conventional CMP polish tool can be employed in the method of the present invention. It will be appreciated, however, that the method of the present invention does not employ conventional metal CMP which is used in prior art to form metal interconnects **38** via damascene metal processing. As described above, with conventional metal CMP, the metal is polished selectively with respect to the surrounding oxide; i.e., the metal is polished at a rate that is larger than the rate at which the dielectric is polished.

In contrast, with the method of the present invention, a one-step CMP process which polishes both metal and dielectric (oxide) at the same rate both locally and globally is employed to simultaneously polish the layer of metal **42** and the layer of oxide **40**. Thus, the layer of oxide **40** which is exposed is polished as well in this single polishing step. This single polishing step planarizes both the surface **44** of the metal interconnects **38** and the surface **46** of the layer of oxide **40**. Accordingly, FIG. 3e depicts the surface **46** of the layer of oxide **40** as planar. As described above, the rate of polishing of the metal and the dielectric is controlled by the composition of the polishing slurry.

Since both the metal interconnects **38** and the layer of dielectric **40** are planarized in a single polishing step which polishes the metal and the dielectric at rates which are essentially the same, the surface **44** of the metal interconnects is level or co-planar with the surface **46** of the layer of oxide.

It will be appreciated that endpoint detection may be employed as is conventional to determine when to stop polishing. Alternately, the CMP process could be a timed polish process. A timed polish process ensures that the surface **44** of the metal interconnects **38** is co-planar with the surface **46** of the layer of oxide **40** because polishing is not stopped until the surface of the metal interconnects and the surface of the layer of oxide are co-planar. In either case, the method of the present invention will ensure that the surface **44** of the conducting interconnects (metal interconnects) **38** and the surface **46** of the layer of dielectric (layer of oxide) **40** are co-planar both locally and globally.

As described above, other suitable dielectrics may be employed in the practice of the present invention. Examples of dielectrics suitably employed as the layer of dielectric **40** include doped oxide (e.g., boron silane-based glass, phosphorous silane-based glass, boron phosphorous silane-based glass, and boron phosphorous tetra-ethyl orthosilicate), nitride (e.g., silicon nitride), or low-k dielectric (e.g., deposited low-k dielectric or low-k spin-on dielectric).

The method of the present invention is applicable to IC technology having feature sizes of 0.5 μm and smaller.

The advantages of the method of the present invention include the following:

First, the thickness of the layer of dielectric **40** is substantially the same over each of the metal lines **16** at the stage when the via etch is performed. Consequently, via etch control is simplified as variation in the thickness of the layer of dielectric **40** which is to be etched is minimized.

Second, the process of the present invention simplifies manufacturing and construction of conducting interconnects **38** and makes the via etch process easy; thereby lowering cost and improving efficiency. Additionally, the throughput of the process of the present invention is high in comparison with prior art damascene processes since one less CMP process is employed. Consequently, the process of the present invention is more economical than prior art damascene processes.

Third, the method of the present invention described above can be repeated to build multilayer interconnects comprising additional levels of conducting interconnects **38** electrically isolated by layers of dielectric **40** which serve as interlevel dielectric layers.

INDUSTRIAL APPLICABILITY

The method of the present invention is expected to find use in the fabrication of deep sub-micrometer IC technology.

The foregoing description of the preferred embodiment of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. Many variations of films and materials are possible. It is possible that the invention may be practiced in other fabrication technologies in MOS or bipolar processes. Similarly, any process steps described might be interchangeable with other steps in order to achieve the same result. The embodiment was chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

CLAIMS

What Is Claimed Is:

1. A method of forming at least one conducting interconnect (38) embedded in a dielectric formed over an integrated circuit structure (10), said method comprising the steps of:

(a) forming a layer of dielectric (40) having a surface (46) which is not polished over said integrated circuit structure (10);

(b) patterning said layer of dielectric (40) thereby forming openings (32) therein;

(c) depositing a layer of interconnect material (42) filling said openings (32);

(d) polishing said layer of interconnect material (42) using chemical mechanical polishing to remove a portion thereof such that said surface of said layer of dielectric (46) is exposed and conducting interconnects (38) each having a surface (44) are thereby formed; and

(e) continuing polishing to planarize said layer of dielectric (40) and said conducting interconnects (38), both said layer of interconnect material (42) and said layer of dielectric (40) being polished at rates which are essentially the same such that said surface of said layer of dielectric (46) which is exposed is level with said surface of said conducting interconnects (44).

2. The method of Claim 1 wherein said conducting interconnects (38) are selected from the group consisting of conducting lines, contacts, and vias.

3. The method of Claim 1 wherein said conducting interconnects (38) comprise material selected from the group consisting of metal and polysilicon.

4. The method of Claim 3 wherein said metal is selected from the group consisting of tungsten, aluminum, copper, gold, silver, and alloys thereof.

5. The method of Claim 1 wherein said layer of dielectric (40) comprises dielectric material selected from the group consisting of oxide, nitride, and low-k dielectric.

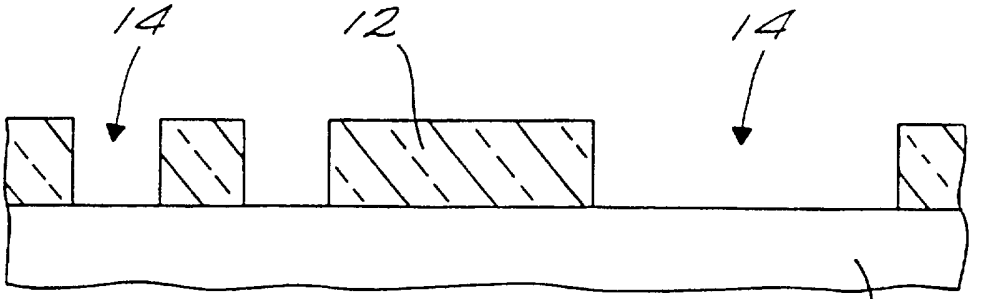
6. The method of Claim 5 wherein said layer of dielectric (40) comprises dielectric material selected from the group consisting of silicon dioxide and silicon nitride.

7. The method of Claim 5 wherein said layer of dielectric (40) comprises doped oxide.

8. The method of Claim 7 wherein said doped oxide is selected from the group consisting of boron silane-based glass, phosphorous silane-based glass, boron phosphorous silane-based glass, and boron phosphorous tetra-ethyl orthosilicate.

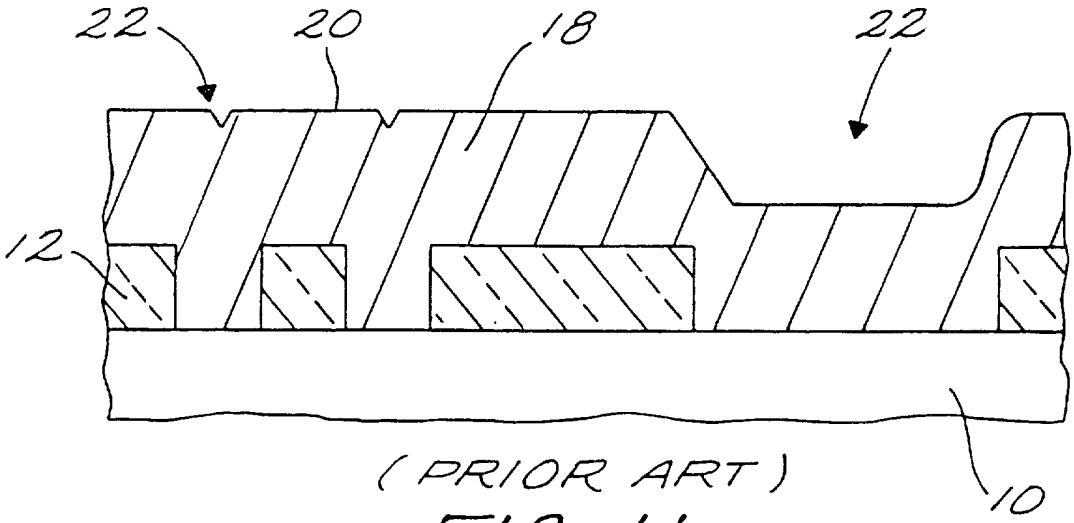
9. The method of Claim 1 wherein said layer of interconnect material (42) is formed by a deposition process selected from the group consisting of chemical vapor deposition, hot metal deposition, physical vapor deposition (PVD) sputtering, electroplating, and electroless deposition.

10. The method of Claim 1 wherein said steps (a) through (e) are repeated to form multiple layers of conducting interconnects (38).



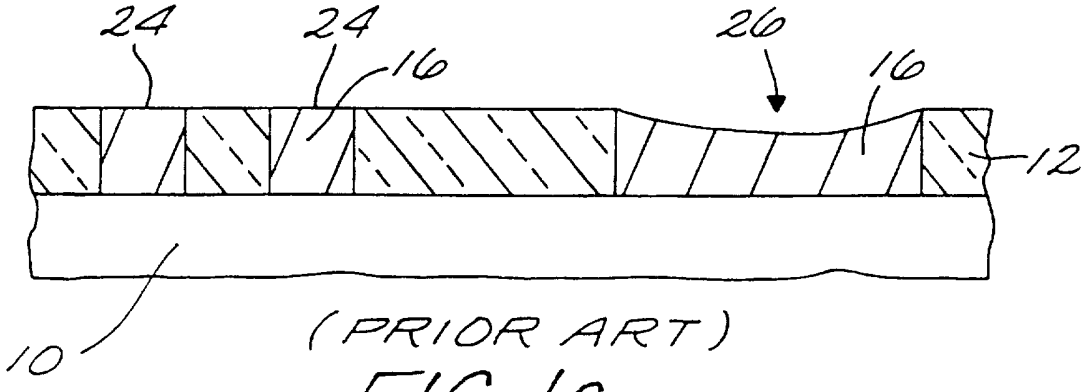
(PRIOR ART)

FIG. 1a



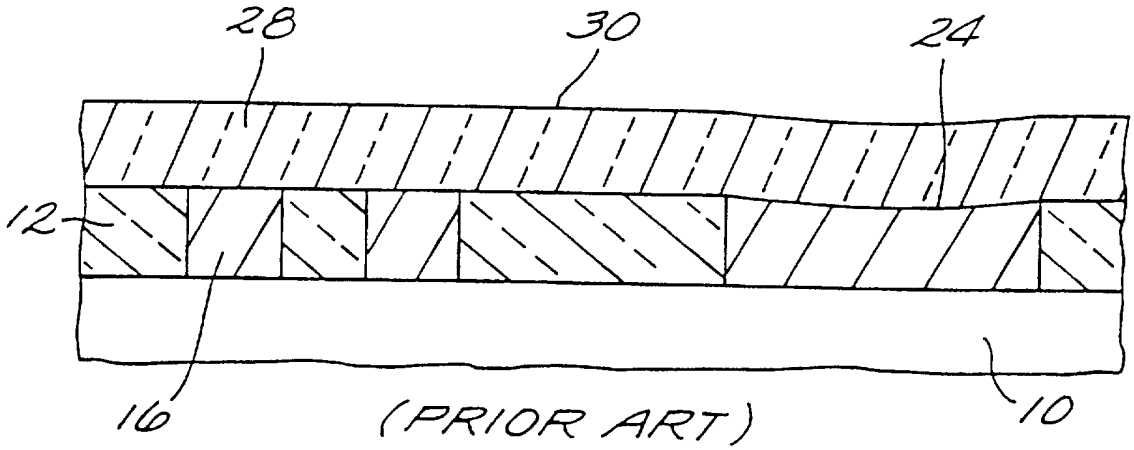
(PRIOR ART)

FIG. 1b



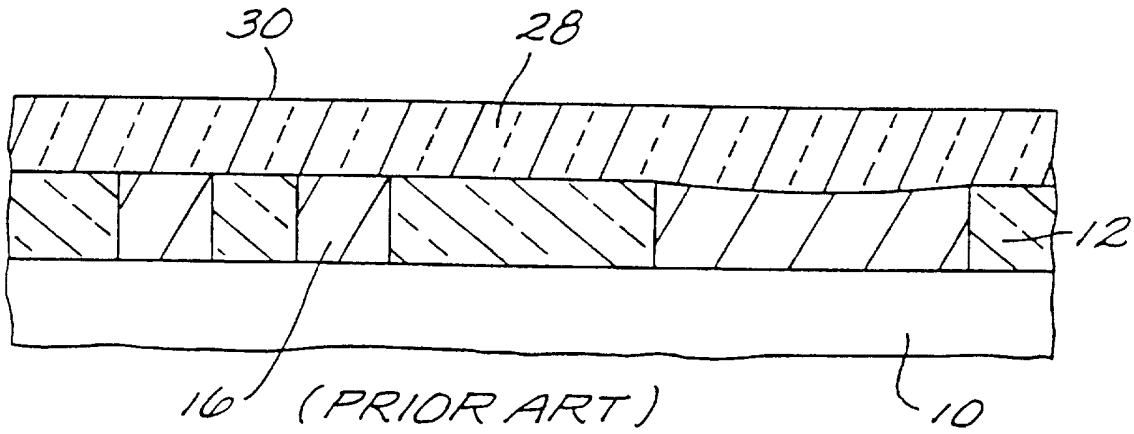
(PRIOR ART)

FIG. 1c



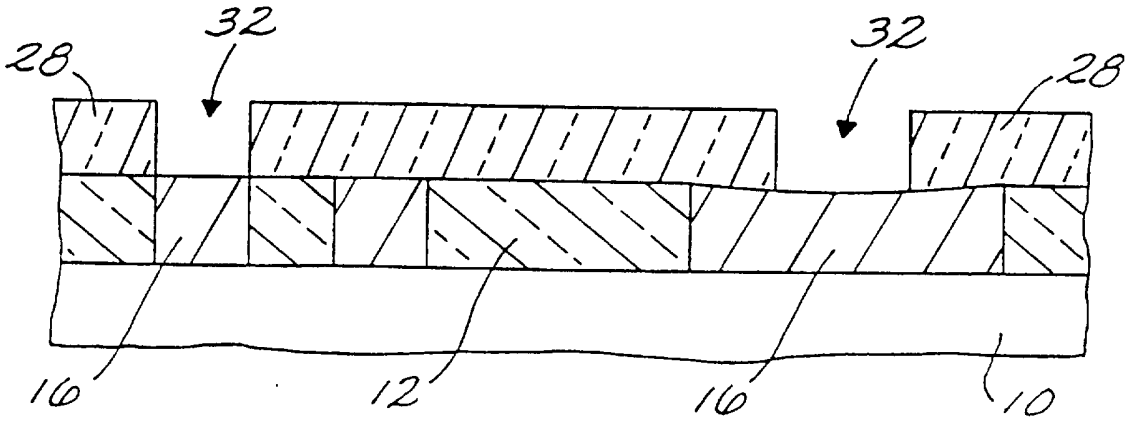
(PRIOR ART)

FIG. 1d



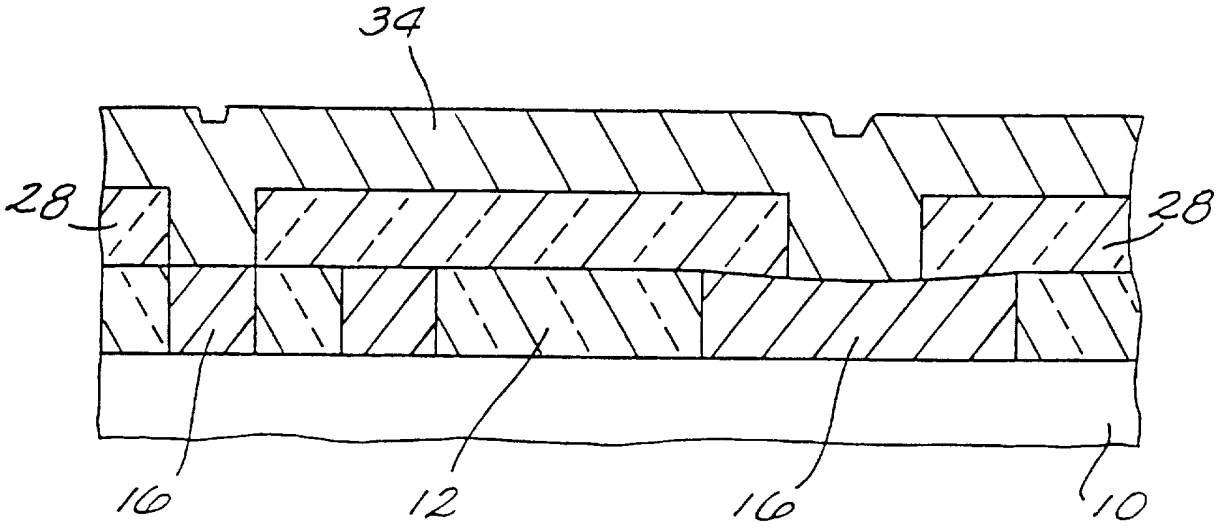
(PRIOR ART)

FIG. 1e



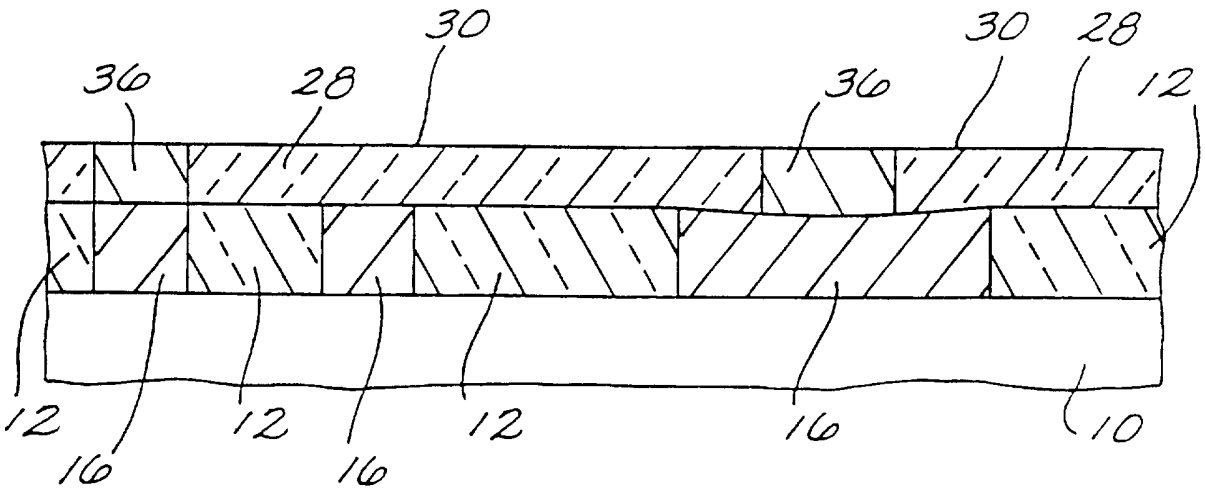
(PRIOR ART)

FIG. 1f



(PRIOR ART)

FIG. 1g



(PRIOR ART)

FIG. 1h

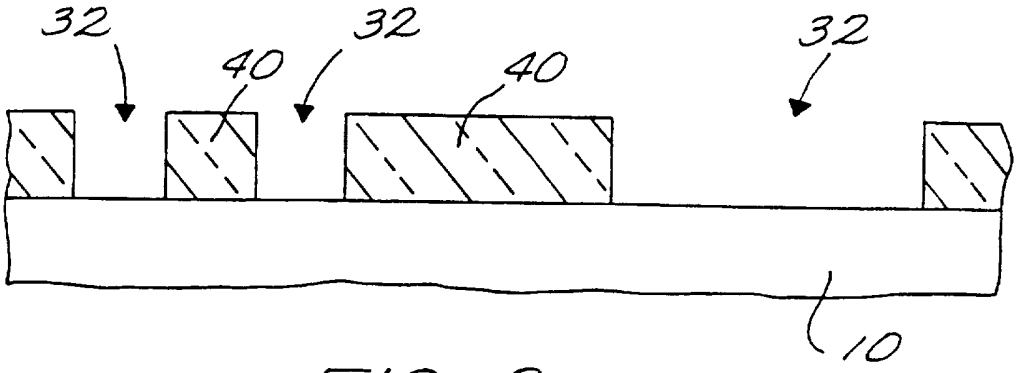


FIG. 2a

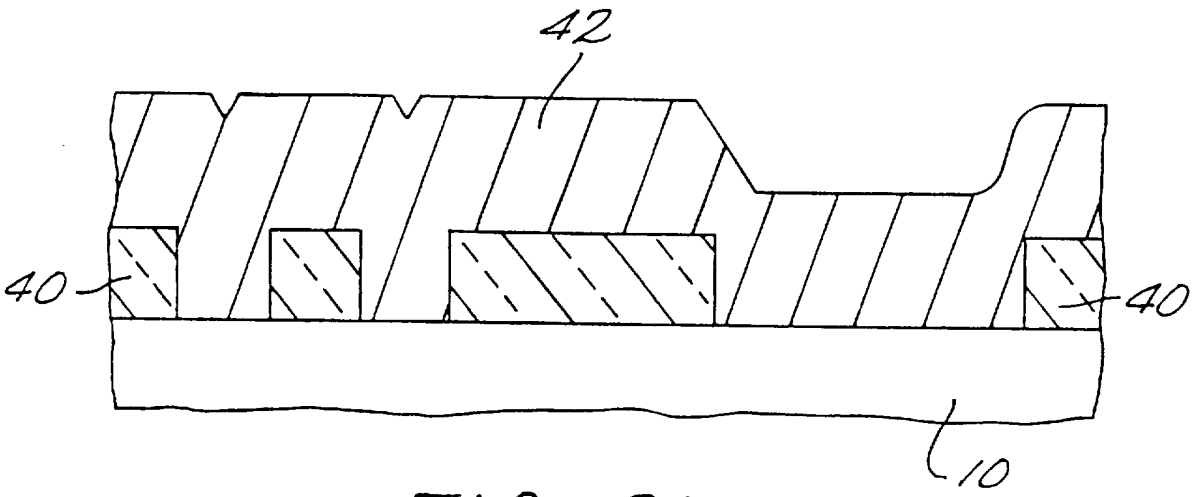


FIG. 2b

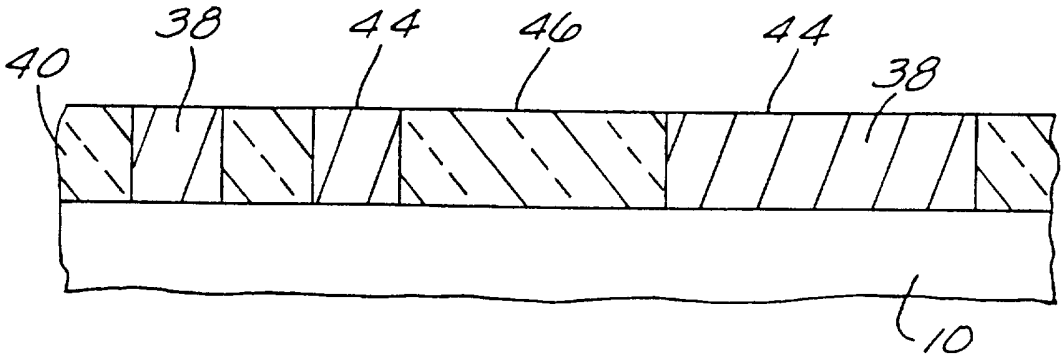


FIG. 2c

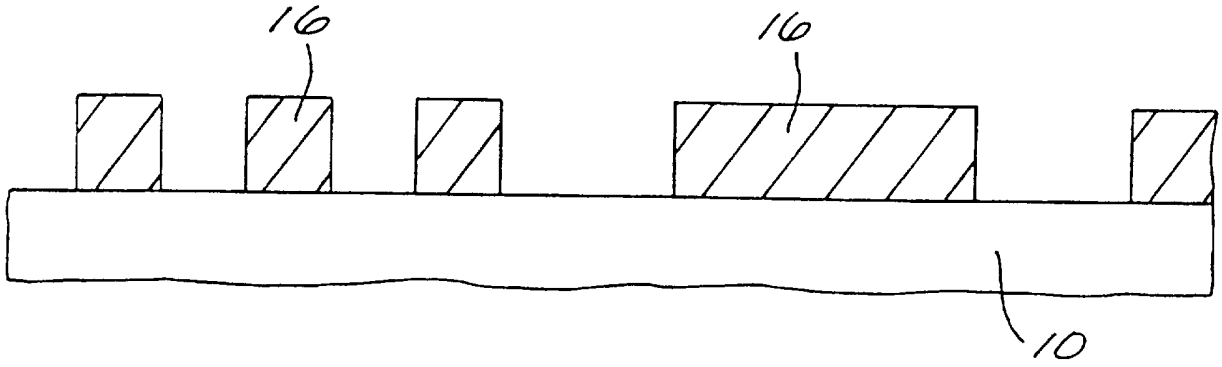


FIG. 3a

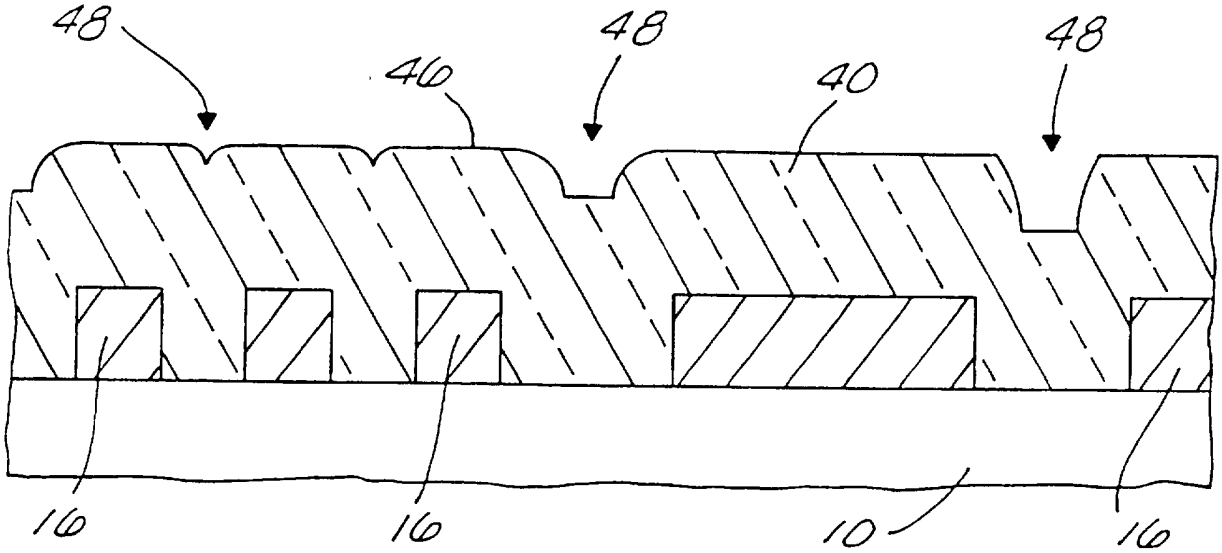


FIG. 3b

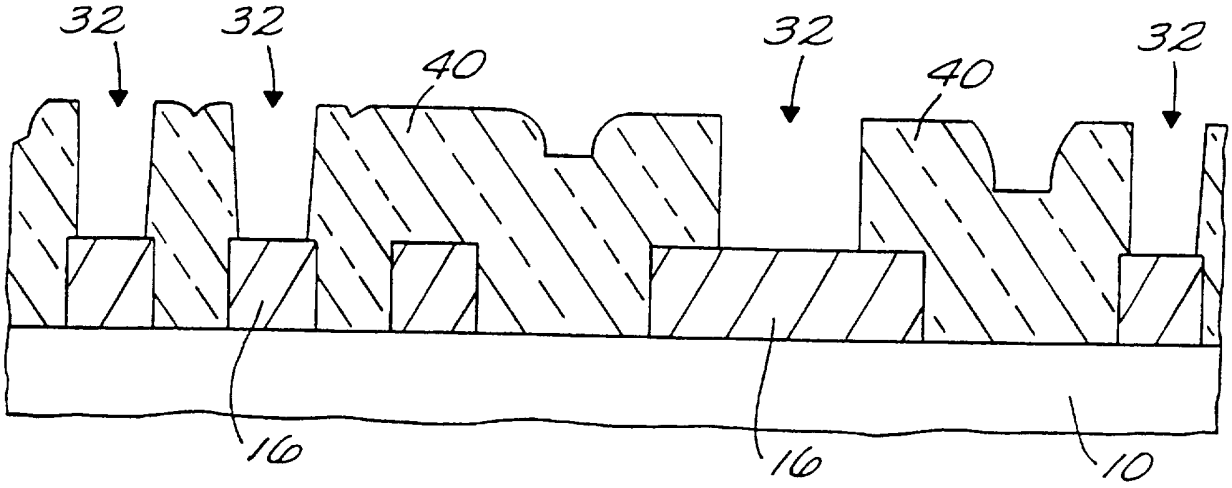


FIG. 3c

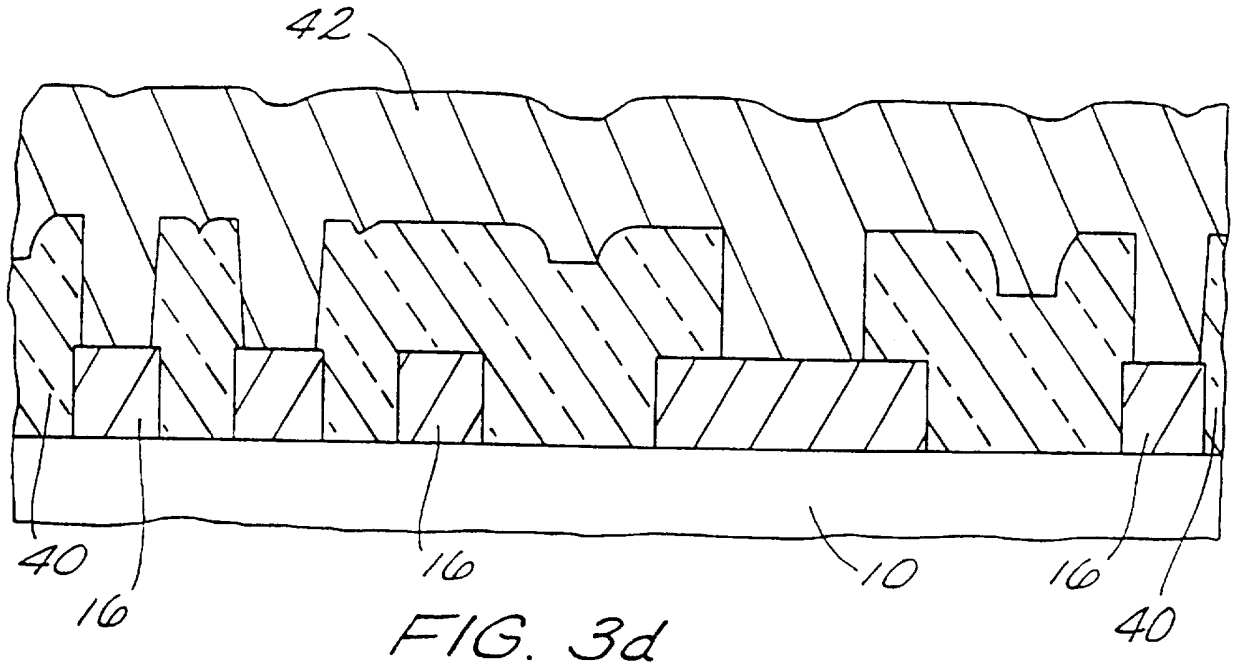


FIG. 3d

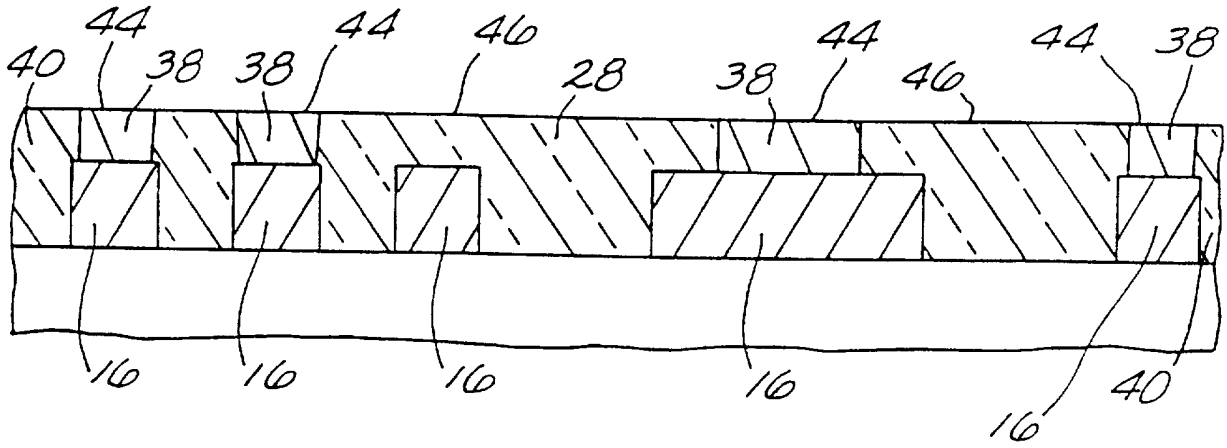


FIG. 3e

INTERNATIONAL SEARCH REPORT

Inter ial Application No
PCT/US 97/01714

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	THIN SOLID FILMS, vol. 220, no. 1 / 02, 20 November 1992, pages 1-7, XP000354467 LANDIS H: "INTEGRATION OF CHEMICAL-MECHANICAL POLISHING INTO CMOS INTEGRATED CIRCUIT MANUFACTURING" see paragraph 10; figure 7 ---	1-10
Y	DE 43 01 451 A (MICRON TECHNOLOGY INC) 5 August 1993 see column 2, line 50 - column 3, line 19 see column 4, line 56 - column 5, line 68; figures 3,4 ---	1-10
A	US 4 879 258 A (FISHER WAYNE G) 7 November 1989 see column 3, line 21 - column 4, line 8; figures ---	1-6

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 May 1997	11 -06- 1997

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Roussel, A

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INTERNATIONAL SEARCH REPORT

Inter. ial Application No
PCT/US 97/01714

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 954 459 A (AVANZINO STEVEN C ET AL) 4 September 1990 cited in the application see column 7, line 52 - column 9, line 64; figures 3-16	1
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 43, no. 5, 1 May 1996, pages 739-744, XP000596269 KIKUTA K ET AL: "ALUMINUM-GERMANIUM-COPPER MULTILEVEL DAMASCENE PROCESS USING LOW-TEMPERATURE REFLOW SPUTTERING AND CHEMICAL MECHANICAL POLISHING" see abstract; figure 1	10

1

INTERNATIONAL SEARCH REPORT

...formation on patent family members

Inter ...al Application No
PCT/US 97/01714

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		EP 0341898 A	15-11-89
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