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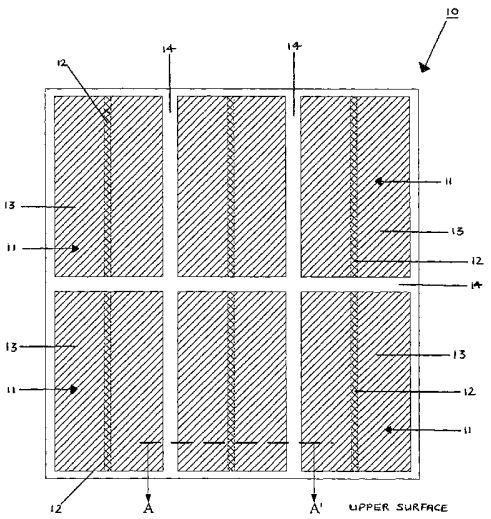
(54) Title: METHOD OF DICING A COMPLEX TOPOLOGICALLY STRUCTURED WAFER



(57) Abstract: In the present invention, the boundary of the or each chip on a wafer is defined by the absence of metallization and the presence of a continuous etched trench. The metallization, comprising the deposition of a metal layer, is not formed monolithically on the wafer, but is patterned to cover only the surface of the or each chip, thereby providing for electrical contact to the chip. The metal layer so deposited, contributes to the structural integrity and mechanical strength of the chip, but does not form a mechanical link between neighbouring chips. The trenches are etched to a depth that is substantially below the surface topology of the wafer. In particular, the trenches are etched to a depth that is substantially below layers in the wafer that contribute to the operation of devices fabricated on the wafer. Typically this would mean at least 3μm into the wafer substrate below the active regions grown on the substrate.

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METHOD OF DICING A COMPLEX TOPOLOGICALLY STRUCTURED WAFER

Field of the Invention

The present invention relates to a technique for separating devices fabricated on a common wafer, and particularly a wafer with a complex topological structure.

Background to the Invention

There is frequently a need to fabricate many types of small optical, electrical or mechanical devices in large number. In order to do this cheaply and efficiently they are often fabricated from a common wafer. Examples of such devices include the electronic integrated circuit (IC), the opto-electronic integrated circuit (OEIC) and micro-electro-mechanical system (MEMS). The individual devices reside on a region of the wafer which is generally termed a "die" when separated from the wafer.

One of the problems associated with multiple device fabrication on a single wafer is the subsequent need to separate the individual dies, a process known as "singulation". In the case of devices, such as silicon ICs, that are relatively homogeneous and planar in construction, the topological build up of the wafer surface is generally flat and any metallization is generally confined to the device boundaries. The height of the final wafer surface structure of classically designed electronic components and integrated circuits devices, typically varies by no more than a few times the feature size of the device circuitry. Commonly used for methods for dicing the wafer, to obtain single planar device chips, include wafer sawing procedures and wafer cleaving along the device boundaries.

In the case of OEICs, MEMS, or a combination of the two fabricated on a common wafer, the chips may comprise optical sources, optical waveguide devices, mechanical elements and structures for thermal control and stability. For such wafers, the topological structure height may vary by several tens or hundreds of times the feature size of any associated circuitry. Devices based on OEICs and MEMS are usually constructed from III-V semiconductor materials, which allows easy integration with electronic design elements on a single chip, but leads to a surface landscape that has a relatively complex topological structure. In particular, surface structures may include deep grooves and open envelopes that are up to 80 microns deep and 100 microns wide, to accommodate optical fibres and other waveguide components.

A further consideration is that for some devices, such as an OEIC comprising a laser diode, the side facet of the device is integral to its operation. Any damage to the

facet will lead to a degradation in device performance or even complete component failure. Thus a mechanical sawing process carries the inherent risk of damaging the device, by leaving chipped or scratched facets. The alternative procedure of cleaving the III-V material exposes clean facets, which at an interface with air exhibit a Fresnel reflectivity of approximately 35%. This level of reflectivity may be appropriate for the operation of some laser devices, but often the optimum value is much lower, 1% for example. Therefore, although the cleave and break approach is commonly used, the resulting device facets have subsequently to be coated with a low reflectivity optical coating.

During the manufacturing process the handling of device chips, which are only a few hundred microns thick, is extremely difficult and the devices are prone to damage. In order to control the subsequent dicing of the wafer, cleave stress points are used to define the desired break directions across the wafer. However, due to the deep surface relief structures and high topological structures, the controlled propagation of a break across the wafer can be interrupted and the cleave line then deviates from the desired path between the die boundaries and cracks through a well-constructed OEIC or MEMS chip, destroying the chip as a result.

An improved technique for dicing silicon IC chips fabricated on a wafer has been disclosed in U.S. patent No. 6,075,280, which proposes the wet etching of a V-groove into the silicon substrate upon which the IC chips are located, making use of the susceptibility of certain crystal planes of silicon to wet etching in order to realise the V-grooves. The wafer is then cleaved along the V-grooves to separate the individual IC chips.

However, there is still a clear need for an improved technique, whereby chips comprising complex optical, electrical and mechanical devices, and therefore characterized by complex topological structures fabricated on a wafer, may be cleanly separated with a reduced risk of degradation or damage to the chips and the devices thereon.

Summary of the Invention

According to the present invention, there is provided a method for processing a wafer having a plurality of chips integrated thereon, comprising the steps of:

applying a metal layer, by a metallization process, over an upper surface of the chips formed on an upper surface of the wafer, whilst leaving regions between adjacent chips unmetallized ;

etching a trench into said unmetallized regions of the wafer to a depth substantially below layers of material that form devices on the wafer; and,

cleaving the wafer along lines defined by the trenches formed in the wafer.

Preferably, the wafer is thinned to the desired final thickness by applying a planarization process to the lower surface of the wafer.

Preferably, using a metallization process, a metal layer is applied over a lower surface of the wafer directly opposite the metallized areas formed over the upper surface of the wafer, so as to create corresponding unmetallized regions of the wafer on the lower surface of the wafer.

Preferably, a trench is etched into said unmetallized regions of the lower surface of the wafer.

In the present invention, the boundary of the or each chip on a wafer is defined by the absence of metallization and the presence of a continuous etched trench. The metallization, comprising the deposition of a metal layer, is not formed monolithically on the wafer, but is patterned to cover only the surface of the or each chip, thereby providing for electrical contact to the chip. The metal layer so deposited, contributes to the structural integrity and mechanical strength of the chip, but does not form a mechanical link between neighbouring chips.

The trenches are etched to a depth that is substantially below the surface topology of the wafer. In particular, the trenches are etched to a depth that is substantially below layers in the wafer that contribute to the operation of devices fabricated on the wafer. Typically this would mean at least 3μm into the wafer substrate below the active regions grown on the substrate.

Preferably, the trenches are of sufficient width to allow a crack to propagate without damaging or stressing nearby structures, for example in the range 12 - 20 μm.

A number of etching processes are available for defining the device facets. Anisotropic dry etching can achieve a good vertical etch to define smooth side walls to an etched trench.

The chips on the wafer may comprise many devices whose facets have been defined during previous processing steps. However, it is also possible that a portion of a sidewall of a trench, fabricated in accordance with the present invention, may constitute a facet of at least one device located on at least one chip, which is bounded in part by the trench.

Thus, the facets of many devices, including optical devices, may simultaneously be defined by the etching of trenches that mark the boundaries of one or more chip. In this case it may be preferable to use anisotropic etching to define smooth flat vertical facets. However, other processes can be employed at this stage to define trenches with more complex cross sections, particularly when part of the trench sidewall constitutes the facet of a device. Features such as angled device facets, for example, may be realised in this way.

As a range of different integrated optical, electrical and mechanical devices may be fabricated on the wafer, it is preferred that the wafer comprises III-V semiconductor materials.

Once the definition of all structures on the wafer is complete, the wafer is diced up into individual chips. This may be done by scribing a series of grooves across the wafer, to mark out preferred paths for cleaving, and then breaking the wafer by the controlled propagation of cracks along the scribed grooves. However, dicing can also be achieved by initiating and propagating a crack along the bottom of an etched trench.

Preferably, at least one break is achieved by initiating and propagating a crack along the bottom of an etched trench.

Preferably, the crack is propagated substantially along the centre of the trench.

Thus, a wafer can be diced into individual chips by cleaving along the etched trench directions, with a much reduced risk of a break deviating from the desired path and also aided by the more robust, crack resistant chips. The present invention will therefore contribute to increased yield for a range of devices and at lower cost in a manufacturing environment.

Brief Description of the Drawings

Examples of the present invention will now be described in detail with reference to the accompanying drawings, in which:

Figure 1 is a schematic showing a top view of a wafer, comprising several optoelectronic devices, fabricated in accordance with the present invention;

Figure 2 is a schematic showing a bottom view of the wafer of Figure 1;

Figure 3 is a schematic of a process flow for achieving the cross-sectional (AA') structure between the wafer layers shown in Figures 1 and 2; and,

Figures 4A and 4B show the post-processing wafer structure with a top and bottom recess, and with only a top recess, respectively.

Detailed Description

Figure 1 shows a schematic plan view of the upper surface of a wafer 10 prepared in accordance with the present invention. In this example the wafer 10 comprises a number of optoelectronic chips 11, each with an active stripe region 12 running along the length. A particular example would be an optoelectronic chip comprising a laser diode. As shown, the surface of each chip is metallized with a layer of electrically conductive foil 13, thereby providing electrical contact to the device chip and also adding to the mechanical rigidity of the chip. The deposition process used ensures good adhesion of the metal foil to the material compound from which the chip is formed.

If the metal layer were fabricated monolithically such that the entire surface of the wafer were covered, the coated regions between individual chips would form a mechanical link between neighbouring chips and offer resistance during cleaving of the wafer. Such an arrangement would be detrimental to the accurate dicing of the wafer and might result in unnecessary stress being applied to chips located on the wafer during the cleaving procedure.

Therefore, the present invention proposes the use of patterned metallization such that only the surfaces of individual chips 11 are covered with a metal layer 13. Furthermore the proposed method prescribes the etching of deep recesses or trenches 14 at the boundaries of the chips 11, where the metal foil is absent. The prime aim of using deep etched recesses 14 is to remove, from the wafer, bulk III-V material located well below the surface topology. The deep recess thus produced, provides a clean definition of the chip boundary and also provides a minimum stress route for propagating a cleave along an upper part of the wafer following a planar path. The deep recess may also define the facets of devices located on chips separated by the recess, thereby allowing coating of device facets at the wafer level, as described in our co-pending British patent application number 0127690.6 (Agent's reference PJF01224GB).

In order to further improve chip definition and quality of cleave, the same metallization 15 and deep recess etching 16 is also performed on the corresponding regions of the lower surface of the wafer, as shown in Figure 2. The combined effect of the upper and lower surface metallization is to provide strength to the individual chips and to their peripheral boundaries. This helps ensure that, during cleaving, chips are neither fragmented nor suffer edge damage that would challenge their functional integrity.

A suitable process flow for preparing a complex topologically structured wafer for cleaving, in the manner illustrated in Figures 1 and 2, is shown in Figure 3. Firstly, a

patterned metal deposition procedure (step 100) is used to metallize the surface of individual chips on the wafer. The patterning ensures that there is a gap in the metallization at the appropriate places to determine the boundaries of a chip. Etch resistant masks are then deposited over the metallized regions to protect them during etching of the deep recesses or channels. An etch is then performed (step 110) on the upper surface of the wafer to produce a trench of the desired depth, namely well below the front surface topological structures and any points of localized stress that could be affected during the cleaving process. The etch mask is then removed.

Subsequently, the wafer is thinned down (step 120) to the desired chip thickness by applying a planarization process to the lower surface of the wafer. After wafer thinning, metal coating is performed on the lower surface of the wafer, and the metal foil deposited is protected with an etch resistant mask (step 130). The unprotected regions are then etched to generate a set of trenches in the lower surface of the wafer (step 140), after which the etch mask is removed. As the purpose of the etched trenches is to accurately define the chip boundaries, in addition to removing bulk material, it is important that the trenches on the upper and lower surface are accurately located opposite each other, spaced by the remaining bulk wafer material. This remaining material, between pairs of deep etched channels, will then provide a zone of minimum stress suitable for cleaving.

Although it is preferred that trenches be etched in both the upper and lower wafer surfaces, it is possible the neglect the latter steps and apply only a patterned metallization to the lower surface. This approach still provides a trench for cleave propagation, whilst the structural integrity of the individual chips is maintained by the upper and lower surface metallizations. This process flow requires less steps and may be adequate for some types of structure, however the quality and reliability of cleave propagation will typically be lower than when opposing sets of trenches are present. The post-processing cross-sections of a wafer using the two approaches are shown in Figures 4A and 4B.

The final step is the actual cleaving of the wafer to separate the individual device chips. This is done by initiating a cleave at a location on the edge of the wafer that will run along an etched trench. Preferably, the cleave is initiated at a point midway between the walls of the trench. Under the application of controlled stress, or by other means, the cleave will propagate along the etch trench of the wafer without interruption from chip structures and localized stress locations, and without imparting unnecessary stress to structures on the chip.

Thus the present invention provides a simple and versatile method of separating a plurality of device chips fabricated on a common wafer which, by virtue of their complex surface topology, would otherwise present a non-planar path with localized stress points to any cleave propagation. The present invention is expected to be of particular use in the dicing of III-V semiconductor wafers comprising OEIC and MEMS chips, which are characterized by varied device height leading to a complex and highly non-planar surface relief. Careful and accurate dicing of semiconductor wafers, with low risk of device damage, is of key importance for the high yield, low cost production of devices of this type.

CLAIMS

1. A method for processing a wafer having a plurality of chips integrated thereon, comprising the steps of:

applying a metal layer, by a metallization process, over an upper surface of the chips formed on an upper surface of the wafer, whilst leaving regions between adjacent chips unmetallized;

etching a trench into said unmetallized regions of the wafer to a depth substantially below layers of material that form devices on the wafer; and,

cleaving the wafer along lines defined by the trenches formed in the wafer.

2. A method according to claim 1, further comprising the step of thinning the wafer to the desired final thickness by applying a planarization process to a lower surface of the wafer.

3. A method according to claim 1 or 2, further comprising the step of applying, by means of a metallization process, a metal layer over a lower surface of the wafer directly opposite the metallized areas formed over the upper surface of the wafer, so as to create corresponding unmetallized regions of the wafer on the lower surface of the wafer.

4. A method according to claim 3, further comprising the step of etching a trench into the unmetallized regions of the lower surface of the wafer.

5. A method according to any preceding claim, in which a portion of a side wall of an etched trench defines a facet of a device on a chip.

6. A method according to claim 5, in which the device is an optical device.

7. A method according to claim 6, in which the facet is disposed at an angle of between 30 degrees and 90 degrees to the optical axis of the device.

8. A method according to any preceding claim, in which the step of etching comprises an anisotopic dry etch.

9. A method according to any preceding claim, in which the step of cleaving the wafer comprises the step of initiating and propagating a crack along the base of a trench.

10. A method according to claim 9, in which the step of step of cleaving the wafer further comprises the step of scribing a groove along the base of a trench to define a preferred path for cleaving prior to propagating the crack.

11. A method according to any preceding claim, in which a metallized area provides for electrical contact to a chip.

12. A method according to any preceding claim, in which the etched trenches have a width in the range 10 to 20 microns.

13. A method according to any preceding claim, in which the wafer comprises a III-V semiconductor material.

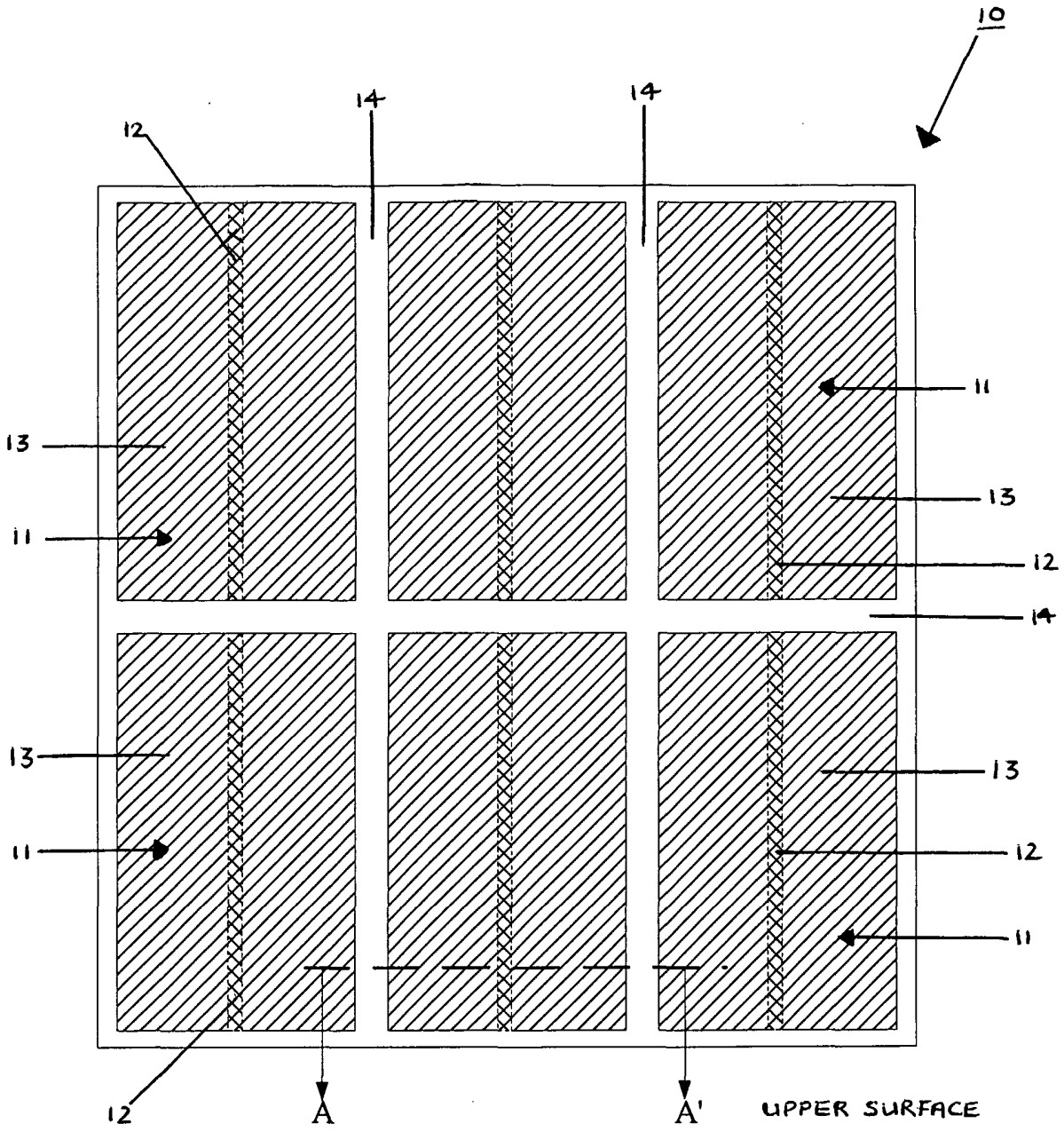

Figure 1

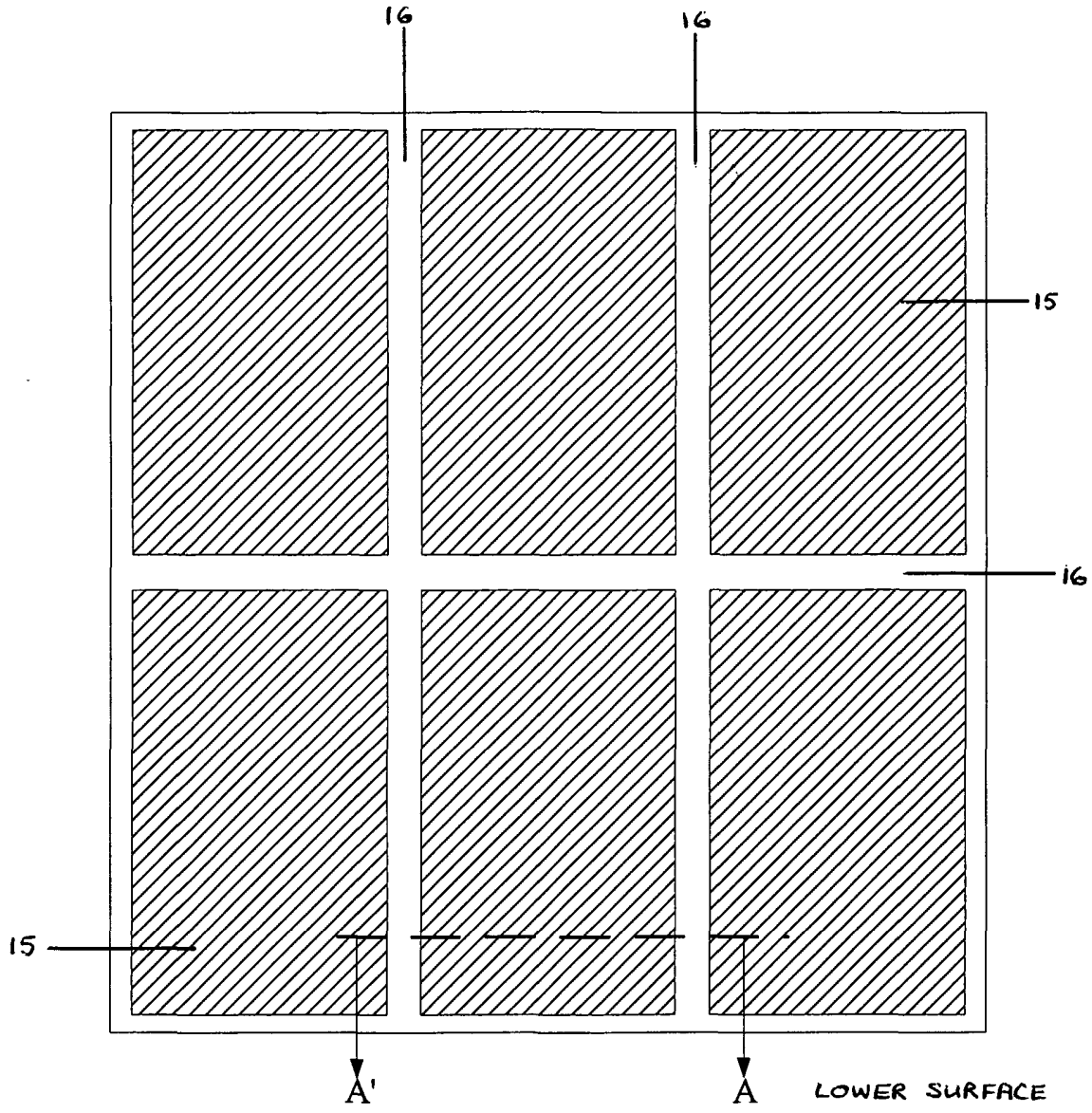

Figure 2

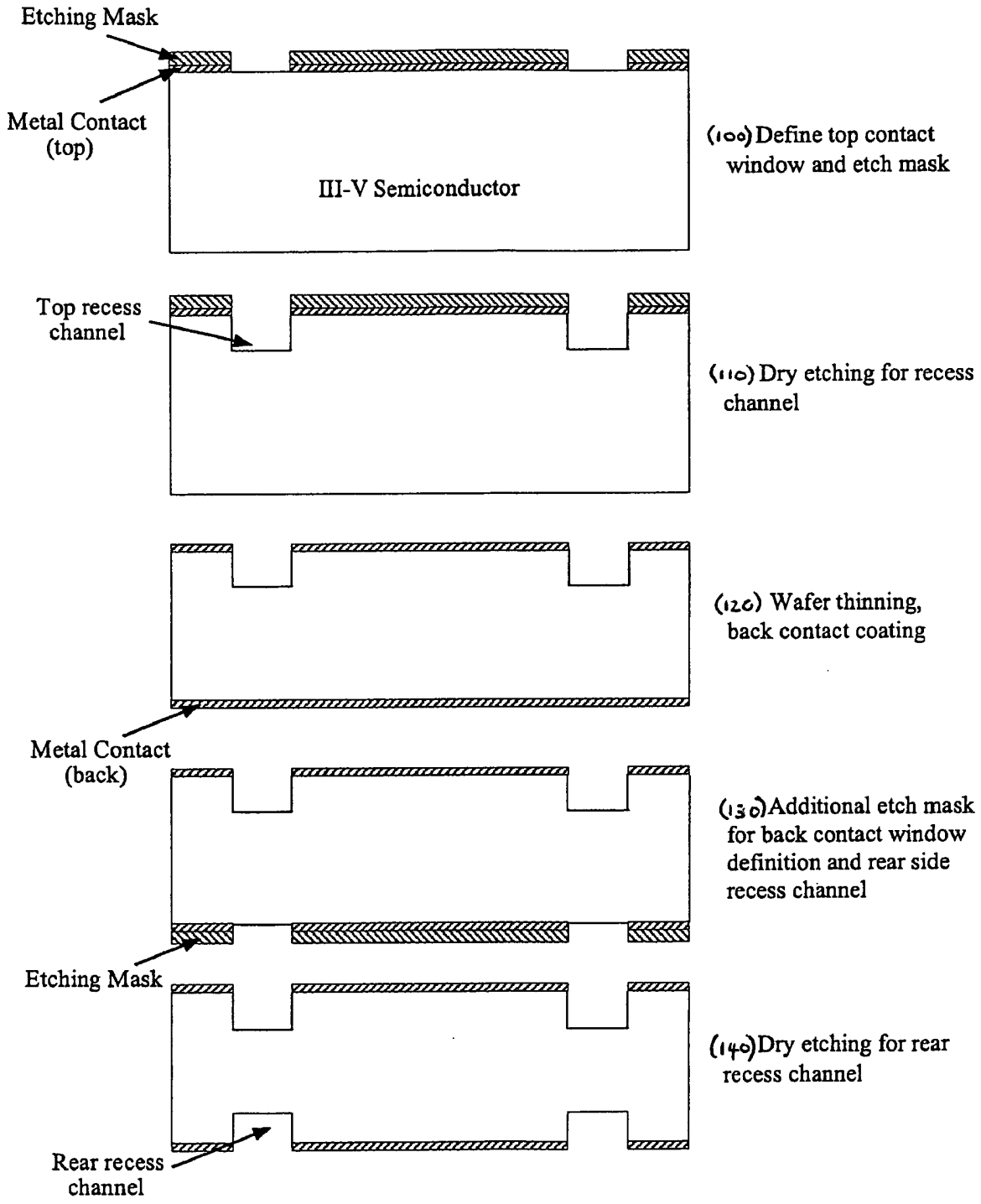
Etching Mask
Metal Contact (top)
III-V Semiconductor
(100) Define top contact window and etch mask
Top recess channel
(110) Dry etching for recess channel
(120) Wafer thinning, back contact coating
Metal Contact (back)
(130) Additional etch mask for back contact window definition and rear side recess channel
Etching Mask
(140) Dry etching for rear recess channel
Rear recess channel

Figure 3

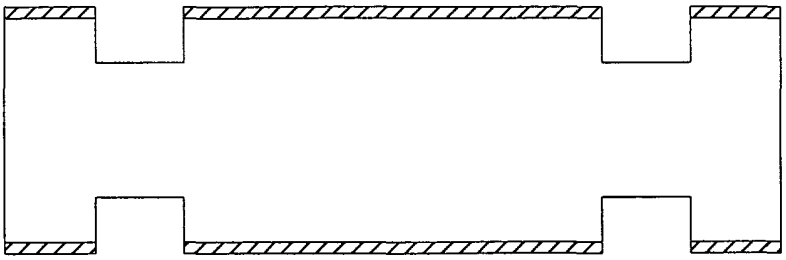

Figure 4A

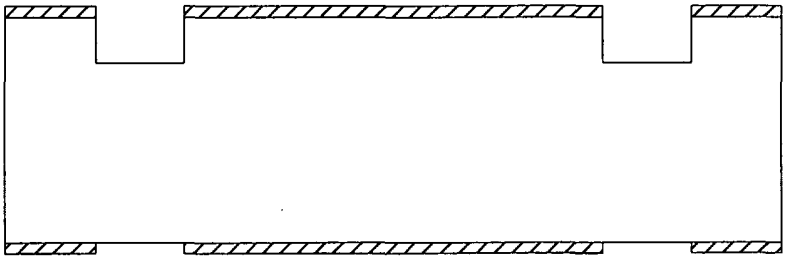

Figure 4B