(54) Title: PMOS PIXEL STRUCTURE WITH LOW CROSS TALK

(57) Abstract: An image sensor with an image area having a plurality of pixels each having a photodetector of a first conductivity type, the image sensor includes a substrate of the first conductivity type; a first layer of the second conductivity type between the substrate and the photodetectors, spanning the image area and biased at predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk; one or more adjacent active electronic components disposed in the first layer within each pixel; and electronic circuitry disposed in the substrate outside of the image area.

PMOS PIXEL STRUCTURE WITH LOW CROSS TALK

FIELD OF THE INVENTION

The invention relates generally to the field of image sensors, and in

5   particular to active pixel image sensors having an n-type pinning layer and a p-

type collection region in an n-type well for reducing cross talk.

BACKGROUND OF THE INVENTION

Current day active pixel image sensors are typically built on either

10   p- or n-type silicon substrates. Active pixel sensors refer to sensors having an

active circuit element such as an amplifier in, or associated with, each pixel.

CMOS refers to "complimentary metal oxide silicon" transistors in which two

transistors composed of opposite dopants (one of p-type and one of n-type) are

wired together in a complimentary fashion. Active pixel sensors also typically use

15   CMOS transistors, and as such, are used interchangeably.

The CMOS sensors built on p-type substrates typically contain a

higher level of circuit integration on chip due to the fact that the process is derived

from standard CMOS, which is already fully developed and contains all the

necessary devices and circuit libraries to support this high level of integration.

20   Unfortunately, these sensors suffer from high levels of pixel-to-pixel cross talk

that results from the lateral diffusion of minority carriers within the p-type

substrates on which they are built. On the other hand, CMOS image sensors built

using processes derived from typical interline CCD image sensors, (wherein the

focal plane is built in a p-well on an n-type substrate), have much lower cross talk

25   due to the elimination of lateral carrier diffusion as a result of the vertical-

overflow drain (VOD) structure. For these devices, color cross talk is primarily

optical as limited by the transmission of the overlying CFAs.

Although there have been several recent proposals to reduce the

electrical cross talk within the silicon substrates for CMOS sensors built on p-type

30   substrates, (U.S. Provisional Application Nos. 60/721,168 and 60/721,175, both

filed on September 28, 2005), the cross talk can not be reduced low enough using

these techniques for certain applications. And although a CMOS process could be developed on n-type substrates, it would require the complete re-engineering of all of the support circuitry and devices. It would also require that the AC ground plane, in this case the substrate, be biased at the VDD supply voltage, which is not

5   desirable from a noise point of view. N-type substrates are also more difficult to getter than p-type substrates, which can result in a higher level of dark current defects.

Therefore, there exists a need within the art to provide a CMOS image sensor with reduced cross talk while maintaining all of the current

10   advantages and level of development of existing mainstream CMOS processes.

SUMMARY OF THE INVENTION

The present invention is directed to overcoming one or more of the problems set forth above. Briefly summarized, according to one aspect of the

15   present invention, the present invention resides in an image sensor with an image area having a plurality of pixels each having a photodetector of a first conductivity type, the image sensor comprising a substrate of the first conductivity type; a first layer of the second conductivity type between the substrate and the photodetectors, spanning the image area and biased at predetermined potential with respect to the

20   substrate for driving excess carriers into the substrate to reduce cross talk; one or more adjacent active electronic components disposed in the first layer within each pixel; and electronic circuitry disposed in the substrate outside of the image area.

These and other aspects, objects, features and advantages of the present invention will be more clearly understood and appreciated from a review

25   of the following detailed description of the preferred embodiments and appended claims, and by reference to the accompanying drawings.

Advantageous Effect Of The Invention

The present invention has the advantage of reducing cross talk and

30   the bulk-diffusion component of dark current while retaining all the advantages of using mainstream standard CMOS integrated on a p-type substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the top view of an image-area pixel used in a typical prior art CMOS image sensor;

Fig. 2a shows a schematic view of a two-dimensional doping structure taken through a cross section through the transfer gate and floating diffusion of a typical prior art pinned photodiode detector;

Fig. 2b shows the 1-D doping profile vs. depth into the silicon through the middle of the prior art photodiode;

Fig. 2c shows the 1-D potential profile vs. depth into the silicon through the middle of the prior art photodiode;

Fig. 3 illustrates example results of a 2-D calculation of pixel-to-pixel cross talk vs. depletion depth of a prior art CMOS active pixel image sensor pixel;

Fig. 4a shows a schematic view of a two-dimensional doping structure for the PMOS pixel structure of the present invention taken through a cross section through the transfer gate, floating diffusion, and reset gate;

Fig. 4b shows a top view of an exemplary layout for the image sensor of Fig. 4a;

Fig. 4c shows the 1-D doping profile vs. depth into the silicon through the middle of the PMOS pixel structure of the present invention;

Fig. 4d shows the 1-D potential profile vs. depth into the silicon through the middle of the PMOS pixel structure of the present invention;

Fig. 5 shows the results of a 2-D calculation of pixel-to-pixel cross talk vs. overflow or sink depth for various photodiode depletion depths for the PMOS pixel structure of the present invention built in a well; and

Fig. 6 is an illustration of a digital camera for illustrating a typical commercial embodiment of the present invention to which the ordinary consumer is accustomed.

DETAILED DESCRIPTION OF THE INVENTION

Historically, charge-coupled device (CCD) -based image sensors have primarily used electrons as the signal-charge carrier to take advantage of their higher mobility to maintain good transfer efficiency at high data rates. To reduce

5 . color cross talk and smear, and to provide blooming protection, CCD imagers are also typically built in a well, or vertical-overflow drain (VOD) structure (see for example US Patent 4,527,182). Therefore, building a VOD structure along with the requirement for an n-channel requires that a p-well be formed in an n-type substrate.

10   CMOS-based image sensors have since become more readily available. Current day CMOS image sensors are typically built on either p- or n-type silicon substrates. Those built on p-type substrates using mainstream CMOS processing can contain high levels of circuit integration, but suffer from high levels of color cross talk. Those built using a typical CCD-like process on n-type

15   substrates (S. Inoue et al., "A 3.25 M-pixel APS-C size CMOS Image Sensor," in Eizojoho Media Gakkai Gijutsu Hokoku (Technology Report, The Institute of Image Information and Television Engineers) Eijogakugiho, vol. 25, no. 28, pp. 37-41, March 2001. ISSN 1342-6893.) have low color cross talk, but have other shortcomings as previously described above.

20   Unlike CCD image sensors, CMOS image sensors have only one transfer, i.e., from the photodiode to the floating diffusion. Hence, a CMOS image sensor does not require as high a charge carrier mobility. As such, the lower mobility of holes would not be a deficiency for a CMOS image sensor. It is therefore one object of the present invention to disclose a CMOS image sensor

25   employing a PMOS (p-channel) pixel structure using holes as the signal-charge carrier. This PMOS structure of the present invention allows the pixel to be built in an n-well on p-type epi to reduce pixel-to-pixel cross talk. However, unlike a typical CCD-based image sensor, this well is only used underneath (or spanning) the imaging section of the sensor. All of the digital and analog CMOS support

30   circuitry integrated on the chip is formed in the p-type epi (see Fig. 4b, i.e., analog or digital circuits 80, digital logic 90, row decoder 100, and column decoder 110).

This means that all of the physical aspects of the devices in the standard CMOS circuitry portion of the chip are retained. Additionally, unlike the CCD image sensors built in a well wherein this well is biased at ground and the substrate at some positive potential, by biasing the n-well of the present invention structure at

5   VDD, the ground plane (i.e., the p-type epitaxial substrate) for the CMOS circuitry can be maintained at 0 V. This means that all of the electrical aspects of the standard CMOS circuitry portions of the chip are also retained. Only the direction of some logic pulses and the signal swing(s) in the digital and analog sections need to be inverted where appropriate, which is readily accomplished by those

10   skilled in the art. Therefore, all of the advantages of p-type substrates mentioned above in the Background section are retained. The well-type structure also reduces dark current by eliminating the diffusion component from the substrate.

The top view of a typical prior art CMOS image sensor pixel is shown in Fig. 1. The typical pixel consists of a photodiode (PD); a transfer gate

15   (TG) for reading charge out of the photodiode; a floating diffusion (FD) for converting the signal charge into a voltage signal; a source-follower transistor (SF) which acts as a signal buffer whose gate is electrically connected to FD; a row-select transistor (RS) that selectively connects the outputs of the source-follower transistors to the column output circuits (not shown in Fig. 1); and a reset gate

20   (RG) for resetting the potential of the floating diffusion. A power supply voltage (VDD) is used to power the source follower and drain off signal charge from the floating diffusion during its reset operation.

A typical prior art CMOS image sensor pixel contains a pinned photodiode with a p+ type pinning layer and an n-type storage region built on p-

25   /p++ epitaxial silicon wafers as illustrated by way of example in Figs. 2a-2c. The depletion region depth (shown in Figs. 2a and 2c) defines the collecting boundary of the photodiode. An example doping profile down through the center of the prior art photodiode is shown in Fig. 2b. Charge carriers (electrons) generated from shorter wavelength light that are created within the collecting region (i.e.,

30   depletion region boundary) are captured and stored as signal charge. Charge carriers generated from longer wavelengths that are created past this depletion

depth are free to diffuse in any direction via thermal diffusion. Any charge that diffuses laterally and gets collected by adjacent pixels is called electrical cross talk.

5   Cross talk can be quantified by defining it as the ratio of the signal in the non-illuminated to the illuminated pixel(s), and can be expressed as either a fraction or percentage. Therefore, cross talk represents the relative amount of signal that does not get collected by the pixel(s) under which it was generated. The dependence of cross-talk on depletion depth for the example prior-art pixel is illustrated in Fig. 3. The cross-talk calculation assumes that every other pixel

10   along a line is illuminated (and the alternating, interleaved pixels are not). A wavelength of 650 nm is assumed, because cross talk is more of a problem at longer wavelengths because the optical absorption coefficient is lower at longer wavelengths, (i.e., the photons are absorbed deeper). It can be seen from this figure that although increasing the depletion depth can reduce cross talk, it does

15   not go to zero even for depletion depths up to 3um, which is approximately one over the absorption coefficient for silicon at 650 nm.

A cross section of the PMOS pixel architecture of the present invention is shown in Fig. 4a. The top view of an example CMOS image sensor containing this pixel structure is shown in Fig. 4b. An example doping profile

20   down through the center of the photodiode is shown in Fig. 4c. An example potential profile down through the center of the empty photodiode is shown in Fig. 4d. As can be seen by Figs. 4a and 4c, the pinned photodiode 10 of the present invention embodies an n+ pinning layer 20 and p-type buried storage region 30 built within an n-type well 40 on a p-/p++ epitaxial substrate 50. Because the

25   photodiode's surface pinning layer 20 of the present invention is n-type, arsenic can be used. This makes it easier to create a shallow pinning layer due to the shorter implant range of arsenic compared to that of boron. (The prior art structure has a p-type pinning layer for which boron is typically used). Also, because the photodiode's storage region 30 is now p-type instead of n-type, boron

30   can be used, (which has a longer implant range than phosphorous or arsenic as required for the storage region of the prior art structure), thereby making it easier

to make this implant deep. The n+ pinning layer 20 is electrically connected to the n-well 40 via the n+ type isolation implant 60 around the typical shallow trench isolation (STI) region as can be seen in Fig. 4a. This pinning layer 20 maintains the surface of the diode in accumulation (of electrons). Signal charge is stored in

5   the form of holes in the p-type buried storage region 30 of the pinned photodiode 10. The n-type well 40 is only formed in the image area 70 having a plurality of pixel as illustrated by the top view shown in Fig. 4b. By forming this well 40 only in the image area 70, the image sensor 75 uses standard mainstream CMOS devices and circuitry in the analog or digital circuits 80, digital logic 90, row

10   decoder 100, and column decoder 110 while retaining all the benefits of a p-type substrate. It is preferable to form this n-well 40 at the beginning of the process so that its formation does not affect other device structures. For example, if it is formed via an implant and thermal drive, by doing this prior to the standard CMOS processing, the thermal drive step will not cause diffusion of shallow

15   junction regions as required by the devices used in the CMOS support circuitry surrounding the image area. When formed in this n-well 40, the pixel's transfer gate (TG), reset gate (RG), and source follower (SF) transistors are all preferably p-type metal oxide silicon (note that the gate is not usually metal; it is polysilicon, and sometimes the dielectric is not solely oxide), field effect transistors (PMOS

20   FETs). A row select transistor (RS not shown) in series with the output of the source follower amplifier (SF) would also be a PMOS device. All of the peripheral supporting CMOS circuitry 80, 90, 100 and 110 is formed within the p-/p++ epitaxial substrate. The substrate is at ground and the n-well 40 is biased at a convenient positive bias, such as VDD. After (or during) image integration, the

25   floating diffusion (FD) is reset with a negative going pulse on the reset gate (RG) prior to signal transfer from the photodiode. A convenient FD reset voltage level is ground. After the floating diffusion is reset, (i.e., after the RG pulse), transfer of charge (holes) from the photodiode to floating diffusion is initiated by a negative going pulse on the transfer gate, TG. An example of convenient clock voltages

30   (VDD) used for these pulses are shown in Fig. 4a. Other voltages may be possible without departing from the scope of the invention. Since the signal charge is holes

for the present invention structure, the signal swing on the floating diffusion and source follower (SF) output will be positive going. Any photosignal (holes) that is generated within the n-well 40 beneath the photodiodes collecting region 30 is swept into the substrate 50 before it can diffuse to neighboring pinned photodiodes

5   10, thereby eliminating electrical cross talk. The signal would be read out from the chip in the usual manner as would be well known by those working in the art. The potential barrier between the substrate and photodiode that results from this structure also eliminates the diffusion component of dark current from the substrate (bulk) into the photodiode.

10   Electrical cross talk for the pixel structure of the present invention with a pinned photodiode built in an n-well on a p-type substrate is greatly reduced as shown in Fig. 5. Cross talk is shown versus sink depth (the depth past which carriers are drained to the substrate) for various depletion depths. The calculations are carried out by the methods described by E.G. Stevens and J.P. Lavine in *IEEE*

15   *Trans. on Electron Devices*, vol. 41, no. 10, p. 1753, Oct. 1994. For this sample calculation, a constant n-well doping concentration vs. depth was assumed. For an actual device wherein the n-well would preferably be formed via ion implantation, the resulting doping gradient (such as shown in Fig. 4c) would create a potential gradient (as shown in Fig. 4d) such that minority carriers (holes) in the n-well

20   would be driven into the substrate thereby resulting in the virtual elimination of electrical cross talk and the substrate dark current component.

          Referring to Fig. 6, there is shown a digital camera 120 having an image sensor 75 of the present invention disposed therein for illustrating a typical commercial embodiment to which the ordinary consumer is accustomed.

25   Although the preferred embodiment of the present invention shown incorporates a pinned photodiode consisting of an n+ pinning (top surface) layer and a p-type buried collecting region within an n-well on a p-type epi substrate, it will be understood the those skilled in the art that other structures can be used without departing from the scope of the invention. For example, a simple

30   unpinned p-type diode formed in an n-type well could be used, if desired. Also, although a simple non-shared pixel architecture is shown, a shared architecture,

(such as US Patent 6,107,655 for example), could also be used without departing from the scope of the invention.

PARTS LIST:

	10	pinned photodiode
	20	n+ pinning layer
5	30	p-type buried storage region
	40	n-type well
	50	p-/p++ epitaxial substrate
	60	n+ type isolation implant
	70	image area
10	75	image sensor
	80	analog or digital circuits
	90	digital logic
	100	row decoder
	110	column decoder
15	120	digital camera

CLAIMS:

1. An image sensor with an image area having a plurality of pixels each having a photodetector of a p conductivity type which use holes as charge carriers, the image sensor comprising:

(a) a substrate of the p conductivity type;

(b) a first layer of n conductivity type between the substrate and the p-type photodetectors, spanning the image area and biased at predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk;

(c) one or more adjacent active electronic components disposed in the first layer within each pixel; and

(d) CMOS electronic support circuitry disposed in the substrate outside of the image area and electrically connected to the image area.

2. The image sensor as in claim 1, wherein the one or more active electronic components include a reset transistor and floating diffusion.

3. The image sensor as in claim 1, wherein the one or more active electronic components include an amplifier.

4. The image sensor as in claim 1 further comprising a p-epitaxial layer disposed between the substrate and the first layer; wherein the substrate is p+ type and the first layer is n-type.
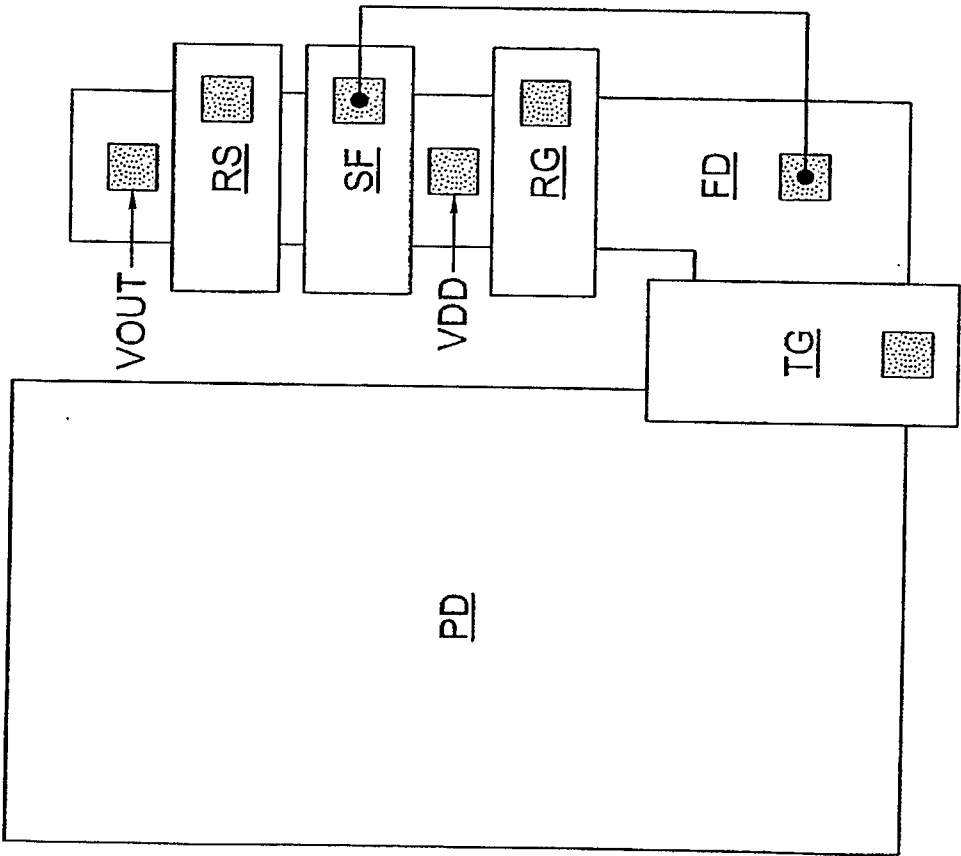
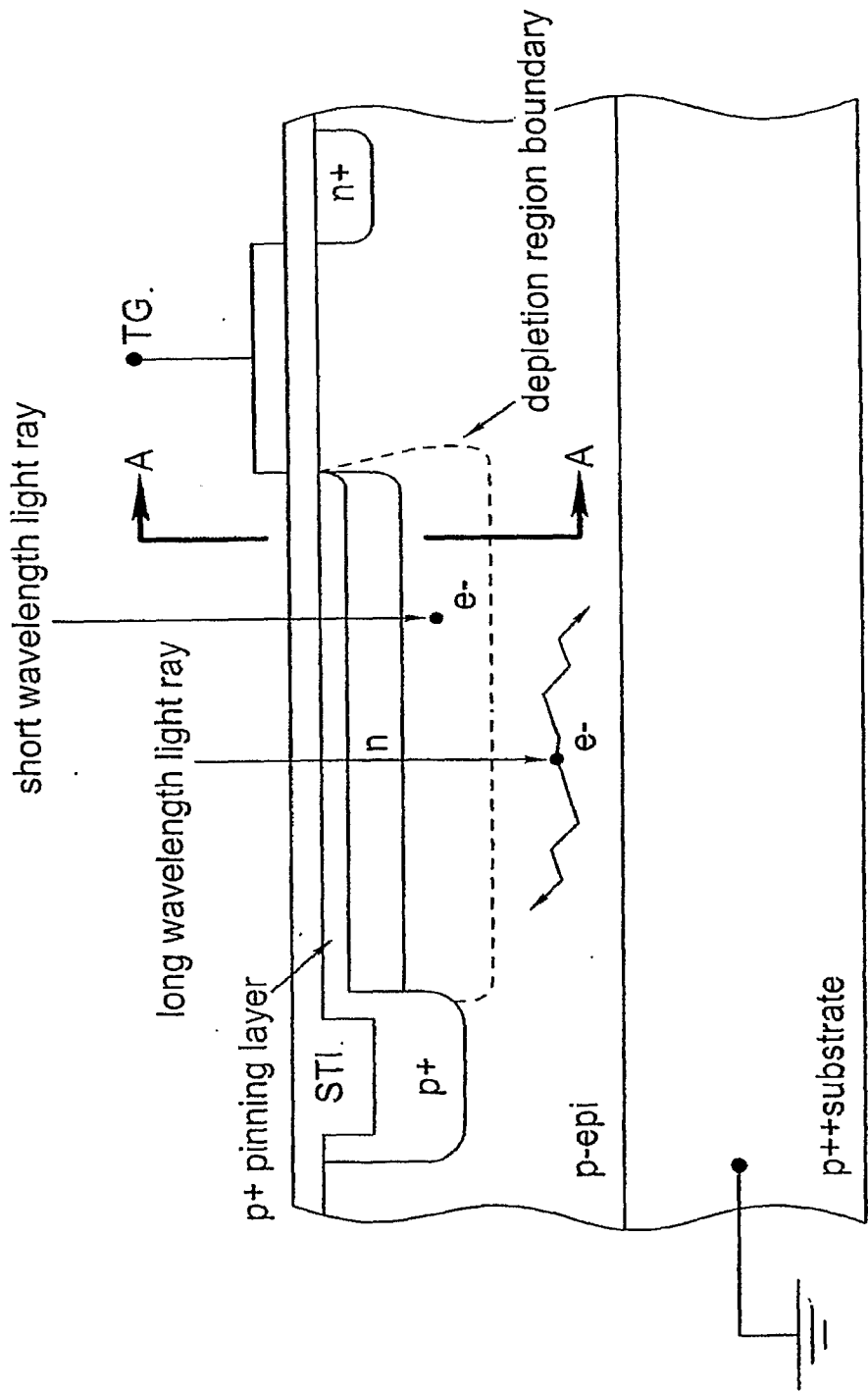5. The image sensor as in claim 1, wherein the photodetector is a pinned photodiode.

6. The image sensor as in claim 1, wherein the one or more active electronic components include a floating diffusion amplifier.

7. The image sensor as in claim 1, wherein the first layer includes doping that is graded so as to drive excess carriers into the substrate.
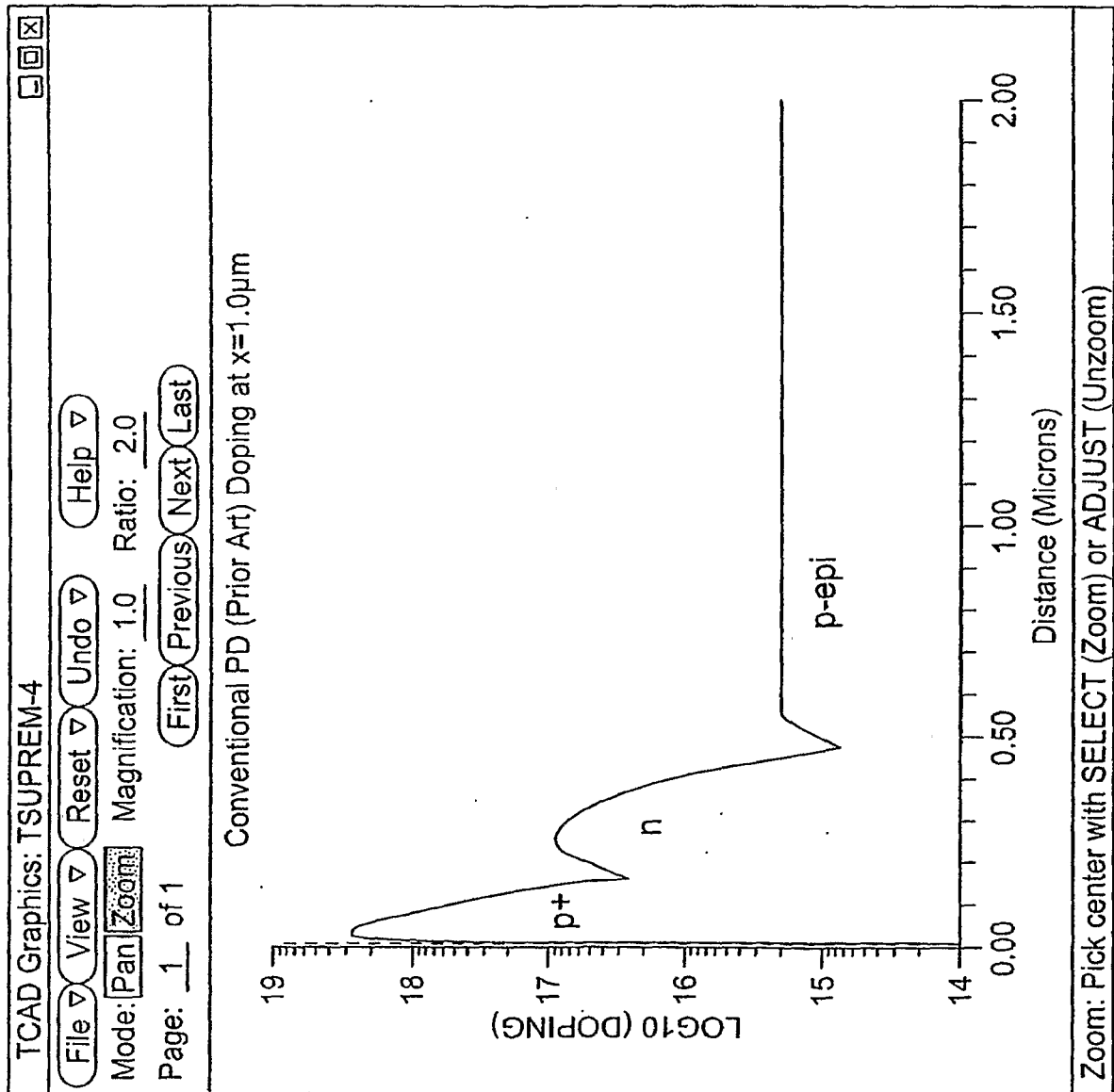
8. A camera comprising:

an image sensor with an image area having a plurality of pixels each having a photodetector of a p conductivity type which use holes as charge carriers , the image sensor comprising:

(a) a substrate of the p conductivity type;

(b) a first layer of n conductivity type between the substrate and the p-type photodetectors, spanning the image area and biased at predetermined potential with respect to the substrate for driving excess carriers into the substrate to reduce cross talk;

(c) one or more adjacent active electronic components disposed in the first layer within each pixel; and

(d) CMOS electronic support circuitry disposed in the substrate outside of the image area and electrically connected to the image area.

9. The camera as in claim 8, wherein the one or more active electronic components include a reset transistor and floating diffusion.

10. The camera as in claim 8, wherein the one or more active electronic components include an amplifier.

11. The camera as in claim 8 further comprising an epitaxial layer disposed between the substrate and the first layer; wherein the substrate is p+ type and the first layer is n-type.

12. The camera as in claim 8, wherein the photodetector is a pinned photodiode.

13. The camera as in claim 8, wherein the first conductivity type is p-type and the second conductivity type is n-type.

14. The camera as in claim 8, wherein the one or more active
5   electronic components include a floating diffusion amplifier.

15. The camera as in claim 8, wherein the first layer includes doping that is graded so as to drive excess carriers into the substrate.

FIG. 1
PRIOR ART

FIG. 2a
PRIOR ART

FIG. 2b
PRIOR ART

FIG. 2c
PRIOR ART

FIG. 3
PRIOR ART

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FIG. 4a

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ANALOG OR DIGITAL OUTPUT CIRCUITS

COLUMN DECODER

IMAGE AREA
AND n-well

ROW DECODER

DIGITAL LOGIC

FIG. 4b

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FIG. 4c

FIG. 4d

NEW PIXEL STRUCTURE: CROSSTALK VS SINK DEPTH

2.7μm pixel, Nn-well=2E15, λ=650nm

yd=1.2μm
yd=2.0μm
yd=3.0μm

SINK DEPTH (μm)

2-D CROSS TALK

FIG. 5

FIG. 6

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/146

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 332 049 A (HEWLETT PACKARD CO [US] HEWLETT PACKARD CO [US]; AGILENT TECHNOLOGIES) 9 June 1999 (1999-06-09) page 5; figures 12,13	1,3,8, 10,13
X	TAKAHASHI H ET AL: "A 3.9-MUM PIXEL PITCH VGA FORMAT 10-B DIGITAL OUTPUT CMOS IMAGE SENSOR WITH 1.5 TRANSISTOR/PIXEL" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 39, no. 12, December 2004 (2004-12), pages 2417-2425, XP001224181 ISSN: 0018-9200 figures 9,10	1-3,5,6, 9-14
X	US 5 608 204 A (HOEFFLINGER BERND [DE] ET AL) 4 March 1997 (1997-03-04) figures 1,2	1,3,8, 10,13

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| X | Further documents are listed in the continuation of Box C. | | X | See patent family annex. |

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 July 2007	02/08/2007

| Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340-2040, Tx. 31 651 epo nl, Fax: (+31–70) 340-3016 | Authorized officer Cabrita, Ana |

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6 023 293 A (WATANABE TAKASHI [JP] ET AL) 8 February 2000 (2000-02-08) figure 1	1-15
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			EP	1208598 A1	29-05-2002
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