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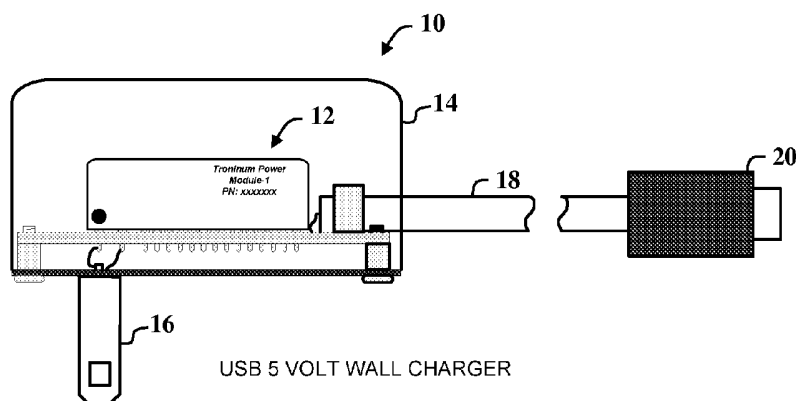


Figure 1

(57) Abstract: An electrical circuit for providing electrical power for use in powering electronic devices is described herein. The electrical circuit includes a primary power circuit and a secondary power circuit. The primary power circuit receives an alternating current (AC) input power signal from an electrical power source and generates an intermediate direct current (DC) power signal. The intermediate DC power signal is generated at a first voltage level that is less than a voltage level of the AC input power signal. The secondary power circuit receives the intermediate DC power signal from the primary power circuit and delivers an output DC power signal to an electronic device. The output DC power signal is delivered at an output voltage level that is less than the first voltage level of the intermediate DC power signal.



ELECTRICAL CIRCUIT FOR POWERING CONSUMER ELECTRONIC DEVICES

CROSS-REFERENCES TO RELATED APPLICATIONS

[001] This application claims priority to U.S. Provisional Patent Application Serial No. 62/069,672, filed on October 28, 2014, claims priority to U.S. Provisional Patent Application Serial No. 61/949,171, filed on March 6, 2014, and claims priority to U.S. Provisional Patent Application Serial No. 61/896,557, filed on October 28, 2013, all of which are hereby incorporated by reference in their entirety for all purposes.

FIELD OF THE INVENTION

[002] The present invention relates generally to electrical power circuits and, more particularly, to an electrical power circuit for providing electrical power for use in charging and/or powering consumer electronic devices.

BACKGROUND OF THE INVENTION

[003] The Energy Crises Requires Demand Side Response That Lowers Current Loads. The Energy Crisis is upon us worldwide. For instance, the U. S. Department of Energy predicts that by 2015 there will not, on the average, be enough electric power to supply average demand in the U.S.

[004] One of the controllable offenders is “Vampire Loads”. Also called “Wall Wart Power” or “Standby Power”, this electricity waste is estimated by the U.S. Department of Energy (DOE) to be in excess of 100 Billion kW annually, costing over Ten Billion Dollars in wasted energy. Vampire Load producers includes cell phone chargers, lap top chargers,

notebook chargers, calculator chargers, small appliances, and other battery powered consumer devices.

[005] The U.S. Department of Energy said in 2008:

[006] "Many appliances continue to draw a small amount of power when they are switched off. These "phantom" loads occur in most appliances that use electricity, such as VCRs, televisions, stereos, computers, and kitchen appliances. This can be avoided by unplugging the appliance or using a power strip and using the switch on the power strip to cut all power to the appliance."

[007] According to the U.S. Department of Energy, the following types of devices consume standby power:

1. Transformers for voltage conversion. (Including cell phone, lap top and notepad, calculators and other battery powered devices that use wall chargers).
2. Wall wart power supplies powering devices which are switched off. (Including cell phone, lap top and notepad, calculator, battery powered drills and tools, all of which have wall chargers and have either completely charged the batteries or are actually disconnected from the device).
3. Many devices with "instant-on" functions which respond immediately to user action without warm-up delay.
4. Electronic and electrical devices in standby mode which can be awakened by a remote control, e.g. some air conditioners, audio-visual equipment such as a television receiver.
5. Electronic and electrical device which can carry out some functions even when switched off, e.g. with an electrically powered timer. Most modern computers consume standby power, allowing them to be awakened remotely (by Wake on LAN,

etc.) or at a specified time. These functions are always enabled even if not needed; power can be saved by disconnecting from mains (sometimes by a switch on the back), but only if functionality is not needed.

6. Uninterruptible power supplies (UPS)

[008] All this means that even when a cell phone, lap top or like device is completely charged, current is still flowing, but not accomplishing anything and wasting electricity. More recently manufactured devices and appliances continue to draw current all day, every day—and cost you money and add to the Energy Crisis Worldwide.

[009] The National Institute of Standards and Technology (NIST) (a division of the U.S. Department of Commerce) through its Buildings Technology Research and Development Subcommittee in 2010 stated its goals for reducing “plug loads,” stating:

[0010] “The impact of plug loads on overall consumption is quite significant. For commercial buildings, plug loads are estimated at 35% of total energy use, for residential 25%, and for schools 10%.

[0011] Opportunities for lowering plug loads include:

- 1) more efficient plugged devices and appliances,
- 2) automated switching devices that turn off unused appliances and reduce “vampire” loads from transformers and other small but always on appliances, or
- 3) modifying occupant behaviors.”

[0012] One of the problems experienced by virtually all modern electronics is that power supplies, whether external or embedded “power modules”, are not energy efficient. This is true for a number of reasons, one of which dates back to 1831 when Michael Faraday invented the transformer. Transformers are inherently inefficient because, as an analog device, they can only produce one power output for each specific winding. So if two power

outputs are necessary, two secondary windings are necessary. Moreover, there are often over 50 parts and pieces that are necessary to work with a transformer to create a common modern external power supply, the numbers only get somewhat lower with internal or embedded power modules. The number of parts in a power supply is inherently inefficient because current must travel in, around and through the various parts, each with different power dissipation factors; and even the circuit traces cause resistive losses creating energy waste.

[0013] Further, the way a transformer works is creating and collapsing a magnetic field. Since all of the electrons cannot be “recaptured” by the magnetic field creation/collapse, those that escape often do so as heat, which is why cell phone, lap top and tablet chargers feel warm or hot to the touch. It is also the primary reason why all consumer electronics create heat, which not only wastes energy/electricity, but causes eventual detrition through heating of other associated electronic parts.

[0014] Another inefficiency found in current electronics is the need for multiple internal power supplies to run the different parts. For instance, in the modern world power modules, MOSFETS have become a more and more important part of the “real world” interfaces in circuitry.

[0015] Metal–oxide–semiconductor field-effect transistors (MOSFETs) enable switching, motor/solenoid driving, transformer interfacing, and a host of other functions. At the other end of the spectrum is the microprocessor. Microprocessors are characterized by steady reduced operating voltages and currents, which may be 5 volts, 3.3 volts, 2.7 volts or even 1.5 volts. In most systems the MOSFETS and microprocessors are used together or in combination to make the circuitry work. However, most often the microprocessor and the drivers for the MOSFETS operate at different voltages, causing the need for multiple power supplies within a circuit.

[0016] A standard high-voltage NMOS MOSFET requires a driver that can deliver a gate voltage of 5-20 volts to successfully turn it on and off. In the case of turn on, there is actually a requirement that the gate driver voltage exceed the rail power to be effective. Specialty drivers using charge pump technology have been devised for this purpose. The other main function of the high-voltage MOSFET gate driver is to have a reduced input drive requirement making it compatible with the output drive capability of modern CMOS processor.

[0017] This MOSFET/driver arrangement, common in most external power supplies, like chargers, actually requires three separate power supplies. The first power supply needed is the main power rail, which is normally composed of the rectified Line voltage in the range of 127 VDC to 375 VDC supplied to the MOSFET. The second power supply needed is the 15 volts (or higher) required by the MOSFET drivers. Finally, the microprocessors require another isolated power supply for their many different and varying voltages.

[0018] A good example of the current inefficiencies and energy waste is found in a typical television, which requires as many as four to six different power supply modules to run the screen, backlighting, main circuit board, and sound and auxiliary boards. This current system requires multiple transformers and dozens of parts for each power supply needed. The transformers and the parts (including MOSFETS) multiply heat through their duplicated inefficiencies, which is one reason the back of a television is always hot to the touch. In addition, the more transformers that are needed for various power outputs, the more parts are needed, and more causation for energy waste is created.

[0019] In addition to the heat problem, the multiple transformer based power supplies all need typically from forty to sixty parts to operate, requiring dozens of parts for a typical transformerbased television power supply module which increases costs and total component

size while decreasing reliability. With the multiplicity of parts comes increased system resistance which ends up in wasted energy as heat.

[0020] The present invention is aimed at one or more of the problems identified above to provide better efficiencies and create more control over electrical inrush currents from rail sources.

SUMMARY OF THE INVENTION

[0021] In one aspect of the present invention, an electrical circuit for providing electrical power for use in charging applications and/or powering a constant supply circuit for electronic devices is provided. The electrical circuit includes a primary power circuit that is adapted to be electrically coupled to an electrical power source, and a secondary power circuit that is electrically coupled to the primary power circuit. The primary power circuit is configured to receive an alternating current (AC) input power signal from the electrical power source and generate an intermediate direct current (DC) power signal. In the AC input case, the intermediate DC power signal is generated at a first voltage level that is less than the voltage level of the AC input power signal. The secondary power circuit is configured to receive the intermediate DC power signal from the primary power circuit and deliver an output DC power signal to an electronic device. The output DC power signal is delivered at an output voltage level that is less than the first voltage level of the intermediate DC power signal.

[0022] In another aspect of the present invention, a power module for providing electrical power for use in powering electronic devices, like monitors, televisions, white goods, data centers, and telecom circuit boards, is provided. The power module includes a rectifier circuit, a switch capacitor voltage breakdown circuit and controller integrated circuit, and a forward converter circuit. The rectifier circuit receives an AC power input signal from an

electrical power source and generates a rectified DC power signal. The switch capacitor voltage breakdown circuit and controller integrated circuit receives the rectified DC power signal and generates an intermediate DC power signal based upon an integrated controller which senses the voltage level of the AC power input signal and adjusts the gain of the switch capacitor voltage breakdown circuit as a function of the sensed voltage level. The forward converter circuit includes a transformer that receives the intermediate DC power signal and generates an output DC power signal that is delivered to the electronic device.

[0023] In a further aspect of the present invention, a high-efficiency switch capacitor voltage breakdown circuit for AC-DC and DC-DC conversion is provided. The high-efficiency switch capacitor voltage breakdown circuit includes a pair of flyback capacitors electrically coupled in parallel, and a plurality of switch assemblies that are electrically coupled to each of the pair of flyback capacitors. In one embodiment, the gates between the capacitors are shared. The switch assemblies may be operated to selectively deliver an input DC power signal to each of the pair of flyback capacitors during a charge phase, and to selectively deliver an output DC power signal to an electronic device during a discharge phase that has a lower voltage level than the input DC power signal. At least one switch assembly may include an N-channel MOSFET switch and a level shifter for delivering a control signal to the N-channel MOSFET switch. In addition, a dickson charge pump may be coupled to the level shifter to receive the input DC power signal and generate an output power signal having a higher voltage level than the input DC signal. The output power signal is delivered to the level shifter for use in operating N-channel MOSFET switch (or closing for other types of MOSFETs). In addition, the switch capacitor voltage breakdown circuit may include a control circuit that includes a voltage sensing circuit for sensing a voltage level of the input DC power signal and a gain controller configured to select a gain setting of the switch

capacitor voltage breakdown circuit as a function of the sensed voltage level and operate each of the plurality of switch assemblies as a function of the selected gain setting.

[0024] The electrical circuit may also includes a vampire load elimination system that is configured to determine when a consumer device has finished charging and/or is disconnected from the power circuit, and operates the power circuit to disconnect the supply of power to the power circuit and/or the electronic device, and also capable of creating a flea powered “stand-by” mode.

[0025] In another aspect of the invention, the power circuit is formed on a semiconductor chip that includes analog and digital components on the same chip. A semiconductor process such as a 350V Silicon-on-Insulator (SoI) BCD process could be used for the semiconductor, which would permit the integration on one die of the microcontroller, timer/quartz real-time clock, PID controller and PWM controllers, MOSFETs, and corresponding drivers. In addition, the typical specific capacitance in CMOS technology ranges from 0.1 fF/ μm^2 (polypoly capacitors) to 5 fF/ μm^2 (MIM capacitors) or ceramic capacitors can be considered. Moreover, a process like DMOS can be used, or a bi/substrate can be considered, such as a layer of Silicon Carbonate, with Gallium Nitrate or Silicon Dioxide bi/substrata's also can be used. Or alternatively, Gallium Nitrate or Gallium Arsenide and the use of Deep Trench capacitors could be used for construction of the chip rather than silicon. All of these options are necessary because of the capacitance needed with the low R_{on} MOSFETS or transistors.

[0026] A BCDMOS process may be used to manufacture the power circuit. BCDMOS includes a process for integrating Bipolar (analog), CMOS (logic) and DMOS (power) functions on a single chip for ultra high voltage (UHV) applications. BCDMOS provides a broad range of UHV applications such as LED lighting, AC-DC conversion and switched mode power supplies. Capable of operating directly “off line” from a 110/220VAC source,

integrated circuits (ICs) implemented with a non-Epi process can deploy optimized 450V/700V DR-LDMOS transistors that specify low on resistance and a breakdown voltage that exceeds 750V. When used in power switching applications, designers can expect lower conduction and switching losses.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] Other advantages of the present invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings wherein:

[0028] Figure 1 is a schematic diagram of an electronic charging device for use in providing electrical power to electronic devices, according to an embodiment of the present invention;

[0029] Figure 2 is a block diagram of a power circuit that may be used with the charging device shown in Figure 1, for use in providing electrical power to electronic devices, according to an embodiment of the present invention;

[0030] Figure 3 is a schematic diagram of a buck regulator circuit that may be used with the power circuit creating a “Hybrid” voltage break-down circuit as shown in Figure 2, according to an embodiment of the present invention;

[0031] Figures 4-7 are schematic diagrams of a switch capacitor voltage breakdown circuit that may be used with the power circuit shown in Figure 2, including the sharing of gates between capacitors for further reducing RDS_{ON} losses, according to an embodiment of the present invention;

[0032] Figure 8 is a schematic diagram of a portion of the switch capacitor voltage breakdown circuit shown in Figure 4, according to an embodiment of the present invention;

[0033] Figure 9 is a table illustrating gain settings for use with the switch capacitor voltage breakdown circuit shown in Figure 8, according to an embodiment of the present invention;

[0034] Figures 10-12 are schematic illustrations of the switch capacitor voltage breakdown circuit shown in Figure 8 in a charge phase mode and a discharge phase mode associated with each of the gain settings shown in Figure 9, according to an embodiment of the present invention;

[0035] Figure 13 is a schematic diagram of a forward converter circuit that may be used with the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0036] Figure 14 is a schematic diagram of an alarm control circuit that may be used with the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0037] Figure 15 is another schematic diagram of the power circuit shown in Figure 2, including a power controller integrated circuit, according to an embodiment of the present invention;

[0038] Figures 16, 17A, and 17B are block diagrams of the power controller integrated circuit shown in Figure 10, according to embodiments of the present invention;

[0039] Figure 18 is a block diagram of a power management unit that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0040] Figure 19 is a graphic illustration of Power-On-Reset threshold voltages that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B;

[0041] Figure 20 is a schematic illustration of a Proportional to Integral and Differential Regulator Control circuit that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0042] Figures 21 and 22 are block diagrams of a digital control block that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to embodiments of the present invention;

[0043] Figure 23 is a flow chart illustrating a method of operating the power circuit shown in Figure 2 for use in providing electrical power to electronic devices, according to an embodiment of the present invention;

[0044] Figure 24 is a graphic illustration of state transitions that may be used with the method shown in Figure 23, according to an embodiment of the present invention;

[0045] Figure 25 is a schematic illustration of a communication interface that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0046] Figure 26 is a schematic illustration of a microprocessor communication protocol that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0047] Figure 27 is a schematic illustration of an Inter-Integrated Circuit that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0048] Figure 28 and 29 are schematic illustrations of the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0049] Figure 30 is a connection diagram that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0050] Figure 31 and 32 are additional schematic illustrations of the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to embodiments of the present invention;

[0051] Figure 33 is a flow chart of an algorithm for a low-current detection and an error detection that may be used with the power controller integrated circuit shown in Figures 16, 17A, and 17B, according to an embodiment of the present invention;

[0052] Figures 34 and 35 are schematic illustrations of the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0053] Figure 36 is a schematic illustration of Level Shifter that may be used with the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0054] Figure 37 is a schematic illustration of an RCD circuit that may be used with the forward converter circuit shown in Figure 13, according to an embodiment of the present invention;

[0055] Figures 38 and 39 are additional schematic illustrations of the power circuit shown in Figure 2, according to an embodiment of the present invention;

[0056] Figure 40 is a schematic illustration of a portion of the power circuit shown in Figure 2, according to an embodiment of the present invention; and,

[0057] Figure 41 is another schematic illustrations of the power circuit shown in Figure 2, according to an embodiment of the present invention.

[0058] Corresponding reference characters indicate corresponding parts throughout the drawings.

DETAILED DESCRIPTION OF INVENTION

[0059] With reference to the drawings and in operation, the present invention overcomes at least some of the disadvantages of known power delivery systems by providing a power module that includes a power circuit that provides DC voltage output power to consumer electronic devices from an AC mains supply (typically 120VAC (US) to 240VAC[EU/Asia]). The power circuit is configured to provide electrical power to charge electronic storage

devices and/or power consumer electronic products including, but not limited to, a cell phone, a smartphone, a tablet computer, a laptop, and/or any suitable electronic device that may benefit from this invention due to extremely high efficiencies and very low stand-by power requirements. In general, the power circuit includes a primary power circuit and a secondary power circuit for receiving high voltage AC power from an electrical power source and delivering a low voltage DC power signal to one or more electronic devices. The primary power circuit receives the AC power signal from an AC power supply and generates an intermediate direct current (DC) power signal at a reduced voltage level. The secondary power circuit receives the intermediate DC power signal from the primary power circuit and generates and delivers an output DC power signal having a voltage level suitable for use in powering and/or charging consumer electronic devices.

[0060] The primary power circuit includes a rectification circuit for receiving the AC power signal and generating a rectified DC power signal, and a switch capacitor voltage breakdown circuit for dividing the rectified DC voltage to a reduced voltage for use by the secondary power circuit. The switch capacitor voltage breakdown circuit includes fly-back capacitors to maximize power efficiency and a hold capacitor to minimize the voltage ripple. In one embodiment, the switch capacitor voltage breakdown circuit is configured to deliver up to 50mA and maintain $\geq 95\%$ efficiency across the range of load currents from 50mA to less than 1mA under light load conditions. The primary power circuit may also include a switch-mode buck regulator that is connected in parallel with the switch capacitor voltage breakdown circuit for handling large current loads, for example, up to 430mA of current. The buck regulator may include a P-channel MOSFET switch, a high voltage buck diode, and a buck energy storage inductor. In addition, the buck regulator may also include a pulse-width modulator (PWM) controller for generating a pulse width modulated signal to control

the on/off time of the buck regulator PMOSFET, which may also be expressed as an NMOSFET with the appropriate gate drivers.

[0061] The secondary power circuit includes a forward converter power circuit that includes a transformer for receiving the intermediate DC power signal from the primary power circuit and generating the output DC power signal. The forward converter also includes a MOSFET connected to the primary side of the transformer and a control circuit to operate the MOSFET to regulate the voltage at the output of the forward converter as load current is drawn from the secondary-side of the transformer. For example, the forward converter control loop may be configured to regulate the output voltage under heavy fluctuation (4.5nA to 4.5A) of load current without triggering any instability.

[0062] In the modern world, the MOSFET has become a more and more important part of "Real World" interfaces. It enables motor/solenoid driving, transformer interfacing, and a host of other functions. At the other end of the spectrum is the Microprocessor. It is characterized by steadily reduced operating voltages and currents. In many systems these parts are used together. A standard high-voltage MOSFET requires a driver that can deliver on the order of a 5v to 20v volt swing to the FET gate in order to successfully turn the FET on or off. In the case of turn-on for an NMOSFET, it is actually required that this gate drive voltage exceed the power rail voltage. Specialty drivers using charge pump technology have been devised for this purpose, but they are typically discrete parts and increase the number of power rails needed on a circuit. The FET driver's other main function is to have a reduced input voltage requirement making it compatible with the output port capability of a modern CMOS microprocessor. This arrangement is costly in terms of power and typically requires three power supplies. First is the main power rail. It is composed of a voltage in the range of 100 to 600 volts supplied to the MOSFET. The second supply is the 5-20 volts required by

the driver and finally is the supply required by the microprocessor. This present invention combines all these rails within the chip, such that the power and parts normally associated with the circuit are minimized and therefore efficiencies increased.

[0063] In many circumstances, the power supplies constitute a significant percentage of both the parts count and cost in a small system. A consolidated part can substantially alter this equation. This new part would consist of a combination of a high power MOSFET as the base part to which is added the appropriate driver with an included charge pump. Also added is the power supply required for the driver derived from the main rail supply internally. A final addition is an output pin to supply power for the microprocessor from this internal supply. In many modest systems the complete parts list would consist of this new device, the microprocessor, and the main power rail parts. This would allow the next generation of low cost/low assembly count microprocessor subsystems.

[0064] The power module includes the advanced power supply system on a chip (Tronium PSSoC), which is the subject of this present invention, including a controller application specific integrated circuit (ASIC) to provide a low-cost, highly efficient means to convert the AC line voltage present at a typical home or business electrical outlet to a reduced regulated DC voltage for consumer electronic applications. Typical applications include, but are not limited to, charging systems for cell-phones, tablets or other handheld devices, USB power conversion, power supplies for consumer, medical and industrial devices, and many other possible uses.

[0065] The Tronium PSSoC is configured for use in two primary power module applications including an Autonomous Power Module and a Universal Power Module. The Autonomous Power Module operates in an autonomous mode of operation that is based upon an analog feedback approach for reduced cost. The Universal Power Module operates in a universal

mode of operation that utilizes a microprocessor (μ P) controller to provide feedback for regulation of the final output voltage, which can be one power rail which is controlled/monitored or more. Some key features of the Tronium PSSoC include, but are not limited to, 90 VAC to 264 VAC Line Voltage Operation (other input voltage either AC or DC may be used), Programmable Output Voltage, Hybrid switch capacitor voltage breakdown circuit & Switch-Mode Buck Regulator (which is synchronously rectified for efficiency) for DC-DC Conversion, PID Regulation Control Loop for High Accuracy, Digital State Machines for Current and Temperature Monitoring, Ultra-Low Power Dissipation for Idle (Vampire) Mode of Operation, Opto-Isolated Microprocessor Interface for Configuration and Control, I2C Slave Port for Manufacturing Test, auto-detect input voltage range: 127 VDC to 373 VDC (world-wide voltages 110VAC-260VAC), featured Out Power: 22.5W (any wattage possible), hybrid voltage converter for high-efficiency operation, stacked Switch Capacitor Voltage Breakdown Modules, PID regulation loops with PWM gate drivers, power scaling function for high efficiency at multiple load levels and flea power Stand-by Mode, thermal sensing and shut-off, short circuit and over-current protection, adjustable no-load / light load shut-off with restart and control logic, selectable analog or digital control, minimal or no external circuitry part count and discrete device size, and optional digital interface for bi-directional communication.

[0066] In addition ,the Switch Mode Buck Regulator circuit may include a what is typically know as a Buck/Boost circuit; or the Buck/Boost may be replaced with a SEPIC, Cúk, or Push Pull or other topologies. These will have synchronous rectification for efficiency and may either use a fly-back or forward convertor typologies.

[0067] The Tronium PSSoC is an advanced power controller integrated circuit that is configured to provide output voltage regulation with high-efficiency and high accuracy. The

advanced features of the Tronium PSSoC provide the user with a multi-purpose device which can be used in a large variety of applications in either a “charger” mode or “constant supply” mode. Programmable output voltages (1.7V to 48V or higher) are possible with the Tronium PSSoC, with little or no loss of efficiency across a variety of current load conditions, which feature is called the “Dial-a-Voltage” feature. In addition, multiple output currents may be created by the combination of the Hybrid Circuit, or the Switch Capacitor Circuit by itself, so as to create multiple voltage/current combinations ranging typically from 1.7V to 48V, which is sufficient to power most electronic devices. This “Dial-a-Voltage” feature, is factory programmable or programmable by a customer with a proper code, so that the same chip may be used for a 1.7V output or a 48V output, with only nominal changes in any external components like the transformer winding and the FETs which drives the transformer.

[0068] The Tronium Power Supply System on a Chip (PSSoC) ASIC is an advanced power control device that enables high efficiencies across a very wide range of output power. While typical ‘high efficiency’ power supply controllers boast ~50% efficiencies down to 10% of full load, the Tronium device is intended to provide > 90% efficiency down to and below 1% of full load.

[0069] The Tronium PSSoC provides a revolutionary topology for high voltage power conversion by implementing an intermediary voltage rail, allowing the power capabilities of the system to scale with the load demand. It also shrinks parts into the ASIC, minimizing external parts needed; and enables a wider range of transformer options for enhanced optimization of power with lower coil losses. The Tronium PSSoC also provides a PID switching controller with which to drive the primary side of a transformer if isolation is required, or other topologies of conversion and regulation. It also features either secondary or primary side control/feedback.

[0070] In one embodiment, the Tronium PSSoC uses a proprietary high-voltage intermediate voltage capacitor voltage breakdown conversion scheme, which can be used alone, or in combination with a switch-mode buck regulator to maintain high-efficiency regardless of the load voltage or current. When no current is being drawn by the load, the device will enter a low-current mode of operation of approximately ½ milliwatt in order to minimize and virtually eliminate the traditional ‘vampire’ current required to stay awake.

[0071] The Tronium PSSoC may include the following major circuit blocks: Intermediate Capacitor Voltage Break-Down Converter Module (CVBD Module) (can be one or more stages for desired current output); High-Voltage Single-Stage or Two-Stage switch capacitor voltage breakdown circuit; Proportional to Integral and Differential (PID) Regulator Control Block for PWM Control of Forward Converter; Switch-Mode Buck Regulator PID Controller (optional Hybrid typology for voltage output); Buck Regulator Switch Driver; Current and Temperature Sense Blocks; 12-bit ADC for Voltage and Current Monitoring; 10-bit DAC's for Feedback Control; Digital Control Block for Current Monitoring State Machine; Serial Input for Opto-Isolator Communications Interface; I2C Serial Interface Port for Test, Evaluation, Repair and Communication; Oscillators for generation of internal clock signals; Power Manager for On-Chip Voltage and Current Generation; Adapted for use with or without a microcontroller which can be embedded into the chip or external; Primary Side Sensing or Secondary Side Sensing Capabilities; and Synchronous forward convertor.

[0072] The power module may also include a Tronium PSSoC that includes both analog and digital control in order to optimize performance and efficiency. In order to enable not only analog control but also digital control the proper inputs and outputs must be available on the Tronium PSSoC. Given these availabilities, and coupled with power loop control from an internal clock - control of the clock can be driven and controlled with external signals. The

novel approach is that these signals can be driven from the secondary side while the Tronium PSSoC sits on the primary side of the transformer.

[0073] Digital control is commonly accomplished on the same side of the isolation barrier. However, given that the Tronium PSSoC is inherently an isolated system, and end to end efficiency optimization is required, control from primary side or secondary back to primary side may be utilized. This is accomplished in a number of different ways given the Tronium implementation. This can be done with optocouplers transmitting the digital control signal from a microcontroller as well as analog signals from a current sense circuit. Furthermore, this can be accomplished by using a third winding on the isolation transformer.

[0074] Some or all of the circuits and/or electrical devices include in the power circuit may be integrated onto the chip using either a silicon process, Gallium nitride (GaN) or Gallium Arsenide (GaA), or by using Deep Trench Capacitors, or other available processes which provides high efficiency parts, if high efficiency is desired. Thus, one or all of these parts may be embedded in the ASIC rather than be external discretes, even the transformer, using the known transformer in silicon (or GaN-GaA) techniques. In addition, the use of MIM and MOM capacitors along with low $R_{DS\text{ON}}$ MOSFETS, integrated decoupling capacitors and/or flying capacitors (C_{FLY}), for ripple reduction, which in turn decreases the size of needed capacitors may be used where capacitors or FETS are called for herein. Also, the introduction of integrated inductors on chip helps achieve the highest efficiencies. Alternatively, the highest efficiency parts, like GaA, GaN or Schottky diode parts are to be used.

[0075] In addition, the capacitors may be nano-capacitors, and may be based upon ferroelectric and core-shell materials as well as those based on nanowires, nanopillars, nanotubes, and nanoporous materials.

[0076] The substrata for the Tronium PSSoC could be made from customary films currently used in capacitors (if external) or within semiconductor substrates such as high or low Ohmic silicon substrate, polysilicon, gallium nitride, gallium arsenide, silicon germanium or substances like silicon carbide or indium phosphide.

[0077] They key is on-board ASIC integration of as many discretes as possible where the process permits, and if efficiency is key then identification of low RDSon values, high efficient parts, and sufficient voltage break-down parts. Another key is to run the Switch Buck Module at higher frequencies, so that parts become smaller, and sufficiently smaller to become on-board chip devices.

[0078] A selected embodiment of the present invention will now be explained with reference to the drawings. It will be apparent to those skilled in the art from this disclosure that the following description of the embodiment of the present invention is provided for illustration only and not for the purpose of limiting the invention as defined by the appended claims and their equivalents.

[0079] Figure 1 is a schematic diagram of an electronic charging device 10 for use in providing electrical power to electronic devices. Figure 2 is a block diagram of a power module 12 that may be used with the electronic charging device 10. In the illustrated embodiment, the electronic charging device 10 includes a housing 14, a pair of power prongs 16 extending outwardly from the housing 14 and a device connection assembly 18 that is adapted to connect to an electronic device 20 to deliver electric power from the charging device 10 to the electronic device. The electronic charging device 10 also includes the power module 12 that includes a power circuit 22 that is configured to receive power from an electrical power source 24 and deliver power to the electronic device 20 such as, for example, portable consumer electronic devices including, but not limited to, a cell phone, a

smartphone, a tablet computer, a laptop, and/or any suitable electronic device. In addition, the power circuit 22 may deliver power for use in charging electronic storage devices such as, for example, mobile phone/laptop/tablet power storage batteries. In one embodiment, the power circuit 22 may be configured to provide low voltage DC output (typically 5VDC) from an AC mains supply typically 120VAC (US) to 264VAC[EU/Asia].

[0080] In the illustrated embodiment, the power circuit 22 includes a primary power circuit 26 and a secondary power circuit 28. The primary power circuit 26 is adapted to be electrically coupled to the electrical power source 24 and is configured to receive an AC (or DC) input power signal from the electrical power source 24 and generate an intermediate direct current (DC) power signal. The intermediate DC power signal being generated at a first voltage level that is less than a voltage level of the AC input power signal. The secondary power circuit 28 is electrically coupled to the primary power circuit 26 and is configured to receive the intermediate DC power signal from the primary power circuit 26 and deliver an output DC power signal to the electronic device 20. The output DC power signal is delivered at an output voltage level that is less than the first voltage level of the intermediate DC power signal. For example, in one embodiment, the primary power circuit 26 is configured to receive the AC input signal having a voltage level between a range of 127 volts to 375 volts AC and to deliver the intermediate DC power signal at a voltage level of approximately 110volts DC. The secondary power circuit 28 is configured to receive the intermediate DC power signal and deliver the output DC power signal at approximately 5 volts DC.

[0081] In the illustrated AC-DC embodiment, the primary power circuit includes a rectifier circuit 30, an intermediate voltage converter 32, a buck regulator 34, and a hold capacitor 36 that is electrically coupled to the intermediate voltage converter 32 and the buck regulator 34.

The intermediate voltage converter 32 and the buck regulator 34 are coupled in parallel between the rectifier circuit 30 and the secondary power circuit 28. The rectifier circuit 30 is configured receive the AC power input signal from the electrical power source 24 and generate a rectified DC power signal that is delivered to the intermediate voltage converter 32 and the buck regulator 34. In one embodiment, the rectified DC power signal is delivered having a voltage level that is approximately equal to the voltage level of the AC input power signal. As shown in Figures 13 and 15, in the illustrated embodiment, the rectifier circuit 30 includes a plurality of diodes 38 that are arranged in a full-wave bridge rectifier having first and second input terminals coupled to the high and low sides of the electrical power source 24 for producing a DC power signal from an AC input power signal. In one embodiment, the rectifier circuit 30 may also include a filter capacitor 40 that is coupled to the full-wave bridge rectifier. In yet another embodiment, the rectifier circuit 30 does not include the filter capacitor 40. In another embodiment, the rectifier circuit 30 may include a half-bridge rectifier (not shown).

[0082] Figure 3 is a schematic diagram of the buck regulator circuit 34 that may be used with the power circuit 22. In the illustrated embodiment, the buck regulator circuit 34 includes a regulator switch assembly 42 that is coupled to a voltage reduction circuit 44. The voltage reduction circuit 44 includes a high voltage buck diode 46, a buck energy storage inductor 48, and a capacitor 50. The regulator switch assembly 42 is operated to selectively deliver the rectified DC power signal to the voltage reduction circuit 44. In the illustrated embodiment, the regulator switch assembly 42 includes a P-channel MOSFET 52, a driver circuit 54 that is coupled to the P-channel MOSFET 52, and a level shifter 56 that is coupled to the driver circuit 54. In one embodiment the regulator switch assembly 42 may include an N-channel MOSFET and/or a P-channel MOSFET. In the illustrated embodiment, the buck regulator 34

also includes a regulator control circuit 58 that includes a regulator PWM controller 60 (also shown in Figures 16, 17A, and 17B) for generating a pulse width modulated signal to control P-channel MOSFET 52. In one embodiment, the control circuit 58 may also include a voltage sensing circuit 62 that is connected to the primary side of the forward converter transformer for sensing the voltage level of the intermediate DC power signal being delivered to the secondary power circuit 28. The regulator PWM controller 60 may generate a pulse-width modulated control signal as a function of the sensed first voltage level to adjust a duty cycle of the PWM control signal being delivered to the P-channel MOSFET 52 to maintain the voltage level of the intermediate DC power signal. The Buck Regulator servo loop 58 is voltage controlled and the V_{primary} is sensed and used to modulate the duty cycle of the driver 54.

[0083] In one embodiment, the sensing circuit 62 includes one or more Hall Effect sensors that are coupled to the primary side of the forward converter transformer for sensing a magnetic field being generated within the transformer. The Hall Effect sensors facilitate determining a zero-crossing of the transformer by directly sensing the magnetic field being generated by the transformer during operation. In one embodiment, the sensing circuit 62 includes a primary side Hall Effect sensor coupled to the primary side of the transformer. The primary side Hall Effect sensor is connected to the PWM controller 60 for transmitting a signal to the PWM controller 60 for use in determining when the transformer nears the “zero-crossing”. In another embodiment, the sensing circuit 62 includes a secondary side Hall Effect sensor that is coupled to the secondary side of the transformer, and is connected to the forward converter controller (shown in Figure 13) for transmitting a signal indicative of the transformer magnetic field for use in determining the time at which the transformer reaches the “zero-crossing”.

[0084] Figures 4-8 are schematic diagrams of the intermediate voltage converter 32. Figure 9 is a table illustrating gain settings that may be used with the intermediate voltage converter 32. Figures 10-12 are schematic illustrations of the intermediate voltage converter 32 in a charge phase mode 66 and a discharge phase mode 68 for each of the gain settings shown in Figure 9. In the illustrated embodiment, the intermediate voltage converter 32 includes a single-stage switch capacitor voltage breakdown circuit that is coupled to the hold capacitor 36 and the secondary power circuit 28. The switch capacitor voltage breakdown circuit includes a pair of flyback capacitors 70 that are electrically coupled in parallel and a plurality of switch assemblies 72 that are electrically coupled to each of the flyback capacitors 70. The switch assemblies 72 are selectively operated between the charge phase mode 66 and the discharge phase mode 68. During the charge phase mode 66 the switch assemblies 72 are operated to form a charging circuit 74 to connect the flyback capacitors 70 to the rectifier circuit 30 to deliver the rectified DC power signal to each of the flyback capacitors 70. During the discharge phase mode 68, the switch assemblies 72 are operated to form a discharging circuit 76 to connect the flyback capacitors 70 to the secondary power circuit 28 to deliver the intermediate DC power signal to the hold capacitor 36.

[0085] In one embodiment, as shown in Figure 8, the single-stage switch capacitor voltage breakdown circuit 32 may include a first flyback capacitor Cfb1 and a second flyback capacitor Cfb2, and nine switch assemblies S1, S2, S3, S4, S5, S6, S7, S8, and S9. In addition, two of the switch assemblies S3 and S9 are coupled to ground. During operation, the gain setting of the switch capacitor voltage breakdown circuit may be adjusted by selectively operating the switch assemblies according to the gain setting table shown in Figure 9. For example, during the charge phase mode 66 (Phase 1), switches S1, S4, S7, and S8 are turned on and moved to a closed position and switch assemblies S2, S3, S5, S6, and S9

are turned off and moved to an open position to form the charging circuit 74 to connect the flyback capacitors Cfb1 and Cfb2 to the rectifier circuit 30. As shown in Figure 10-12, in the charging circuit 74 the top plate of each flyback capacitor Cfb1 and Cfb2 are connected to the rectifier circuit 30 line voltage, Vline. For a gain setting equal to $G=1x$, during the discharge phase mode 68 (Phase 2), switch assemblies S2, S3, and S7 are turned on and switch assemblies S1, S4, S5, S6, S8, and S9 are turned off to form a discharging circuit 76 shown in Figure 10 that includes the top plate of capacitor Cfb1 connected to the hold capacitor 36 and the top plate of capacitor Cfb2 connected to the bottom plate of capacitor Cfb1. With reference to Figures 9 and 11, for a gain setting equal to $G=1/2x$, during the discharge phase mode 68 (Phase 2), switch assemblies S2, S5, and S9 are turned on and switch assemblies S1, S3, S4, S6, S7 and S8 are turned off to form a discharging circuit 76 that includes the top plate of capacitor Cfb1 connected to the hold capacitor 36, the bottom plate of capacitor Cfb1 connected to ground, and the top plate of capacitor Cfb2 connected to the hold capacitor 36, the bottom plate of capacitor Cfb2 connected to ground. Referring to Figures 9 and 12, for example, a gain setting equal to $G=2/3x$, during the discharge phase mode 68 (Phase 2), switch assemblies S2, S6, and S9 are turned on and switch assemblies S1, S3, S4, S5, S7 and S8 are turned off to form a discharging circuit 76 that includes the top plate of capacitor Cfb1 connected to the hold capacitor 36, top plate of capacitor Cfb2 connected to the bottom plate of capacitor Cfb1, and bottom plate of capacitor Cfb2 connected to ground.

[0086] In one embodiment, multiple “stages” of the switch capacitor circuits, as explained herein, are linked together, which may be used to gain additional current output, with or without the need for the addition of the Hybrid power conversion/regulation circuits.

[0087] Referring to Figure 7, in the illustrated embodiment, the switch capacitor voltage breakdown circuit 32 also includes a control circuit 78 that is coupled to each of the switch

assemblies 72 to operate the switch capacitor voltage breakdown circuit 32. The control circuit 78 includes a voltage sensing circuit 80 for sensing a voltage level of the rectified DC power signal being received from the rectifier circuit 30 and a gain controller 82 that is configured to select a gain setting of the switch capacitor voltage breakdown circuit 32 as a function of the sensed voltage level and operate each of the plurality of switch assemblies as a function of the selected gain setting. By providing a control circuit 78 that selects the gain setting of the switch capacitor voltage breakdown circuit 32 as a function of the sensed input voltage level, the switch capacitor voltage breakdown circuit 32 is able to adjust the operation of the switch capacitor voltage breakdown circuit 32 to account for variations of AC voltage levels in different countries and/or power grids and deliver the intermediate DC output signal at a predefined voltage level and maintain optimum power efficiency. In the illustrated embodiment, the control circuit 78 includes a resistor divider 84, a pair of comparators 86, a logic decoder 88, and a gain controller 82. The negative input of the comparators 86 is connected to a bandgap generator and the positive inputs are connected to the rectifier circuit 30 line voltage, V_{line} .

[0088] Referring to Figures 4-6, in the illustrated embodiment, one or more switch assemblies includes an N-channel MOSFET switch 90, and a level shifter 92 that is connected to the N-channel MOSFET switch 90 for delivering a control signal to the N-channel MOSFET switch 90 to facilitate operating the N-channel MOSFET 90. In addition, one or more switch assemblies 72 include a Dickson charge pump 94 that is connected to the level shifter 92 to provide a high-voltage signal required to close the N-channel gate during operation. The Dickson charge pump 94 is configured to generate an output power signal having a voltage level that is greater than a switch assembly source voltage to enable the level shifter 92 to operate the N-channel MOSFET switch 90. In one embodiment, each of the

switch assemblies 72 includes an N-channel MOSFET 90, a level shifter 92 coupled to the N-channel MOSFET 90, and a Dickson charge pump 94 coupled to the level shifter 92. In another embodiment, two or more level shifters 92 may be connected to a single Dickson charge pump 94. Wherever in this specification the term NMOS is used, it could be substituted with a PMOS and vice versa.

[0089] In the illustrated embodiment, at least one switch assembly 72 includes a level shifter 92 that is connected to an N-channel MOSFET switch 90. In addition, a Dickson charge pump 94 is connected to the level shifter 92 to provide a power signal sufficient to close the gate of the N-channel MOSFET switch 90. In the illustrated embodiment, the Dickson charge pump 94 is connected to the source voltage, V_{source} , of the N-channel MOSFET and is configured to deliver an output signal to the level shifter 92 that has a voltage level that is greater than the voltage level of the source voltage, V_{source} in the case of using an NMOS. In one embodiment, the Dickson charge pump 94 is configured to deliver an output power signal, V_{DCP} , having a voltage level that is approximately 15-20 volts greater than the source voltage, V_{source} in order to assure proper gate operation. The gain controller 82 is connected to the level shifter 92 for providing a low voltage control signal to the level shifter 92. The level shifter 92 is connected to the source voltage, V_{source} , and to the Dickson charge pump 94, and is configured to deliver the control signal to the N-channel MOSFET 90 having a voltage level sufficient to operate the switch assembly 72 as a function of the received control signal.

[0090] Figure 13 is a schematic diagram of the secondary power circuit 28 including a forward converter circuit 96. In the illustrated embodiment, the forward converter circuit 96 includes a primary voltage reduction circuit 98 and a secondary voltage reduction circuit 100. The primary voltage reduction circuit 98 is configured to receive the intermediate DC power

signal from the primary power circuit 26 and deliver a secondary DC power signal to the secondary voltage reduction circuit 100. The secondary DC power signal has a voltage level that is less than the voltage level of the intermediate DC power signal. The secondary voltage reduction circuit 100 is configured to receive the secondary DC power signal and generate the output DC power signal being delivered to the electronic device 20.

[0091] In the illustrated embodiment, the primary voltage reduction circuit 98 includes a transformer 102. The primary side of the transformer 102 is connected to the primary power circuit 26 and the secondary side of the transformer 102 is connected to the secondary voltage reduction circuit 100. In one embodiment, the primary voltage reduction circuit 98 may include a switch assembly 104 including a FET that is coupled to the transformer primary side, and a control circuit 103 that is coupled to the switch assembly 104 for selectively operating the switch assembly 104 to adjust a voltage level of the secondary DC power signal. The transformer control circuit 103 may include a primary side voltage sensing circuit 105 for sensing voltage and current level of the DC output signal and operate the transformer switch assembly 104 to maintain the voltage level of the DC output signal at a predefined output voltage level and required current level. In this fashion at least five parts are removed from the equation, which are normally needed with a secondary side sense controller, including an opto-coupler, opamp, an inductor, diode and a capacitor. The secondary voltage reduction circuit 100 includes a pair of diodes, an inductor, and a capacitor. The forward converter 96 may also include a resistor, capacitor, diode (RCD) circuit 150 (shown in Figure 37). The RCD circuit 150 is configured to perform a transformer reset when the primary side switch 104 is off to avoid saturating the transformer 102. The forward converter 96 is a pulsed based step down converter. A duty cycle modulated digital pulse is applied to the primary side switch 104 to convert the incoming DC

voltage to an AC voltage. The transformer winding ratio provides the step down. In this case, the step down is from 11:1. The secondary side sees an ac voltage on its terminals. This AC voltage is rectified by the secondary voltage reduction circuit 100 diodes and filtered by the LC filter to produce a stepped down DC voltage on the output. The duty cycle is modulated by either an analog or a digital servo loop. This servo loop looks at the dc voltage on the output side, compares it with a response to produce an error signal. This error signal is used to drive a comparator which converts this error in a pulse width modulated DC pulse. This DC pulse when applied to the primary side switch gate 104 corrects the error on the output and maintains regulation for various load levels.

[0092] In one embodiment, the transformer control circuit 103 may include a primary side current sense circuit 107 that is connected to the primary side of the transformer 102 to sense the load current and the load voltage to facilitate regulating the DC output signal to within 5% of a predefined load voltage. The control circuit 103 uses a current sense resistor 109 and measures across the primary winding. In the illustrated embodiment, the transformer control circuit 103 includes a comparator 111 that drives the FET 104. In one embodiment, the resistor 109 is a .10 ohm resistor. The control circuit 103 is configured to sense the load current on a pulse by pulse basis and sense the peak current. For example, in one embodiment, the control circuit 103 senses the voltage across the resistor 109 and provides the sense current in a voltage format when the switch 104 is on. When the switch 104 is off, the control circuit 103 senses the differential voltage across the primary side of the transformer 102 which may be approximately equal to V_{primary} minus the drain of the off transistor 104. When the transistor 104 is off, there is a drain voltage across it so that is also a sawtooth signal. Both the voltage and the current are sampled using a switch capacitor sample and hold circuit that is scaled down to low voltages and includes resistor dividers to

set the differential voltage part of the primary winding and bring the voltage into the sample and hold circuit. The differential voltage is equal to the ΔV across the winding including V_{primary} and the bottom of the V_{primary} . The sample and hold circuit and the resistor dividers take the primary voltage down to less than 5 volts and then takes the deferential that gets the ΔV out. The sample and hold circuit drives the comparator 111. The other input of the comparator 111 is a sample and held peek current voltage that we sense across the 0.1 ohm resistor 109. The inputs into the comparator 111 are scaled and gained up and offset so that the inputs are under steady state, and the comparator 111 drives a set-reset flow clock. The FET 104 includes an AND-gate that is driven by the comparator 111. A clock off the comparator 111 adjusts the duty cycle of the AND-gate. The AND-gate also has a high duty cycle driven by a high pulse width clock, which is a sawtooth signal. The other input of the AND-gate is the output of the comparator 111 so then the comparator 111 modulates that duty cycle to small duty cycle or to a large duty cycle. In one embodiment, the clock is the 100 KHz clock for the forward converter servo loop.

[0093] A tertiary winding from the transformer is not needed as a supply for the sensor. The supply is available from the primary side because the sensing circuit is on the primary side and supply is not needed from the secondary side. The voltage across the primary side inductor and the current that is going to the primary side FET 104 is used to determine the output voltage of the system. In one embodiment, the FET 104 includes a 200 volt Philips part device having a 2-volt threshold, which may use a 5v signal to drive the FET 104 to turn it on without level shifting. In another embodiment, a 10 volt LDO or 20 volt LDO may be used with a level shifter to go from 5 volts to 10 volts, or 5 volts to 20 volts to operate the FET 104.

[0094] In the illustrated embodiment, the control circuit 103 uses the sense resistor 109 that is in the drain path of the MOSFET 104 to implement a gated approach in which a sample and hold circuit obtains the peak voltage right when the switch 104 is on between each square wave in the PWM cycle. The gating arrangement samples when the switch is on, because when the switch is off there is no information available at that time.

[0095] In the illustrated embodiment, the power circuit 22 is configured accommodate different transformers having different turn ratios to generate a DC output signal having various current and/or voltage requirements.

[0096] In one embodiment, the power circuit 22 may not include the full wave bridge 38, rectifier circuit 30, and input capacitor, 40, such that V_{LINE} is DC and thus the circuit can receive a direct current (DC) if the use case requires, and then conduct the voltage break down as further explained herein using the regulated buck circuit 34 and switch cap VB 32 are still used. However, in some use cases, especially with low DC to DC voltage breakdown, the buck regulator 34 would not be needed, and only the switch cap VB 32 would be used, whether one stage (as shown in Figures 2-12) only would be used. In this case, one could eliminate the control signal 105 from the output, and rely solely on the current sense resistor 109 and still maintain a tightly regulated voltage.

[0097] In another embodiment, for DC input variation of the circuit, the use case may not require a transformer (if the transformer is not needed for the voltage/current conversion, or if isolation is not needed) like in the case of an internal part, such as is found in smart phones. In this instance, the transformer is not necessary and may be removed from the circuit together with the FET that drives the transformer. In this case the entire forward convertor controller circuit 96, 28 can be removed, and the C_{hold} capacitor 36 would be replaced with

the sense resistor circuit segment 109. Further, if an AC circuit does not need to be rectified or isolated, than this circuit can work with AC as well as DC.

[0098] Figure 15 is schematic diagram of the power module 12 including a power controller integrated circuit (Tronium PSSoC) 106 that may be used with the electrical power circuit 22. Figures 16, 17A, and 17B are block diagrams of the Tronium PSSoC 106. In the illustrated embodiment, the power module 12 includes a printed circuit board 108 and the Tronium PSSoC 106 that is formed within a packaged chip and is coupled to the printed circuit board 108. At least a portion of the electrical circuit 22 is included within the Tronium PSSoC 106. In addition, the digital control may be conducted by either a microprocessor, external or embedded on the chip or a state machine. In one embodiment, some or all of the electrical circuits and electrical components included in the electrical circuit 22 are included within the Tronium PSSoC 106. The Tronium PSSoC 106 may be configured for use in two primary power module applications including an Autonomous Power Module (shown in Figures 16 and 28) and a Universal Power Module (shown in Figures 17A, 17B, and 29). For example, as shown in Figure 16, the Autonomous Power Module includes a Tronium PSSoC 106 that is configured to operate in an autonomous mode of operation that is based upon an analog feedback approach for reduced cost. The Universal Power Module, shown in Figures 17A and 17B, includes a Tronium PSSoC 106 that is configured to operate in a universal mode of operation and that utilizes a microprocessor (μ P) controller to provide feedback for regulation of the final output voltage.

[0099] In the illustrated embodiment, the Tronium PSSoC 106 is configured to meet predefined requirements for traceability, marking, solderability, and/or solvent resistance. The Tronium PSSoC 106 is marked to indicate a date code, plant identifier, and traceability/authenticity code. The authenticity code provides a means of identification and

verification as a genuine part against “knock-offs”. All production packaged components on a tape and reel include the same unique date code, plant identifier, and traceability/authenticity code. Lot segregation may exist in such a way as to prevent the mixing of date codes within the same lot of components. Packaged parts shall be marked to indicate the part number, date code and traceability code. Terminals are configured to meet the solderability requirements of IPC-J-STD-001 and IPC-J-STD-002 for the packaged Tronium PSSoC. The packaged Tronium PSSoC and its markings are configured to meet the requirements of the MIL-STD-202 test method 215.

[00100] The Tronium PSSoC 106 is an advanced power controller integrated circuit designed to provide output voltage regulation with high-efficiency and high accuracy. The Tronium PSSoC 106 provides the user with a multi-purpose device which can be used in a large variety of applications and because of the “Dial-a-Voltage” feature, the same chip can be configured to work in practically any electronic device. Likewise, programmable output voltages are possible with the Tronium PSSoC, with little or no loss of efficiency across a variety of current load conditions.

[00101] In the illustrated embodiment, the Tronium PSSoC 106 uses the switch capacitor circuit 32 and the switch-mode buck regulator 34 to maintain high-efficiency regardless of the load voltage or current. For example, when no current is being drawn by the load the electronic device 20, the Tronium PSSoC 106 enters a low-current mode of operation to minimize the traditional ‘vampire’ current required to stay awake. In the illustrated embodiment, the Tronium PSSoC 106 includes the single-stage switch capacitor circuit 32, a PID regulator control block 110 (shown in Figure 20) for PWM control of the forward converter secondary transformer 102, a switch-mode buck regulator controller 112, a buck regulator switch driver 114, a current and temperature sense blocks 116, 12-bit Analog-to-

Digital Converter (ADC) 118 for voltage and current monitoring, a 10-bit Digital-to-Analog Converter (DAC) 120 (shown in Figures 17A and 17B) for feedback control, a digital control block 122 for current monitoring state machine, serial input for opto-isolator communications interface, a I2C serial interface port, and power manager unit 124 for on-chip voltage and current generation. Other types of sensors, such as, sound, photo-detection, radiation and shock can also be added depending on the use case.

[00102] Figure 18 is a block diagram of the Power Management Unit 124. In the illustrated embodiment, the power management unit (PMU) circuit block 124 generates and supervises the bias voltages and currents required for proper operation of the Tronium PSSoC. Two linear voltage regulators provide regulated 5.0V supplies for the low-voltage circuits of the IC, as well for external support devices such as the opto-isolators and an optional external microprocessor. In addition to providing proper initialization of the IC upon connection to the line voltage, the PMU 124 monitors the voltage supplies for fault conditions and provides a master power-on-reset (POR) 126. In the illustrated embodiment, the PMU 124 includes the bandgap voltage reference, current reference generator, a line-side low-power linear voltage regulator, a transformer primary-side linear voltage regulator, and power-on-reset. To reduce power dissipation, the line-side circuits are powered from the LINE_0P1 pin which supplies a voltage of approximately one-tenth of the LINE_IN voltage (Vline). This voltage is generated internally using an external resistor divider connected to the LINE_IN and LINE_RDIV pins of the IC. Initialization of the PMU 124 begins with the application of the rectified voltage at the LINE_IN pin.

[00103] The PMU 124 contains a low-power bandgap reference voltage and current generator for the Tronium PSSoC 106 which is powered from the line voltage. A high-precision temperature-compensated output voltage is provided for use as a reference by

subsequent circuit blocks, along with multiple bandgap Proportional To Absolute Temperature (PTAT) current outputs. The bandgap output voltage can be trimmed at wafer probe to optimize the temperature coefficient with the `bg_trim[7:0]` register bits and stored in an one-time programmable (OTP) memory stored in a microprocessor. The bandgap cell is self-starting, requiring only the default trim value for initialization. The bandgap cell is not disabled during sleep mode, but is always powered on, and is designed for ultra-low power operation.

[00104] The PMU 124 also includes a low-power linear voltage regulator (LPREG) that is provided to convert the high-voltage present at the `LINE_IN` input of the PSSoC to a regulated voltage for the low-power voltage domain. The LPREG uses the bandgap reference voltage to generate a regulated output of 5.0V to drive the low power on-chip circuit blocks that are always powered on including the Low-Frequency Oscillator for the switch capacitor circuit 32, on-chip logic, etc. An external (off-chip) bypass capacitor may be used for noise filtering, connected to the LPREG pin. The regulator is not disabled during sleep mode, but is always powered on.

[00105] The PMU 124 may also include a primary-side low voltage regulator that is provided to supply the higher current requirements of off-chip opto-isolators, PWM gate drivers and other support circuits. An external 10 μ F bypass capacitor is required for noise filtering, connected to the `VREG5` pin. The voltage regulator may be disabled for test purposes with the use of the `en_Xv` signal. When the `en_Xv` input to the cell is 'low', all of the internal analog currents in the cell are disabled and the outputs are high impedance.

[00106] The POR 126 block monitors the internal supply voltage of the Tronium PSSoC as generated by the LPREG circuit block. For example, Figure 19 illustrates POR threshold voltages that may be used with the POR 126. In one embodiment, for voltages at the LPREG

pin less than the V_{POR} threshold voltage, the POR output will be asserted 'high' indicating a reset condition. In addition, for voltages at the LPREG pin greater than the V_{POR} threshold voltage, the POR output will be de-asserted 'low' for normal operation. Hysteresis is provided such that a reduction in the threshold voltage occurs once the V_{POR} threshold is exceeded. The threshold derived from hysteresis is then equal to $V_{POR} - V_{HYS}$. An inverted version of the POR signal may also be provided at POR_B.

[00107] In the illustrated embodiment, the switch capacitor voltage breakdown circuit (SCVBC) 32 included in the Tronium PSSoC 106 is configured as a voltage divider through Capacitive Voltage Break Down techniques (CVBD). Through capacitors, it divides the rectified DC voltage present at the LINE_IN pin to a reduced voltage at the CP2_OUT pin for use by the external transformer 102 and secondary voltage control loop. The external transformer 102 then further reduces this voltage to the desired application voltage as a function of the primary-to-secondary windings ratio. In one embodiment, the SCVBC 32 is configured as a cascade of two identical stages, as shown in Figures 17A. In another embodiment the SCVB 32 includes multiple switch capacitor stages, as shown in Figures 38-39. The SCVBC 32 is configured to deliver up to 50mA per Capacitive Break Down block, which consists of Switch Capacitor blocks which provide the voltage breakdown by half or other divisionals. This provides and maintains $\geq 95\%$ efficiency across the range of load currents from 50mA to less than 1mA under light load conditions on the primary side of the transformer 102. For example, assuming a $\geq 97\%$ efficiency for the external transformer & rectifier, and overall module efficiency of $\geq 92-97\%$ has been simulated and is achievable. In one embodiment, the SCVBC 32 may include on-chip fly-back capacitors to maximize power efficiency, external 2.2 μ F bucket capacitors and two external 7.5 μ F hold capacitors to minimize the voltage ripple. These capacitors are connected to the CP1_OUT and CP2_OUT

pins, respectively, for the outputs of the 1st and 2nd stages of the switch capacitor circuit. Both stages are clocked at a rate of 1KHz from a two-phase non-overlapping clock generator which is derived from an on-chip RC Oscillator.

[00108] Referring to Figures 17A and 17B, in one embodiment, for the Tronium PSSoC 106, the SCVBC 32 output voltage at CP2_OUT is programmable over the range of 120-90 Volts in steps of 0.117 Volts with the use of an 8-bit binary-weighted digital-to-analog converter. The SCVBC output is limited to this range to ensure that the forward converter transformer 102 provides most of the output current in the step-down process. The SCVBC is limited to an output current of 50mA. If additional current is required for the application, the switch-mode buck regulator 34 may be enabled to provide up to 430mA of current. Each stage of the SCVBC 32 may be programmed to produce a voltage conversion ratio. This programming is done automatically in the Course Gain Control where the rectified LINE_IN voltage is compared to the 8-bit DAC setting. The digital control of this DAC enables multiple voltages to be programmed to obtain the desired final output voltage required for the target application. An example of the load voltages which can be programmed with the DAC as a function of the transformer turns ratio.

[00109] Referring to Figure 16, in one embodiment, the SCVBC 32 may include a single-stage switch capacitor circuit with a corresponding divider ratio of 1, 0.66 or 0.5. The output voltage present is then reduced by the external (off-chip) forward converter 96 to obtain the final application output voltage of 5.0V. All analog and digital signals for the SCVBC (and Buck Controller) are generated in the 5V domain. The SCVBC Error Voltage is scaled to be within the XV domain using a resistor divider. The LINE_IN voltage is also scaled so that processing can be done within the XV voltage domain.

[00110] In one embodiment, shown in Figure 16, the SCVBC 32 includes a Gain Control block that uses the scaled LINE_IN voltage to determine the appropriate divider ratio for the SCVBC 32. The scaled LINE_IN voltage is compared to the Bandgap reference voltage to select one of three or more possible divider ratios as a function of the AC Mains voltage. Final regulation of the output voltage may be performed in the switch capacitor regulator where the clock is turned on and off to control the amount of charge delivered to the hold capacitor.

[00111] Referring to Figures 17A and 17B, in one embodiment, the SCVBC Gain Control block may use the scaled LINE_IN voltage and Output Voltage DAC setting to determine the appropriate Course Divider ratio derived from the combined divider steps in CP1 and CP2. In this way, settings for the 120 and 90 Volt outputs as a function of world-wide AC input voltages can be achieved. Final regulation of the CP2 output voltage is performed in the switch capacitor regulator where the clock is turned on and off to control the amount of charge delivered to the CP1 and CP2 hold capacitors. The lowest divider ratio required for CP1 and CP2 should be programmed for the CP1 stage to minimize the voltage drop across the high-voltage NMOS switches.

[00112] The CP2 output feeds the primary winding of the Forward Regulator. The final output voltage of the system is set by the following equation:

$$(V_{SET}/XFMR_{RATIO})*dc = V_{OUT}$$

[00113] Where dc is the duty cycle for the Forward Regulator and should be maintained at 0.5 or less to ensure the system transformer does not saturate.

[00114] The SCVBC 32 includes a Dickson charge pump (DCP) 94 (shown in Figures 5 and 6) that may be used to provide a boosted voltage for the gates of the NMOS high-voltage switches. The DCP's may be clocked at a clock rate of 1.6 MHz and generate gate voltages equal to the voltage at the LINE_IN pin plus approximately 18V. In addition, each NMOS

high-voltage switch 90 may include a corresponding level shifter to translate the drive signal from the low-voltage domain to the boosted voltage provided by the DCP's. In one embodiment, this requires dual level shifters, other requirements may only need one level shifter. The input to the level-shifter is 5V and is translated to the 20V domain for use by the SCVBC 32. This same type of level shifter, scaled for output current drive, may be used throughout the Tronium PSSoC 106.

[00115] In one embodiment, as shown in Figures 17A and 17B, the Tronium PSSoC 106 may include a Digital-to-Analog converter (DAC) that provides programmability for the output voltage of the switch capacitor circuit. An R2R current-mode DAC topology digitally scales the bandgap reference voltage to the control voltage required by the switch capacitor circuit to maintain the output voltage programmed by the user. The output voltage range of the DAC is from 120-90V programmed in steps of 118mV by the CP_DAC[7:0] register bits.

[00116] The SCVBC 32 may also include a switch capacitor regulator that includes a comparator and an AND gate that are used to control the charging of the SCVBC. In one embodiment, the comparator's inputs may include the Output Voltage DAC and the scaled version of the CP2 output voltage. For example, if the scaled voltage from the CP2 output is greater than the DAC voltage, the comparator output is low and the 1 KHz CP clock is gated OFF. If the DAC Voltage is greater than the scaled CP2 output voltage, then the comparator output is asserted high and the AND gate enables the clock to charge up the output. In addition, the comparator may be designed with hysteresis to minimize the CP2 output voltage ripple. Moreover, the regulator may run both CP stages in the discontinuous mode; that is, the clock pulses are only present when charging of the 7.5μF hold capacitors is required.

[00117] In the illustrated embodiment, if a stack of CVBD Modules are not used, then large current loads (up to 430mA or more) are easily handled with the use of a hybrid topology

which includes a Switch-Mode Buck Regulator (SWR) 34 and the CVBD Module. The Tronium PSSoC 106 contains the controller for the SWR 34, which makes use of an external (off chip) PMOS switch (which can be an internal to the Chip PMOS or NMOS [with additional Dickson Charge Pumps for gates]) to supply the high-current demands of the load. Since the high-current path is external to the PSSoC, the PSSoC is not required to dissipate the majority of the load current. This improves the overall system efficiency by eliminating the source of additional parasitic losses in the PSSoC due to the ON-resistance of the high-voltage devices. The SWR may be regulated at the same frequency as the CVBD Module, or run at higher (500KHz-1MHz) to very high frequencies, while the CVBD Module is running at lower frequencies in order to remain more efficient. (The CVBD Module can be run at higher frequencies, but with current devices offered in semiconductor platforms today, this increases gate openings/closings, which increases losses).

[00118] In one embodiment, the buck regulator 34 may include the following external (off chip) components: 1. Series High PMOS Switch. The PMOS Switch may be selected for low $R_{DS\text{ON}}$, low input capacitance and a V_{DS} of $> 400\text{V}$; 2. High Voltage Buck Diode with High Volt Breakdown, extremely low leakage and switching current; and 3. Buck Energy Storage Inductor. The inductor must have low ESR and be able to handle appropriate de-rated current. However, these parts, usually depending on the frequency which runs the Buck (the higher the frequency the smaller the value of the parts needed), may be internal devices/components on the chip, and not external. With the application of GaN and/or GaA and Deep Trench Capacitor technologies, as well as technologies which put transformers on the chip, all parts may exist on one chip.

[00119] The Tronium PSSoC 106 may also include a high-frequency oscillator that is divided down to produce a 100 KHz (nominal) clock for use by the Buck Regulator PWM

controller. The 100 KHz clock is dithered with a pseudo random algorithm in the Digital Control block to ensure the suppression of harmonics in the EMI spectrum. This clock is then Pulse Width Modulated to control the on/off time of the external Buck Regulator PMOS/NMOS FET. The 100 kHz clock is converted to a saw-tooth ramp inside the Tronium PSSoC 106 where it is compared to the Error Amplifier output. The Pulse Width Modulated signal from the Comparator output is then applied to the level shifter input to control the on/off time of the external Buck Regulator PMOSFET. The Error Amplifier of the Buck regulator 34 receives feedback from the regulator by scaling the voltage at CP2_OUT with the use of a resistor divider. The voltage feedback signal is then conditioned using internal resistors and capacitors to control the response of the Buck Regulator under all conditions. The resulting transfer function for the regulation servo loop is comprised of multiple poles and zeros to ensure that the regulator output is stable for the full range of load conditions from 50mA to 430mA. The Error Amplifier and PWM Controller for the Buck Regulator are all located in the 5 Volt domain with the final control signal being level shifted to drive the external high-voltage PMOSFET switch.

[00120] The Tronium PSSoC 106 may also include a LDO Buck Regulator 128 that is used to create the high-side voltage necessary to drive the gate of the PMOS / NMOS FET for the Buck regulator 34. This voltage is then used to supply the gate voltage required to drive the external PMOS / NMOS FET. A capacitor is connected for filtering.

[00121] In the illustrated embodiment, the Tronium PSSoC 106 includes a Current Sense Amplifier of the Tronium PSSoC senses the voltage across the external current sense resistor at pins RCSP and RCSN. This voltage is sampled and held by a switched-capacitor difference amplifier and digitized by the on-chip general-purpose ADC. The digital word is then compared against programmed thresholds to enable or disable the Buck Regulator 34 as

needed to optimize efficiency. The output of the Current Sense Amplifier is also monitored for possible fault or alarm conditions such as over current, allowing a digital state machine that controls the current sense feedback to disable the SCVBC 32 to prevent possible damage.

[00122] The Tronium PSSoC 106 may also contain at least two free-running RC oscillators which share a common trim controller including a 16 KHz RC Oscillator and a 9.6 MHz RC Oscillator. The oscillator frequencies can be trimmed using the osc_trim register bits.

[00123] The low-frequency (16 KHz) RC Oscillator is a line-side RC Oscillator that runs continuously after the application of the line voltage at LINE_IN. It is supplied by the LPREG regulator. This oscillator output frequency is divided down to a number, like 1KHz to provide the clock for the SCVBC 32. The oscillator output, in that case, is also used as the reference clock for the Sleep mode Shut-down Timer. A high-frequency (9.6MHz) RC Oscillator provides the master clock for the decoding of the single-wire serial data input. The oscillator 9.6MHz output is divided by 6 to provide the 1.6MHz clock required by the Dickson Charge Pumps in the switch capacitor circuit. It is further divided to provide the clock source for the Buck Regulator and Forward Converter PWM Control Blocks. These 100 KHz clocks are dithered with a pseudo random algorithm by the digital logic to ensure suppression of the harmonics in the EMI spectrum. The oscillator can be enabled with the osc_en register bit and is powered by the LPREG regulator on the line side.

[00124] In the illustrated embodiment, the Tronium PSSoC 106 includes an ultra-low power ADC 118 to digitize a temperature sensor and current sense amplifier analog voltages. These digitized voltages can then be compared by the Digital Control block to disable or restart the analog circuitry. The ADC uses a successive-approximation (SAR) topology for low-power and enhanced INL / DNL performance. The input to the ADC is provided by a multiplexer. The multiplexer can select each of the channels of interest for digitization by the ADC. The

converted sample values are then stored in the ADC_SAMP register for use by the Control State Machine. The ADC uses a low voltage supply and will be disabled when the device is in sleep mode.

[00125] Figure 20 is a schematic illustration of a Proportional to Integral and Differential (PID) Regulator Control circuit 110 that may be used with the Tronium PSSoC 106. In the illustrated embodiment, the Tronium PSSoC 106 includes a PID servo loop 130 to regulate the voltage at the output of the forward converter 96 as load current is drawn from the secondary-side of the external transformer. The PID block includes an Error Amplifier, Saw-tooth Waveform Generator, Comparator and PWM Clock Control Block. The PID loop is designed to regulate the output voltage under heavy fluctuation of load current without triggering any instability.

[00126] A PID Buffer Amplifier receives the feedback to close the Forward regulation loop via the AUTO_ERR input. This is the output of the Opto-Isolator which provides a voltage to the PSSoC which represents the output voltage of the Forward Converter. This voltage is then scaled on the PSSoC with a resistor divider and buffered for the Error Amplifier.

[00127] The Error Amplifier for the Autonomous PID Loop is located on the Tronium PSSoC with the compensation resistors and capacitors on-chip. The Error Amplifier uses the bandgap voltage as the reference for the PID Servo Loop. A Saw-tooth, or other, Waveform Generator provides a clock-based means of pulse-width-modulation (PWM) for the PID Servo Loop. The circuit receives the 100KHz clock from the digital logic and converts it to a saw-tooth waveform of the same frequency to be compared to the output of the Error Amplifier. The outputs of the Error Amplifier and Saw-tooth Waveform Generator are compared by the PID Comparator to generate the PWM clock required to drive the Forward Converter. A Duty Cycle Limiter is provided to ensure that the PWM output provided by the

PID Comparator does not exceed 65%. This output is applied at the FWDOUT pin to drive the external transformer. In normal operation, the PWM duty cycle is limited to a range of 10-65% to avoid saturation of the transformer.

[00128] In one embodiment, the PID Servo Loop is designed to operate at low voltage and deliver a maximum of the required DC current to the load. The regulation can be controlled up to a high percentage of absolute accuracy by using an LC filter on the secondary side and by properly sizing the internal R's and C's of the 3rd order compensation network. The LC filter double pole is given by the following equation: $FLC = 1/2\pi\sqrt{L_1C_4}$.

[00129] The C1 capacitor has a certain ESR (series resistor) which produces a zero. This zero generates a +90 degree phase shift: $FESR = 1/2\pi C_1 R_{ESR}$.

[00130] The compensation loop has a certain bandwidth (F_c) which is approximately 1/10th of the clock rate of the forward converter. The goal of the network is to maintain at least 45 degrees of phase margin at F_c : $\text{Phase Margin} = 180 \text{ degrees} + \text{Phase of loop}$.

[00131] The PID loop has 2 zeroes and 2 poles. The 2 zeroes are necessary to provide 180 degree of phase boost in order to negate the 180 degree of phase loss due to the output LC filter. Both zeroes are placed at about ~50% of the LC filter pole frequency. Two poles are then located at the switching frequency of the converter (100KHz). This allows us to calculate C1, C2, C3, R2 and R3. R1 is set to a reasonable value in order to start the calculation procedure.

[00132] In another embodiment, the PID Servo Loop is designed to operate for multiple output voltages which can be programmed by the user for the required application. The loop may deliver any current, but in this illustrated case 4.5A of DC current to the load with a regulation of up to 0.1% of absolute accuracy. Feedback for the Universal loop is provided by the external microprocessor and voltage sense support circuits, and is input to the Tronium

pin as a serial data stream. A parallel-to-serial conversion is then performed on the digital word which is converted to an analog voltage for application to the error amplifier as shown in Figure 20. Conversion to analog is performed with an on-chip DAC which is updated at the frequency of the incoming data rate. The reference voltage for the PID error amplifier is generated by a second DAC which is programmed by the microprocessor.

[00133] A Digital-to-Analog converter (DAC) generates the analog reference voltage for the PID Control Loop based upon the digital programmed input from the microprocessor. The Digital-to-Analog converter (DAC) as shown is a 10-bit scheme, but can be any number of bits. The DAC may also provide feedback for the PID Control Loop by converting the digital word received from the pin to an analog voltage for input to the loop. The DAC voltage is input to the error amplifier and compared to the analog reference voltage to produce the error voltage for the control loop. The DAC provides updates to the loop at the rate of the incoming data.

[00134] Referring to Figures 17A and 17B, in one embodiment, the Tronium PSSoC 106 may include an on-chip ΔV based temperature sensor that enables the IC to sense the temperature of the die or module. In this example, a general purpose 12-bit ADC is used to digitize the differential voltage. The digitized value is then compared to programmable thresholds in order to shut down or re-enable the Tronium PSSoC depending on temperature concerns.

[00135] In the illustrated embodiment, the Tronium PSSoC 106 provides two modes of operation and four wake-up states (W0-W3) applied upon powerup.

[00136] Startup Mode. During Startup Mode, the Tronium PSSoC controls the startup behavior of the module when power is first applied or when a phone is plugged in (in the case of a charger). When power is first connected to the AC Mains, the rectified and filtered LINE

voltage present at the LINE_IN pin of the IC increases until it reaches its final DC value. The basic support circuits of the Tronium PSSoC are consequently powered up to initiate the power management functions. A timing diagram of an exemplary startup sequence of events is shown in Figure 24, beginning with the application of the LINE_IN voltage at $t=0$.

[00137] The line side has three circuit blocks that are always powered ON: 1. Low-Power Bandgap Reference; 2. Low-Power 5V Regulator (LPREG); and 3. Low-Frequency RC Oscillator. Other circuits may be powered, but in this example it has been reduced to three in this instance in order to draw extremely low stand-by power. These circuits draw power directly from the LINE_IN input with no transformer action to increase the available current. As a result, they are designed for ultra-low power consumption. Alternatively, the transformer could be enabled, but this would reduce efficiency.

[00138] Normal Mode. Following the application of power and the completion of the wake-up states, the Tronium PSSoC 106 will enter the Normal Mode of operation. The Normal Mode of operation is maintained until the voltage/current becomes extinct or passes a low current threshold where typically the microchip inside the battery system begins resisting the current to prevent overload. In the normal mode of operation, the Tronium PSSoC exits the Sleep Mode as a result of the detection of load current. Regulation of the load occurs as the Buck Regulator and SCVBC supply the necessary current. In this mode of operation all Tronium circuits are powered ON and responding to the external stimulus.

[00139] In one embodiment, combining the elements of Normal Mode, Start Up Mode and Sleep Mode the battery can be provided a “bump” charge. In this instance another mode, called Bump Charge Mode would be executed when it is determined by the logic in the chip that a full charge has been executed, meaning a drain from a higher current to lower current over a given period of time. This Bump Charge mode of operation can exist in the state

machine or be enabled/disabled via the I2C interface and would instruct the circuit to “disconnect” several times and begin recharging up to a maximum threshold of approximately 150 milliamps with an interval in between. In this fashion, the battery would be prompted to receive an additional trickle charge to ensure that it is really full, not just stating “full” on the device battery indicator. This will solve the problem where cell phones only charge to about 80-90% of their batteries capacities, thus, over time, while the indicator still registers the battery at 100%, it is really a 100% of 80% of the battery’s capacity, not 100% of 100% of the battery’s capacity. Under the Bump Charge Mode, the Tronium PSSoC digital provides an additional current threshold which is higher than the sleep threshold so that the Sleep Mode function, set out below, is not compromised.

[00140] Sleep Mode. The Tronium PSSoC must use minimal power when connected to the AC Mains power and no charging or power supply function is required. This requires the electrical circuit 22 to have at least two distinct power domains: 1) the line side domain and 2) the primary side domain. The line input side is the domain that must be capable of being powered at all times. There is also a 1.6 MHz RC oscillator that is used for the Dickson Charge pumps. This oscillator remains OFF in the SLEEP mode. The 16 KHz oscillator is used as a countdown timer to wake the Tronium PSSoC when the programmed countdown time has been reached.

[00141] In the illustrated embodiment, the Tronium PSSoC 106 includes a Digital Control block 122 that provides the user the ability to manage numerous aspects of the Tronium application in setup, programmable, normal, test, or evaluation modes of operation. A microprocessor or state machines are provided to monitor the output voltage and current of the Switch capacitor circuit and include configurable registers which provide feature selection and programmability for both the normal mode of operation and the low-current or

‘sleep’ operating mode. Communication interfaces are also provided for external devices as required by the application.

[00142] Figure 21 is a block diagram of a Tronium universal digital control block 132 that may be used with the Tronium PSSoC 106. Figure 22 is a block diagram of a Tronium autonomous digital control block 134 that may be used with the Tronium PSSoC 106. Figure 23 is a flow chart illustrating a method of operating the power circuit 22. Figure 24 is a graphic illustration of a state transitions that may be implemented by the Tronium PSSoC 106.

[00143] Referring to Figure 21, in one embodiment, the Tronium PSSoC 106 includes the universal digital control block 132. The Tronium universal digital control block 132 provides the following functions for control of the Universal Module: Control State Machine, Clock Generator, ADC Controller, Clock Dither LSFR, I2C Interface – Mono or Dual Communication Mode, Programmable Communication Mode, microprocessor Interface, Test/Eval Multiplexer, and/or Register File.

[00144] The Control State Machine or microprocessor/microcontroller determines the proper operating mode of the Tronium Module by monitoring the output current of the switch capacitor circuit. At least two modes of operation are provided including a Sleep mode and a Normal regulation mode. The Control State Machine or microprocessor also provides four states to wake-up the PSSoC, plus the Bump Charge Mode, upon the first application of power, or when exiting from the Sleep mode. In addition, the state machine or microprocessor continually monitors the output voltage current for an over-or-under-current alarm condition.

[00145] Monitoring of the switch capacitor output current is achieved in the analog subsystem or in the microprocessor with the use of a Current Sense Amplifier and an Analog-

to-Digital Converter (ADC). The Digital Control block provides control of the ADC and can perform periodic gain and offset correction for the ADC. The ADC samples are then compared to the programmed digital thresholds for switch capacitor current required by the Control State Machine.

[00146] A Clock Generator provides the clocks required for the analog and digital subsystems, and also enables clock gating to minimize power consumption in the Sleep mode of operation.

[00147] The Digital Control block provides a single-wire serial interface to support configurability of the PSSoC via an external microprocessor; or a multi-wire interface which will support two way communication between the Tronium PSSoC and the microprocessor or state machine. A Clock Dither Linear Feedback Shift Register (LSFR) is included to generate pseudo-random numbers for dithering of the Forward and Buck Regulator PWM clocks. The pseudo-random number is used by the analog subsystem to dither the high-frequency oscillator output. An I2C port is included for manufacturing settings, test, evaluation, updates, health-checks and debug. The Register File which contains configuration registers for device operation can be accessed using the I2C interface. A digital multiplexer is provided to selectively multiplex various internal digital signals to the DIGTST output pin for test purposes.

[00148] Referring to Figure 22, in one embodiment, the Tronium PSSoC includes the autonomous digital control block 134 that provides the following functions for control of the Autonomous Module: the Control State Machine or microcontroller; Clock Generator; ADC Controller; Clock Dither LSFR; I2C Interface; Test Multiplexer; and Register File. The Control State Machine determines the proper operating mode of the Tronium PSSoC 106 by monitoring the output current of the switch capacitor circuit at the CP_OUT pin. Two modes

of operation are provided including a Sleep mode and a Normal regulation mode. The Control State Machine or microcontroller also provides four states to wake-up the IC upon the first application of power, or when exiting from the Sleep mode. In addition, the state machine monitors the output current for an over-under-current alarm condition and Bump Charge Mode.

[00149] Monitoring of the switch capacitor output current is achieved in the analog subsystem with the use of a Current Sense Amplifier and an 12-bit Analog-to-Digital Converter (ADC) is used in this example. The Digital Control block provides control of the ADC and can perform periodic gain and offset correction for the ADC. The ADC samples are then compared to the programmed digital thresholds for switch capacitor current required by the Control State Machine and/or microcontroller.

[00150] A Clock Generator provides the clocks required for the analog and digital subsystems, and also enables clock gating to minimize power consumption in the Sleep mode of operation or Bump Charge Mode.

[00151] A Clock Dither Linear Feedback Shift Register (LSFR) is included to generate pseudo-random numbers for dithering of the Forward and Buck Regulator PWM clocks. The pseudo-random number is used by the analog subsystem to dither the high-frequency oscillator output.

[00152] An I2C port is included for manufacturing settings, evaluation, upgrades, resets, chip health-checks, test and debug. The Register File which contains configuration registers for device operation can be accessed using the I2C interface.

[00153] A digital multiplexer is provided to selectively multiplex various internal digital signals to the DIGTST output pin for test purposes.

[00154] In the illustrated embodiment, the Tronium autonomous digital control block 134 includes a State Machine to determine the proper mode of operation for the Autonomous Module based upon the load current.

[00155] As shown in Figures 23 and 24, the Control State Machine provides four wake-up states (W0, W1, W2 and W3) and two operating modes; a Normal Mode and a Sleep Mode.

[00156] Wake-Up 0 (W0) - When power is applied, the line-side circuits wake up: the bandgap (BG) and the low-power regulator (LPREG) power up. After the LPREG is stable, por_b is released and the system transitions to Wake-Up 1 (W1).

[00157] Wake-Up 1 (W1) - The low-frequency oscillator (LF_OSC) and the gain_control (GAIN_CTRL) get enabled. At the same time, the high-frequency oscillator (HF_OSC) and the charge_pump (CP) get enabled. The CP is set to not regulate. When the LF_OSC is stable, the lf_clk to the digital block is released at which point (a) the 10mS counter starts up and (b) the 1kHz clock to the switch capacitor becomes active. When the 10ms counter expires, the system transitions to Wake-Up 2 (W2).

[00158] Wake-Up 2 (W2) - The switch-regulator (SWR) gets enabled, the CP is set to regulate and the 1mS counter starts. When the 1mS counter expires, the system transitions to Wake-Up 3 (W3).

[00159] Wake-Up 3 (W3) - The forward PID gets enabled and two counters start up: the 20mS counter and the 250mS counter. The following scenarios provoke transitions from this state: a. The 20mS counter expires and the forward PID override option is on: The system transitions to normal mode (NM); b. The 20mS counter expires, the forward PID override option is off and the forward PID stabilizes before the 250mS counter expires: The system transitions to normal mode (NM); c. Sleep mode is not disabled, the forward PID override

option is off and when the 250mS counter expires, the forward PID has not stabilized yet: The system transitions to sleep mode.

[00160] Normal Mode (NM) - The current sense block (CUR_SNS) and the ADC get enabled. If self-calibration is not disabled, the ADC uses the first two samples for gain and offset calibration and signals that the ADC data is okay when the third sample is ready. If self-calibration is disabled, the ADC performs gain and offset correction with the values programmed in the designated registers and signals that the ADC data is okay when the third sample is ready. When the ADC data is okay, the system monitors the current load. The following mutually exclusive conditions, the thresholds for which are programmable, can occur: 1. Over-current condition: The system sets the over-current status bit. If sleep mode is not disabled, the system transitions to sleep mode (SM); and 2. Under-load condition: If the LCSD_EN pin is high and sleep mode is not disabled, the system transitions to sleep mode (SM); and 3. Low-load condition: The system shuts down the SWR when it detects a low-load condition and turns the SWR back when the low-load conditions subsides.

[00161] Sleep Mode (SM) - The system disables the HF_OSC, the CP, the SWR, the forward PID, the CUR_SNS) and the ADC. It also starts the sleep counter, the duration of which is programmable. The default sleep time is approximately 5 seconds, which may be adjusted depending on use application. The system stays in sleep mode if the forward PID previously hadn't stabilized on entry to sleep mode. In this case, the system can be restarted in W1 by triggering the EXT_RST pin or in W0 by removing power. If the forward PID was okay on entry to sleep mode, the system transitions to the W1 state when the sleep counter expires.

[00162] In the illustrated embodiment, the transition between the Normal and Sleep modes of operation is achieved by monitoring the output current of the switch capacitor circuit via

the Current Sense Amplifier and the ADC. In addition, the Control State Machine can disable the SWR Buck Regulator if the load current decreases to the programmed digital threshold. Monitoring of the current and the corresponding mode transitions is illustrated in the diagram of Figure 24.

[00163] Referring to Figures 21 and 22, the digital control block 122 may include a clock generator which generates all the clocks required by the digital subsystem. Three clock domains are provided which are asynchronous to each other, a low-frequency clock domain, a high-frequency clock domain, and a I2C clock domain.

[00164] The Low-Frequency Oscillator in the analog subsystem provides a clock, in the illustrated example, a 16kHz clock for the digital subsystem (lf_clk). In addition to the clock used by the Register File, the Clock Generator derives the following clocks from lf_clk: 1. sys_clk – An 8kHz clock with a 50% duty cycle which clocks the control state machine. 2. adc_gclk – A gated version of sys_clk which clocks the ADC controller. This clock is gated off in sleep mode. 3. lfdiv_clk - A divided clock with a programmable frequency of 1, 2 or 4kHz with a 50% duty cycle to be used in the analog block. This clock is gated off in sleep mode.

[00165] The oscillator can be bypassed in the analog subsystem via the TSTMD0 input to enable the application of a 16kHz clock from the EXT_CLK pin.

[00166] The High-Frequency Oscillator in the analog subsystem provides a 1.6MHz, 50% duty-cycle clock which is further divided by the Clock Generator to create the hfdiv_clk. The hfdiv_clk is programmable via the Register File to provide frequencies of 100, 200, and 400kHz. The hfdiv_clk is also used in the digital for the Clock Dither LFSR and in the analog for the Buck Regulator and Forward PID loops. The clock shuts off in sleep mode when the HF Oscillator is disabled in the analog.

[00167] The I2C Interface uses the clock input at the SCLK pin to control operation of the I2C port. Data rates of up to 100Kbps are supported.

[00168] In the illustrated embodiment, the digital control block 122 also includes an ADC controller which generates the control signals for the general purpose 12-bit ADC in the analog subsystem. It also controls selection of the input to the ADC for conversion via the ADC multiplexer and the ADC_MUX_SEL registers in the CONTROL0 register. The ADC output format is magnitude. The Digital Control block performs a self-calibration routine once when the ADC is first enabled. The Digital Control block can configurably use the gain and offset correction values calculated during the self-calibration, or use the gain and offset correction values written to the ADC_GAIN and ADC_OFFSET registers.

[00169] During the self-calibration routine the offset and gain correction values are determined as described below.

[00170] The Offset is determined first as follows: Set the ADC input mux to select the Reflo reference voltage. Do one ADC conversion. The Ideal value would be 0. Load the ADC Conversion data into the local ADC Offset Correction Register.

[00171] The Gain is determined next as follows: Set the ADC input mux to select the Refhi reference voltage. Do one ADC conversion. The Ideal value would be 4095. Load the local ADC Gain Correction register with the results of $(\text{ADC Conversion data} - \text{Offset Correction})/4095$.

[00172] Following the self-calibration phase, the ADC Conversion values are corrected as follows: $\text{ADC Corrected data} = (\text{ADC Conversion data} - \text{Offset Correction})/4095$.

[00173] The Clock Dither LFSR provides pseudo-random number values to implement dithering on the 1.6MHz clock to mitigate EMI. The LFSR is a 12-bit, maximum-sequence, Galois-type LFSR with the polynomial of $x^{12} + x^6 + x^4 + x + 1$. The dither value is

generated as shown in the table below. The Clock Dither LFSR can be selectively enabled or disabled with the dith_en register bit in the Control register.

[00174] In one embodiment, the Tronium PSSoC digital control block 122 may include a configurable down counter with a range of 0.512 Sec to 16.384 Sec, to implement the Sleep Timer function. The Step size is 512mS. The counter receives its clock from the Clock Generator block where it is divided down from the LF Oscillator clock. The counter is loaded with the sleep_time value programmed in the SLEEP_CTRL register. The counter will count down from this value until it reaches zero at which time it notifies the Control State Machine that the Sleep Timer has expired.

[00175] Figure 25 is a schematic illustration of a communication interface that may be used with the Tronium PSSoC 106. Figure 26 is a schematic illustration of a microprocessor communication protocol that may be used with the Tronium PSSoC 106. In the illustrated embodiment, the communication may be uni-directional or bi-directional. The Tronium PSSoC 106 contains one or more communication interfaces, here described as three interfaces: 1) a microprocessor interface, 2) a single or dual communications/update interface for programming values or returning information to the state machine/micro, and 3) a test/eval interface. The microprocessor interface will be used to communicate with an external microprocessor for certain products, the communications/update interface may update the micro or any of the values internal in the chip. This allows for product configurability and for implementation of a control loop for the Tronium charger. For the Tronium PSSoC, this can be either a read/write or a write only interface, i.e. the microprocessor will or will not be able to read from the PSSoC depending on the type of communication determined: one way or multilateral..

[00176] The test/eval interface will be used in the manufacturing test environment, and for bench evaluation of the Tronium PSSoC. It will allow for write and read access to the on-chip registers. The upgrade, eval, health-check and reset interface will be used to reprogram a chip, change its voltage/current output, or change other reprogrammable portions of the control logic, including thresholds, as well as run scans to help determine if anything is wrong with the chip (health-check).

[00177] Typically, only one interface can be selected at a time, but this can be changed based on the state machine or micro settings. The IF_SEL input pin selects the I2C when '1' and the microprocessor interface when '0'.

[00178] Microprocessor Communication Interface. The Tronium PSSoC may also provide a single-wire serial interface to support configurability of the PSSoC. The interface consists of uni- or multi-directional data input/output. The protocol is shown in Figure 26. All packets will be homogenous in structure and length unless otherwise necessary. Each packet will be a certain number of bits. The packet fields are described below. By adding another wire, a dual communication interface may be had so that the information is multi-directional.

[00179] To support reliable communication, the data may be Manchester Encoded per the IEEE 802.3 Communication Standard. The receiver will then use an over-sampling clock to maintain bit synchronization over the packet. The bit rate will be 600Kbps. The incoming data will be oversampled by a factor of 16 times the bit rate. The oversampling clock is therefore 9.6MHz, and is sourced from an on-chip RC oscillator.

[00180] Start: A single bit whose value is the non-idle state of the signal line. This will be '1' for this application. R/W : A single bit to indicate a read or write request. When '0', the data is written to the selected Tronium register. Note that Tronium only supports write accesses. Addr[4:0]: 5 bits used to address the Tronium configuration registers. Data[9:0]:

10 bits to be written to the selected Tronium register. For cases where the target register is less than 10 bits, data will be right justified. For example when writing to an eight bit register, Data[7:0] will be written to the addressed register location. Idle: A single bit whose value is the idle state of the signal line. This will be '0' for this application.

[00181] Data is transferred MSB first. For example, Addr[4] is transmitted first in time by the host. The Tronium implementation will or will not support read operations of the ASIC registers by the host depending on the programming. The R/W bit is included for future expansion.

[00182] Figure 27 is a schematic illustration of an Inter-Integrated Circuit 136 that may be included in the Tronium PSSoC 106. In the illustrated embodiment, the Tronium PSSoC 106 contains an I2C slave port to support testing of the device. The I2C address is configurable using the I2C_ADDR pins. The I2C_ADDR inputs are compared to the I2C Slave Address bits. The Tronium I2C Bus protocol is shown Figure 27. The I2C Interface supports bit transfer rates up to 100Kbs. The I2C interface runs entirely off the I2C SCLK clock input.

[00183] I2C Write Operations: The Tronium PSSoC supports writes to the Tronium Memory Mapped registers over the I2C Slave port. After receiving an I2C slave address which matches the Tronium I2C address, the next byte, shown as byte1 in Figure 27, will contain the 5 bit address field for the Tronium Register File addresses. The Tronium PSSoC only supports access of one register per command.

[00184] I2C Read Operations: The Tronium PSSoC supports reads from the Tronium Memory Mapped registers over the I2C Slave port. The read operation requires two I2C operations. First, an I2C write to the RDREQ register where the data in byte2 is the Tronium Memory Map address of the register to read. Then an I2C read command will read the requested register. The Tronium only supports accessing one register per command.

[00185] Note that there is a delay between the I2C Write operation and the time at which the RDREQ register is updated. This means that following the I2C Write operation, the I2C Master must wait 400 μ sec before issuing the I2C Read operation. This wait time only applies to the first I2C read following the I2C Write to update the RDREQ register.

[00186] In one embodiment of the Tronium PSSoC the digital memory has intelligence where if the Tronium PSSoC is powering a television, if a television has not been used from a certain time period to another, such as midnight to 7:00 o'clock A.M. for a fixed number of days, the Tronium would always put itself into Sleep Mode during these times to conserve energy and not re-engage in the current sensing routine of the wake-up sequencing.

[00187] In another embodiment of the invention, the Tronium PSSoC is connected through its I2C interface to wireless (like Bluetooth®) or power-line type communication protocols and devices, either external, on-chip or on-module, in order to receive instructions to the state machine or microprocessor. In this fashion there could be “real-time” instructions given to the Tronium about when to go to Sleep Mode, when to wake up, and reset, upgrade or change other preconditions, like over-voltage or PWM regulation. In this fashion, the Tronium PSSoC can have “real-time” sensing and switching of its control mechanism to achieve different levels of frequency, speed, or adapt to low power situations, like in some countries, where the grid typically runs under-voltage during significant portions of the time. In this case the Tronium PSSoC can get real-time information about resets, operation, or shutdowns/restarts, including real-time commands from its owner, even from a cell phone or tablet through the use of cell system to inside the home communication technologies. In this case a person may want to shut down power to certain electronic equipment or electronic devices powered by the Tronium PSSoC while away, and this could be accomplished through the communication interface over wireless or wire communication technologies giving

specific instructions through the I2C interface in the Tronium PSSoC, instructing it to shut down the device, and even pre-setting the time it should wake up.

[00188] In another embodiment of the invention, and when used as a charger or constant supply power, the Tronium PSSoC is small enough to fit into a wall plug attached to the cord, therefore eliminating the need for a charger “box” or laptop “brick”.

[00189] In one embodiment, the Tronium PSSoC 106 has several test structures to support manufacturing, programming, eval, upgrading, health-check, communication, test and bench evaluation. The Tronium PSSoC provides two test registers for controllability and observability of key internal functions and control signals. The TEST_CTRL0 register provides the user with the ability to selectively enable, disable, or override the control of individual analog circuit functions in the Tronium PSSoC to provide an alternate method of control should the Control State Machine need to be bypassed. The TEST_CTRL1 register provides the ability to multiplex internal analog and digital signals to the ANATST and DIGTST output pins for test purposes.

[00190] Many modifications and variations of the present invention are possible in light of the above teachings. The invention may be practiced otherwise than as specifically described within the scope of the appended claim.

[00191] Figure 30 is a connection diagram that may be used with the Tronium PSSoC 106. Figure 31 and 32 are additional schematic illustrations of the Tronium PSSoC 106. Figure 33 is a flow chart of an algorithm for a low-current detection and an error detection that may be used with the Tronium PSSoC 106. Figures 34 and 35 are schematic illustrations of the power circuit 22 including the Tronium PSSoC 106. In the illustrated embodiment, the Tronium PSSoC 106 is an advanced power controller integrated circuit (IC). The Tronium PSSoC 106 and corresponding integrated Module provide a low-cost, highly efficient means

to convert the AC line voltage present at a typical home or business electrical outlet to a reduced regulated DC voltage for consumer electronic applications. Typical applications include, but are not limited to, charging systems for cell-phones, tablets or other handheld devices, USB power conversion, power supplies for consumer, medical and industrial devices, and many other possible uses.

[00192] The Tronium PSSoC provides high efficiency, low noise, and low EMI with the configurations and features as set out above. In addition, the AC-DC, DC-DC converter has high power density, low cost, and electric isolation. These advantages are achieved from integrating otherwise discrete parts onto the chip, utilization of the Switch Capacitors Voltage Breakdown scheme and primary side sense/control. Thus, the key features of the Tronium PSSoC are as follows: Support for wide range of available AC input voltages and frequencies; Programmable Output Voltage and auto-detect of input voltage with automatic setting to configure to the input voltage for proper operation; High-Efficiency switch capacitor circuit for AC-DC, DC-DC Conversion; PID (or similar) Regulation Control Loop for High Accuracy; Digital State Machines for Current and Temperature Monitoring; Ultra-Low Power Dissipation for Idle (Vampire) Mode of Operation; Opto-Isolated Microprocessor Interface for Configuration and Control; and Communications Port for Manufacturing Test.

[00193] The analog and digital interfaces, inputs, and outputs of the Tronium PSSoC are able to withstand Voltages and Currents that are outside of the typical operating range. The unit is also operable over a wide temperature range and provide ample ESD immunity.

[00194] The Tronium PSSoC provides inputs and outputs to interface to the outside world and external circuitry. These include but are not limited to: power inputs, power outputs, low current shutdown enable inputs, mode selection input, intermediary connections for which

external circuitry is required, test connections, communications connections, power outputs, regulator outputs, connections for PID based PWM, FET drive outputs, and feedback inputs.

[00195] The Tronium PSSoC is an advanced power controller integrated circuit designed to provide output voltage regulation with high-efficiency and high accuracy. The advanced features of the Tronium PSSoC provide the user with a multi-purpose device which can be used in a large variety of applications. Programmable output voltages are possible with the Tronium PSSoC, with little or no loss of efficiency across a variety of current load conditions.

[00196] The Tronium PSSoC uses a proprietary switch capacitor circuit system to maintain high-efficiency regardless of the load voltage or current. When no current is being drawn by the load, the device will enter a low-current mode of operation to minimize the traditional ‘vampire’ current required to stay awake as well as scale the number of active subsystems to the load in order provide high efficiencies across a wide loading range.

[00197] A top-level block diagram of the Tronium PSSoC is shown below, and is comprised of the following major circuit blocks: High-Voltage Multi-Stage / Multi-Branch switch capacitor voltage breakdown circuit; PID (or other switched mode control scheme), Regulator Control Block for PWM Control of Secondary Transformer; Current and Temperature Sense Blocks; ADC or Comparator for Voltage and Current Monitoring; DAC, PWM, or other signal for Feedback Control; Digital Control Block for Voltage & Current Monitoring State Machines; Communications Interfaces; and Power Management for On-Chip Voltage and Current Generation and other power requirements.

[00198] Power Management. The power management block provides necessary power rails and references to the rest of the IC. It is comprised of voltage regulators, current references and voltage references. It also includes all necessary buffering and amplification needed for

IC usage. The power management system also contains a reset controller which manages the shut down and start up of the system on power cycle.

[00199] Switch Capacitor Voltage Breakdown Circuit. The switch capacitor voltage breakdown circuit of the Tronium PSSoC works as a near lossless voltage divider. It divides the rectified DC voltage present at the LINE_IN pin to a reduced voltage at the CP2_OUT pin for use by the external transformer and secondary voltage control loop. An external transformer can then further reduce this voltage to the desired application voltage as a function of the primary-to-secondary windings ratio, as well as provide isolation if desired.

[00200] The switch capacitor circuit is configured as a cascade of multiple identical stages with multiple parallel branches as shown below. The parallel branches are switched in or out of the circuit based upon the load current that is sensed by the current sense amplifier. This enables the switch capacitor circuit to maintain high efficiency across the wide range of load currents. In the diagram below, the number of parallel subsystems is 4 comprising two stages. The number of parallel systems and conversion stages may change so that the system is best optimized for a particular input/output voltage ratio or power requirement.

[00201] The switch capacitor circuit uses on-chip or off-chip fly-back capacitors to maximize power efficiency and external hold capacitors to minimize the voltage ripple. These capacitors are connected to the CP1_OUT and CP2_OUT pins, respectively, for the outputs of the 1st and 2nd stages of the switch capacitor circuit. All stages are clocked by an oscillator, or each stage may have its own dedicated oscillator. Each branch of the switch capacitor circuit may have an independent enable.

[00202] The output voltage is programmable over the range of voltages for a given range of applications with high resolution with the use of a digital-to-analog converter (DAC). The

digital control of this DAC enables multiple voltages to be programmed at the CP2_OUT pin to obtain the desired final output voltage required for the target application.

[00203] The switch capacitor circuit output settings of the other switch capacitor circuit stages can be determined by the user or derived from the measured AC line V_{in} , so that an optimum ratio between V_{in} and V_{out} can be realized.

[00204] Regulation of each switch capacitor circuit stage is obtained with the use of an Operational Trans-conductance Amplifier (OTA). The OTA regulates the current applied to the fly-back capacitors in each stage as a function of the difference between the output voltage and the input reference voltage. The input reference voltage may be programmed, derived, or fixed depending on application.

[00205] Voltage measurement of the incoming line may be taken in order to optimize the switch capacitor circuit settings. This setting calculation can be performed on-chip, off-chip, or on the fly through appropriate on chip circuitry, so that the outputs of each switch capacitor circuit stage are in the most optimized ratios.

[00206] Current Sense Amplifier. The current sense amplifier in the Tronium PSSoC allows the device to measure current as part of the feedback loop as well as error reporting. The current can be measured by an ADC or through a series of comparators with varying thresholds.

[00207] PID Control Loop. The Tronium PSSoC provides a Proportional-to-Integral-and-Differential, PID, loop or alternative PWM control circuit in order to drive the primary side of the isolation transformer, a buck, a boost, or a buck-boost circuit. This circuit is to provide post regulation and isolation if necessary.

[00208] Feedback to the PID loop can be from either a digital source for example, but not limited to, a serialized ADC stream or an analog signal, both of which are dependent on the

output of the circuit. This feedback can provide information relating regulated output current or voltage.

[00209] Temperature Sensor. An on-board temperature sensor may be realized so that ample protection from over temperature situations exists. Actions taken to protect against thermal damage may include de-rating of output power and complete shut-down of output.

[00210] Control Circuitry. The Tronium PSSoC provides for control whether through digital means or through analog circuitry. Through this control circuitry, the IC is able to set and change existing control thresholds and control points as well as enable / disable specific functionality. This can be done through registers or fuses in a digital interface situation or through applied voltages to analog pins should analog setting be desired.

[00211] If the feature is enabled, the Tronium PSSoC allows the output of the system to be disabled or de-rated. This can take place by turning off the PWM, switch capacitor circuit, or through de-ration of either or both subsystems. The output can be disabled as a result of error detection or as a result of a low output current or output power situation such as arises when a connected device that includes a battery is done charging the battery and the Tronium PSSoC is only providing power to the non-battery charging functionality. Once the Tronium PSSoC has entered into a low current shut-down state, it will intermittently re-apply output power to the end device in order to check whether or not it now requires power above certain threshold indicating that the battery now needs further charge. The time spent in the off state may be adjusted for varying applications. Figure 33 illustrates an example of the algorithm for low-current detection and error detection.

[00212] The Tronium PSSoC provides multiple interfaces to external circuitry so that devices may control and configure the IC. These interfaces can include, but are not limited to, SPI, I2C, UART or other synchronous / asynchronous serial stream. Alternate encoding

to NRZ formats can also be realized to optimize the size and part count of external circuitry. Likewise these communications interfaces can be connected to isolation devices in order to enable communications from an isolated region should this be desired.

[00213] Clock Generator. The Tronium PSSoC may have the ability to generate its own internal clocks which may also include frequency controlling circuits including, but not limited to: internal RC oscillators, PLLs, FLLs, clock dividers, VCOs, and trimming circuitry. Additionally the clocking tree may implement intentional clock jitter or other means to vary the clock edge placement in order to minimize the effects of the clocking on radiated and conducted EMI.

[00214] Module Description. The Tronium PSSoC is intended for use as a power supply device which is to be incorporated into a module which accepts AC power in, converts this power to a DC Voltage, and supplies this power external devices. The module can take many forms, which can include either analog or digital feedback of the output to the ASIC, or the ASIC can operate in open loop mode with no feedback. Additionally, module circuitry can be constructed so that individual outputs (should there be a plurality of connected outputs) can be discretely monitored and controlled. The sensing capabilities within the module are meant to supplement or replace the measurements taken by ASIC depending on the application and regulation requirements.

[00215] Figure 34 is a schematic of the power circuit 22 including Digital Feedback module with isolation and discrete output sensing. Figure 35 is a schematic illustration of the power circuit 22 including Analog Feedback module with linearization of feedback isolation. These represent an analog feedback version and a digital feedback version. Both of these diagrams also indicate an isolation transformer as part of the design. This component may or may not be included in the module depending on the requirements of the application. Both examples

describe a synchronous rectification scheme, however an asynchronous system could also be realized.

[00216] Digital Feedback Description. The digital feedback module includes a microcontroller, standalone ADC, or secondary ASIC in order to monitor the output voltage and to allow very precise measurements to be taken at the output connection. This allows the module to compensate for component losses, temperature, and other variables that may cause variance in the output voltage. This data is then formatted and sent back to the ASIC to provide the digital feedback stream. Current sensing and output enable transistors are also shown so that should a multitude of outputs be connected to the module with individual sensing at each. In this manner the low power shut-off functionality described in the ASIC description could be applied to individual loads even though the power is shared.

[00217] Analog Feedback Description. If for cost or other reasons it is desired to use an analog feedback system, the Tronium PSSoC allows this to be realized through the analog feedback input. In the embodiment shown, the current through an opto-isolation LED is proportional to the output voltage. The circuit is designed so that the voltage at the analog feedback pin on the IC is at nominal voltage when the output voltage is at the target output. Current monitoring is performed by the IC at the primary side of the transformer, and the measurements are scaled by the turns ratio of the transformer.

[00218] Figure 36 is a schematic illustration of a Level Shifter circuit that may be used with the power circuit 22. In one embodiment, the switch capacitor voltage breakdown circuit 32 and the buck regulator 34 relies on a level shifter that can take a static CMOS level digital signal and voltage shift the signal to various levels. This is done to properly drive the gates of high voltage switches both off and on Tronium PSSoC chip. The level shifter is comprised of a differential pair with a static dc current bias current. The diff pair amplifies the CMOS level

signal and then shifts to a higher rail. There are cascodes used in the signal path to avoid any transistor breakdown. The level shifter can be disabled via a p-channel switch to avoid any static current drain. Once the signal is shifted to another rail, it is further amplified converted to single ended and then converted back to static CMOS levels to drive high voltage switches.

[00219] Figures 38 and 39 are additional schematic illustrations of the power circuit 22. In one embodiment, the forward converter transformer 102 may include a tertiary winding 152 (shown in Figures 39 and 40) that may be used as a replica of the secondary side for current sensing. For example, some Tronium PSSoC applications can run at low voltages and a self driven synchronous rectifier may not be a reliable solution. More gate voltage would ensure a robust system. For example there will be an application for a 1.8 Volt DC output. Assume a 12:1 transformer and a 43 Volts CP_DAC2 setting, 3.6 VDC is the peak voltage on the secondary winding. A 12:2 auxiliary winding can be used to produce 7.2 Volts of gate drive for the synchronous rectifier FETs. The transformer design may include the auxiliary winding 152 on the secondary side to support this requirement.

[00220] Figure 41 is a schematic diagram of the power circuit 22 including a DC-DC conversion circuit. In the illustrated embodiment the power circuit 22 includes the switch capacitor voltage breakdown circuit 32 for receiving a DC input power signal and generating a DC output power signal having a lower voltage level. In one embodiment, the power circuit 22 may also include the switch-mode buck regulator 34 coupled in parallel with the SCVBC 32. The high-efficiency switch capacitor voltage breakdown circuit 32 includes a pair of flyback capacitors electrically coupled in parallel, and a plurality of switch assemblies that are electrically coupled to each of the pair of flyback capacitors. In one embodiment, the gates between the capacitors are shared. The switch assemblies may be operated to selectively deliver an input DC power signal to each of the pair of flyback capacitors during a

charge phase, and to selectively deliver an output DC power signal to an electronic device during a discharge phase that has a lower voltage level than the input DC power signal. At least one switch assembly may include an N-channel MOSFET switch and a level shifter for delivering a control signal to the N-channel MOSFET switch. In addition, a dickson charge pump may be coupled to the level shifter to receive the input DC power signal and generate an output power signal having a higher voltage level than the input DC signal. The output power signal is delivered to the level shifter for use in operating N-channel MOSFET switch (or closing for other types of MOSFETs). In addition, the switch capacitor voltage breakdown circuit may include a control circuit that includes a voltage sensing circuit for sensing a voltage level of the input DC power signal and a gain controller configured to select a gain setting of the switch capacitor voltage breakdown circuit as a function of the sensed voltage level and operate each of the plurality of switch assemblies as a function of the selected gain setting.

[00221] This written description uses examples to disclose the invention, including the best mode, and also to enable any person skilled in the art to practice the invention, including making and using any devices or systems and performing any incorporated methods. The patentable scope of the invention is defined by the claims, and may include other examples that occur to those skilled in the art. Other aspects and features of the invention can be obtained from a study of the drawings, the disclosure, and the appended claims. The invention may be practiced otherwise than as specifically described within the scope of the appended claims. It should also be noted, that the steps and/or functions listed within the appended claims, notwithstanding the order of which steps and/or functions are listed therein, are not limited to any specific order of operation.

[00222] Although specific features of various embodiments of the invention may be shown in some drawings and not in others, this is for convenience only. In accordance with the principles of the invention, any feature of a drawing may be referenced and/or claimed in combination with any feature of any other drawing.

CLAIMS

What is claimed is:

1. An electrical circuit for providing electrical power for use in powering electronic devices, comprising:

a primary power circuit adapted to be electrically coupled to an electrical power source, the primary power circuit configured to receive an alternating current (AC) input power signal from the electrical power source and generate an intermediate direct current (DC) power signal, the intermediate DC power signal being generated at a first voltage level that is less than a voltage level of the AC input power signal; and

a secondary power circuit electrically coupled to the primary power circuit, the secondary power circuit configured to receive the intermediate DC power signal from the primary power circuit and deliver an output DC power signal to an electronic device, the output DC power signal being delivered at an output voltage level that is less than the first voltage level of the intermediate DC power signal.

2. An electrical circuit in accordance with claim 1, the primary power circuit including a rectifier circuit configured to receive the AC power input signal from the electrical power source and generate a rectified DC power signal, the rectified DC power signal having a voltage level that is approximately equal to the voltage level of the AC input power signal.

3. An electrical circuit in accordance with claim 2, the rectifier circuit including a full-wave bridge rectifier.

4. An electrical circuit in accordance with claim 2, the primary power circuit including a switch capacitor voltage breakdown circuit coupled to the rectifier circuit for

receiving the rectified DC power signal from the rectifier circuit and generating the intermediate DC power signal.

5. An electrical circuit in accordance with claim 4, the switch capacitor voltage breakdown circuit including:

a pair of flyback capacitors electrically coupled in parallel;

a plurality of switch assemblies electrically coupled to each of the pair of flyback capacitors, the plurality of switch assemblies being operated between a charge phase and a discharge phase; and

a hold capacitor electrically coupled to each of the pair of flyback capacitors, the plurality of switch assemblies being operated to selectively deliver the rectified DC power signal to each of the pair of flyback capacitors during the charge phase and to selectively deliver the intermediate DC power signal to the hold capacitor during the discharge phase.

6. An electrical circuit in accordance with claim 5, at least one of the switch assemblies including:

a N-channel MOSFET switch;

a level shifter coupled to the N-channel MOSFET switch for delivering a control signal to the N-channel MOSFET switch; and

a dickson charge pump coupled to the level shifter, the dickson charge pump configured to receive the rectified DC power signal and generate an output power signal having a voltage level that is greater than the voltage level of the rectified DC power signal, the output power signal being delivered to the level shifter for use in operating N-channel MOSFET switch.

7. An electrical circuit in accordance with claim 5, the switch capacitor voltage breakdown circuit including a control circuit coupled to each of the plurality of switch assemblies, the control circuit including:

a voltage sensing circuit for sensing a voltage level of the rectified DC power signal;
and

a gain controller configured to select a gain setting of the switch capacitor voltage breakdown circuit as a function of the sensed voltage level and operating each of the plurality of switch assemblies as a function of the selected gain setting.

8. An electrical circuit in accordance with claim 4, the primary power circuit including a buck regulator circuit electrically coupled in parallel with the switch capacitor voltage breakdown circuit, the buck regulator circuit for receiving the rectified DC power signal from the rectifier circuit and generating the intermediate DC power signal.

9. An electrical circuit in accordance with claim 8, the buck regulator circuit including a regulator switch assembly coupled to a voltage reduction circuit, the voltage reduction circuit including a diode, an inductor, and a capacitor, the regulator switch assembly being operated to selectively deliver the rectified DC power signal to the voltage reduction circuit.

10. An electrical circuit in accordance with claim 9, the buck regulator circuit including a control circuit for providing a pulse-width modulated control signal to the regulated switch assembly to selectively deliver the rectified DC power signal to the voltage reduction circuit, the control circuit including:

a voltage sensing circuit for sensing the first voltage level of the intermediate DC power signal; and

a regulator controller for generating the pulse-width modulated control signal as a function of the sensed first voltage level, the regulator controller configured to adjust a duty cycle of the control signal being delivered to maintain the voltage level of the intermediate DC power signal at a predefined voltage level.

11. An electrical circuit in accordance with claim 1, the secondary power circuit including a forward converter circuit including a primary voltage reduction circuit and a secondary voltage reduction circuit, the primary voltage reduction circuit configured to receive the intermediate DC power signal from the primary power circuit and deliver a secondary DC power signal to the secondary voltage reduction circuit, the secondary DC power signal having a voltage level that is less than the voltage level of the intermediate DC power signal, the secondary voltage reduction circuit configured to receive the secondary DC power signal and generate the output DC power signal being delivered to the electronic device.

12. An electrical circuit in accordance with claim 11, the primary voltage reduction circuit including a transformer, a primary side of the transformer being coupled to the primary power circuit and a secondary side of the transformer being coupled to the secondary voltage reduction circuit.

13. An electrical circuit in accordance with claim 12, the secondary voltage reduction circuit including a pair of diodes, an inductor, and a capacitor.

14. A power module for providing electrical power for use in powering electronic devices, comprising:

a rectifier circuit configured to receive an AC power input signal from an electrical power source and generate a rectified DC power signal;

a switch capacitor voltage breakdown circuit and integrated circuit controller coupled to the rectifier circuit for receiving the rectified DC power signal from the rectifier circuit, the integrated circuit controller for sensing the voltage level of the AC power input signal and adjusting the gain of the switch capacitor voltage breakdown circuit as a function of the sensed voltage level to generate an intermediate DC power signal; and

a forward converter circuit coupled to the switch capacitor voltage breakdown circuit, the forward converter circuit including a transformer for receiving the intermediate DC power signal and generating an output DC power signal being delivered to an electronic device.

15. A power module in accordance with claim 14, including a buck regulator circuit electrically coupled in parallel with the switch capacitor voltage breakdown circuit, the buck regulator circuit including a regulator switch assembly for receiving the rectified DC power signal from the rectifier circuit and generating the intermediate DC power signal.

16. A power module in accordance with claim 15, the integrated circuit controller including a buck regulator control circuit for providing a pulse-width modulated control signal to the regulated switch assembly.

17. A power module in accordance with claim 14, the forward converter circuit including a transformer switch assembly coupled to the transformer primary side, the integrated circuit including a transformer control circuit for selectively operating the transformer switch assembly to maintain a voltage level of the output DC power signal.

18. A power module in accordance with claim 14, the switch capacitor voltage breakdown circuit including:

a pair of flyback capacitors electrically coupled in parallel; and

a plurality of switch assemblies electrically coupled to each of the pair of flyback capacitors.

19. A power module in accordance with claim 18, at least one of the switch assemblies including:

a N-channel MOSFET switch; and

a dickson charge pump coupled to the N-channel MOSFET switch.

20. A power module in accordance with claim 18, wherein the N-channel MOSFET is formed within the integrated circuit.

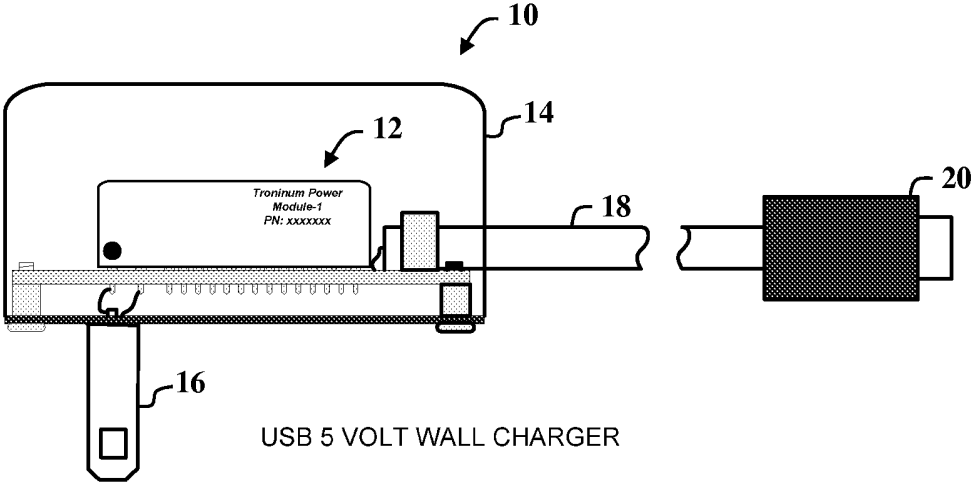


Figure 1

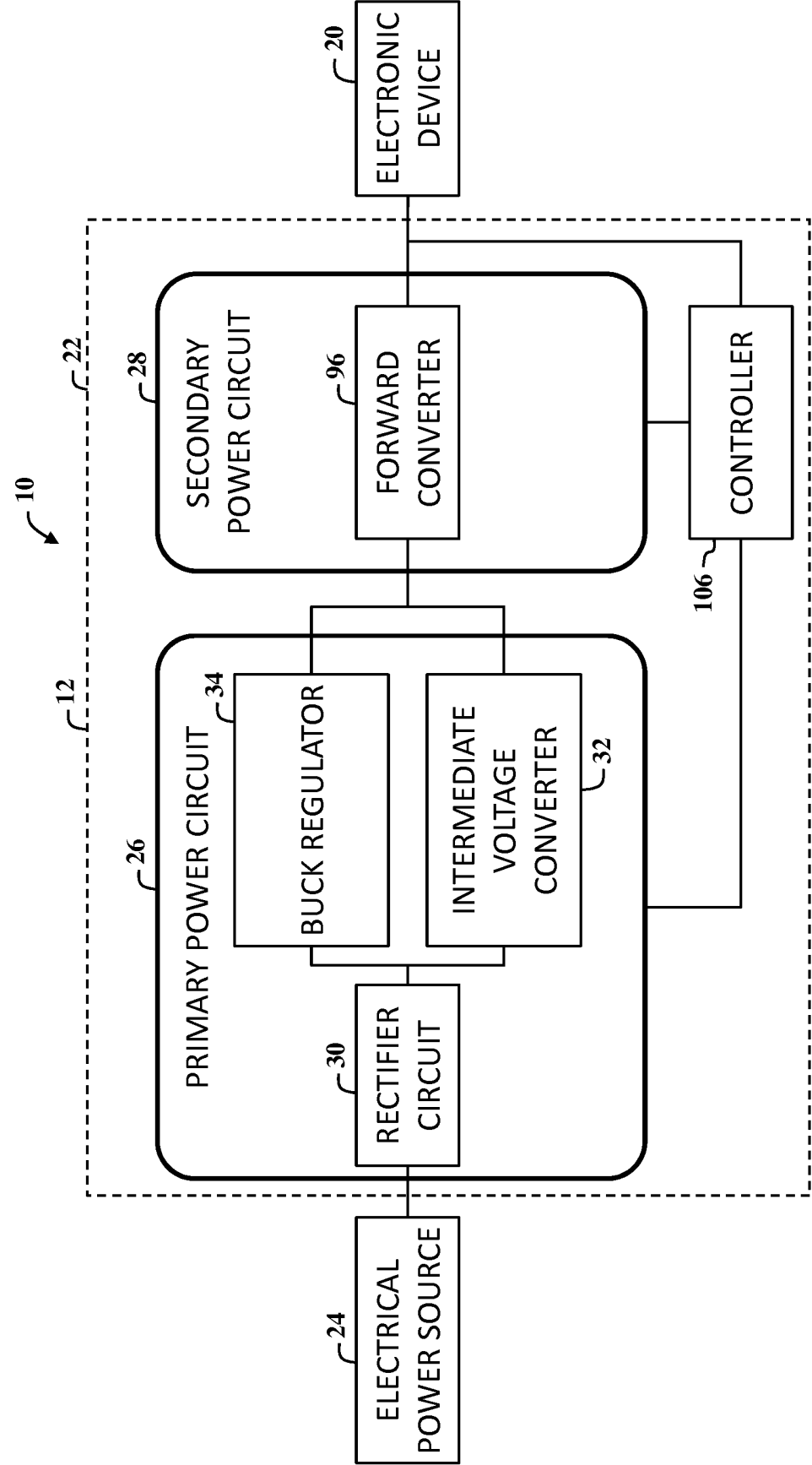


Figure 2

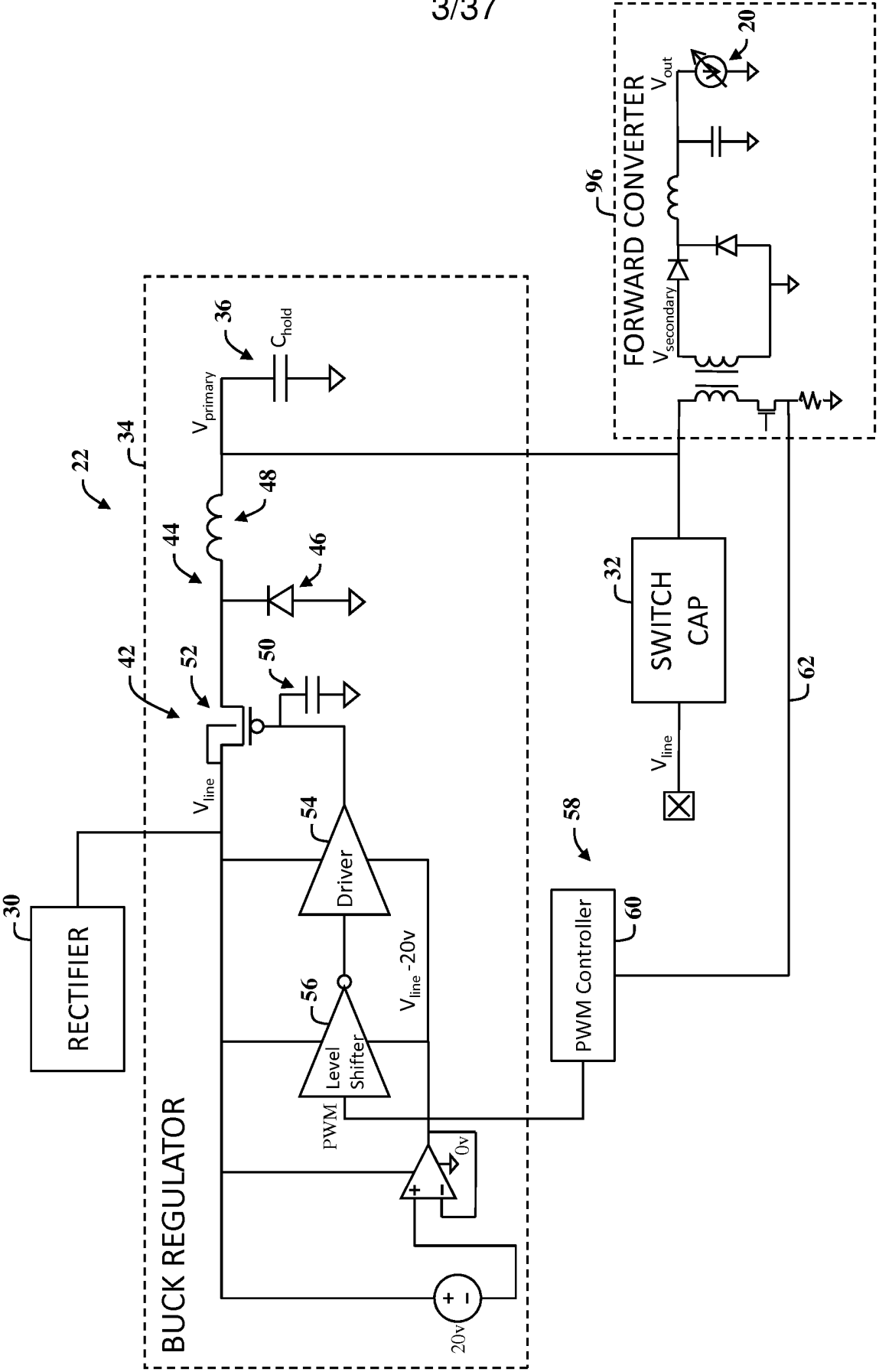


Figure 3

4/37

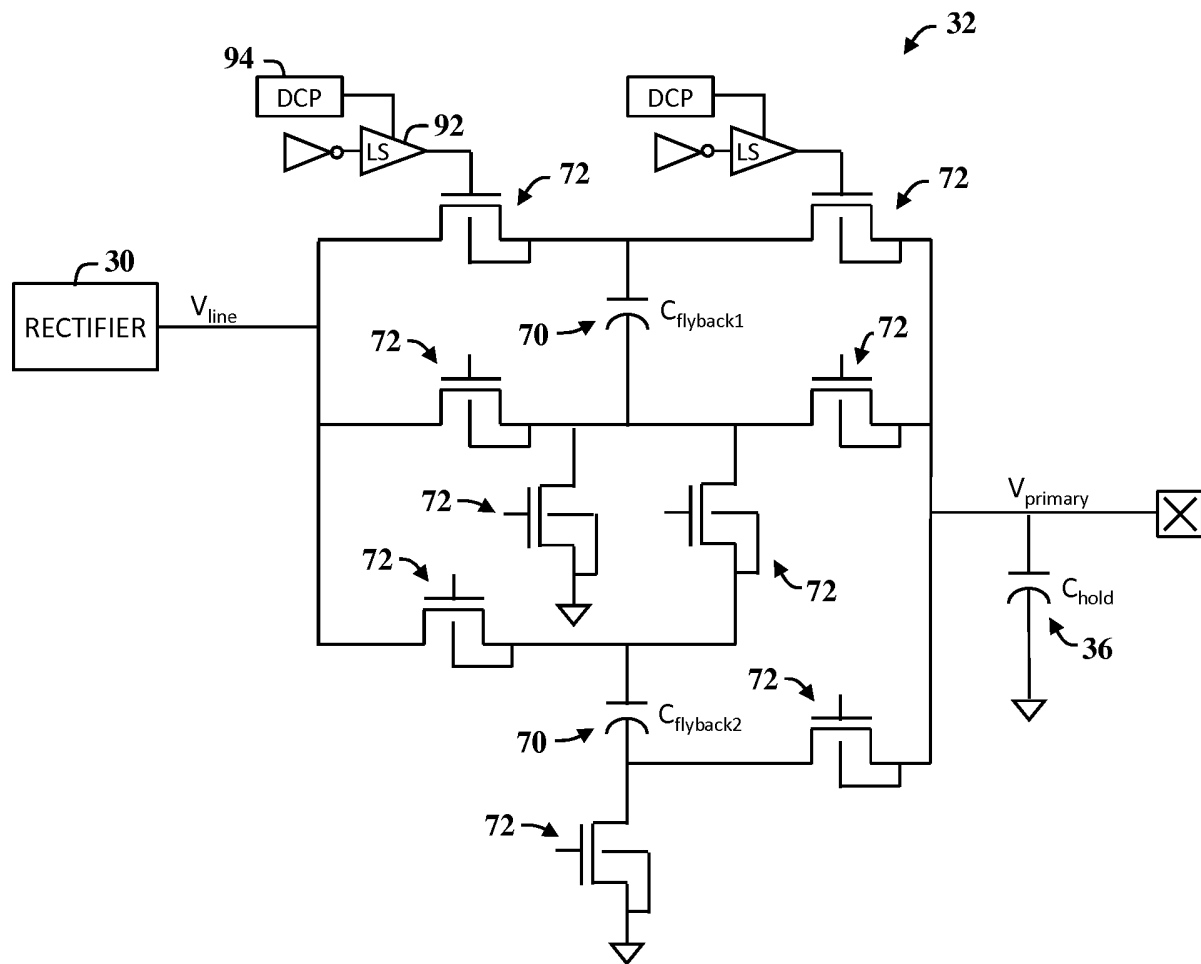


Figure 4

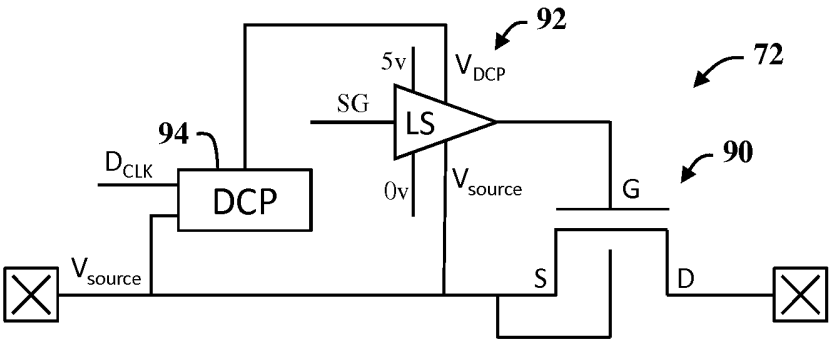


Figure 5

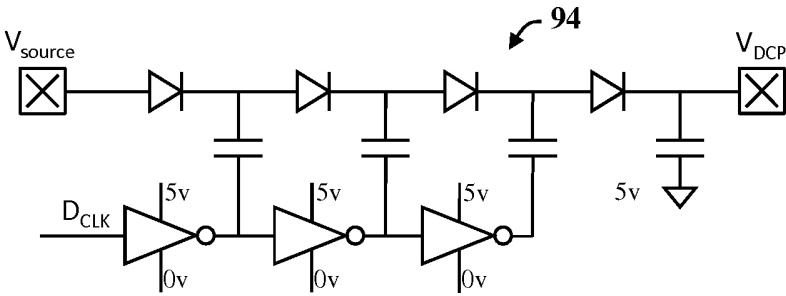


Figure 6

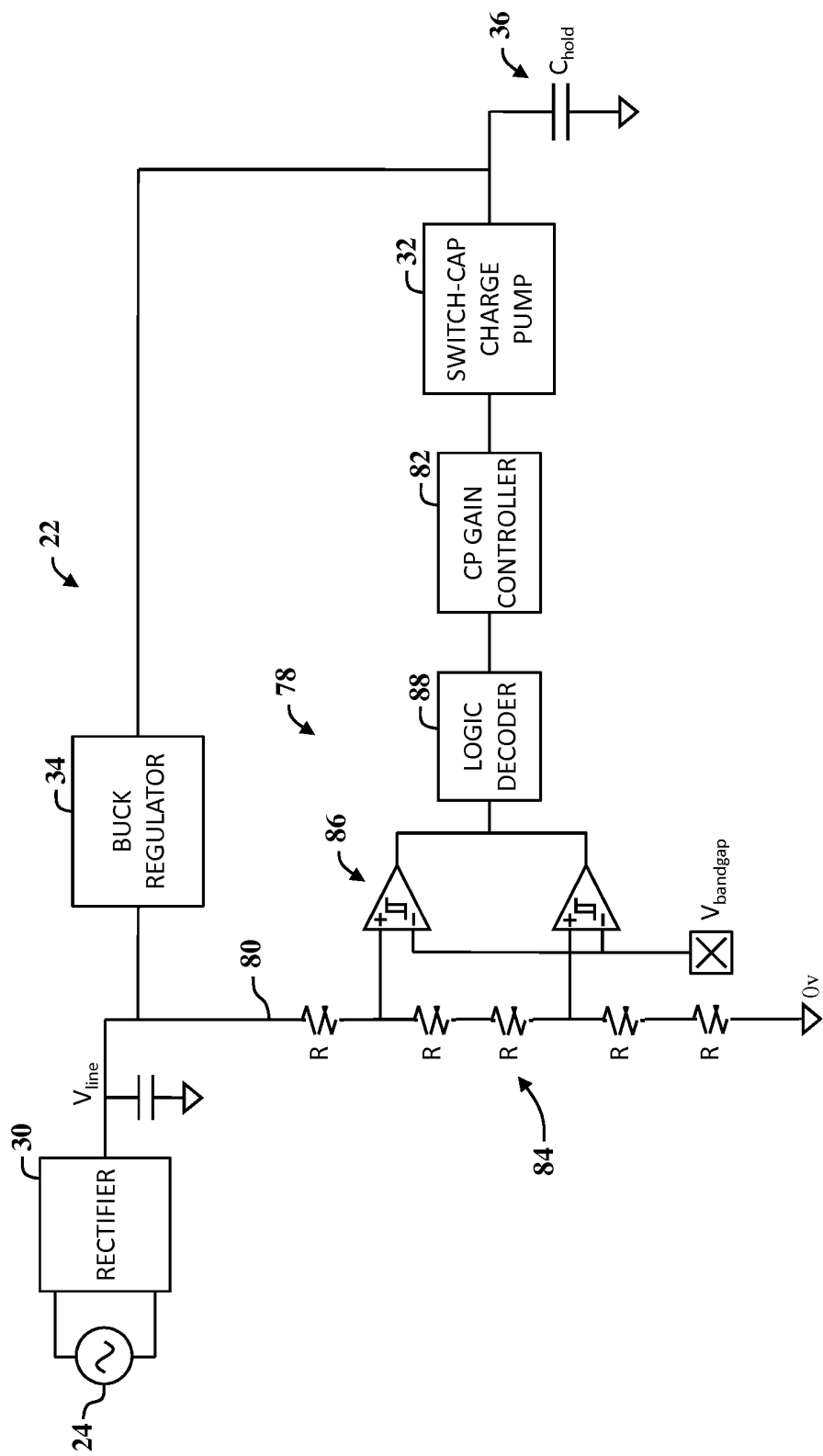
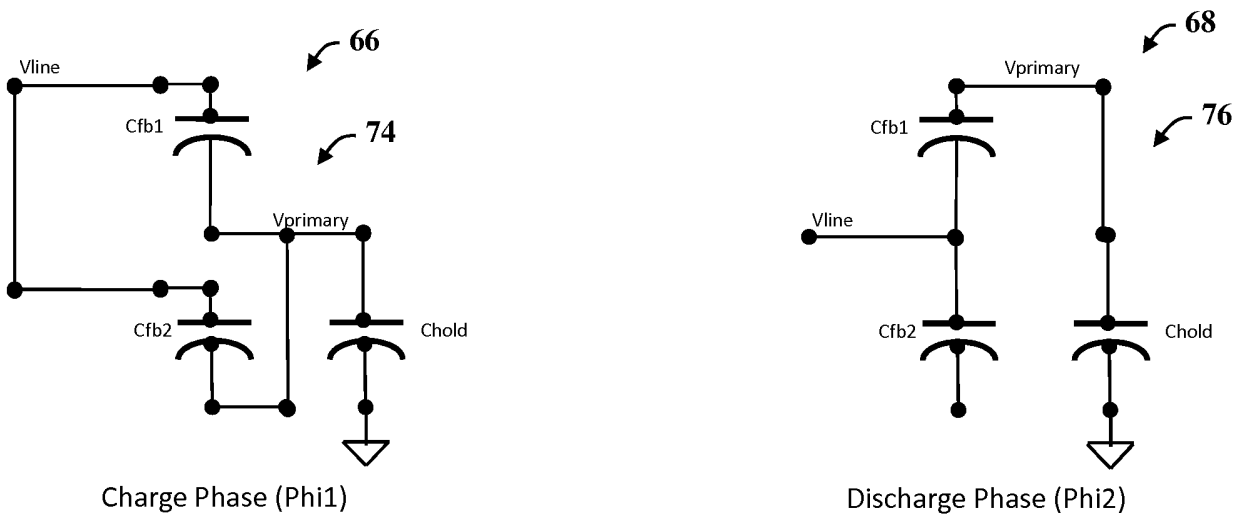


Figure 7

Switch Name	Phase 1	Phase 2 G=1/2	Phase 2 G=2/3	Phase 2 G=1
S1	On	Off	Off	Off
S2	Off	On	On	On
S3	Off	Off	Off	On
S4	On	Off	Off	Off
S5	Off	On	Off	Off
S6	Off	Off	On	Off
S7	On	Off	Off	On
S8	On	Off	Off	Off
S9	Off	On	On	Off

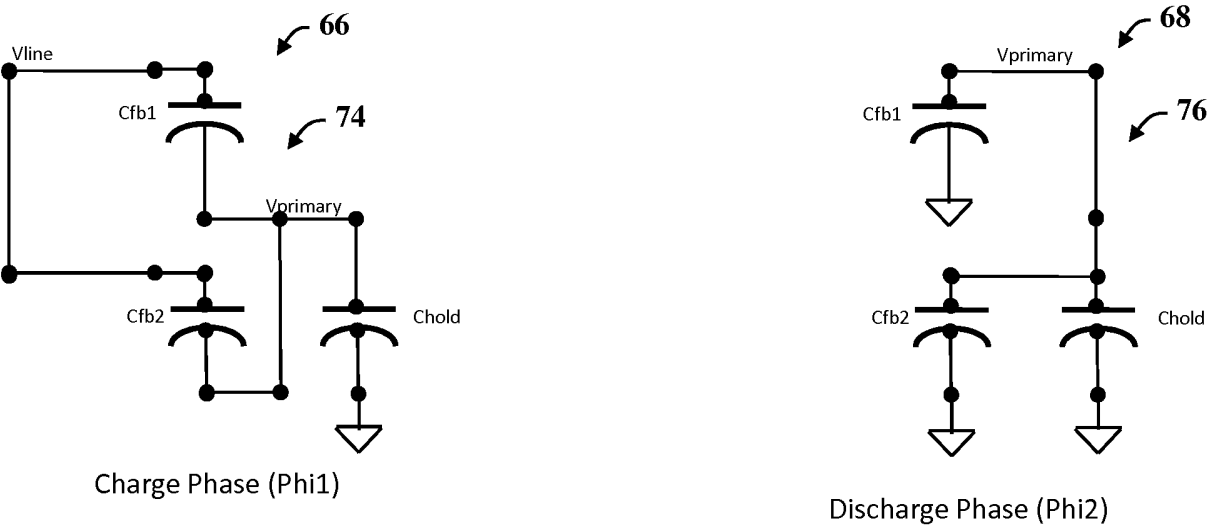
Figure 9



Switched Capacitor Gain: 1x

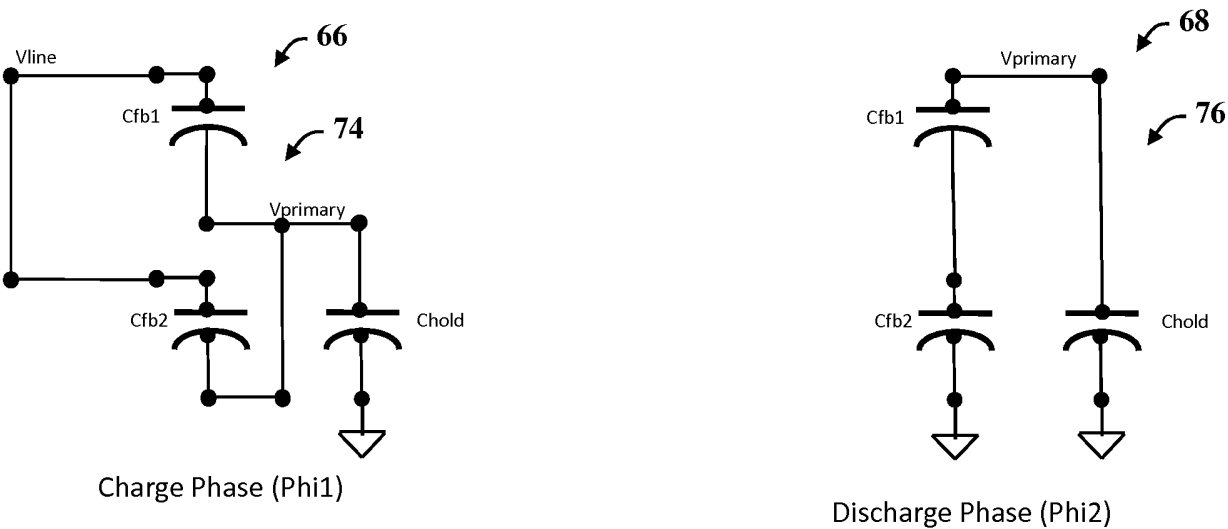
Figure 10

9/37



Switched Capacitor Gain: $1/2x$

Figure 11



Switched Capacitor Gain: $2/3 x$

Figure 12

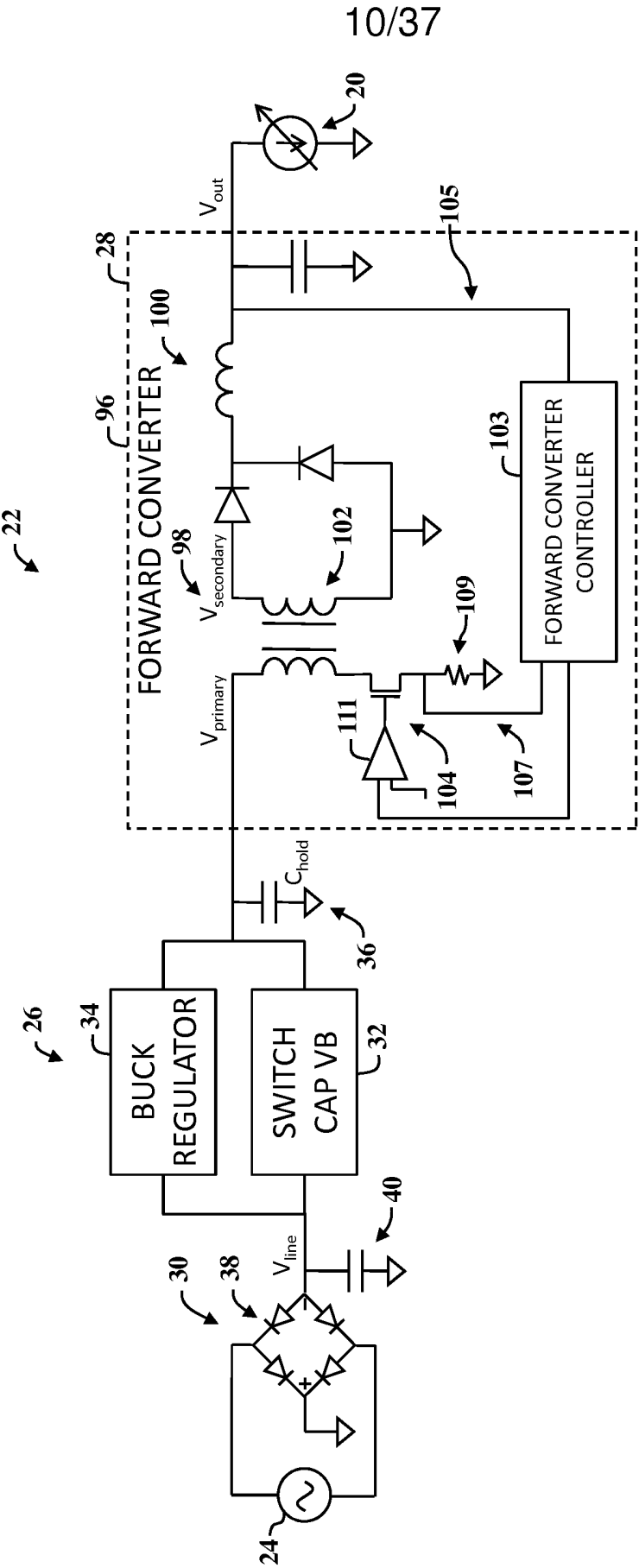


Figure 13

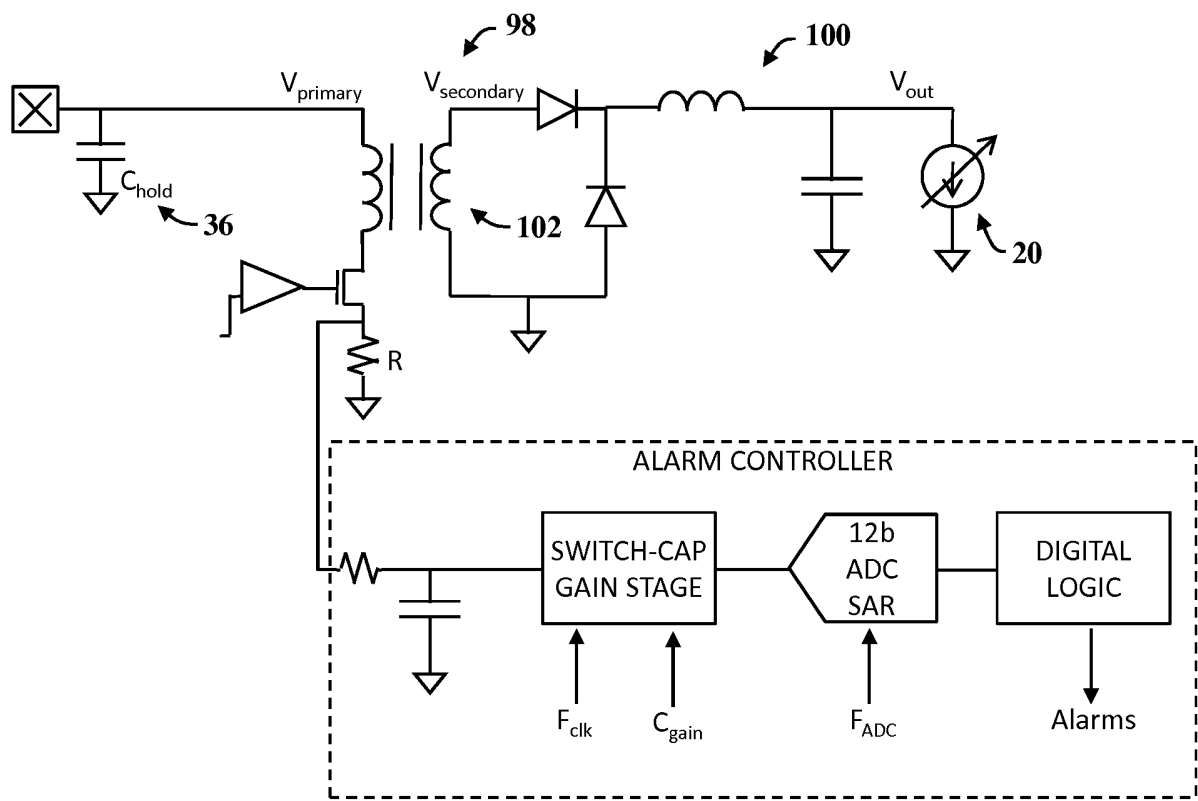


Figure 14

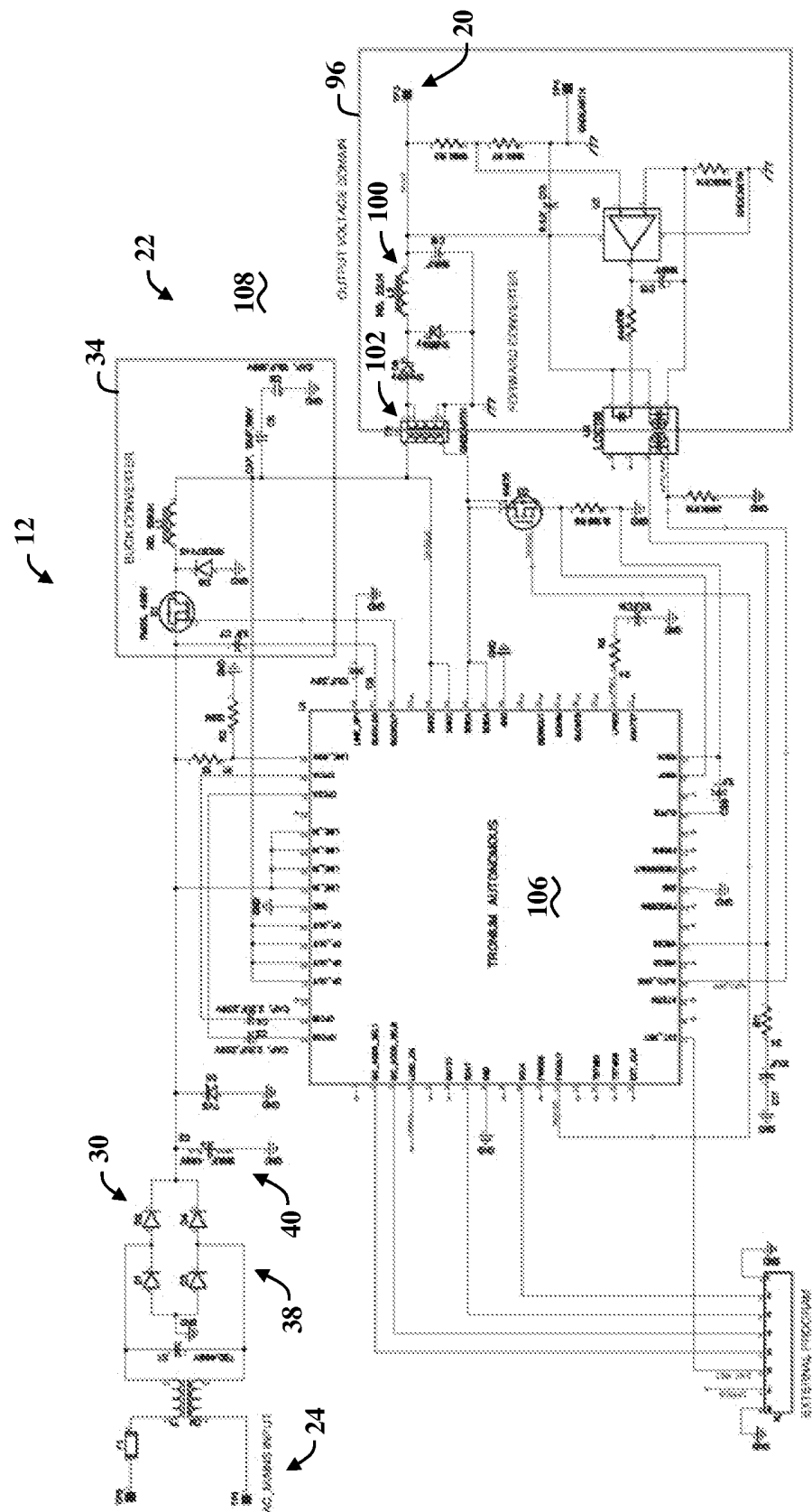


Figure 15

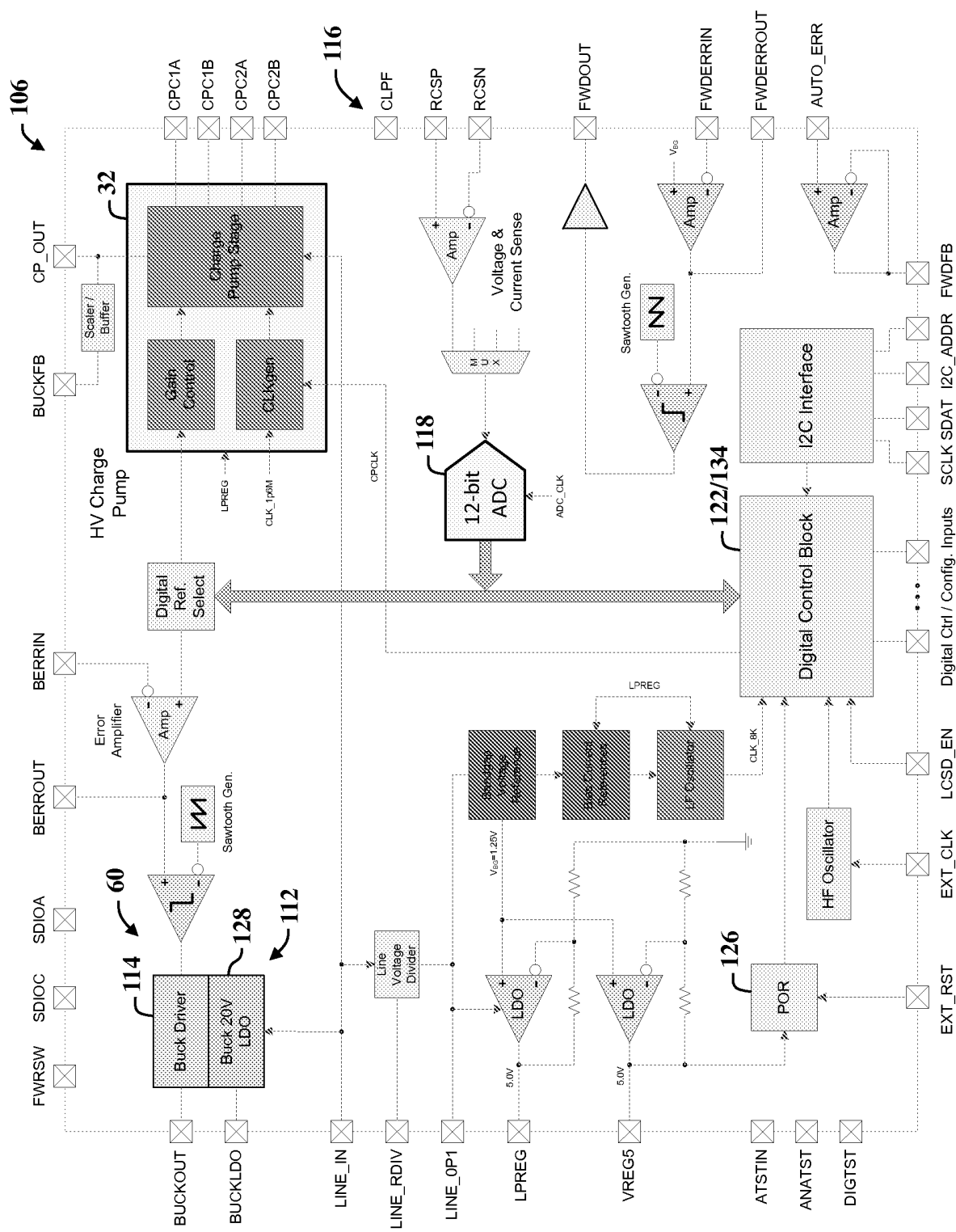


Figure 16

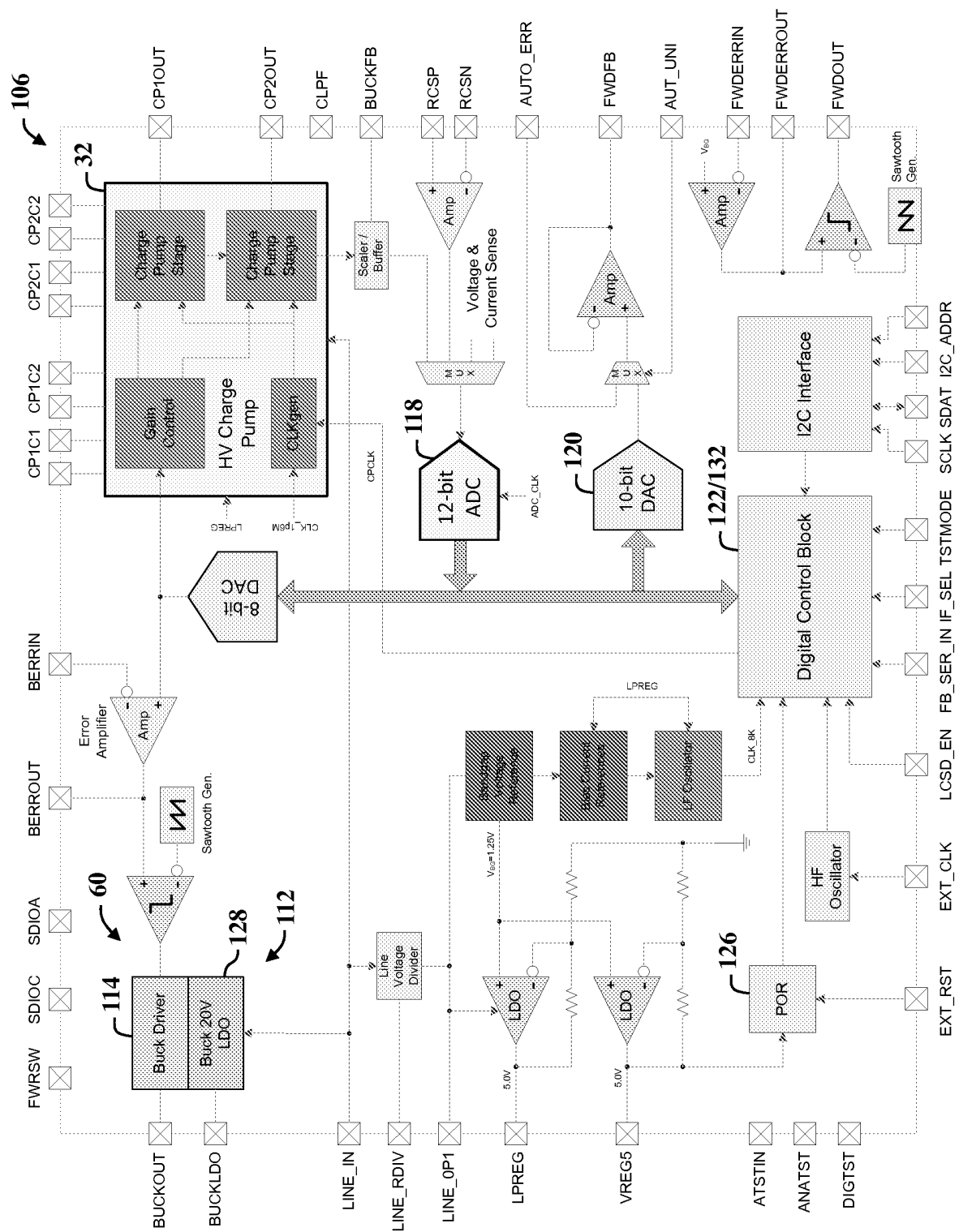


Figure 17A

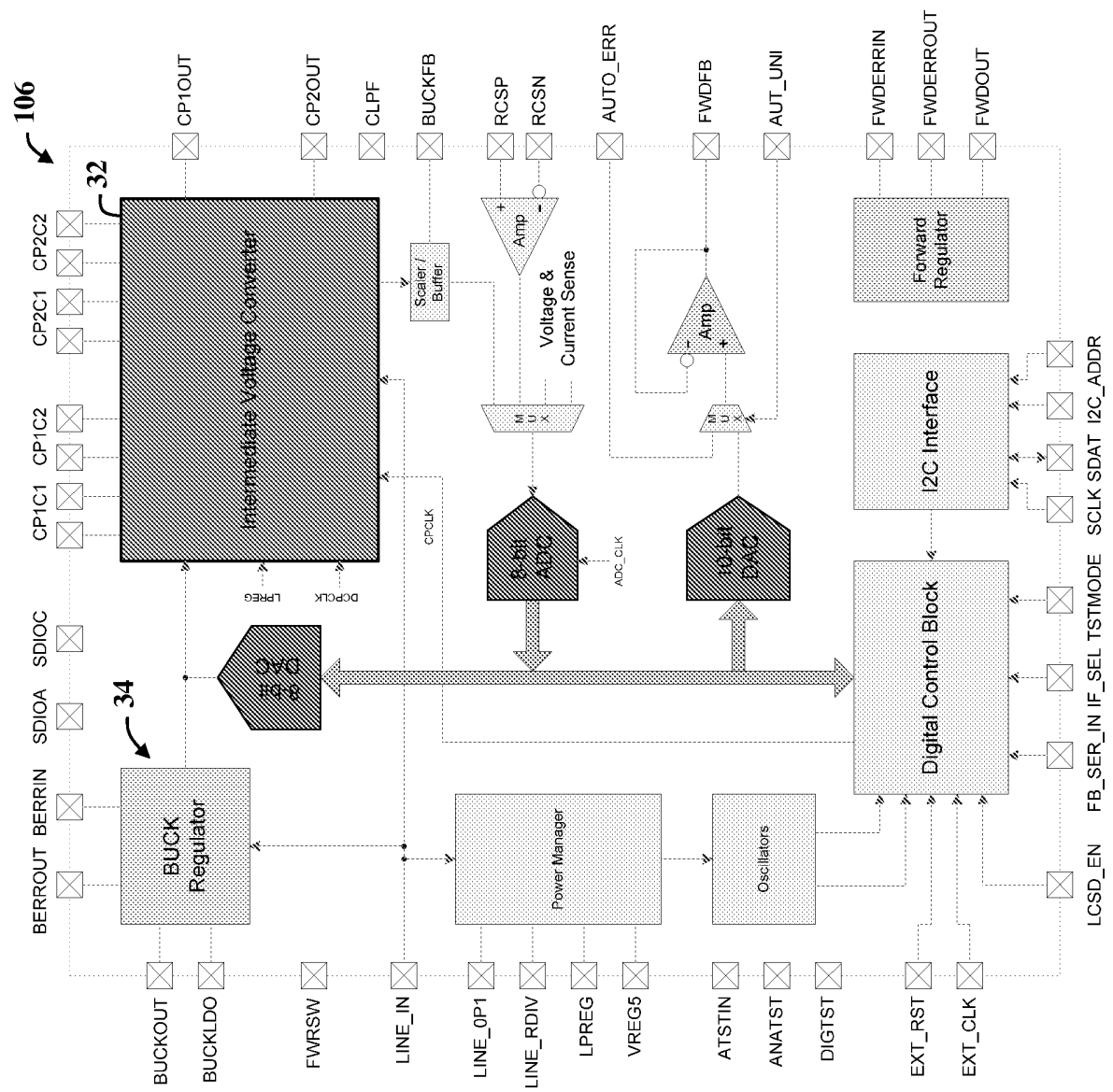


Figure 17B

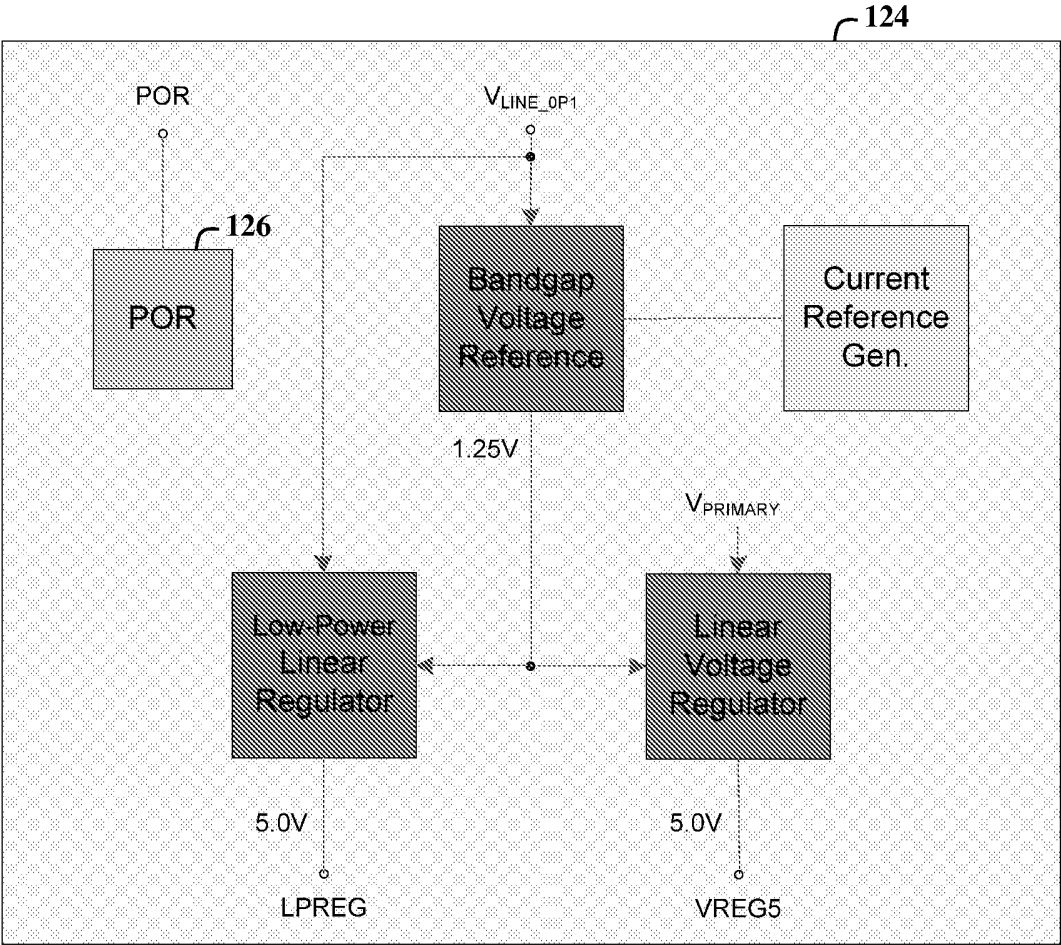
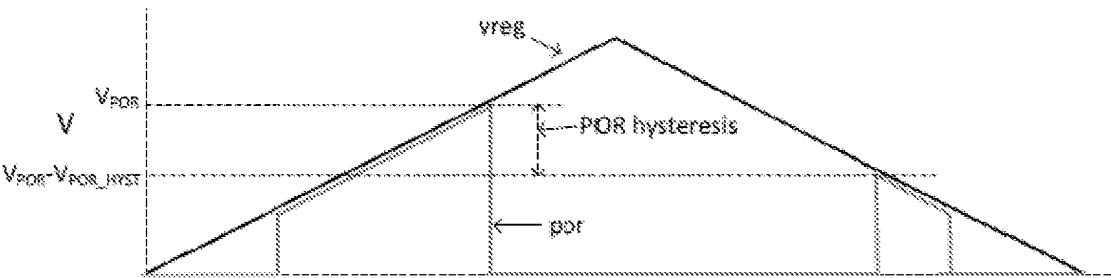


Figure 18



POR Threshold Voltages

Figure 19

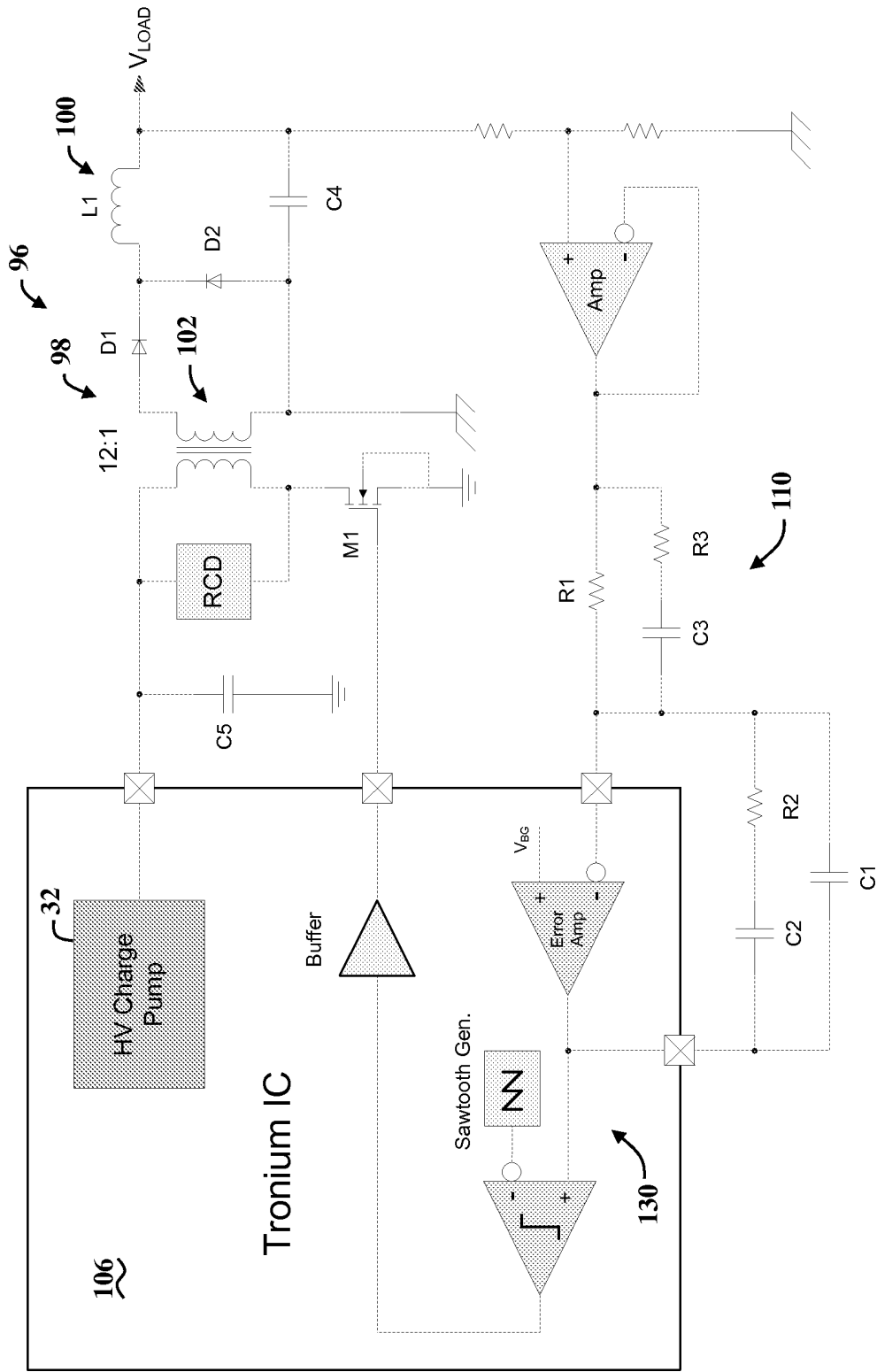


Figure 20

18/37

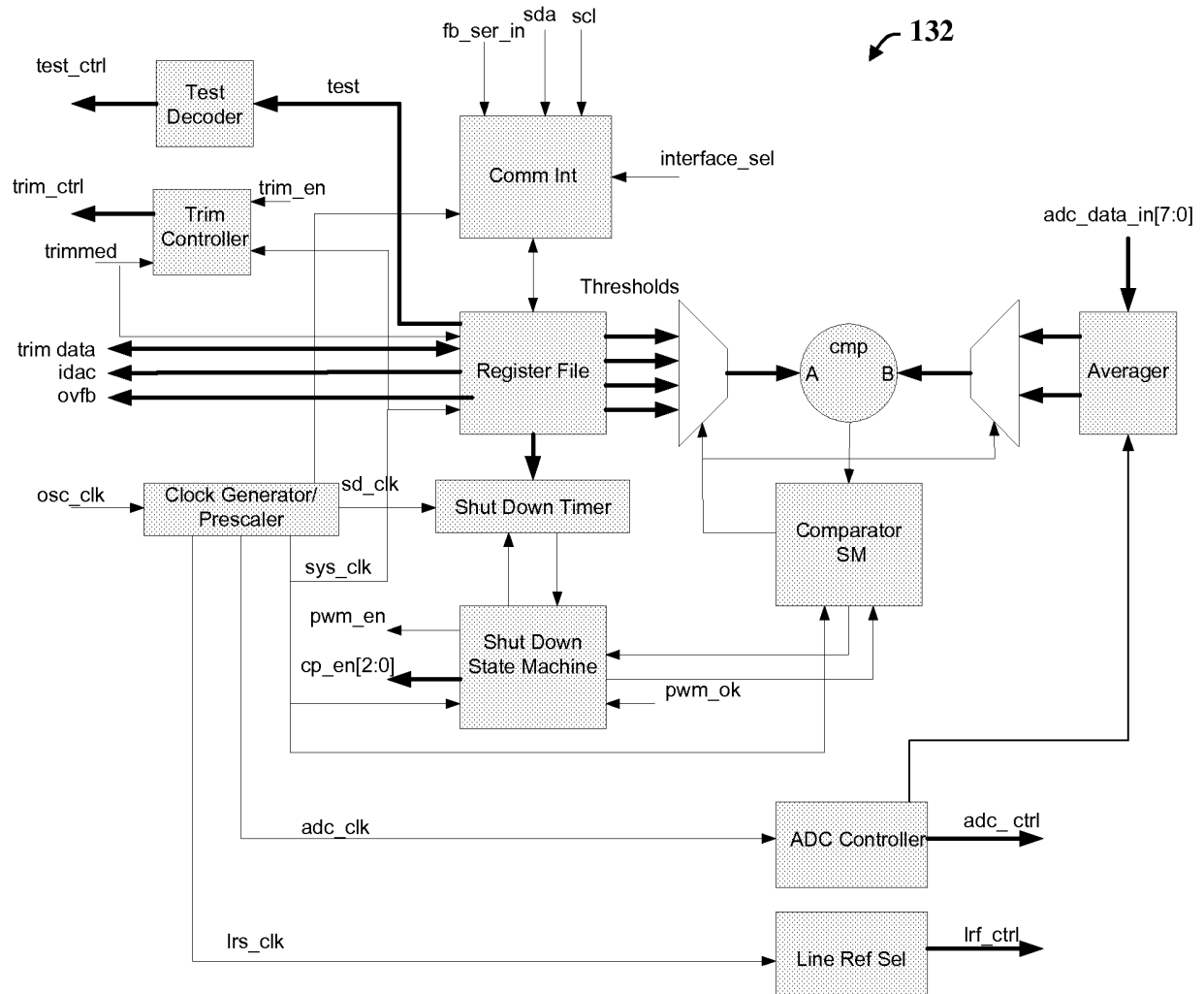


Figure 21

19/37

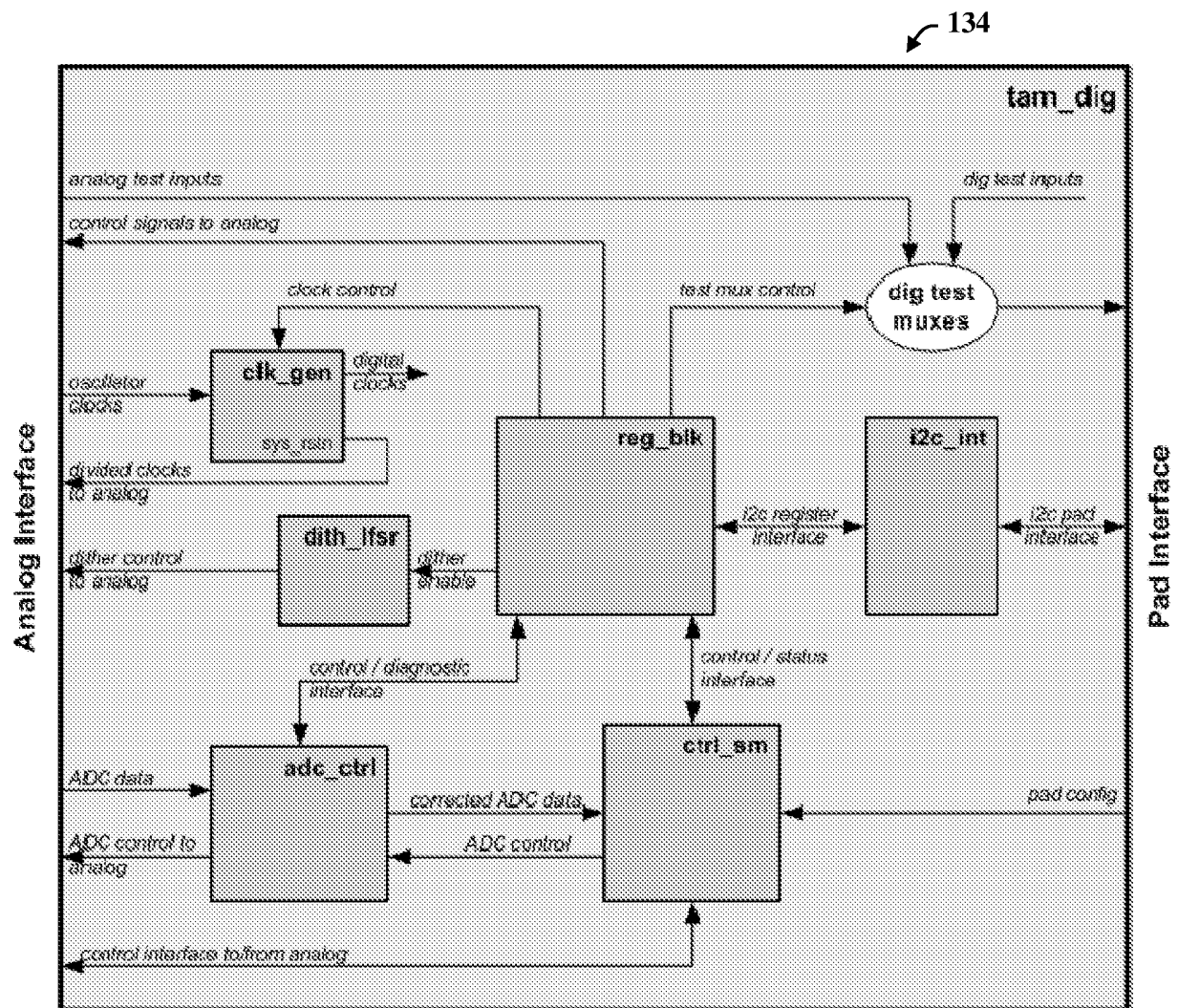


Figure 22

20/37

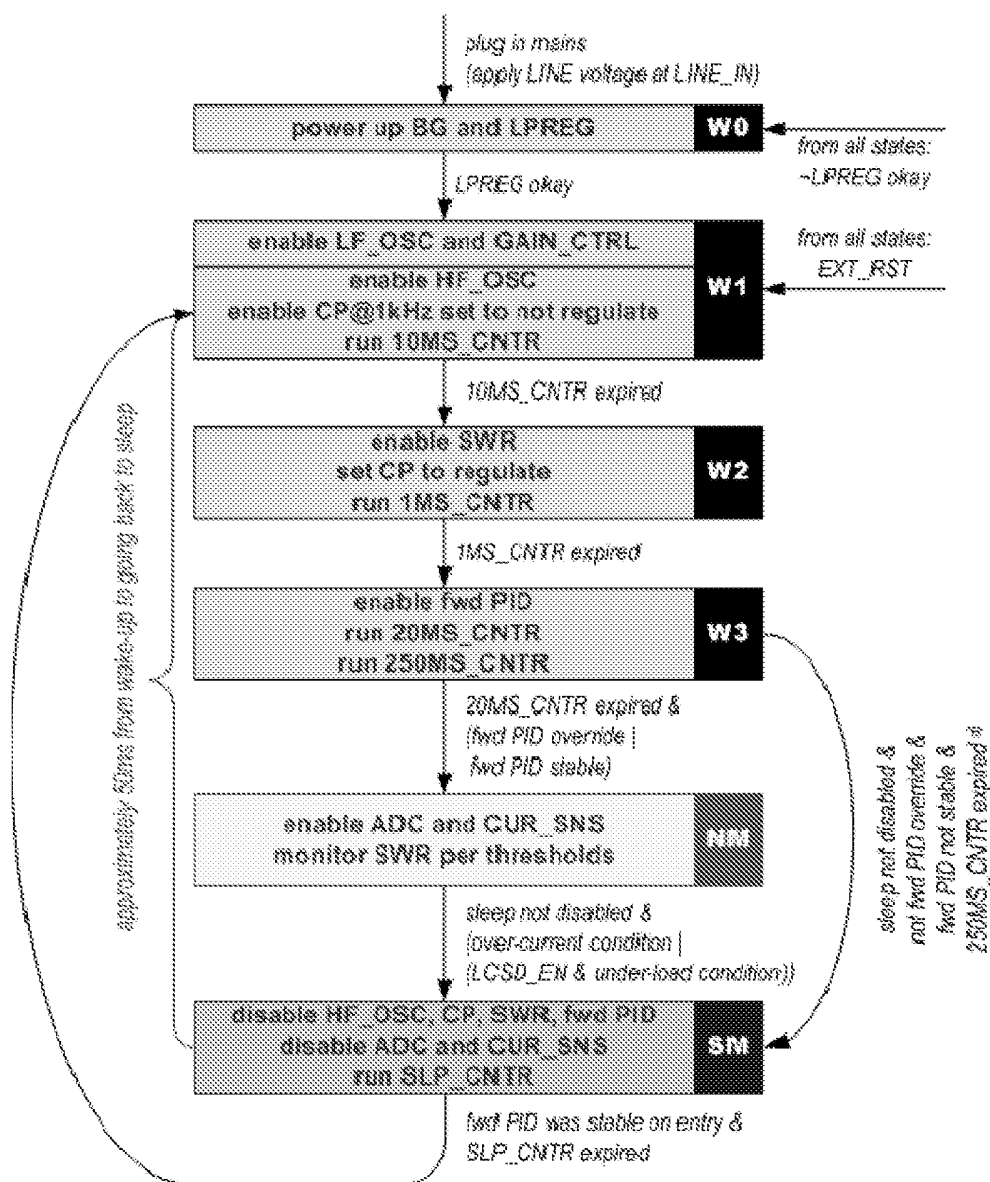


Figure 23

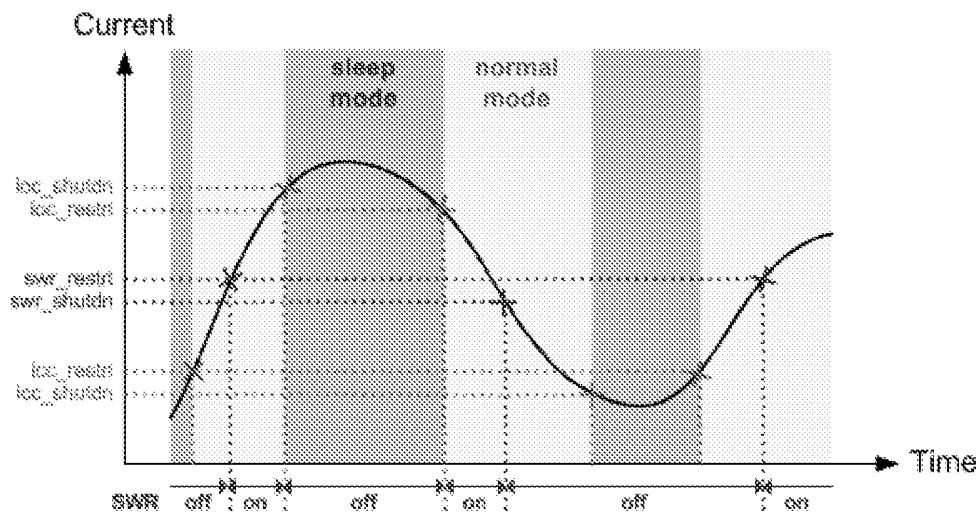


Figure 24

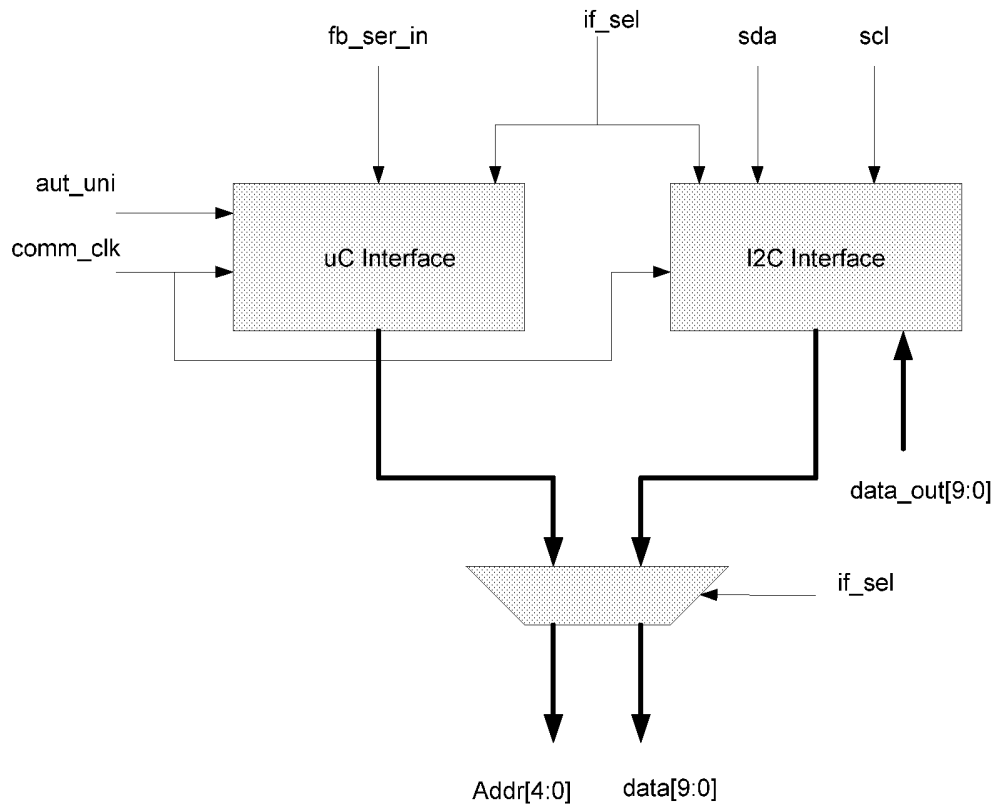


Figure 25

Packet Format

START	R/W	Addr[4:0]	Data[9:0]	IDLE
-------	-----	-----------	-----------	------

Start = Not Idle State
Idle = Inactive state from Optical Isolator
RW = 1 for Read

22/37

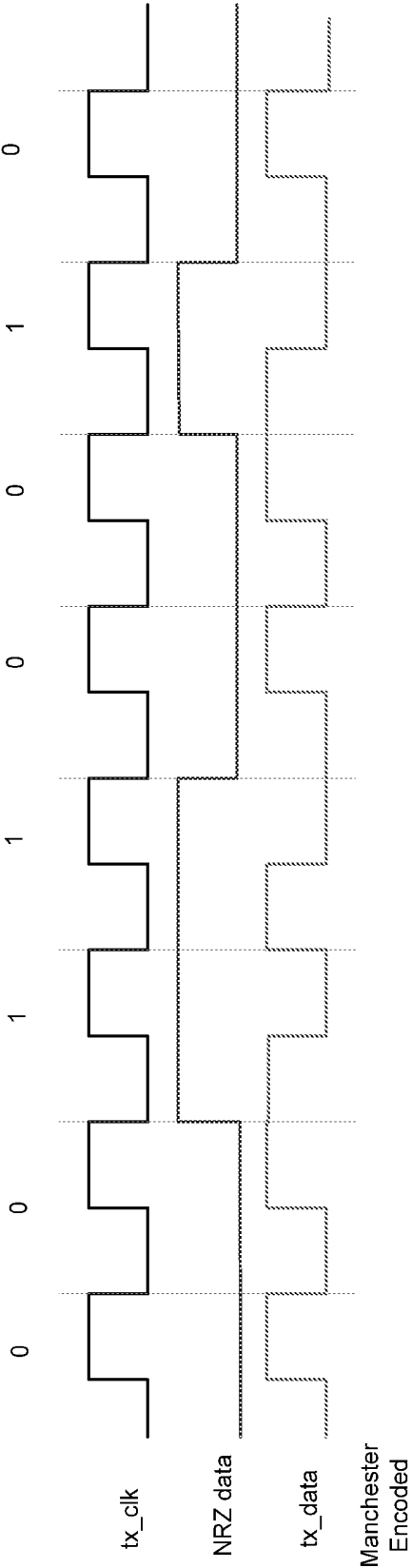
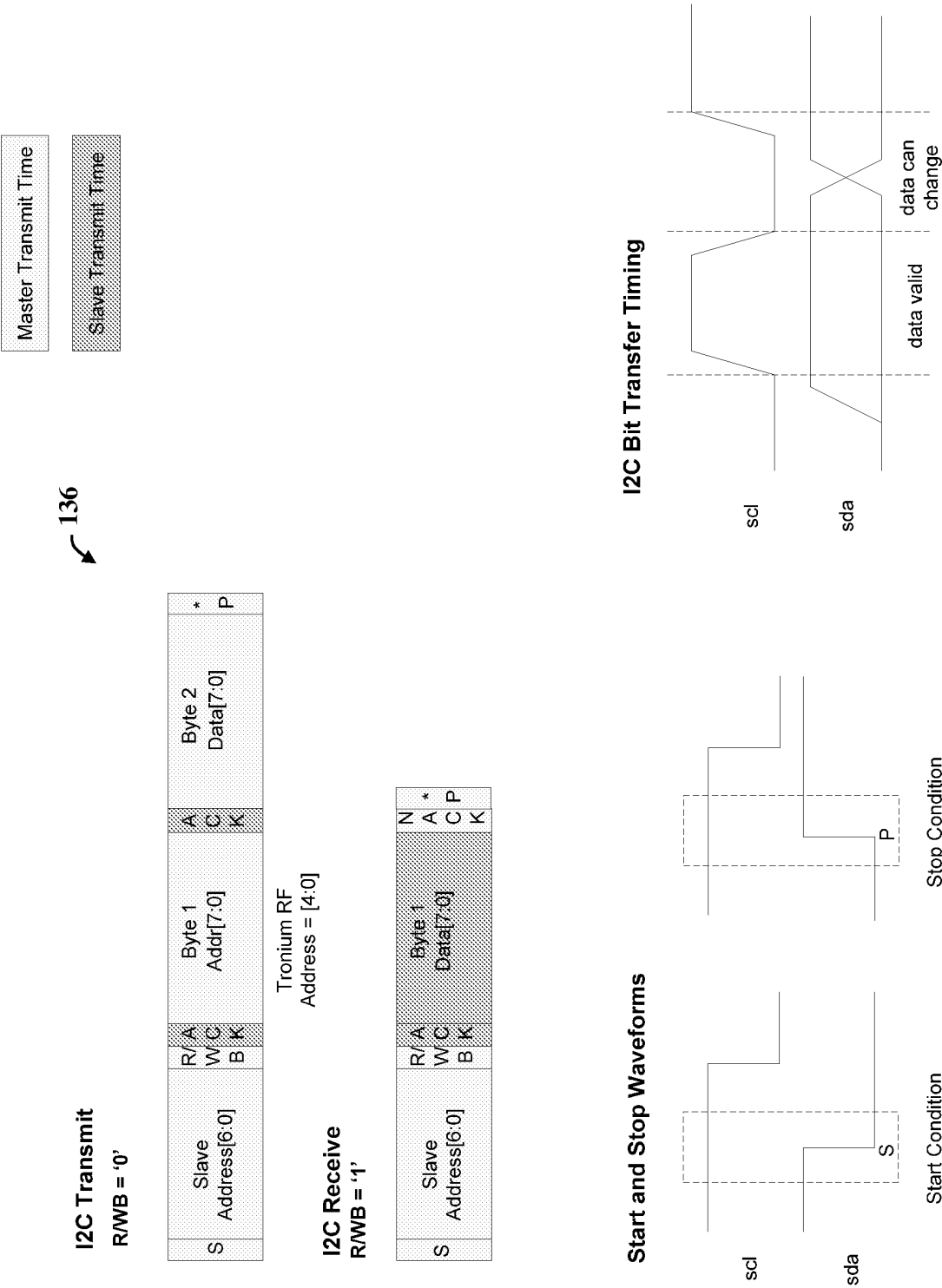


Figure 26



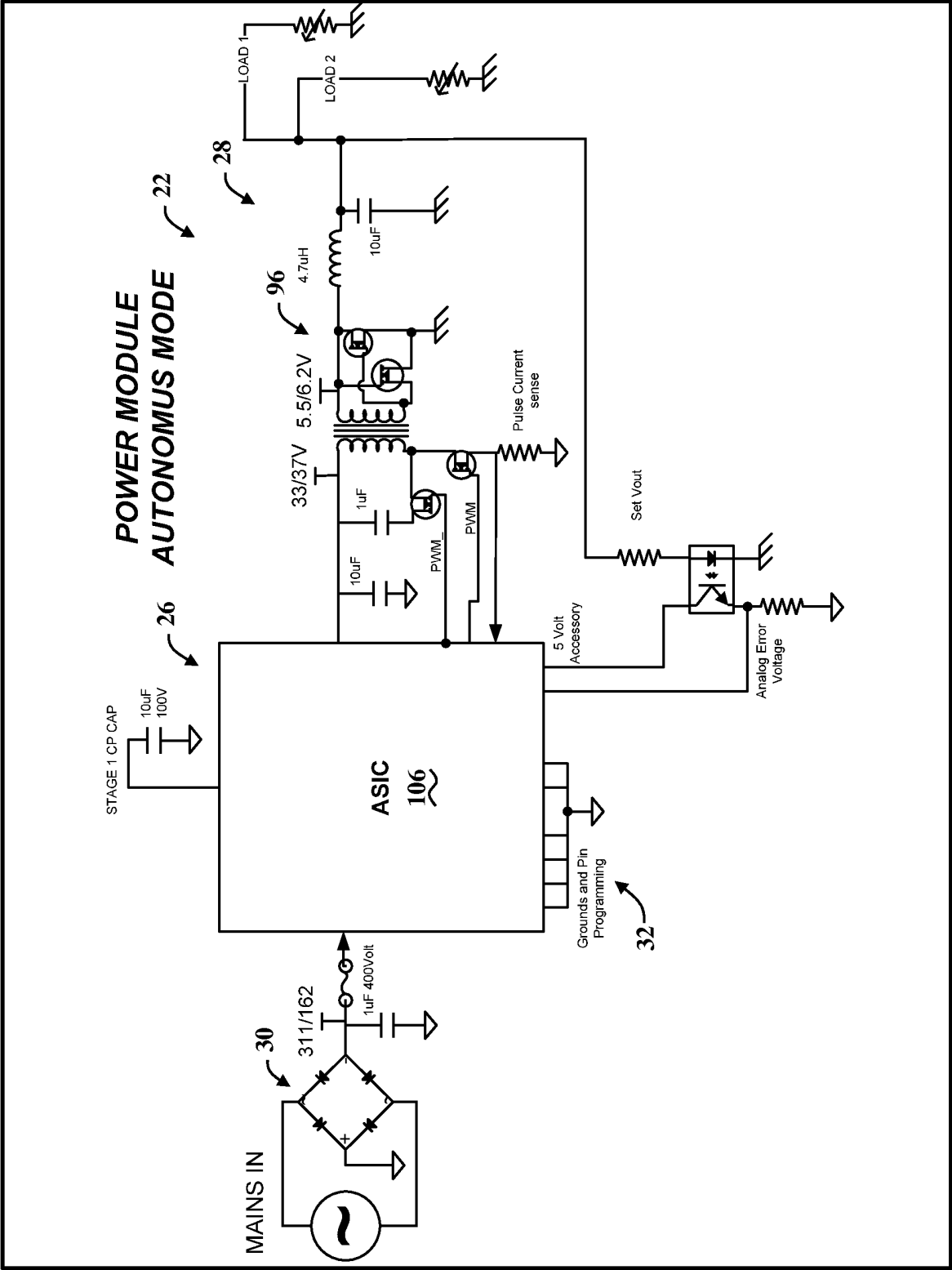


Figure 28

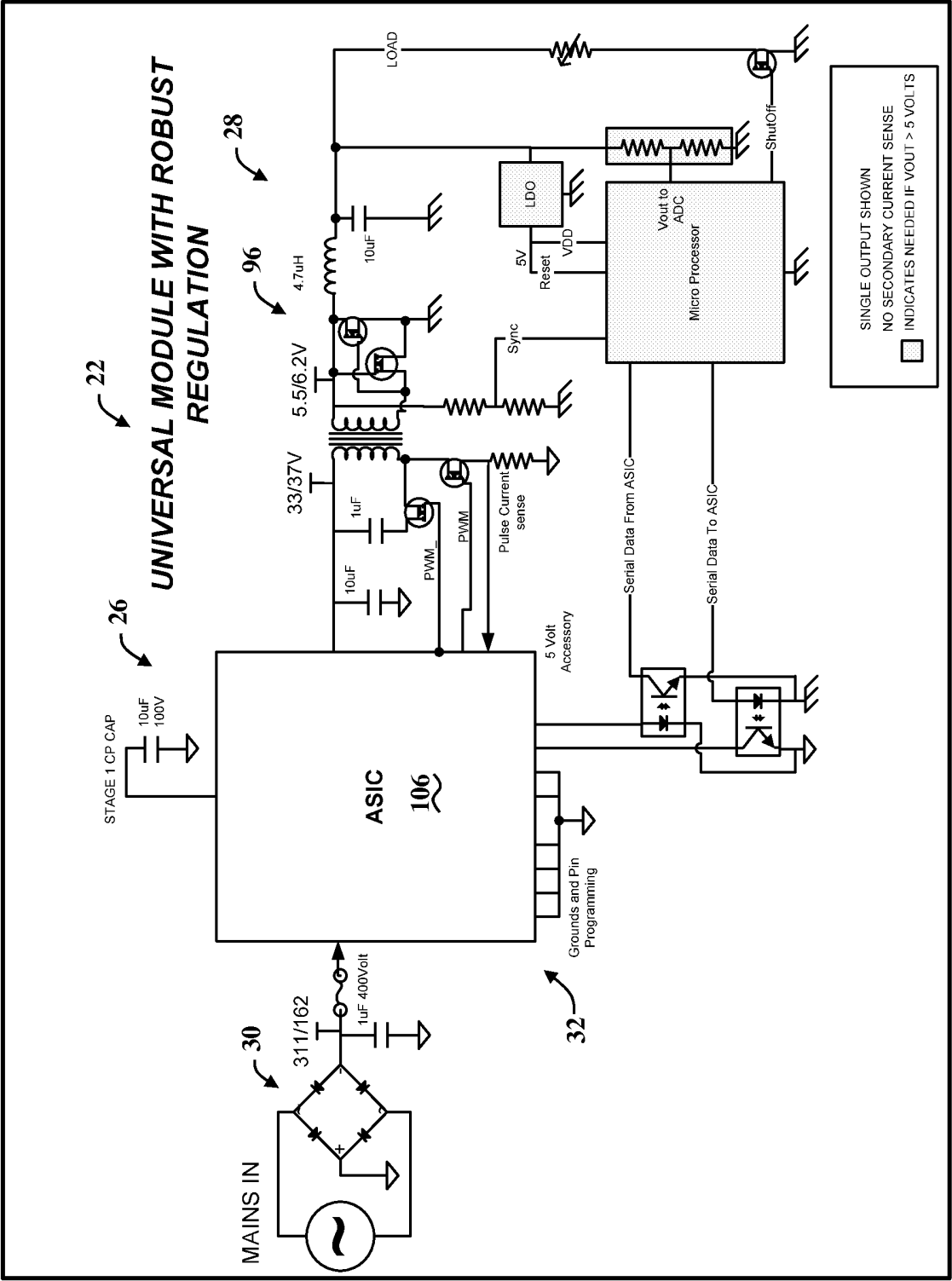


Figure 29

26/37

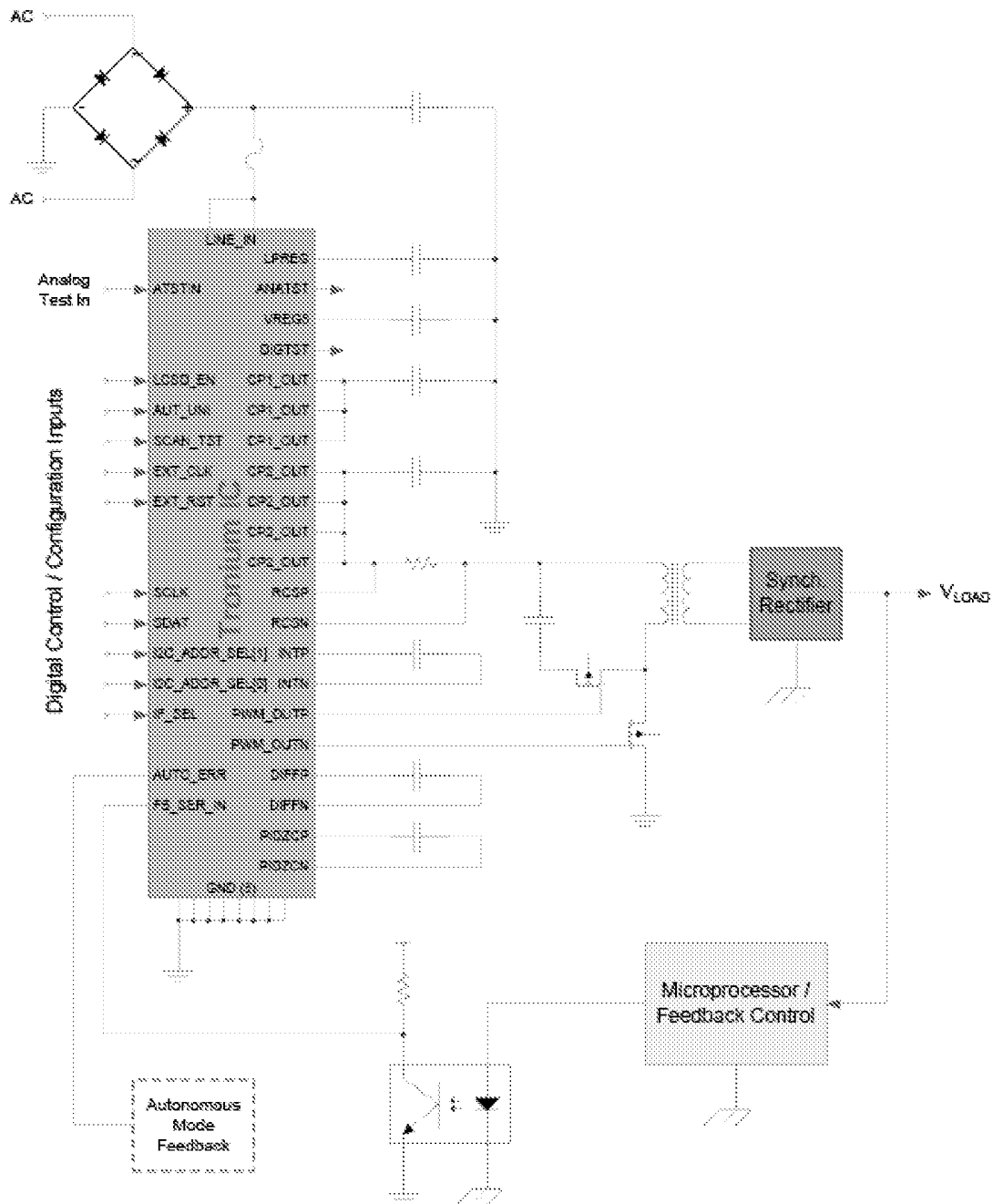


Figure 30

27/37

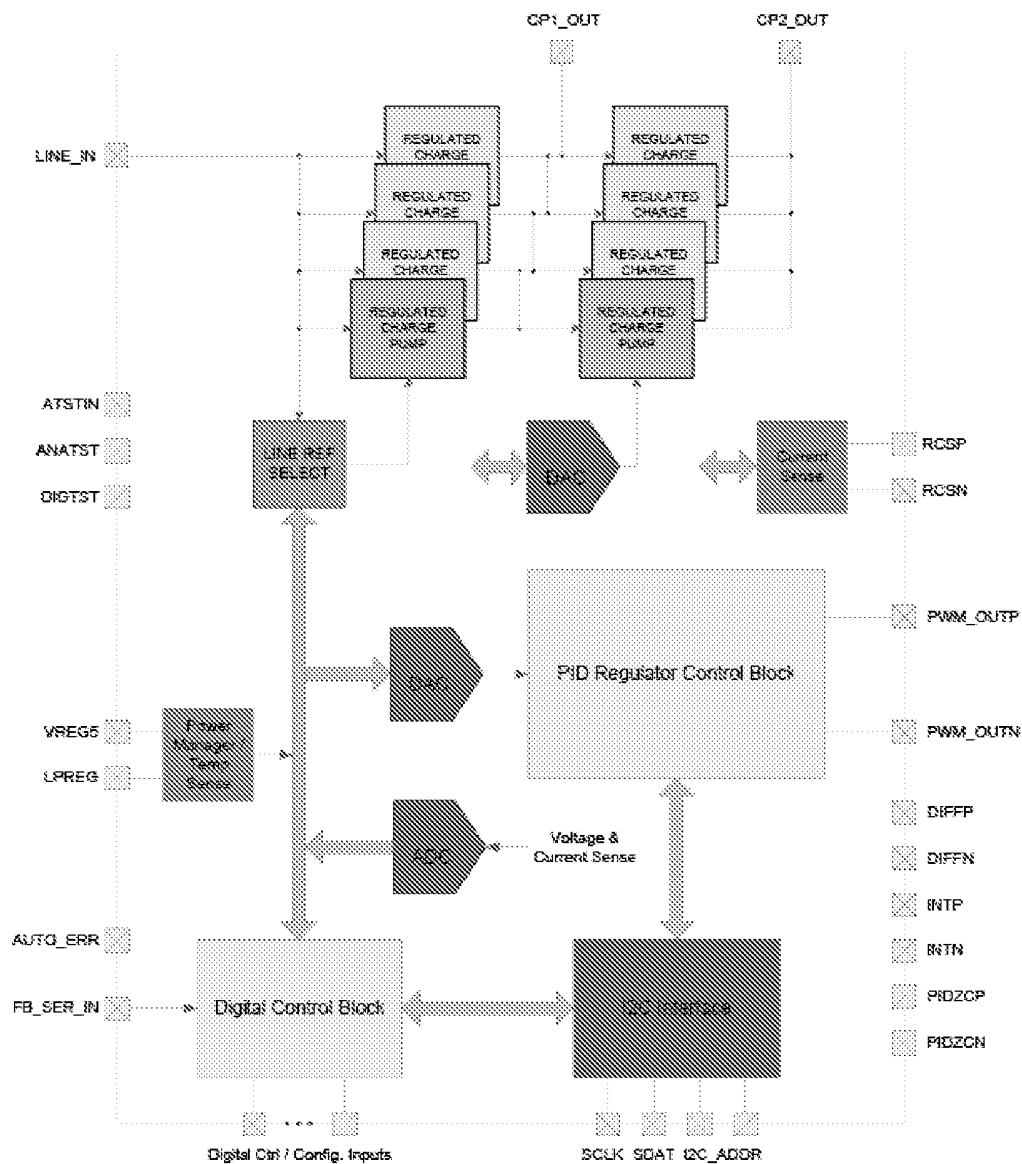


Figure 31

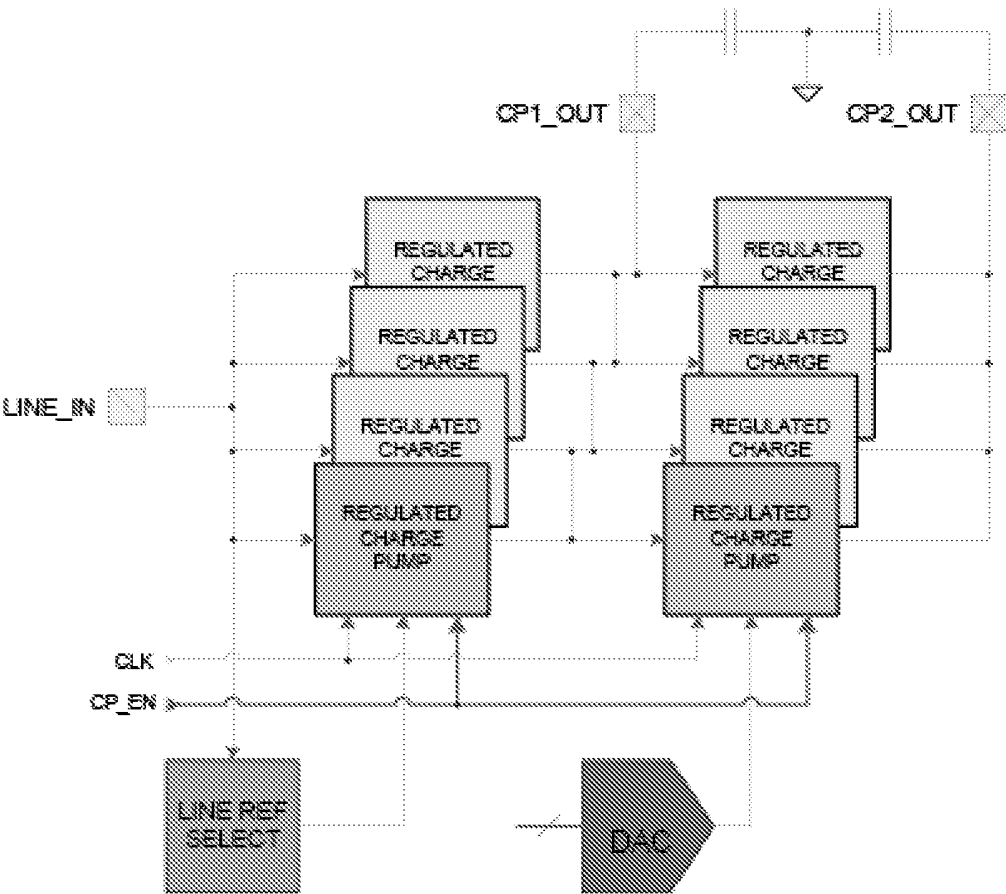


Figure 32

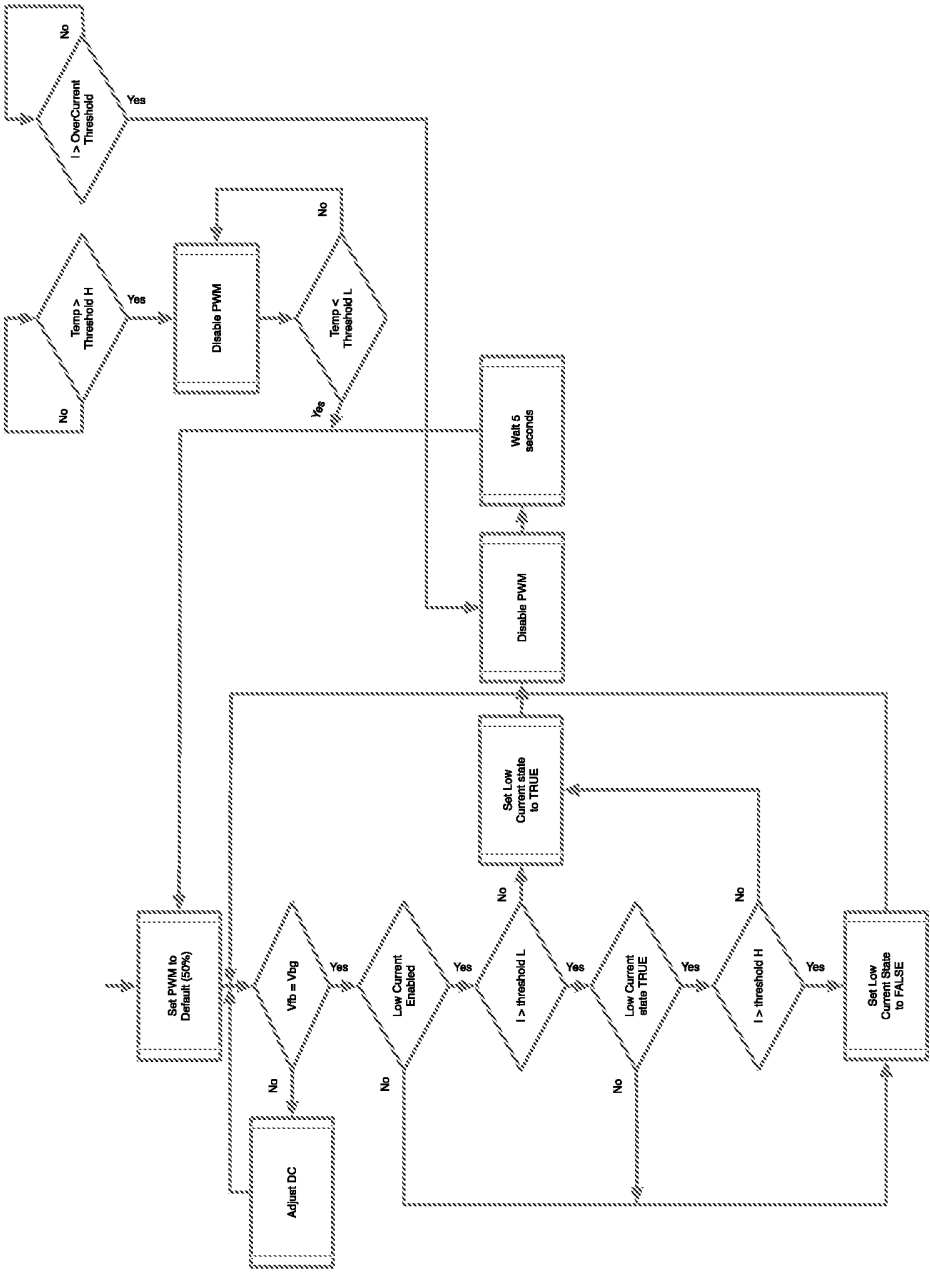


Figure 33

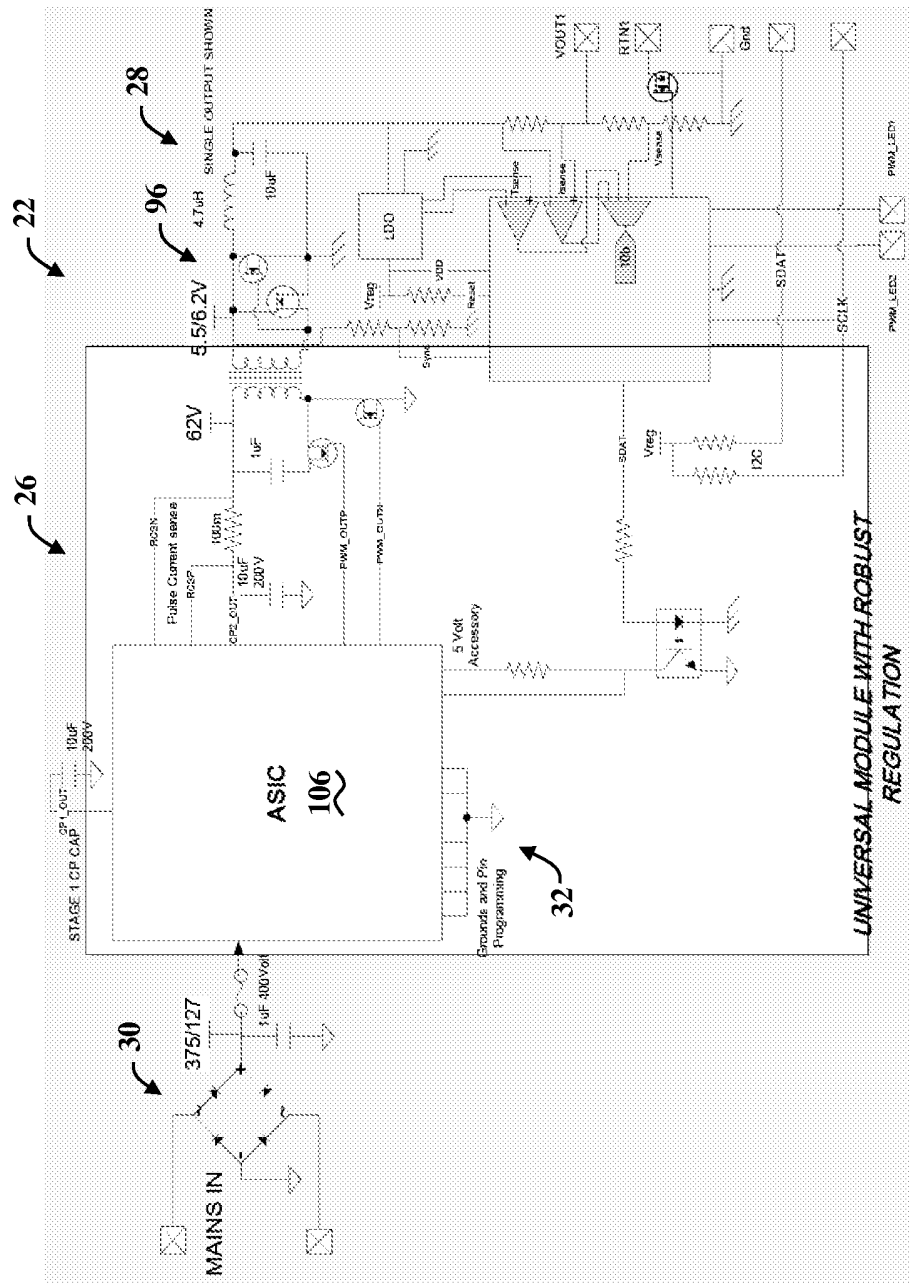


Figure 34

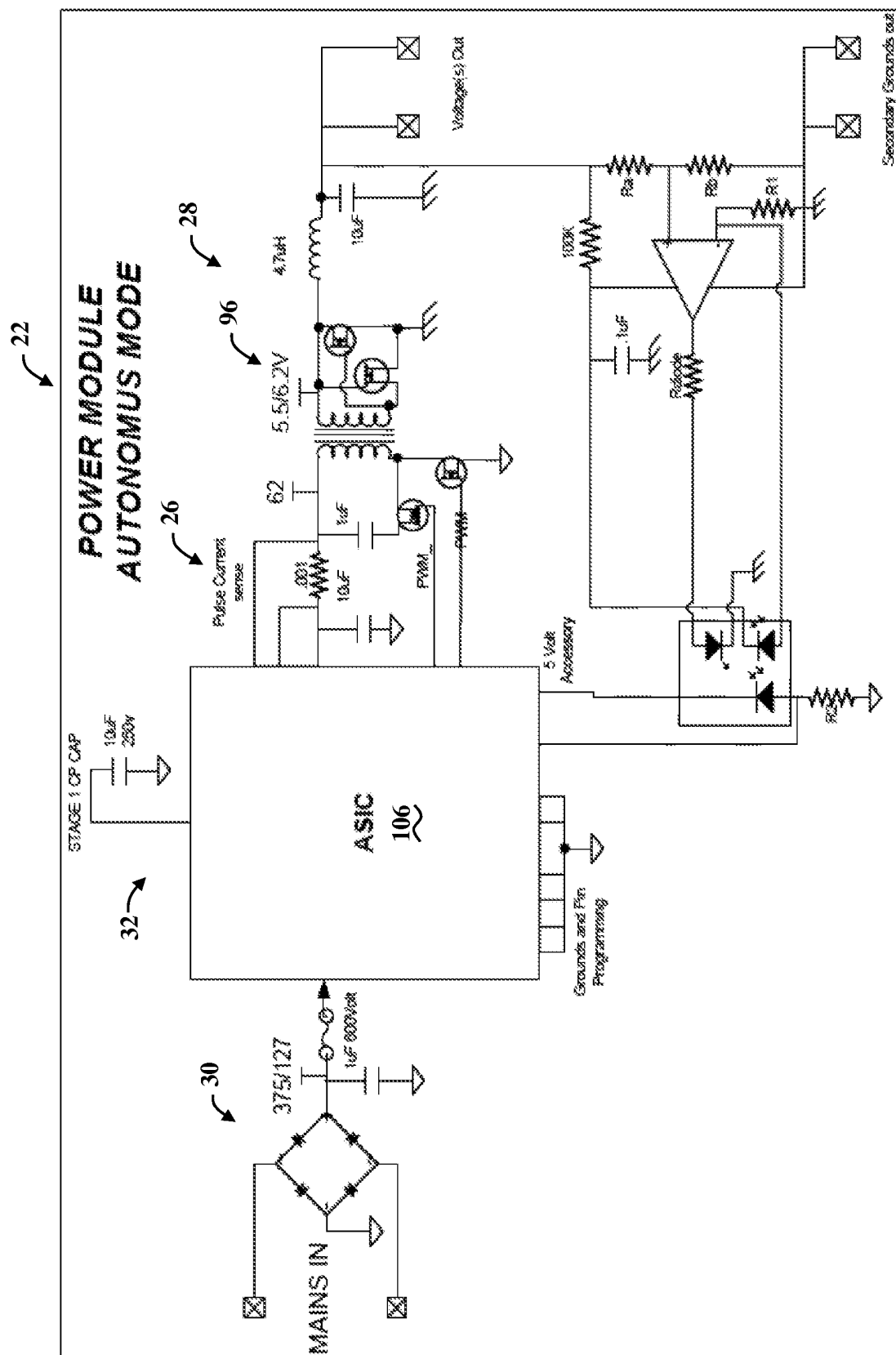


Figure 35

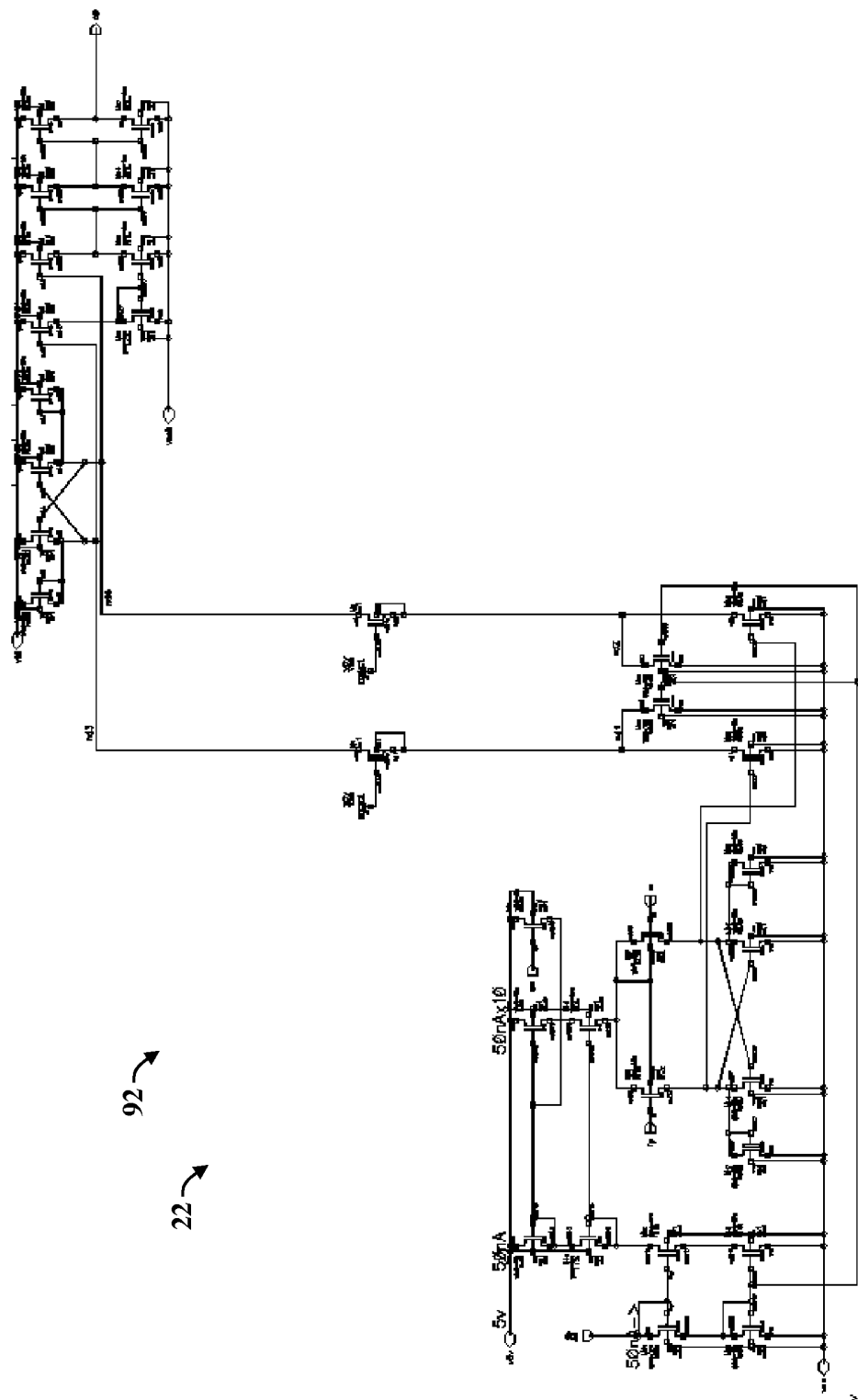


Figure 36

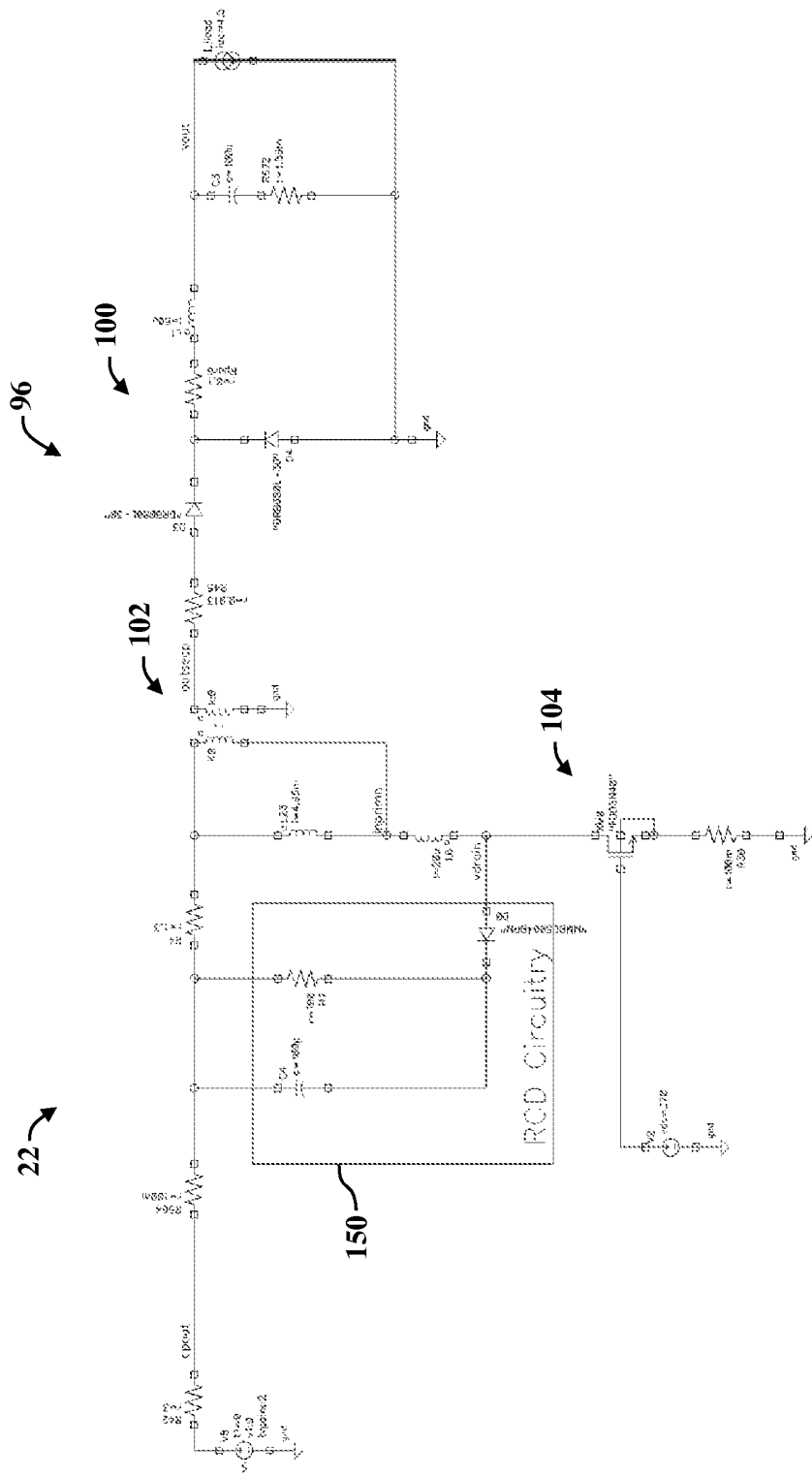


Figure 37

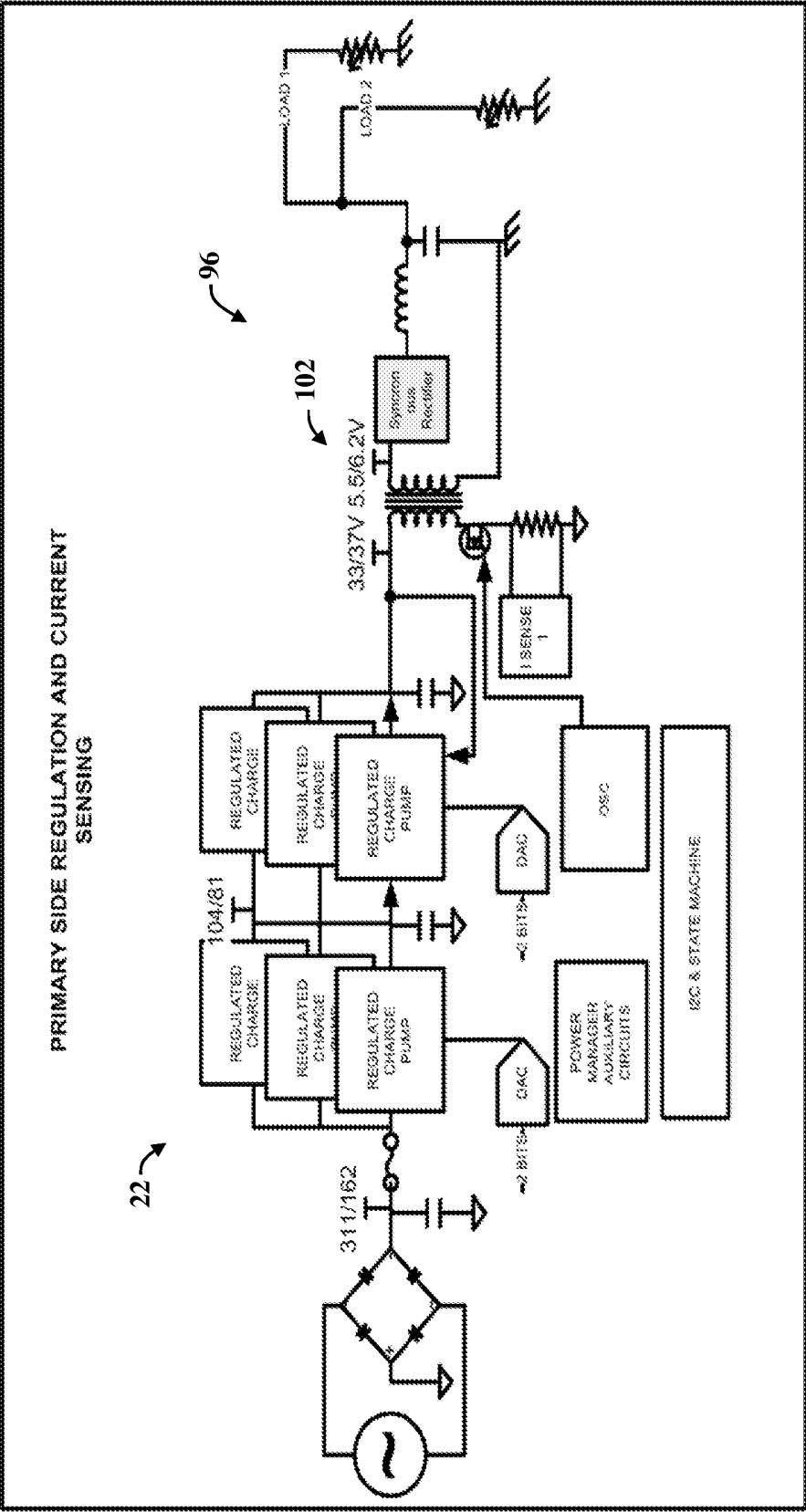


Figure 38

35/37

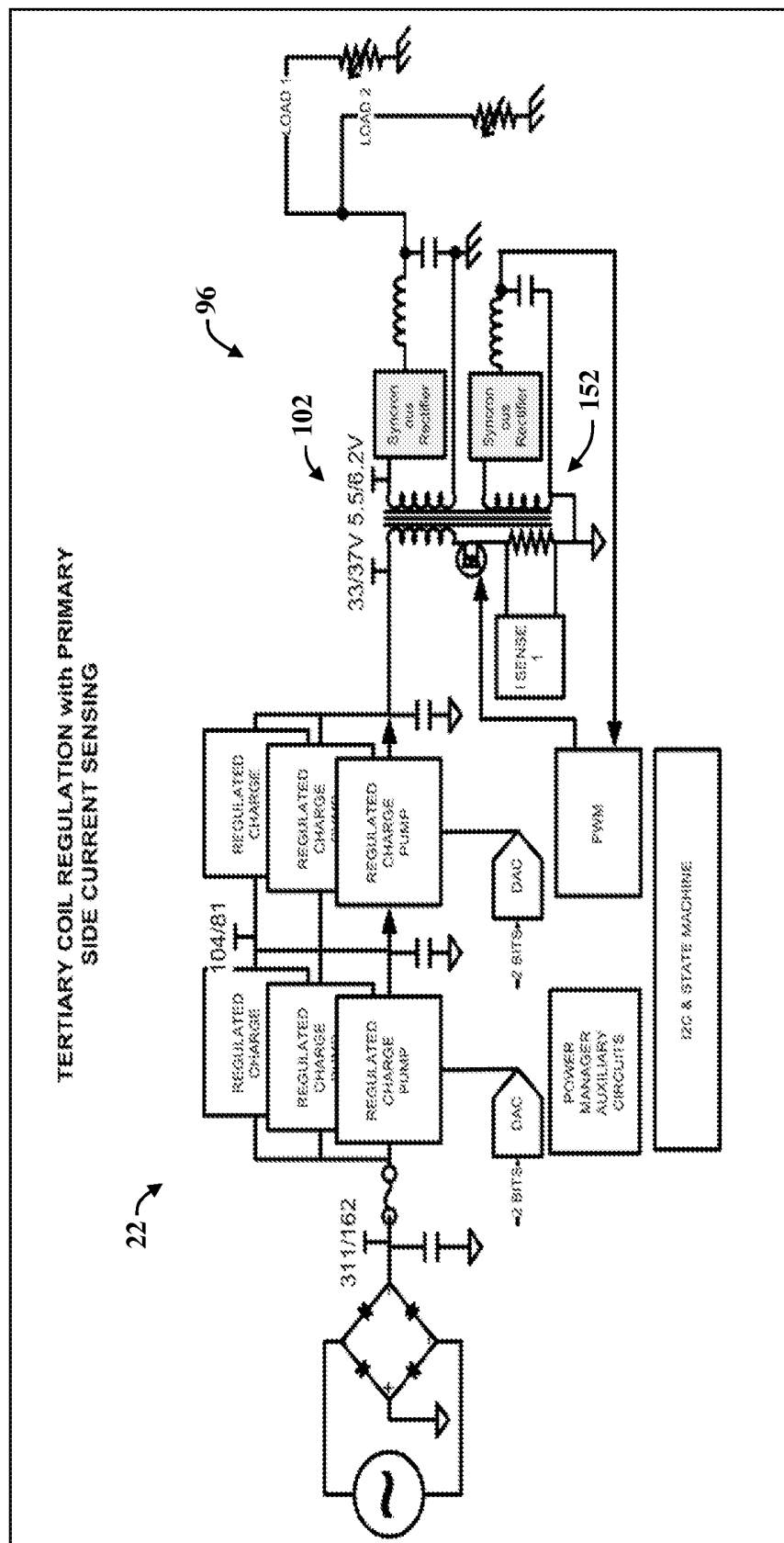


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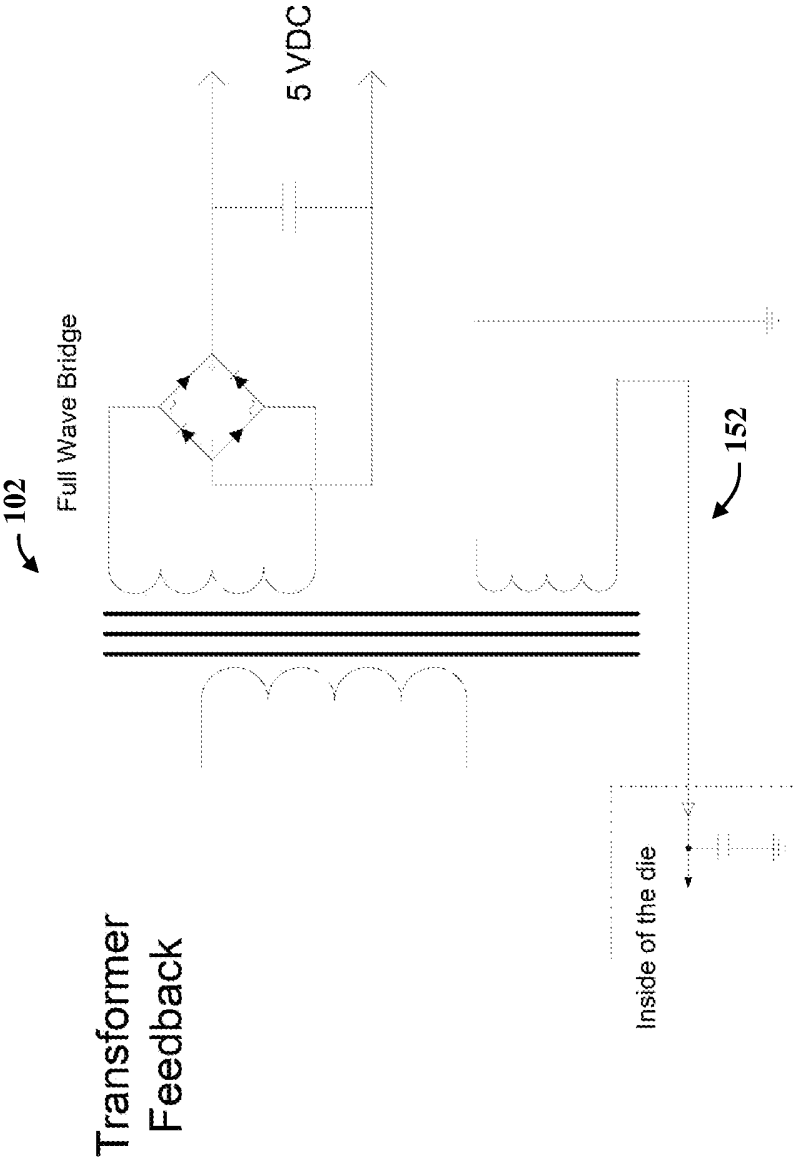


Figure 40

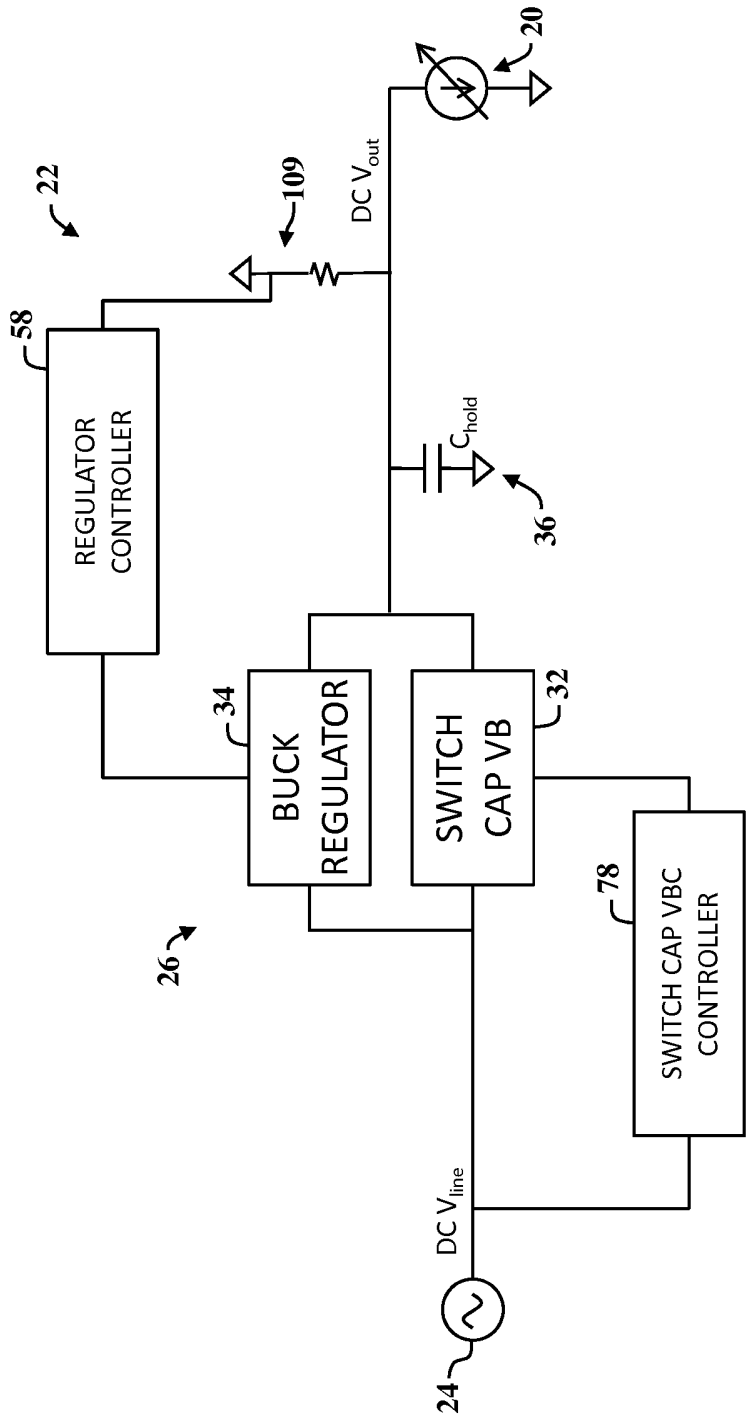


Figure 41

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US14/62740

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H02M 1/14, 7/02, 7/04 (2015.01)

CPC - H02M 1/42, 1/425, 7/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8) Classification(s): H02M 1/00, 1/08, 1/14, 1/15, 1/16, 1/42, 3/22, 3/24, 7/00, 7/02, 7/04 (2015.01); CPC Classification(s): H02M 2001/0006, 2001/0009, 2001/0045, 2001/0067, 1/42, 1/425, 2001/4291, 7/00, 7/02, 7/04, Y02B 70/00, 70/10, 70/1441

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSeer (US, EP, WO, JP, DE, GB, CN, FR, KR, ES, AU, IN, CA, INPADOC Data); ProQuest (Derwent, INSPEC, NTIS, PASCAL, Current Contents Search, Dissertation Abstracts Online, Inside Conferences); IP.com; Google Scholar; KEYWORDS: AC, DC, converter, inverter, step down, buck, intermediate, two stage, rectifier, level shift, charge pump, Dickson

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0036340 A1 (SCARLATESCU, G) February 17, 2005; abstract; figures 1-3; paragraphs [0011, 0026, 0027-0029, 0032]	1-4, 11-14, and 17
A	US 2010/0244935 A1 (KIM, S et al.) September 30, 2010; figures 1 and 2; paragraphs [0030 and 0032]	5 and 18
A	US 5,717,581 A (CANCLINI, A) February 10, 1998; figure 3; column 3, lines 48-67; column 4, lines 1-17	5 and 18
A	US 2003/0099122 A1 (CHO, J) May 29, 2003; figures 28 and 29; paragraphs [0215, 0242, 0245, 0249]	8 and 15
A	US 2007/0053211 A1 (LANNI, T) March 08, 2007; entire document	1-20
A	US 2011/0032731 A1 (COLEMAN, C et al.) February 10, 2011; entire document	1-20

☐ Further documents are listed in the continuation of Box C.


* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use; exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 January 2015 (12.01.2015)

Date of mailing of the international search report

22 JAN 2015

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H02M 7/02(2006.01)

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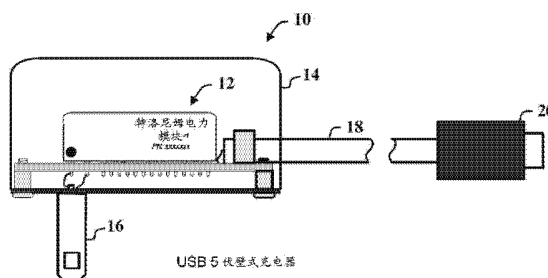
权利要求书3页 说明书29页 附图37页

(54) 发明名称

用于将电力递送到消费型电子装置的电路

(57) 摘要

本文描述一种用于提供电力来用于为电子装置供电的电路。所述电路包括一次电力电路和二次电力电路。所述一次电力电路接收来自电力源的交流 (AC) 输入电力信号,且产生中间直流 (DC) 电力信号。所述中间 DC 电力信号是在小于所述 AC 输入电力信号的电压电平的第一电压电平下产生。所述二次电力电路接收来自所述一次电力电路的所述中间 DC 电力信号,并将输出 DC 电力信号递送到电子装置。所述输出 DC 电力信号是在小于所述中间 DC 电力信号的所述第一电压电平的输出电压电平下递送。



1. 一种用于提供电力来用于为电子装置供电的电路,其包括:

一次电力电路,其适于电耦合到电力源,所述一次电力电路被配置来接收来自所述电力源的交流 (AC) 输入电力信号,并产生中间直流 (DC) 电力信号,所述中间 DC 电力信号是在小于所述 AC 输入电力信号的电压电平的第一电压电平下产生;以及

二次电力电路,其电耦合到所述一次电力电路,所述二次电力电路被配置来接收来自所述一次电力电路的所述中间 DC 电力信号,并将输出 DC 电力信号递送到电子装置,所述输出 DC 电力信号是在小于所述中间 DC 电力信号的所述第一电压电平的输出电压电平下递送。

2. 根据权利要求 1 所述的电路,所述一次电力电路包括整流器电路,其被配置来接收来自所述电力源的所述 AC 电力输入信号,并产生经整流的 DC 电力信号,所述经整流的 DC 电力信号具有大约等于所述 AC 输入电力信号的所述电压电平的电压电平。

3. 根据权利要求 2 所述的电路,所述整流器电路包括全波桥式整流器。

4. 根据权利要求 2 所述的电路,所述一次电力电路包括开关电容器电压击穿电路,其耦合到所述整流器电路,用于接收来自所述整流器电路的所述经整流的 DC 电力信号,且产生所述中间 DC 电力信号。

5. 根据权利要求 4 所述的电路,所述开关电容器电压击穿电路包括:

一对并行电耦合的反激电容器;

多个开关组合件,其电耦合到所述对反激电容器中的每一个,在充电阶段与放电阶段之间操作所述多个开关组合件;以及

保持电容器,其电耦合到所述对反激电容器中的每一个,所述多个开关组合件被操作来在所述充电阶段期间,选择性地将所述经整流的 DC 电力信号递送到所述对反激电容器中的每一个,且在所述放电阶段期间,选择性地将所述中间 DC 电力信号递送到所述保持电容器。

6. 根据权利要求 5 所述的电路,所述开关组合件中的至少一个包括:

N- 沟道 MOSFET 开关;

电平移位器,其耦合到所述 N- 沟道 MOSFET 开关,用于将控制信号递送到所述 N- 沟道 MOSFET 开关;以及

迪克森电荷泵,其耦合到所述电平移位器,所述迪克森电荷泵被配置来接收所述经整流的 DC 电力信号,并产生具有大于所述经整流的 DC 电力信号的所述电压电平的电压电平的输出电力信号,所述输出电力信号被递送到所述电平移位器,来用于操作 N- 沟道 MOSFET 开关。

7. 根据权利要求 5 所述的电路,所述开关电容器电压击穿电路包括耦合到所述多个开关组合件中的每一个的控制电路,所述控制电路包括:

电压感测电路,其用于感测所述经整流的 DC 电力信号的电压电平;以及

增益控制器,其被配置来依据所述感测到的电压电平来选择所述开关电容器电压击穿电路的增益设定,且依据所述选定的增益设定来操作所述多个开关组合件中的每一个。

8. 根据权利要求 4 所述的电路,所述一次电力电路包括与所述开关电容器电压击穿电路并行电耦合的降压调节器电路,所述降压调节器电路用于接收来自所述整流器电路的所述经整流的 DC 电力信号,并产生所述中间 DC 电力信号。

9. 根据权利要求 8 所述的电路,所述降压调节器电路包括耦合到电压降低电路的调节器开关组合件,所述电压降低电路包括二极管、电感器和电容器,所述调节器开关组合件被操作来选择性地将所述经整流的 DC 电力信号递送到所述电压降低电路。

10. 根据权利要求 9 所述的电路,所述降压调节器电路包括控制电路,其用于将经脉冲宽度调制的控制信号提供给经调节的开关组合件,以选择性地将所述经整流的 DC 电力信号递送到所述电压降低电路,所述控制电路包括:

电压感测电路,其用于感测所述中间 DC 电力信号的所述第一电压电平;以及

调节器控制器,其用于依据所述感测到的第一电压电平来产生所述经脉冲宽度调制的控制信号,所述调节器控制器被配置来调整待递送的所述控制信号的工作周期,以使所述中间 DC 电力信号的所述电压电平维持在预定义的电压电平。

11. 根据权利要求 1 所述的电路,所述二次电力电路包括正向转换器电路,其包括一次电压降低电路和二次电压降低电路,所述一次电压降低电路被配置来接收来自所述一次电力电路的所述中间 DC 电力信号,并将二次 DC 电力信号递送到所述二次电压降低电路,所述二次 DC 电力信号具有小于所述中间 DC 电力信号的所述电压电平的电压电平,所述二次电压降低电路被配置来接收所述二次 DC 电力信号,并产生待递送到所述电子装置的所述输出 DC 电力信号。

12. 根据权利要求 11 所述的电路,所述一次电压降低电路包括变压器,所述变压器的一次侧耦合到所述一次电力电路,且所述变压器的二次侧耦合到所述二次电压降低电路。

13. 根据权利要求 12 所述的电路,所述二次电压降低电路包括一对二极管、一电感器和一电容器。

14. 一种用于提供电力来用于为电子装置供电的电力模块,其包括:

整流器电路,其被配置来接收来自电力源的 AC 电力输入信号,并产生经整流的 DC 电力信号;

开关电容器电压击穿电路和集成电路控制器,其耦合到所述整流器电路,用于接收来自所述整流器电路的所述经整流的 DC 电力信号,所述集成电路控制器用于感测所述 AC 电力输入信号的电压电平,并依据所述感测到的电压电平来调整所述开关电容器电压击穿电路的增益,以产生中间 DC 电力信号;以及

正向转换器电路,其耦合到所述开关电容器电压击穿电路,所述正向转换器电路包括变压器,其用于接收所述中间 DC 电力信号,且产生待递送到电子装置的输出 DC 电力信号。

15. 根据权利要求 14 所述的电力模块,其包括与所述开关电容器电压击穿电路并行电耦合的降压调节器电路,所述降压调节器电路包括调节器开关组合件,其用于接收来自所述整流器电路的所述经整流的 DC 电力信号,并产生所述中间 DC 电力信号。

16. 根据权利要求 15 所述的电力模块,所述集成电路控制器包括降压调节器控制电路,其用于将经脉冲宽度调制的控制信号提供给经调节的开关组合件。

17. 根据权利要求 14 所述的电力模块,所述正向转换器电路包括耦合到变压器一次侧的变压器开关组合件,所述集成电路包括变压器控制电路,其用于选择性地操作所述变压器开关组合件,以维持所述输出 DC 电力信号的电压电平。

18. 根据权利要求 14 所述的电力模块,所述开关电容器电压击穿电路包括:

一对并行电耦合的反激电容器;以及

多个开关组合件,其电耦合到所述对反激电容器中的每一个。

19. 根据权利要求 18 所述的电力模块,所述开关组合件中的至少一个包括:

N- 沟道 MOSFET 开关;以及

迪克森电荷泵,其耦合到所述 N- 沟道 MOSFET 开关。

20. 根据权利要求 18 所述的电力模块,其中所述 N 沟道 MOSFET 形成于所述集成电路内。

用于将电力递送到消费型电子装置的电路

[0001] 相关申请的交叉引用

[0002] 本申请要求 2014 年 10 月 28 日提交的美国临时专利申请号 62/069,672 的优先权, 要求 2014 年 3 月 6 日提交的美国临时专利申请号 61/949,171 的优先权, 且要求 2013 年 10 月 28 日提交的美国临时专利申请号 61/896,557 的优先权, 上述临时专利申请全部出于所有目的以全文引用的方式并入本文中。

技术领域

[0003] 本发明大体上涉及电力电路, 且更明确地说, 涉及用于提供电力来用于为消费型电子装置充电和 / 或供电的电力电路。

背景技术

[0004] 能源危机需要降低电流负载的需求侧响应。能源危机在全世界正在到来。举例来说, 美国的能源部预测, 到 2015 年, 平均起来, 将没有足够的电力来供应美国的平均需求。

[0005] 可控罪魁祸首之一是“吸血鬼负载”。也称为“插墙式电力”或“待机电力”, 美国能源部 (DOE) 估计此电力浪费每年超过 1000 亿 kW, 造成上百亿美元的能源浪费。吸血鬼负载产生者包括手机充电器、膝上型计算机充电器、笔记本型计算机充电器、计算器充电器、小家电以及其它电池供电的消费型装置。

[0006] 美国能源部在 2008 年说:

[0007] “许多电器在关掉后仍继续汲取少量的电力。这些“幽灵”负载在使用电的大多数电器中发生, 例如 VCR、电视机、音响、计算机和厨房电器。这可通过拔去所述电器的插头, 或使用电源插排并在所述电源插排上使用开关来切断到所述电器的所有电力来避免。”

[0008] 根据美国能源部的说法, 以下类型的装置消耗待机电力:

[0009] 1. 用于电压转换的变压器。(包括使用壁式充电器的手机、膝上型计算机和笔记本、计算器和其它电池供电的装置)。

[0010] 2. 为关掉的装置供电的插墙式电力供给。(包括手机、膝上型计算机和笔记本、计算器、电池供电的钻孔机和工具, 其全部具有壁式充电器且其电池已完全充满电, 或实际上与所述装置断开)。

[0011] 3. 许多装置具有随开即用功能, 其立即响应用户动作, 而无热身延迟。

[0012] 4. 处于待机模式的电子和电气装置可通过遥控器来唤醒, 例如一些空调、视听设备, 例如电视机接收器。

[0013] 5. 电子和电气装置, 其可甚至在被关掉时也进行一些功能, 例如具有电动定时器。大多数现代计算机消耗待机电力, 从而允许它们被远程唤醒 (通过 LAN 唤醒等), 或在指定时间唤醒。即使不需要, 这些功能也总是被启用; 可通过从电源 (有时通过背后的开关) 断开来节约电力, 但只有在不需要功能性的情况下。

[0014] 6. 不间断电力供给 (UPS)

[0015] 所有这一切都意味着即使在手机、膝上型计算机或类似装置被完全充电时, 电流

也仍在流动,但不完成任何事情且浪费电。最近制造的装置和电器仍然整天、每天汲取电流,并且花费您的钱,还增加全世界的能源危机。

[0016] 国家标准和技术协会 (NIST) (美国商务部的一个部门) 在 2010 年通过其建筑技术研发小组陈述了其减少“插头负载”的目标,陈述如下:

[0017] “插头负载对总消费量的冲击相当大。对于商业建筑,估计插头负载占总能量使用的 35%,对于住宅为 25%,且对于学校为 10%。

[0018] 降低插头负载的机会包括:

[0019] 1) 更高效插拔的装置和电器,

[0020] 2) 自动化的开关装置,且断开不用的电器,并减小来自变压器以及其它小型但总是接通的电器的“吸血鬼”负载,或

[0021] 3) 改变占用人行为”。

[0022] 实际上,所有现代电子器件所经历的问题之一是电力供给(不管是外部还是嵌入式“电力模块”)不是节能的。这是真的,原因很多,其中之一要追溯到 1831 年,迈克尔·法拉第发明变压器的时候。变压器本来就是低效的,因为作为模拟装置,它们只能为每一特定绕组产生一个电力输出。因此,如果两个电力输出是必要的,那么需要两个二次绕组。此外,通常存在超过 50 个必需结合变压器工作的零件和工件,来创造常见的现代外部电力供给,对于内部或嵌入式电力模块,数字只是稍低。电力供给中的所述数目的零件本来就是低效的,因为电流必须在各种零件中、围绕各种零件和穿过各种零件行进,每一零件具有不同的功耗因子;且甚至电路迹线导致造成能源浪费的电阻性损耗。

[0023] 另外,变压器的工作方式是形成磁场和使磁场崩溃。由于无法通过磁场形成/崩溃来重获所有电子,因此那些逃逸的电子通常作为热量而逃逸,这就是手机、膝上型计算机和平板计算机充电器摸起来觉得暖或烫的原因。这也是所有消费型电子器件均产生热量的主要原因,这不仅浪费能源/电,而且通过其它相关联电子零件的发热,造成最终耗损。

[0024] 当前电子器件中发现的另一低效性是需要多个内部电力供给来运行不同零件。举例来说,在现代世界电力模块中,MOSFET 已成为电路中的“真实世界”接口的越来越重要的部分。

[0025] 金属氧化物半导体场效晶体管(MOSFET)实现切换、电动机/螺线管驱动、变压器介接以及许多其它功能。另一方面是微处理器。微处理器的特征在于稳定的降低的操作电压和电流,其可为 5 伏、3.3 伏、2.7 伏或甚至 1.5 伏。在大多数系统中,MOSFET 和微处理器一起或组合使用,来使电路工作。然而,最常见的是,微处理器和用于 MOSFET 的驱动器以不同电压操作,从而导致电路内需要多个电力供给。

[0026] 标准的高压 NMOS MOSFET 需要可递送 5 到 20 伏的栅极电压来成功将其接通和断开的驱动器。在接通的情况下,实际上存在栅极驱动器电压超过轨电力为有效的要求。已为此目的设计了使用电荷泵技术的专业驱动器。高压 MOSFET 栅极驱动器的另一主要功能是具有降低的输入驱动要求,使得其可与现代 CMOS 处理器的输出驱动能力兼容。

[0027] 此 MOSFET/驱动器布置(在大多数外部电力供给如充电器中是常见的)实际上需要三个单独的电力供给。需要的第一电力供给为主电力轨,其通常由供应到 MOSFET 的在 127VDC 到 375VDC 的范围内的经整流线电压组成。需要的第二电力供给为 MOSFET 驱动器所需的 15 伏(或更高)。最后,微处理器需要另一隔离的电力供给来用于其许多不同且变化

的电压。

[0028] 在典型的电视机中找到电流低效性和能源浪费的有力实例,典型的电视机需要至多达四个到六个不同的电力供应模块来运行屏幕、背光、主电路板,以及声音和辅助板。此电流系统需要多个变压器以及数十个零件来用于所需的每一电力供给。变压器和零件(包括 MOSFET) 通过其重复的低效性而增加热量,这是电视机的背部摸起来总是发烫的一个原因。另外,各种电力输出需要的变压器越多,就需要越多的零件,且造成能源浪费的越多原因。

[0029] 除热量问题之外,基于多变压器的电力供给全部需要通常从四十到六十个零件来操作,从而对于典型的基于变压器的电视机电力供应模块来说,需要数十个零件,这增加了成本和总组件大小,同时降低了可靠性。伴随着零件多样性的是增加的电阻,其以作为热量的浪费能源告终。

[0030] 本发明旨在解决上文所确定的问题中的一个或多个问题,以提供更好地有效性,且产生对来自轨来源的电涌流的较多控制。

发明内容

[0031] 在本发明的一个方面中,提供一种用于提供电力来用于充电应用和 / 或为电子装置的恒定供应电路供电的电路。所述电路包括:一次电力电路,其适于电耦合到电力源;以及二次电力电路,其电耦合到所述一次电力电路。一次电力电路被配置来接收来自所述电力源的交流 (AC) 输入电力信号,且产生中间直流 (DC) 电力信号。在 AC 输入情况下,中间 DC 电力信号是在小于 AC 输入电力信号的电压电平的第一电压电平下产生。二次电力电路被配置来接收来自所述一次电力电路的中间 DC 电力信号,并将输出 DC 电力信号递送到电子装置。所述输出 DC 电力信号是在小于中间 DC 电力信号的第一电压电平的输出电压电平下递送。

[0032] 在本发明的另一方面中,提供一种用于提供电力来用于为电子装置供电的电力模块,所述电子装置如监视器、电视机、大型家电、数据中心以及电信电路板。所述电力模块包括整流器电路、开关电容器电压击穿电路和控制器集成电路,以及正向转换器电路。所述整流器电路接收来自电力源的 AC 电力输入信号,且产生经整流的 DC 电力信号。所述开关电容器电压击穿电路和控制器集成电路接收所述经整流的 DC 电力信号,且基于感测所述 AC 电力输入信号的电压电平的集成控制器来产生中间 DC 电力信号,并依据所述感测到的电压电平来调整开关电容器电压击穿电路的增益。所述正向转换器电路包括变压器,其接收所述中间 DC 电力信号,且产生待递送到所述电子装置的输出 DC 电力信号。

[0033] 在本发明的另一方面中,提供一种用于 AC 到 DC 和 DC 到 DC 转换的高效开关电容器电压击穿电路。所述高效开关电容器电压击穿电路包括:一对并行电耦合的反激电容器;以及多个开关组合件,其电耦合到所述对反激电容器中的每一反激电容器。在一个实施方案中,电容器之间的栅极是共享的。可操作所述开关组合件来在充电阶段期间,选择性地将输入 DC 电力信号递送到所述对反激电容器中的每一反激电容器,且在具有比输入 DC 电力信号低的电压电平的放电阶段期间,选择性地将输出 DC 电力信号递送到电子装置。至少一个开关组合件可包括 N- 沟道 MOSFET 开关以及电平移位器,所述电平移位器用于将控制信号递送到所述 N- 沟道 MOSFET 开关。另外,迪克森电荷泵 (Dickson charge pump) 可耦合

到所述电平移位器,以接收输入 DC 电力信号,且产生具有比输入 DC 信号高的电压电平的输出电力信号。将所述输出电力信号递送到所述电平移位器,以用于操作 N- 沟道 MOSFET 开关(或关闭其它类型的 MOSFET)。另外,开关电容器电压击穿电路可包括控制电路,其包括:电压感测电路,用于感测输入 DC 电力信号的电压电平;以及增益控制器,其被配置来依据感测到的电压电平来选择开关电容器电压击穿电路的增益设定,且依据选定的增益设定来操作所述多个开关组合件中的每一个。

[0034] 所述电路还可包括吸血鬼负载消除系统,其被配置来确定消费型装置何时已完成充电和/或从电力电路断开,且操作所述电力电路以断开电力到所述电力电路和/或所述电子装置的供应,且还能够创建弱电“待机”模式。

[0035] 在本发明的另一方面中,所述电力电路形成于半导体芯片上,所述半导体芯片在同一芯片上包括模拟和数字组件。例如 350V 绝缘体上硅 (SoI)BCD 工艺等半导体工艺可用于所述半导体,这将允许在一个裸片上集成微控制器、定时器/石英实时时钟、PID 控制器和 PWM 控制器、MOSFET 以及对应的驱动器。另外,CMOS 技术中的典型特定电容的范围从 $0.1\text{fF}/\mu\text{m}^2$ (多极电容器) 到 $5\text{fF}/\mu\text{m}^2$ (MIM 电容器),或可考虑陶瓷电容器。此外,可使用如 DMOS 等工艺,或可考虑 bi/衬底,例如一层碳化硅,还可使用硝酸镓或二氧化硅 bi/衬底。或者,可使用硝酸镓或砷化镓以及深沟电容器的使用来构造不同于硅的芯片。由于低 $R_{\text{接通}}$ MOSFET 或晶体管需要的电容,所有这些选项都是必要的。

[0036] 可使用 BCDMOS 工艺来制造所述电力电路。BCDMOS 包括用于将双极(模拟)、CMOS(逻辑)和 DMOS(电力)功能集成在单个芯片上以用于超高电压(UHV)应用的工艺。BCDMOS 提供较宽范围的 UHV 应用,例如 LED 照明、AC 到 DC 转换和交换模式电力供给。通过能够直接与 110/220VAC 源“离线”操作,用非 Epi 工艺实施的集成电路(IC)可部署优化的 450V/700VDR-LDMOS 晶体管,其指定较低的接通电阻以及超过 750V 的击穿电压。当在电力切换应用中使用,设计者可预期较低的传导率和切换损失。

附图说明

[0037] 将容易了解本发明的其它优点,因为通过参考结合附图考虑时的以下详细描述,将更好地理解所述优点,其中:

[0038] 图 1 是根据本发明的实施方案的用于将电力提供给电子装置的电子充电装置的示意性图;

[0039] 图 2 是根据本发明的实施方案的可结合图 1 中所示的充电装置使用的用于将电力提供给电子装置的电力电路的框图;

[0040] 图 3 是根据本发明的实施方案的可结合如图 2 中所示的电力电路使用来形成“混合”电压击穿电路的降压调节器电路的示意图;

[0041] 图 4 到图 7 是根据本发明的实施方案的可结合图 2 中所示的电力电路使用的开关电容器电压击穿电路的示意图,包括电容器之间的栅极的共享以进一步降低 $R_{\text{DS(on)}}$ 损失;

[0042] 图 8 是根据本发明的实施方案的图 4 中所示的开关电容器电压击穿电路的一部分的示意图;

[0043] 图 9 是示出根据本发明的实施方案的结合图 8 中所示的开关电容器电压击穿电路使用的增益设定的表;

[0044] 图 10 到 12 是根据本发明的实施方案的与图 9 中所示的增益设定中的每一个相关联的处于充电阶段模式和放电阶段模式的图 8 中所示的开关电容器电压击穿电路的示意性例示；

[0045] 图 13 是根据本发明的实施方案的可结合图 2 中所示的电力电路使用的正向转换器电路的示意图；

[0046] 图 14 是根据本发明的实施方案的可结合图 2 中所示的电力电路使用的告警控制电路的示意图；

[0047] 图 15 是根据本发明的实施方案的包括电力控制器集成电路的图 2 中所示的电力电路的另一示意图；

[0048] 图 16、图 17A 和图 17B 是根据本发明的实施方案的图 10 中所示的电力控制器集成电路的框图；

[0049] 图 18 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的电力管理单元的框图；

[0050] 图 19 是可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的上电复位阈值电压的图形例示；

[0051] 图 20 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的比例积分和差分调节器控制电路的示意性例示；

[0052] 图 21 和图 22 是本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的数字控制块的框图；

[0053] 图 23 是示出根据本发明的实施方案的操作图 2 中所示的电力电路来用于将电力提供给电子装置的方法的流程图；

[0054] 图 24 是根据本发明的实施方案的可结合图 23 中所示的方法使用的状态转变的图形例示；

[0055] 图 25 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的通信接口的示意性例示；

[0056] 图 26 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的微处理器通信协议的示意性例示；

[0057] 图 27 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的跨集成电路的示意性例示；

[0058] 图 28 和图 29 是根据本发明的实施方案的图 2 中所述的电力电路的示意性例示；

[0059] 图 30 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的连接图；

[0060] 图 31 和图 32 是根据本发明的实施例的图 16、图 17A 和图 17B 中所示的电力控制器集成电路的额外示意性例示；

[0061] 图 33 是根据本发明的实施方案的可结合图 16、图 17A 和图 17B 中所示的电力控制器集成电路使用的用于低电流检测和误差检测的算法的流程图；

[0062] 图 34 和图 35 是根据本发明的实施方案的图 2 中所示的电力电路的示意性例示；

[0063] 图 36 是根据本发明的实施方案的可结合图 2 中所示的电力电路使用的电平移位器的示意性例示；

[0064] 图 37 是根据本发明的实施方案的可结合图 13 中所示的正向转换器电路使用的 RCD 电路的示意性例示；

[0065] 图 38 和图 39 是根据本发明的实施方案的图 2 中所示的电力电路的额外示意性例示；

[0066] 图 40 是根据本发明的实施方案的图 2 中所示的电力电路的一部分的示意性例示；以及

[0067] 图 41 是根据本发明的实施方案的图 2 中所示的电力电路的另一示意性例示。

[0068] 对应的参考符号在图式中始终指示对应部分。

具体实施方式

[0069] 参考图式且在操作中,本发明通过提供包括电力电路的电力模块来克服已知电力递送系统的缺点中的至少一些缺点,所述电力电路将 DC 电压输出动力从 AC 电源供给(通常为 120VAC(美国)到 240VAC[欧洲/亚洲])提供给消费型电子装置。所述电力电路被配置来提供电力为电子存储装置和/或电力消费型电子产品充电,包括但不限于手机、智能电话、平板计算机、膝上型计算机和/或任何可归因于极高的效率和非常低的待机电力要求而受益于本发明的合适电子装置。一般来说,所述电力电路包括一次电力电路和二次电力电路,用于从电力源接收高压 AC 电力,且将低压 DC 电力信号递送到一个或多个电子装置。所述一次电力电路接收来自 AC 电力供给的 AC 电力信号,且产生处于降低的电压电平的中间直流(DC)电力信号。所述二次电力电路接收来自一次电力电路的中间 DC 电力信号,且产生并递送具有适合用来为消费型电子装置供电和/或充电的电压电平的输出 DC 电力信号。

[0070] 所述一次电力电路包括:整流电路,其用于接收 AC 电力信号且产生经整流的 DC 电力信号;以及开关电容器电压击穿电路,其用于将经整流的 DC 电压分压为降低的电压以供二次电力电路使用。所述开关电容器电压击穿电路包括:反激电容器,其用以最大化电力效率;以及保持电容器,其用以最小化电压纹波。在一个实施方案中,所述开关电容器电压击穿电路被配置来在轻负载条件下递送至多达 50mA,且在从 50mA 到小于 1mA 的负载电流范围内维持 $\geq 95\%$ 的效率。所述一次电力电路还可包括开关模式降压调节器,其与开关电容器电压击穿电路并行连接,用于处置大电流负载,例如至多达 430mA 的电流。所述降压调节器可包括 P 沟道 MOSFET 开关、高压降压二极管以及降压储能电感器。另外,所述降压调节器还可包括脉冲宽度调制器(PWM)控制器,用于产生经脉冲宽度调制的信号来控制降压调节器 PMOSFET 的开/关时间,降压调节器 PMOSFET 也可表达为具有适当栅极驱动器的 NMOSFET。

[0071] 二次电力电路包括正向转换器电力电路,其包括变压器,所述变压器用于接收来自一次电力电路的中间 DC 电力信号,且产生输出 DC 电力信号。所述正向转换器还包括:MOSFET,其连接到所述变压器的一次侧;以及控制电路,其用以在从变压器的二次侧汲取负载电流时,操作所述 MOSFET 来调节正向转换器的输出处的电压。举例来说,正向转换器控制环路可被配置来在负载电流的重波动(4.5nA 到 4.5A)下调节输出电压,而不触发任何不稳定。

[0072] 在现代世界中,MOSFET 已成为“真实世界”接口的越来越重要的部分。MOSFET 实现电动机/螺线管驱动、变压器介接以及许多其它功能。另一方面是微处理器。微处理器

的特征在于稳定降低的操作电压和电流。在许多系统中,这些零件是一起使用的。标准的高压 MOSFET 需要可将大约 5v 到 20v 伏摆动递送到 FET 栅极以便成功接通或断开 FET 的驱动器。在为 NMOSFET 接通的情况下,实际上要求此栅极驱动电压超过电力轨电压。为此目的,已设计了使用电荷泵技术的专门驱动器,但其通常是离散零件,且增加了电路上所需的电力轨的数目。FET 驱动器的另一主要功能是具有降低的输入电压要求,使得其可与现代 CMOS 微处理器的输出端口能力兼容。此布置在电力方面是昂贵的,且通常需要三个电力供给。第一是主电力轨。所述主电力轨由供应到 MOSFET 的在 100 伏到 600 伏的范围内的电压组成。第二供给是驱动器所需的 5 伏到 20 伏,且最后是微处理器所需的供给。本发明将这些轨组合在芯片内,使得通常与所述电路相关联的电力和零件最小化,且因此使得效率增加。

[0073] 在许多情况下,电力供给构成小型系统中的零件计数和成本的重要百分比。综合零件可实质上更改此相等性。此新零件将由作为向其添加包括有电荷泵的适当驱动器的基座零件的高电力 MOSFET 的组合组成。还添加在内部从主轨供给得出的驱动器所需的电力供给。最后添加的是输出引脚,来从此内部供给为微处理器供应电力。在许多适度系统中,完整的零件列表将由此新装置、微处理器和主电力轨部分组成。这将允许下一代低成本 / 低组合件计数微处理器子系统。

[0074] 电力模块在芯片 (特洛尼姆 (Tronium) PSSoC) 上包括先进的电力供应系统,其为本发明的标的物,包括控制器专用集成电路 (ASIC),以提供低成本、高效率途径来将典型的家用或商用电插座处存在的 AC 线电压转换为用于消费型电子应用的降低的经调解 DC 电压。典型应用包括但不限于用于手机、平板计算机或其它手持式装置的充电系统、USB 电力转换、用于消费型、医疗和工业装置的电力供给,以及许多其它可能用途。

[0075] 特洛尼姆 PSSoC 被配置来用于两种一次电力模块应用中,包括自主电力模块和通用电力模块。自主电力模块在基于模拟反馈方法的自主操作模式下操作,以降低成本。通用电力模块在通用操作模式下操作,其利用微处理器 (μP) 控制器来提供对最终输出电压的调节的反馈,最终输出电压可为受控制 / 监视或更多的一个电力轨。特洛尼姆 PSSoC 的一些关键特征包括但不限于 90VAC 到 264VAC 线电压操作 (可使用其它输入电压, AC 或 DC)、可编程输出电压、用于 DC 到 DC 转换的混合开关电容器电压击穿电路和开关模式降压调节器 (其被同步整流,以实现效率)、用于实现高准确性的 PID 调节控制环路、用于电流和温度监视的数字状态机、用于闲置 (吸血鬼) 操作模式的超低电力耗散、用于配置和控制的光电隔离微处理器接口、用于制造测试的 I2C 从属端口、自动检测输入电压范围:127VDC 到 373VDC (全球电压 110VAC 到 260VAC)、特色输出电力:22.5W (任何瓦数都是可能的)、用于高效操作的混合电压转换器、堆叠式开关电容器电压击穿模块、具有 PWM 栅极驱动器的 PID 调节环路、在多个负载电平和弱电待机模式下实现高效率的电力缩放功能、热感测和关断、短路和过流保护、用重启和控制逻辑实现的可调整无负载 / 轻负载关断、可选模拟或数字控制、最小或无外部电路零件计数和离散装置大小,以及用于双向通信的任选数字接口。

[0076] 另外,开关模式降压调节器电路可包括通常称为降压 / 升压电路的电路;或者可用 SEPIC、Ćuk 或推拉或其它拓扑来代替降压 / 升压。这些都将具有同步整流以实现效率,且可使用反激或正向转换器类型。

[0077] 特洛尼姆 PSSoC 是一种先进的电力控制器集成电路,其被配置来提供具有高效率

和高准确性的输出电压调节。特洛尼姆 PSSoC 的先进特征向用户提供以“充电器”模式或“恒定供应”模式用于各种各样的应用中的多用途装置。对于特洛尼姆 PSSoC 来说,可编程输出电压(1.7V 到 48V 或更高)是可能的,在多种电流负载条件下具有很少或没有效率损失,此特征称为“拨电压”特征。另外,可通过混合电路的组合或开关电容器电路本身来产生多个输出电流,以便产生范围通常从 1.7V 到 48V 的多个电压/电流组合,其足以为大多数电子装置供电。此“拨电压”特征是可在工厂编程的或可由具有合适代码的顾客编程的,使得同一芯片可用于 1.7V 输出或 48V 输出,在如变压器绕组和驱动变压器的 FET 等任何外部组件中仅具有名义上的变化。

[0078] 特洛尼姆芯片上电力供应系统 (PSSoC) ASIC 是一种先进的电力控制装置,其实现非常宽输出电力范围上的高效率。虽然典型的“高效率”电力供应控制器吹嘘全负载的~50%向下到 10%的效率,但特洛尼姆装置意在提供全负载的 >90%向下到 1%且低于 1%的效率。

[0079] 特洛尼姆 PSSoC 通过实施中间电压轨来提供用于高压电力转换的革命性拓扑,从而允许所述系统的电力能力随负载需求而缩放。特洛尼姆 PSSoC 也将零件缩小成 ASIC,从而最小化所需的外部零件;并实现较宽范围的变压器选项来以较低的线圈损耗获得增强的电力优化。特洛尼姆 PSSoC 还提供 PID 切换控制器或其它转换和调节拓扑,如果需要隔离,那么使用所述 PID 切换控制器来驱动变压器的一次侧。特洛尼姆 PSSoC 的特征还在于二次或一次侧控制/反馈。

[0080] 在一个实施方案中,特洛尼姆 PSSoC 使用专有高压中间电压电容器电压击穿转换方案,其可单独使用,或结合开关模式降压调节器使用,来维持高效率,而不管负载电压或电流如何。当负载不在汲取电流时,装置将进入大约 1/2 毫瓦的低电流操作模式,以便最小化且实际上消除保持清醒所需的传统的“吸血鬼”电流。

[0081] 特洛尼姆 PSSoC 可包括以下主要电路块:中间电容器电压击穿转换器模块 (CVBD Module) (可为用于所要电流输出的一个或多个级);高压单级或两级开关电容器电压击穿电路;比例积分和差分 (PID) 调整器控制块,其用于正向转换器的 PWM 控制;开关模式降压调节器 PID 控制器(用于电压输出的任选混合类型);降压调节器开关驱动器;电流和温度感测块;用于电压和电流监视的 12 位 ADC;用于反馈控制的 10 位 DAC;用于电流监视状态机的数字控制块;用于光电隔离器通信接口的串行输入;用于测试、评估、修理和通信的 I2C 串行接口端口;用于产生内部时钟信号的振荡器;用于芯片上电压和电流产生的电力管理器;适合结合或不结合可嵌入芯片中或在外部的微控制器使用;一次侧感测或二次侧感测能力;以及同步正向转换器。

[0082] 所述电力模块还可包括特洛尼姆 PSSoC,其包括模拟和数字控制,以便优化性能和效率。以便不仅实现模拟控制,而且实现数字控制,适当的输入和输出必须在特洛尼姆 PSSoC 上可用。在给定这些可用性并与来自内部时钟的电力环路控制耦合的情况下,可用外部信号来驱动和控制所述时钟的控制。新颖方法是从二次侧驱动这些信号,而特洛尼姆 PSSoC 位于变压器的一次侧。

[0083] 通常在隔离势垒的同一侧上实现数字控制。然而,在给定特洛尼姆 PSSoC 内在为隔离系统,且需要端到端效率优化的情况下,可利用来自一次侧或二次返回到一次侧的控制。在给定特洛尼姆实施方式的情况下,这可用若干不同方式来实现。这可用发射来自微

控制器的数字控制信号以及来自电流感测电路的模拟信号的光电耦合器来完成。此外,这可通过在隔离变压器上使用第三绕组来完成。

[0084] 如果需要高效率,那么可使用硅工艺、氮化镓 (GaN) 或砷化镓 (GaA),或通过使用深沟电容器,或其它提供高效率零件的可用工艺来将电力电路中所包括的一些或所有电路和 / 或电气装置集成到芯片上。因此,这些零件中的一个或全部可使用已知的硅 (或 GaN-GaA) 变压器技术嵌入 ASIC 中,而不是外部离散件,甚至变压器也是如此。另外,将 MIM 和 MOM 电容器连同低 RDS_{ON} MOSFET、集成去耦电容器和 / 或飞跨电容器 (C_{FLY}) 用于纹波减少 (这又减小了所需电容器的大小) 可在本文需要电容器或 FETS 的地方使用。并且,芯片上的集成电感器的引入有助于实现最高效率。或者,将使用最高效率零件,如 GaA、GaN 或肖特基二极管零件。

[0085] 另外,所述电容器可为纳米电容器,且可基于铁电体和核壳材料,以及那些基于纳米线、纳米柱、纳米管和纳米多孔材料的电容器。

[0086] 用于特洛尼姆 PSSoC 的衬底可由电容器中 (如果在外部) 或半导体衬底内当前使用的惯例膜制成,例如高或低欧姆硅衬底、多晶硅。氮化镓、砷化镓、锗化硅,或如碳化硅或磷化铟等衬底。

[0087] 关键是在工艺允许的情况下,对尽可能多的离散件进行板上 ASIC 集成,且如果效率是关键,那么识别低 $RDS_{接通}$ 值、高效零件以及足够的电压击穿零件。另一关键是以较高的频率运行开关降压模块,使得零件变得较小,且小到足以成为板上芯片装置。

[0088] 现在将参考图式阐释本发明的选定实施方案。本领域的技术人员从本公开将明白,本发明的实施方案的以下描述是仅为了例示而不是为了限制本发明的目的而提供,本发明由所附权利要求书及其均等物界定。

[0089] 图 1 是用以将电力提供给电子装置的电子充电装置 10 的示意图。图 2 是可结合电子充电装置 10 使用的电力模块 12 的框图。在所示出的实施方案中,电子充电装置 10 包括外壳 14;一对电力耙 16,其从外壳 14 向外延伸;以及装置连接组合件 18,其适于连接到电子装置 20,以将来自充电装置 10 的电力递送到电子装置。电子充电装置 10 还包括电力模块 12,所述电力模块 12 包括:电力电路 22,其被配置来从电力源 24 接收电力,并将电力递送到电子装置 20,例如便携式消费型电子装置,包括但不限于手机、智能电话、平板计算机、膝上型计算机和 / 或任何合适的电子装置。另外,电力电路 22 可递送电力来用于为电子储存装置 (例如,移动电话 / 膝上型计算机 / 平板计算机电力储存电池) 充电。在一个实施方案中,电力电路 22 可被配置来提供来自 AC 电源供给 (通常为 120VAC (美国) 到 264VAC [欧洲 / 亚洲]) 的低压 DC 输出 (代表性为 5VDC)。

[0090] 在所示出的实施方案中,电力电路 22 包括一次电力电路 26 和二次电力电路 28。一次电力电路 26 适于电耦合到电力源 24,且被配置来从电力源 24 接收 AC (或 DC) 输入电力信号,且产生中间直流 (DC) 电力信号。所述中间 DC 电力信号是在小于 AC 输入电力信号的电压电平的第一电压电平下产生。二次电力电路 28 电耦合到一次电力电路 26,且被配置来接收来自一次电力电路 26 的中间 DC 电力信号,并将输出 DC 电力信号递送到电子装置 20。所述输出 DC 电力信号是在小于中间 DC 电力信号的第一电压电平的输出电压电平下递送。举例来说,在一个实施方案中,一次电力电路 26 被配置来接收具有介于 127 伏到 375 伏 AC 的范围之间的电压电平的 AC 输入信号,且以大约 110 伏 DC 的电压电平递送中间 DC 电力信

号。二次电力电路 28 被配置来接收中间 DC 电力信号,并以大约 5 伏 DC 递送输出 DC 电力信号。

[0091] 在所示出的 AC 到 DC 实施方案中,一次电力电路包括整流器电路 30、中间电压转换器 32、降压调节器 34 和保持电容器 36,保持电容器 36 电耦合到中间电压转换器 32 和降压调节器 34。中间电压转换器 32 和降压调节器 34 并行耦合在整流器电路 30 与二次电力电路 28 之间。整流器电路 30 被配置来接收来自电力源 24 的 AC 电力输入信号,并产生经整流的 DC 电力信号,其被递送到中间电压转换器 32 和降压调节器 34。在一个实施方案中,递送具有大约与 AC 输入电力信号的电压电平相等的电压电平的经整流 DC 电力信号。如图 13 和图 15 中所示,在所示出的实施方案中,整流器电路 30 包括多个二极管 38,所述二极管 38 布置在全波桥式整流器中,所述全波桥式整流器具有第一和第二输入端子,其耦合到电力源 24 的高侧和低侧,用于从 AC 输入电力信号产生 DC 电力信号。在一个实施方案中,整流器电路 30 还可包括滤波电容器 40,其耦合到所述全波桥式整流器。在又一实施方案中,整流器电路 30 不包括滤波电容器 40。在另一实施方案中,整流器电路 30 可包括半桥式整流器(未图示)。

[0092] 图 3 是可结合电力电路 22 使用的降压调节器电路 34 的示意图。在所示出的实施方案中,降压调节器电路 34 包括调节器开关组合件 42,其耦合到电压降低电路 44。电压降低电路 44 包括高压降压二极管 46、降压储能电感器 48 和电容器 50。调节器开关组合件 42 被操作来选择性地将经整流的 DC 电力信号递送到电压降低电路 44。在所示出的实施方案中,调节器开关组合件 42 包括 P 沟道 MOSFET 52、耦合到所述 P 沟道 MOSFET 52 的驱动器电路 54,以及耦合到驱动器电路 54 的电平移器 56。在一个实施方案中,调节器开关组合件 42 可包括 N 沟道 MOSFET 和 / 或 P 沟道 MOSFET。在所示出的实施方案中,降压调节器 34 还包括调节器控制电路 58,其包括调节器 PWM 控制器 60(图 16、图 17A 和图 17B 中也示出),用于产生控制 P 沟道 MOSFET 52 的经脉冲宽度调制的信号。在一个实施方案中,控制电路 58 还可包括电压感测电路 62,其连接到正向转换器变压器的一次侧,用于感测待递送到二次电力电路 28 的中间 DC 电力信号的电压电平。调节器 PWM 控制器 60 可依据感测到的第一电压电平产生经脉冲宽度调制的控制信号,以调整待递送到 P 沟道 MOSFET 52 的 PWM 控制信号的工作周期,来维持中间 DC 电力信号的电压电平。降压调节器伺服环路 58 是受电压控制的,且感测 $V_{\text{次}}$,并将其用来调制驱动器 54 的工作周期。

[0093] 在一个实施方案中,感测电路 62 包括一个或多个霍尔效应传感器,其耦合到正向转换器变压器的一次侧,用于感测所述变压器内正产生的磁场。霍尔效应传感器通过直接感测操作期间变压器正产生的磁场来确定变压器的零交越。在一个实施方案中,感测电路 62 包括一次侧霍尔效应传感器,其耦合到变压器的一次侧。一次侧霍尔效应传感器连接到 PWM 控制器 60,来将信号发射到 PWM 控制器 60,用于确定变压器何时接近“零交越”。在另一实施方案中,感测电路 62 包括二次侧霍尔效应传感器,其耦合到变压器的二次侧,且连接到正向转换器控制器(图 13 中示出),用于发射指示变压器磁场的信号,来用于确定变压器到达“零交越”的时间。

[0094] 图 4 到图 8 是中间电压转换器 32 的示意图。图 9 是示出可结合中间电压转换器 32 使用的增益设定的表。图 10 到图 12 是针对图 9 中所示的增益设定中的每一个而处于充电阶段模式 66 和放电阶段模式 68 的中间电压转换器 32 的示意性例示。在所示出的实

施方案中,中间电压转换器 32 包括单级开关电容器电压击穿电路,其耦合到保持电容器 36 和二次电力电路 28。所述开关电容器电压击穿电路包括并行电耦合的一对反激电容器 70,以及电耦合到所述反激电容器 70 中的每一个的多个开关组合件 72。开关组合件 72 在充电阶段模式 66 与放电阶段模式 68 之间选择性地操作。在充电阶段模式 66 期间,操作开关组合件 72 来形成充电电路 74,以将反激电容器 70 连接到整流器电路 30,来将经整流的 DC 电力信号递送到反激电容器 70 中的每一个。在放电阶段模式 68 期间,操作开关组合件 72 来形成放电电路 76,以将反激电容器 70 连接到二次电力电路 28,来将中间 DC 电力信号递送到保持电容器 36。

[0095] 在一个实施方案中,如图 8 中所示,单级开关电容器电压击穿电路 32 可包括第一反激电容器 Cfb1 和第二反激电容器 Cfb2,以及九个开关组合件 S1、S2、S3、S4、S5、S6、S7、S8 和 S9。另外,所述开关组合件中的两个 S3 和 S9 耦合到接地。在操作期间,可通过根据图 9 中所示的增益设定表选择性地操作开关组合件,来调整开关电容器电压击穿电路的增益设定。举例来说,在充电阶段模式 66(阶段 1)期间,接通开关 S1、S4、S7 和 S8,并将其移到闭合位置,且断开开关组合件 S2、S3、S5、S6 和 S9,并将其移到打开位置,以形成充电电路 74,来将反激电容器 Cfb1 和 Cfb2 连接到整流器电路 30。如图 10 到图 12 中所示,在充电电路 74 中,每一反激电容器 Cfb1 和 Cfb2 的顶板连接到整流器电路 30 的线电压, $V_{\text{线}}$ 。对于等于 $G = 1x$ 的增益设定,在放电阶段模式 68(阶段 2)期间,接通开关组合件 S2、S3 和 S7,且断开开关组合件 S1、S4、S5、S6、S8 和 S9,以形成图 10 中所示的放电电路 76,其包括连接到保持电容器 36 的电容器 Cfb1 的顶板,以及连接到电容器 Cfb1 的底板的电容器 Cfb2 的顶板。参考图 9 和图 11,对于等于 $G = 1/2x$ 的增益设定,在放电阶段模式 68(阶段 2)期间,接通开关组合件 S2、S5 和 S9,且断开开关组合件 S1、S3、S4、S6、S7 和 S8,以形成放电电路 76,其包括连接到保持电容器 36 的电容器 Cfb1 的顶板、连接到接地的电容器 Cfb1 的底板,以及连接到保持电容器 36 的电容器 Cfb2 的顶板、连接到接地的电容器 Cfb2 的底板。参看图 9 和图 12,例如,增益设定等于 $G = 2/3x$,在放电阶段模式 68(阶段 2)期间,接通开关组合件 S2、S6 和 S9,且断开开关组合件 S1、S3、S4、S5、S7 和 S8,以形成放电电路 76,其包括连接到保持电容器 36 的电容器 Cfb1 的顶板、连接到电容器 Cfb1 的底板的电容器 Cfb2 的顶板,以及连接到接地的电容器 Cfb2 的底板。

[0096] 在一个实施方案中,如本文所阐释,开关电容器电路的多个“级”链接在一起,其可用来获得额外的电流输出,需要或不需要添加混合电力转换 / 调节电路。

[0097] 参看图 7,在所示出的实施方案中,开关电容器电压击穿电路 32 还包括控制电路 78,其耦合到开关组合件 72 中的每一个,来操作开关电容器电压击穿电路 32。控制电路 78 包括:电压感测电路 80,其用于感测正从整流器电路 30 接收的经整流的 DC 电力信号的电压电平;以及增益控制器 82,其被配置来依据感测到的电压电平来选择开关电容器电压击穿电路 32 的增益设定,且依据选定的增益设定来操作多个开关组合件中的每一个。通过提供依据感测到的输入电压电平来选择开关电容器电压击穿电路 32 的增益设定的控制电路 78,开关电容器电压击穿电路 32 能够调整开关电容器电压击穿电路 32 的操作,来解决不同国家和 / 或电网的 AC 电压电平的变化,并递送处于预定义电压电平的中间 DC 输出信号,且维持最佳电力效率。在所示出的实施方案中,控制电路 78 包括电阻分压器 84、一对比较器 86、逻辑解码器 88 和增益控制器 82。比较器 86 的负输入连接到带隙产生器,且正输入连接

到整流器电路 30 的线电压, $V_{\text{线}}$ 。

[0098] 参看图 4 到图 6, 在所示出的实施方案中, 一个或多个开关组合件包括 N- 沟道 MOSFET 开关 90, 以及电平移位器 92, 其连接到 N- 沟道 MOSFET 开关 90, 用于将控制信号递送到 N- 沟道 MOSFET 开关 90, 以促进操作 N 沟道 MOSFET 90。另外, 一个或多个开关组合件 72 包括迪克森电荷泵 94, 其连接到电平移位器 92, 以提供在操作期间关闭 N 沟道栅极所需的高压信号。迪克森电荷泵 94 被配置来产生具有大于开关组合件源电压的电压电平的输出电力信号, 以使电平移位器 92 能够操作 N- 沟道 MOSFET 开关 90。在一个实施方案中, 开关组合件 72 中的每一个包括 N 沟道 MOSFET 90、耦合到 N 沟道 MOSFET 90 的电平移位器 92, 以及耦合到电平移位器 92 的迪克森电荷泵 94。在另一实施方案中, 两个或两个以上电平移位器 92 可连接到单个迪克森电荷泵 94。在本说明书中使用术语 NMOS 的任何地方, 都可用 PMOS 来代替 NMOS, 且反之亦然。

[0099] 在所示出的实施方案中, 至少一个开关组合件 72 包括电平移位器 92, 其连接到 N- 沟道 MOSFET 开关 90。另外, 迪克森电荷泵 94 连接到电平移位器 92, 以提供足以关闭 N- 沟道 MOSFET 开关 90 的栅极的电力信号。在所示出的实施方案中, 迪克森电荷泵 94 连接到 N 沟道 MOSFET 的源电压, $V_{\text{源}}$, 且被配置来将输出信号递送到电平移位器 92, 所述输出信号具有比源电压 (在使用 NMOS 的情况下为 $V_{\text{源}}$) 的电压电平大的电压电平。在一个实施方案中, 迪克森电荷泵 94 被配置来递送具有比源电压 $V_{\text{源}}$ 大大约 15 到 20 伏的电压电平的输出电力信号 V_{DCP} , 以便确保适当的栅极操作。增益控制器 82 连接到电平移位器 92, 来用于将低压控制信号提供给电平移位器 92。电平移位器 92 连接到源电压 $V_{\text{源}}$, 且连接到迪克森电荷泵 94, 并且被配置来将具有足以依据接收到的控制信号来操作开关组合件 72 的电压电平的电力信号递送到 N 沟道 MOSFET 90。

[0100] 图 13 是包括正向转换器电路 96 的二次电力电路 28 的示意图。在所示出的实施方案中, 正向转换器电路 96 包括一次电压降低电路 98 和二次电压降低电路 100。一次电压降低电路 98 被配置来接收来自一次电力电路 26 的中间 DC 电力信号, 并将二次 DC 电力信号递送到二次电压降低电路 100。二次 DC 电力信号具有比中间 DC 电力信号的电压电平小的电压电平。二次电压降低电路 100 被配置来接收二次 DC 电力信号, 并产生待递送到电子装置 20 的输出 DC 电力信号。

[0101] 在所示出的实施方案中, 一次电压降低电路 98 包括变压器 102。变压器 102 的一次侧连接到一次电力电路 26, 且变压器 102 的二次侧连接到二次电压降低电路 100。在一个实施方案中, 一次电压降低电路 98 可包括: 开关组合件 104, 其包括耦合到变压器一次侧的 FET; 以及耦合到开关组合件 104 的控制电路 103, 用于选择性地操作开关组合件 104, 来调整二次 DC 电力信号的电压电平。变压器控制电路 103 可包括一次侧电压感测电路 105, 其用于感测 DC 输出信号的电压和电流电平, 且操作变压器开关组合件 104 来使 DC 输出信号的电压电平维持在预定义的输出电压电平和所需的电流电平。以此方式, 至少五个部分被从等式去除, 这五个部分对于二次侧感测控制器来说通常是需要的, 包括光电耦合器、运算放大器、电感器、二极管和电容器。二次电压降低电路 100 包括一对二极管、一个电感器和一个电容器。正向转换器 96 还可包括电阻器、电容器、二极管 (RCD) 电路 150 (图 37 中示出)。RCD 电路 150 被配置来在一次侧开关 104 断开时执行变压器复位, 来避免使变压器 102 饱和。正向转换器 96 是基于脉冲的降压型转换器。将经工作周期调制的数字脉冲施加

到一次侧开关 104, 以将传入的 DC 电压转换成 AC。变压器绕组比提供降压。在此情况下, 所述降压是从 11:1 开始。二次侧在其端子上经历 ac 电压。此 AC 电压由二次电压降低电路 100 的二极管整流, 且由 LC 滤波器来滤波, 以在输出上产生经降压的 DC 电压。工作周期由模拟或数字伺服环路调制。此伺服环路考虑输出侧上的 dc 电压, 将其与响应进行比较以产生误差信号。使用此误差信号来驱动比较器, 比较器将此误差转换成经脉冲宽度调制的 DC 脉冲。此 DC 脉冲在被施加到一次侧开关栅极 104 时, 校正输出上的误差, 并维持针对各种负载水平的调节。

[0102] 在一个实施方案中, 变压器控制电路 103 可包括一次侧电流感测电路 107, 其连接到变压器 102 的一次侧, 以感测负载电流和负载电压, 来促进将 DC 输出信号调节到预定义的负载电压的 5% 内。控制电路 103 使用电流感测电阻器 109, 且跨越一次绕组进行测量。在所示出的实施方案中, 变压器控制电路 103 包括驱动 FET 104 的比较器 111。在一个实施方案中, 电阻器 109 为 0.10 欧姆电阻器。控制电路 103 被配置来在逐脉冲基础上感测负载电流, 且感测峰电流。举例来说, 在一个实施方案中, 控制电路 103 感测电阻器 109 上的电压, 并在开关 104 接通时, 以电压格式提供感测电流。当开关 104 断开时, 控制电路 103 感测变压器 102 的一次侧上的差分电压, 其可大约等于 $V_{\text{一次}}$ 减去截止晶体管 104 的漏极。当晶体管 104 断开时, 其上存在漏极电压, 因此, 所述漏极电压也是锯齿波信号。使用开关电容器取样和保持电路来对电压和电流两者进行取样, 所述开关电容器取样和保持电路被按比例缩小到低电压, 且包括电阻分压器来设定一次绕组的差分电压部分, 并将所述电压带入取样和保持电路中。差分电压等于绕组上的 ΔV , 包括 $V_{\text{一次}}$ 以及 $V_{\text{一次}}$ 的最低点。取样和保持电路以及电阻分压器使一次电压下降小于 5 伏, 接着取计算出所述 ΔV 的差分。所述取样和保持电路驱动比较器 111。比较器 111 的另一输入为在 0.1 欧姆电阻器 109 上感测到的取样和保持峰电流电压。到比较器 111 中的输入被按比例缩放, 并获得上调和偏移量, 使得所述输入处于稳定状态, 且比较器 111 驱动设置 - 复位流时钟。FET 104 包括由比较器 111 驱动的 AND 门。比较器 111 的时钟调整 AND 门的工作周期。AND 门也具有由高脉冲宽度时钟驱动的高工作周期, 所述高脉冲宽度时钟为锯齿波信号。AND 门的另一输入为比较器 111 的输出, 因此比较器 111 将所述工作周期调制到小工作周期或大工作周期。在一个实施方案中, 所述时钟为用于正向转换器伺服环路的 100KHz 时钟。

[0103] 无需来自变压器的三次绕组作为传感器的供给。所述供给可从一次侧获得, 因为感测电路位于一次侧, 且无需来自二次侧的供给。使用一次侧电感器上的电压以及去往一次侧 FET 104 的电流来确定所述系统的输出电压。在一个实施方案中, FET 104 包括具有 2 伏阈值的 200 伏飞利浦零件装置, 其使用 5v 信号来驱动 FET 104, 以将其接通, 而无电平移位。在另一实施方案中, 可结合电平移位器使用 10 伏 LDO 或 20 伏 LDO 来从 5 伏转到 10 伏, 或从 5 伏转到 20 伏来操作 FET 104。

[0104] 在所示出的实施方案中, 控制电路 103 使用位于 MOSFET 104 的漏极路径中的感测电阻器 109 来实施门控方法, 其中正当开关 104 在 PWM 周期中的每一方波之间接通时, 取样和保持电路获得峰电压。当开关接通时, 门控布置进行取样, 因为当开关断开时, 那时不存在可用信息。

[0105] 在所示出的实施方案中, 电力电路 22 被配置来适应具有不同匝数比的不同变压, 以产生具有各种电流和 / 或电压要求的 DC 输出信号。

[0106] 在一个实施方案中,电力电路 22 可不包括全波桥 38、整流器电路 30 和输入电容器 40,使得 $V_{\text{线}}$ 为 DC,且因此如果使用情况需要,那么所述电路可接收直流 (DC),且使用经调节的降压电路 34 来进行如本文进一步阐释的电压击穿,且仍使用开关电容 VB 32。然而,在一些使用情况下,尤其是对于低 DC 到 DC 电压击穿,将不需要降压调节器 34,且仅将使用开关电容 VB 32,不管仅将使用哪一阶段(如图 2 到 12 中所示)。在此情况下,可将控制信号 105 从所述输出消除,且仅依靠电流感测电阻器 109,并仍维持经严格调节的电压。

[0107] 在另一实施方案中,对于所述电路的 DC 输入变化,使用情况可能不需要变压器(如果电压/电流转换不需要变压器,或如果不需要隔离),类似于在例如智能电话中发现的内部零件的情况下。在此例子中,变压器是不必要的,且可连同驱动所述变压器的 FET 一起从所述电路去除。在此情况下,可去除整个正向转换器控制器电路 96、28,且将用感测电阻器电路段 109 来代替 $C_{\text{保持}}$ 电容器 36。另外,如果不需要整流或隔离 AC 电路,那么此电路可结合 AC 以及 DC 来工作。

[0108] 图 15 是包括可结合电力电路 22 使用的电力控制器集成电路(特洛尼姆 PSSoC) 106 的电力模块 12 的示意图。图 16、图 17A 和图 17B 是特洛尼姆 PSSoC 106 的框图。在所示出的实施方案中,电力模块 12 包括印刷电路板 108 和特洛尼姆 PSSoC 106,特洛尼姆 PSSoC 106 形成于封装芯片内,且耦合到印刷电路板 108。电路 22 的至少一部分包括在特洛尼姆 PSSoC 106 内。另外,可通过在芯片外部或嵌入在芯片上的微处理器或者状态机来进行数字控制。在一个实施方案中,包括在电路 22 中的电路和电组件中的一些或全部是包括在特洛尼姆 PSSoC 106 内。特洛尼姆 PSSoC 106 可被配置来用于两个一次电力模块应用中,包括自主电力模块(图 16 和图 28 中所示)和通用电力模块(图 17A、图 17B 和图 29 中所示)。举例来说,如图 16 中所示,自主电力模块包括特洛尼姆 PSSoC 106,其被配置来在基于旨在降低成本的模拟反馈方法的自主操作模式下操作。图 17A 和图 17B 中所示的通用电力模块包括特洛尼姆 PSSoC 106,其被配置来在通用操作模式下操作,且利用微处理器(μP)控制器来提供用于最终输出电压的调节的反馈。

[0109] 在所示出的实施方案中,特洛尼姆 PSSoC 106 被配置来满足对可追溯性、标记、可焊性和/或耐溶剂性的预定义要求。对特洛尼姆 PSSoC 106 进行标记来指示日期代码、工厂识别符以及可追溯性/真实性代码。真实性代码提供抵制“盗版”而识别和检验正版零件的途径。载带和卷轴上的所有生产封装的组件包括同样的唯一日期代码、工厂识别符和可追溯性/真实性代码。此方式中存在许多分隔,来防止同样多的组件内的日期代码的混合。将对封装的零件进行标记来指示零件编号、日期代码和可追溯性代码。端子被配置来满足针对经封装特洛尼姆 PSSoC 的可焊性要求 IPC-J-STD-001 和 IPC-J-STD-002。封装的特洛尼姆 PSSoC 及其标记被配置来满足 MIL-STD-202 测试方法 215 的要求。

[0110] 特洛尼姆 PSSoC 106 是被设计来提供具有高效率和高准确性的输出电压调节的先进的电力控制器集成电路。特洛尼姆 PSSoC 106 向用户提供可在各种各样的应用中使用多功能装置,且由于“拨电压”特征,同一芯片可被配置来在实际上任何电子装置中工作。同样地,对于特洛尼姆 PSSoC 来说,可编程输出电压是可能的,在多种电流负载条件下具有很少或没有效率损失。

[0111] 在所示出的实施方案中,特洛尼姆 PSSoC 106 使用开关电容器电路 32 和开关模式降压调节器 34 来维持高效率,而不管负载电压或电流如何。举例来说,当电子装置 20 的负

载不在汲取电流时,特洛尼姆 PSSoC 106 进入低电流操作模式,以最小化保持清醒所需的传统的“吸血鬼”电流。在所示出的实施方案中,特洛尼姆 PSSoC 106 包括单级开关电容器电路 32;PID 调节器控制块 110(图 20 中示出),用于正向转换器二次变压器 102 的 PWM 控制;开关模式降压调节器控制器 112;降压调节器开关驱动器 114、电流和温度感测块 116;12 位模/数转换器(ADC)118,用于电压和电流监视;10 位数/模转换器(DAC)120(图 17A 和图 17B 中示出),用于反馈控制;用于电流监视状态机的数字控制块 122;用于光电隔离器通信接口的串行输入;I2C 串行接口端口;以及用于芯片上电压和电流产生的电力管理器单元 124。也可依据使用情况,添加其它类型的传感器,例如声音、光电检测、辐射和震动。

[0112] 图 18 是电力管理单元 124 的框图。在所示出的实施方案中,电力管理单元(PMU)电路块 124 产生并监测特洛尼姆 PSSoC 的适当操作所需的偏压和电流。两个线性电压调节器为 IC 的低压电路,也例如光电隔离器和任选的外部微处理器等外部支持装置,提供经调解的 5.0V 供给。除在连接到线电压后即刻提供 IC 的适当初始化之外,PMU 124 还监视针对故障条件的电压供给,并提供主上电复位(POR)126。在所示出的实施方案中,PMU 124 包括带隙电压参考、电流参考产生器;线侧低电力线性电压调节器、变压器一次侧线性电压调节器以及上电复位。为了减少电力损耗,从 LINE_OP1 引脚为线侧电路供电,所述 LINE_OP1 引脚供应大约为 LINE_IN 电压($V_{\text{线}}$)的十分之一的电压。使用连接到 IC 的 LINE_IN 和 LINE_RDIV 引脚的外部电阻分压器来在内部产生此电压。PMU 124 的初始化以在 LINE_IN 引脚处施加经整流的电压而开始。

[0113] PMU 124 含有用于特洛尼姆 PSSoC 106 的低电力带隙参考电压和电流产生器,从线电压为特洛尼姆 PSSoC 106 供电。提供高精确性经温度补偿的输出电压来连同多个带隙与绝对温度成正比(PTAT)电流输出,用作后续电路块的参考。在晶圆探针处修整带隙输出电压,以用 bg_修整[7:0]寄存器位来优化温度系数,且将所述带隙输出电压存储在可编程一次(OTP)的存储器中,所述存储器存储在微处理器中。带隙电池是自起动的,仅需要用于初始化的默认修整值。在休眠模式期间,带隙电池未停用,而是一直通着电,且为超低电力操作而设计。

[0114] PMU 124 还包括低电力线性电压调节器(LPREG),提供所述低电力线性电压调节器来将 PSSoC 的 LINE_IN 输入处存在的高压转换成低电力电压域的经调节电压。LPREG 使用带隙参考电压来产生 5.0V 的经调节的输出来驱动总是通着电的低电力芯片上电路块,包括用于开关电容器电路 32 的低频振荡器、芯片上逻辑等。连接到 LPREG 引脚的外部(芯片外)旁路电容器可用于噪声滤波。调节器在休眠模式期间未停用,而是总是通着电。

[0115] PMU 124 还可包括一次侧低压调节器,提供一次侧低压调节器来满足芯片外光电隔离器、PWM 栅极驱动器和其它支持电路的较高电流要求。需要连接到 VREG5 引脚的外部 10 μ F 旁路电容器来进行噪声滤波。出于测试目的,通过使用 en_Xv 信号来停用所述电压调节器。当到电池的 en_Xv 输入为“低”时,所述电池中的所有内部模拟电流被停用,且输出为高阻抗。

[0116] POR 126 的块监视特洛尼姆 PSSoC 的如由 LPREG 电路块产生的内部供应电压。举例来说,图 19 示出可结合 POR 126 使用的 POR 阈值电压。在一个实施方案中,对于 LPREG 引脚处小于 V_{POR} 阈值电压的电压, POR 输出将被断言为“高”,其指示复位条件。另外,对于 LPREG 引脚处大于 V_{POR} 阈值电压的电压, POR 输出将被解除断言为针对正常操作为“低”。提

供滞后,使得一旦超过 V_{POR} 阈值,就发生阈值电压的减小。从滞后得出的阈值于是等于 $V_{POR} - V_{HYS}$ 。POR信号的反相版本也在POR_B处提供。

[0117] 在所示出的实施方案中,通过电容性电压击穿技术(CVBD),将包括在特洛尼姆PSSoC 106中的开关电容器电压击穿电路(SCVBC)32配置为分压器。通过电容器,分压器将LINE_IN引脚处存在的经整流的DC电压分压为CP2_OUT引脚处的降低的电压,以供外部变压器102和二次电压控制环路使用。外部变压器102接着依据一次与二次绕组比,经此电压进一步降低到所要的施加电压。在一个实施方案中,SCVBC 32被配置为两个相同级的级联,如图17A中所示。在另一实施方案中,SCVB 32包括多个开关电容器级,如图38到图39中所示。SCVBC 32被配置来针对每电容性击穿块递送至多达50mA,所述电容性击穿块由提供一半或其它分数的电压击穿的开关电容器块组成。这变压器102的一次侧上,在轻负载条件下,在从50mA到小于1mA的负载电流范围内,提供并维持 $\geq 95\%$ 的效率。举例来说,为外部变压器和整流器假定 $\geq 97\%$ 的效率, $\geq 92\%$ 到 97% 的总模块效率已被模拟,且为可实现的。在一个实施方案中,SCVBC 32可包括:芯片上反激电容器,用以最大化电力效率;外部 $2.2\mu F$ 降压电容器以及两个外部 $7.5\mu F$ 保持电容器,用以最小化电压纹波。这些电容器连接到分别用于开关电容器电路的第1和第2级的输出的CP1_OUT和CP2_OUT引脚。从得自芯片上RC振荡器的两级非重叠时钟产生器以1KHz的速率对两个级进行计时。

[0118] 参看图17A和图17B,在一个实施方案中,对于特洛尼姆PSSoC 106,可使用8位经二元加权的数/模转换器,在120伏到90伏的范围内,以0.117伏的步长对CP2_OUT处的SCVBC 32输出电压进行编程。SCVBC输出限于此范围,以确保正向转换器变压器102提供降压过程中的输出电流的大部分。SCVBC限于50mA的输出电流。如果应用需要额外电流,那么启用开关模式降压调节器34来提供至多达430mA的电流。可对SCVBC 32的每一级进行编程,以产生电压转换比。此编程是在过程增益控制中自动进行,其中将经整流的LINE_IN电压与8位DAC设定进行比较。此DAC的数字控制使得能够编程多个电压,以获得目标应用所需的所要最终输出电压。DAC可依据变压器匝数比来对负载电压的实例进行编程。

[0119] 参看图16,在一个实施方案中,SCVBC 32可包括单级开关电容器电路,其具有1、0.66或0.5的对应分压比。接着通过外部(芯片外)正向转换器96来降低存在的输出电压,以获得5.0V的最终应用输出电压。用于SCVBC(和降压控制器)的所有模拟和数字信号均在5V域中产生。使用电阻分压器将SCVBC误差电压缩放到在XV域内。还缩放LINE_IN电压,使得可在XV电压域内进行处理。

[0120] 在图16中所示的一个实施方案中,SCVBC 32包括增益控制块,其使用经缩放的LINE_IN电压来确定用于SCVBC 32的适当分压比。将经缩放的LINE_IN电压与带隙参考电压进行比较,来依据AC电源电压来选择三个或多个可能分压比中的一个。可在开关电容器调节器中执行输出电压的最后调节,其中接通和断开时钟,来控制递送到保持电容器的电荷的量。

[0121] 参看图17A和图17B,在一个实施方案中,SCVBC增益控制块可使用经缩放的LINE_IN电压和输出电压DAC设定,来确定从CP1和CP2中的组合分压器步长得出的适当过程分压比。以此方式,可实现作为全球AC输入电压的函数的120伏和90伏输出的设定值。在开关电容器调节器中执行CP2输出电压的最后调节,其中接通和断开时钟,来控制递送到CP1和CP2保持电容器的电荷的量。应针对CP1级,对CP1和CP2所需的最低分压比进行编程,

来最小化高压 NMOS 开关上的电压降。

[0122] CP2 输出馈送正向调节器的一次绕组。系统的最终输出电压由以下等式设定：

$$[0123] \quad (V_{\text{设定}} / \text{XFMR}_{\text{比率}}) * \text{dc} = V_{\text{输出}}$$

[0124] 其中 dc 是正向调节器的工作周期,且应维持在 0.5 或以下,以确保系统变压器不饱和。

[0125] SCVBC 32 包括迪克森电荷泵 (DCP) 94 (图 5 和图 6 中示出),其可用来为 NMOS 高压开关的栅极提供升高的电压。可以 1.6MHz 的时钟速率来对 DCP 进行计时,且产生等于 LINE_IN 引脚处的电压加大约 18V 的栅极电压。另外,每一 NMOS 高压开关 90 可包括对应的电平移位器,以将来自低压域的驱动信号转变为 DCP 所提供的升高的电压。在一个实施方案中,这需要双重电平移位器,其它要求可仅需要一个电平移位器。到电平移位器的输入为 5V,且被转变到 20V 域以供 SCVBC 32 使用。可在特洛尼姆 PSSoC 106 各处使用这同一类型的电平移位器,其为输出电流驱动而缩放。

[0126] 在一个实施方案中,如图 17A 和图 17B 中所示,特洛尼姆 PSSoC 106 可包括数 / 模转换器 (DAC),其为开关电容器电路的输出电压提供可编程性。R2R 电流模式 DAC 拓扑以数字方式将带隙参考电压缩放为开关电容器电路维持用户所编程的输出电压所需的控制电压。DAC 的输出电压范围是从 120V 到 90V,其通过 CP_DAC[7:0] 寄存器位以 118mV 的步长来编程。

[0127] SCVBC 32 还可包括开关电容器调节器,其包括比较器和 AND 门,所述 AND 门用于控制 SCVBC 的充电。在一个实施方案中,比较器的输入可包括输出电压 DAC,以及 CP2 输出电压的经缩放版本。举例来说,如果来自 CP2 输出的经缩放电压大于 DAC 电压,那么比较器输出较低,且 1KHz CP 时钟被门控关闭。如果 DAC 电压大于经缩放的 CP2 输出电压,那么比较器输出被断言为高,且 AND 门使时钟能够为所述输出充电。另外,比较器可设计有滞后,以便最小化 CP2 输出电压纹波。此外,调节器可以不连续模式来运行两个 CP 级;就是说,时钟脉冲仅在需要 7.5 μ F 保持电容器的充电时存在。

[0128] 在所示出的实施方案中,如果不使用 CVBD 模块的堆叠,那么容易通过使用包括开关模式降压调节器 (SWR) 34 和 CVBD 模块的混合拓扑来处置大电流负载 (至多达 430mA 或以上)。特洛尼姆 PSSoC 106 含有用于 SWR 34 的控制器,其利用外部 (芯片外) PMOS 开关 (其可在芯片 PMOS 或 NMOS [具有用于栅极的额外迪克森电荷泵] 内部),以满足负载的高电流需求。由于高电流路径在 PSSoC 外部,因此不要求 PSSoC 耗散负载电流的大部分。这通过消除 PSSoC 中归因于高压装置的接通电阻的额外寄生损失的来源来改进总体系统效率。可在与 CVBD 模块相同的频率下调节 SWR,或在较高 (500KHz 到 1MHz) 到非常高的频率下运行 SWR,同时 CVBD 模块在较低频率下运行,以便保持更高效。(CVBD 模块可在较高频率下运行,但对于如今的半导体平台中所提供的电流装置,这增加了门开 / 关,从而增加了损耗)。

[0129] 在一个实施方案中,降压调节器 34 可包括以下外部 (芯片外) 组件: 1. 系列高 PMOS 开关。可针对低 RDS_{on} 、低输入电容以及 >400V 的 V_{DS} 来选择所述 PMOS 开关; 2. 具有高伏特击穿、极低泄漏和切换电流的高压降压二极管; 以及 3. 降压储能电感器。电感器必须具有低 ESR,且能够处置适当调低的电流。然而通常取决于运行降压的频率 (频率越高,所需零件的价值越小),这些零件可为芯片上的内部装置 / 组件,且不在外部。通过应用 GaN 和 / 或 GaAs 以及深沟电容器技术,以及将变压器置于芯片上的技术,所有零件可存在于一个

芯片。

[0130] 特洛尼姆 PSSoC 106 还可包括高频振荡器,其被分频以产生 100KHz (标称) 时钟,供降压调节器 PWM 控制器使用。通过数字控制块中的伪随机算法来使 100KHz 时钟抖动,以确保对 EMI 谱中的谐波的抑制。接着对此时钟进行脉冲宽度调制,以控制外部降压调节器 PMOS/NMOSFET 的开 / 关时间。将 100kHz 时钟转换成特洛尼姆 PSSoC 106 内部的锯齿斜坡,在特洛尼姆 PSSoC 106 处,将锯齿斜坡于误差放大器输出进行比较。接着将来自比较器输出的经脉冲宽度调制的信号施加到电平移位器输入,来控制外部降压调节器 PMOSFET 的开 / 关时间。降压调节器 34 的误差放大器通过借助于使用电阻分压器对 CP2_OUT 处的电压进行缩放,接收来自调节器的反馈。接着使用内部电阻器和电容器来调节电压反馈信号,以控制降压调节器在所有条件下的响应。用于调节伺服环路的所得转移函数由多个极点和零组成,以确保调节器输出针对从 50mA 到 430mA 的整个负载条件范围都是稳定的。用于降压调节器的误差放大器和 PWM 控制器全部位于 5 伏域中,其中最终控制信号经电平移位,以驱动外部高压 PMOSFET 开关。

[0131] 特洛尼姆 PSSoC 106 还可包括 LDO 降压调节器 128,其用来产生驱动用于降压调节器 34 的 PMOS NMOS FET 的栅极所必需的高侧电压。接着使用此电压来供应驱动外部 PMOS/NMOS FET 所需的栅极电压。连接电容器来进行滤波。

[0132] 在所示出的实施方案中,特洛尼姆 PSSoC 106 包括特洛尼姆 PSSoC 的电流感测放大器,其在引脚 RCSP 和 RCSN 处感测外部电流感测电阻器上的电压。此电压由开关电容器差分放大器来取样和保持,并且由芯片上通用 ADC 数字化。接着将数字字对照所编程的阈值进行比较,以按照需要启用或停用降压调节器 34 来优化效率。还监视电流感测放大器的输出,看是否有可能的故障或告警条件,例如过电流,从而允许控制电流感测反馈的数字状态机停用 SCVBC 32 来防止可能的损坏。

[0133] 特洛尼姆 PSSoC 106 还可含有至少两个自由运行的 RC 振荡器,其共享共用修整控制器,包括 16KHz RC 振荡器和 9.6MHz RC 振荡器。可使用 osc_trim(振荡器_修整)寄存器位来修整振荡器频率。

[0134] 低频 (16KHz)RC 振荡器为线侧 RC 振荡器,在 LINE_IN 处施加线电压之后,所述线侧 RC 振荡器连续地运行。所述线侧 RC 振荡器由 LPREG 调节器供应。将此振荡器输出频率下分到某一数字,如 1KHz,来为 SCVBC 32 提供时钟。在所述情况下,振荡器输出也被用作休眠模式关断定时器的参考时钟。高频 (9.6MHz)RC 振荡器提供用于解码单线串行数据输入的主时钟。使振荡器的 9.6MHz 输出除以 6,以提供开关电容器电路中的迪克森电荷泵所需的主时钟。进一步对所述时钟进行分频,来为降压调节器和正向转换器 PWM 控制块提供时钟源。通过数字逻辑进行的伪随机算法来使 100KHz 时钟抖动,以确保对 EMI 谱中的谐波的抑制。振荡器可由 osc_en(振荡器_启用)寄存器位来启用,且由线侧上的 LPREG 调节器供电。

[0135] 在所示出的实施方案中,特洛尼姆 PSSoC 106 包括超低电力 ADC 118,来将温度传感器和电流感测放大器模拟电压数字化。这些数字化的电压可接着由数字控制块进行比较,以停用或重启模拟电路。ADC 使用逐次逼近 (SAR) 拓扑来获得低电力且增强的 INL/DNL 性能。到 ADC 的输入由多路复用器提供。多路复用器可选择感兴趣的信道中的每一个来由 ADC 数字化。接着将经转换的样本值存储在 ADC_SAMP 寄存器中,以供控制状态机使用。ADC

使用低压供给,且将在装置处于休眠模式时被停用。

[0136] 图 20 是可结合特洛尼姆 PSSoC 106 使用的比例积分和差分 (PID) 调节器控制电路 110 的示意性例示。在所示出的实施方案中,特洛尼姆 PSSoC 106 包括 PID 伺服环路 130, 以在从外部变压器的二次侧汲取负载电流时,调节正向转换器 96 的输出处的电压。PID 块包括误差放大器、锯齿波形产生器、比较器和 PWM 时钟控制块。设计 PID 环路来在负载电流的重波动下调节输出电压,而不触发任何不稳定性。

[0137] PID 缓冲放大器接收反馈来关闭经由 AUTO_ERR 输入的正向调节环路。这是将表示正向转换器的输出电压的电压提供给 PSSoC 的光电隔离器的输出。接着在 PSSoC 上用电阻分压器来缩放此电压,并为误差放大器而缓冲。

[0138] 用于自主 PID 环路的误差放大器位于具有芯片上补偿电阻器和电容器的特洛尼姆 PSSoC 上。误差放大器使用带隙电压作为 PID 伺服环路的参考。锯齿或其它波形产生器为 PID 伺服环路提供基于时钟的脉冲宽度调制 (PWM) 手段。所述电路接收来自数字逻辑的 100KHz 时钟,并将其转换成将与误差放大器的输出进行比较的同一频率的锯齿波形。误差放大器和锯齿波形产生器的输出由 PID 比较器进行比较,以产生驱动正向转换器所需的 PWM 时钟。提供工作周期限制器来确保 PID 比较器所提供的 PWM 输出不超过 65%。在 FWDOUT 引脚处施加此输出,来驱动外部变压器。在正常操作中, PWM 工作周期限于 10% 到 65% 的范围,以避免变压器的饱和。

[0139] 在一个实施方案中,将 PID 伺服环路设计成在低压下操作,并将所需 DC 电流的最大值递送到负载。通过在二次侧上使用 LC 滤波器。且通过适当地设计三级补偿网络的内部 R 和 C 的大小,可以至多达较高百分比的绝对准确性来控制所述调节。通过以下等式给出 LC 滤波器双极: $FLC = 1/2 \pi \sqrt{L1C4}$ 。

[0140] C1 电容器具有某一 ESR (系列电阻器),其产生零。此零产生 +90 度的相移: $FESR = 1/2 \pi C1RESR$ 。

[0141] 补偿环路具有大约为正向转换器的时钟速率的十分之一的某一带宽 (F_c)。所述网络的目标是在 F_c 下维持至少 45 度的相位裕量: $\text{相位裕量} = 180 \text{ 度} + \text{环路相位}$ 。

[0142] PID 环路具有 2 个零和 2 个极点。2 个零是必要的,以提供 180 度的相升,以便否定归因于输出 LC 滤波器而导致的 180 度相位损耗。两个零均放于 LC 滤波器极点频率的约 50% 处。两个极点于是位于转换器的切换频率 (100KHz) 处。这允许我们计算 C1、C2、C3、R2 和 R3。将 R1 设定为合理值,以便开始计算程序。

[0143] 在另一实施方案中,将 PID 伺服环路设计成为可由所需应用的用户编程的多个输出电压而操作。通过至多达 0.1% 的绝对准确性的调节,所述环路可将 I_{ny} 电流 (但在此所示出的情况下, 4.5A 的 DC 电流) 递送到负载。用于通用环路的反馈由外部微处理器和电压感测支持电路提供,且作为串行数据流输入到特洛尼姆引脚。接着对转换为模拟电压的数字字执行并行到串行转换,以应用于误差放大器,如图 20 中所示。用以传入数据速率的频率更新的芯片上 DAC 来执行到模拟的转换。PID 误差放大器的参考电压由被微处理器编程的第二 DAC 产生。

[0144] 数 / 模转换器 (DAC) 基于来自微处理器的数字经编程输入来产生用于 PID 控制环路的模拟参考电压。如图所示的所述数 / 模转换器 (DAC) 为 10 位方案,但可为任何数目的位。所述 DAC 还可通过将从引脚接收到的数字字转换成用于输入到环路的模拟电压来提供

用于 PID 控制环路的反馈。将 DAC 电压输入到误差放大器,并将其与模拟参考电压进行比较,以产生控制环路的误差电压。DAC 以传入数据的速率将更新提供给环路。

[0145] 参看图 17A 和图 17B,在一个实施方案中,特洛尼姆 PSSoC 106 可包括芯片上基于 ΔV 的温度传感器,其使 IC 能够感测裸片或模块的温度。在此实例中,使用通用 12 位 ADC 来数字化差分电压。接着将数字化的值与可编程阈值进行比较,以便依据温度关注来关断或再启用特洛尼姆 PSSoC。

[0146] 在所示出的实施方案中,特洛尼姆 PSSoC 106 提供在加电后应用两种操作模式以及四种苏醒状态 (W0 到 W3)。

[0147] 启动模式。在启动模式期间,特洛尼姆 PSSoC 控制当第一次施加电力时或当电话被插入 (在充电器情况下) 时,模块的启动行为。当电力第一次连接到 AC 电源时,存在于 IC 的 LINE_IN 引脚处的经整流和滤波的 LINE 电压增加,直到其达到其最后 DC 值为止。特洛尼姆 PSSoC 的基础支持电路因此被加电,以起始电力管理功能。图 24 中示出示例性启动事件序列的时序图,以在 $t = 0$ 处施加 LINE_IN 电压开始。

[0148] 线侧具有总是通电的三个电路块:1. 低电力带隙参考;2. 低电力 5V 调节器 (LPREG);以及 3. 低频 RC 振荡器。其它电路可被供电,但在此实例中,已减少到此例子中的三个,以便汲取极低待机电力。这些电路直接从 LINE_IN 输入汲取电流而无变压器动作,以增加可用电流。因此,所述电路被设计用于极低电力消耗。或者,可启用变压器,但这将降低效率。

[0149] 正常模式。在施加电力且完成苏醒状态之后,特洛尼姆 PSSoC 106 将进入正常操作模式。维持正常操作模式,直到电压 / 电流变为熄灭或超过低电流阈值为止,其中通常电池系统内部的微芯片开始抵抗电流以防止过载。在正常操作模式下,由于检测到负载电流,特洛尼姆 PSSoC 退出休眠模式。当降压调节器和 SCVBC 供应必要的电流时,对负载的调节发生。在此操作模式下,所有的特洛尼姆电路均通电,且响应外部刺激。

[0150] 在一个实施方案中,通过组合正常模式、启动模式和休眠模式的元件,电池可被提供“突然”充电。在此例子中,当芯片中的逻辑确定已执行完整充电,意味着从较高电流到较低电流的汲取已结束给定时间周期时,将执行另一模式,称为突然充电模式。此突然充电操作模式可存在于状态机中,或经由 I2C 接口来启用 / 停用,且将指令所述电路“断开”若干次,并开始再充电至多达大约 150 毫安的最大阈值,其间存在间隔。以此方式,将提示电池接收额外的涓流充电,以确保其真的充满,而不是仅在装置电池指示器上表明“充满”。这将解决手机仅充电到其电池容量的 80% 到 90% 的问题,因此随着时间的过去,虽然指示器仍显示电池处于 100%,但其实际上是电池容量的 80% 的 100%,而不是电池容量的 100% 的 100%。在突然充电模式下,特洛尼姆 PSSoC 数字提供高于休眠阈值的额外电流阈值,使得下文陈述的休眠模式功能不受损害。

[0151] 休眠模式。当连接到 AC 电源电力且不需要充电或电力供应功能时,特洛尼姆 PSSoC 必须使用最小电力。这要求电路 22 具有至少两个不同电力域:1) 线侧域,以及 2) 一次侧域。线输入侧是必须能够在所有时间均被供电的域。还存在用于迪克森电荷泵的 1.6MHz RC 振荡器。此振荡器在休眠模式下保持关闭。将 16KHz 振荡器用作倒数计时器,来在已达到所编程的倒计时时间时,唤醒特洛尼姆 PSSoC。

[0152] 在所示出的实施方案中,特洛尼姆 PSSoC 106 包括数字控制块 122,其向用户提供

在设置、可编程、正常、测试或评估操作模式中管理特洛尼姆应用的许多方面的能力。微处理器或状态机被提供来监视开关电容器电路的输出电压和电流,且包括可配置寄存器,其为正常操作模式和低电流或“休眠”操作模式两者提供特征选择和可编程性。当应用需要时,还为外部装置提供通信接口。

[0153] 图 21 是可结合特洛尼姆 PSSoC 106 使用的特洛尼姆通用数字控制块 132 的框图。图 22 是可结合特洛尼姆 PSSoC 106 使用的特洛尼姆自主数字控制块的框图。图 23 是示出操作电力电路 22 的方法的流程图。图 24 是可由特洛尼姆 PSSoC 106 实施的状态转变的图形例示。

[0154] 参看图 21,在一个实施方案中,特洛尼姆 PSSoC 106 包括通用数字控制块 132。特洛尼姆通用数字控制块 132 提供以下功能来控制通用模块:控制状态机、时钟产生器、ADC 控制器、时钟抖动器 LSFR、I2C 接口单或双通信模式、可编程通信模式、微处理器接口、测试/评估多路复用器和/或寄存器堆。

[0155] 控制状态机或微处理器/微控制器通过监视开关电容器电路的输出电流来确定特洛尼姆模块的适当操作模式。提供至少两种操作模式,包括休眠模式和正常调节模式。在首次施加电力后,或在退出休眠模式时,控制状态机或微处理器还提供四种唤醒 PSSoC 的状态,加所述突然充电模式。另外,状态机或微处理器连续地监视输出电压电流来识别过电流或欠电流告警条件。

[0156] 开关电容器输出电流的监视是在模拟子系统中或在微处理器中通过使用电流感测放大器和模/数转换器(ADC)来实现。数字控制块提供 ADC 的控制,且可执行对 ADC 的周期性增益和偏移校正。接着将 ADC 样本与控制状态机所需的开关电容器电流的所编程的数字阈值进行比较。

[0157] 时钟产生器提供模拟和数字子系统所需的时钟,且还使时钟门控能够最小化休眠操作模式下的电力消耗。

[0158] 数字控制块提供单线串行接口来经由外部微处理器支持 PSSoC 的可配置性;或多线接口,其将支持特洛尼姆 PSSoC 与微处理器或状态机之间的双向通信。包括时钟抖动线性反馈移位寄存器(LSFR)来产生用于使正向和降压调节器 PWM 时钟抖动的伪随机数字。所述伪随机数字由模拟子系统用来使高频振荡器输出抖动。包括 I2C 端口来用于制造设定、测试、评估、更新、健康检查和调试。可使用 I2C 接口来接入含有用于装置操作的配置寄存器的寄存器堆。提供数字多路复用器来将各种内部数字信号选择性地多路复用到 DIGTST 输出引脚,来实现测试目的。

[0159] 参看图 22,在一个实施方案中,特洛尼姆 PSSoC 包括自主数字控制块 134,其提供用于控制自主模块的以下功能:控制状态机或微控制器;时钟产生器;ADC 控制器;时钟抖动 LSFR;I2C 接口;测试多路复用器和寄存器堆。控制状态机通过在 CP_OUT 引脚处监视开关电容器电路的输出电流来确定特洛尼姆 PSSoC 106 的适当操作模式。提供两种操作模式,包括休眠模式和正常调节模式。控制状态机或微控制器还提供四种状态,来在第一次施加电力后,或在从休眠模式退出时唤醒 IC。另外,状态机监视过-欠电流告警条件和突然充电模式下的输出电流。

[0160] 通过使用电流感测放大器来在模拟子系统中实现开关电容器输出电流的监视,且在此实例中使用 12 位模/数转换器(ADC)。数字控制块提供对 ADC 的控制,且可对 ADC 执

行周期性增益和偏移校正。接着将 ADC 样本与控制状态机和 / 或微控制器所需的开关电容器电流的所编程数字阈值进行比较。

[0161] 时钟产生器提供模拟和数字子系统所需的时钟, 且还使时钟门控能够最小化休眠操作模式或突然充电模式下的电力消耗。

[0162] 包括时钟抖动线性反馈移位寄存器 (LSFR) 来产生用于使正向和降压调节器 PWM 时钟抖动的伪随机数字。所述伪随机数字由模拟子系统用来使高频振荡器输出抖动。

[0163] 包括 I2C 端口来用于制造设定、评估、升级、复位、芯片健康检查、测试和调试。可使用 I2C 接口来接入含有用于装置操作的配置寄存器的寄存器堆。

[0164] 提供数字多路复用器来将各种内部数字信号选择性地多路复用到 DIGTST 输出引脚, 以用于测试目的。

[0165] 在所示出的实施方案中, 特洛尼姆自主数字控制块 134 包括状态机, 以基于负载电流确定自主模块的适当操作模式。

[0166] 如图 23 和图 24 中所示, 控制状态机提供四种苏醒状态 (W0、W1、W2 和 W3) 以及两种操作模式: 正常模式和休眠模式。

[0167] 苏醒 0 (W0) — 当施加电力时, 线侧电路苏醒: 带隙 (BG) 和低电力调节器 (LPREG) 加电。在 LPREG 稳定之后, por_b 被释放, 且系统转变为苏醒 1 (W1)。

[0168] 苏醒 1 (W1) — 低频振荡器 (LF_OSC) 和增益控制 (GAIN_CTRL) 得以启用。在同一时间, 高频振荡器 (HF_OSC) 和电荷泵 (CP) 得以启用。将 CP 设定为不调节。当 LF_OSC 稳定时, 释放数字块的 lf_clk, 此时 (a) 10ms 计数器启动, 且 (b) 到开关电容器的 1kHz 时钟变为活动。当 10ms 计数器到期时, 系统转变为苏醒 2 (W2)。

[0169] 苏醒 2 (W2) — 开关调节器 (SWR) 得以启用, 将 CP 设定为调节, 且 1ms 计数器启动。当 1ms 计数器到期时, 系统转变为苏醒 3 (W3)。

[0170] 苏醒 3 (W3) — 正向 PID 得以启用, 且两个计数器启动: 20ms 计数器和 250ms 计数器。以下情形引起从此状态的转变: a. 20ms 计数器期满, 且正向 PID 超驰选项开启: 系统转换为正常模式 (NM); b. 20ms 计数器到期, 正向 PID 超驰选项关闭, 且正向 PID 在 250ms 计数器到期之前稳定: 系统转变为正常模式 (NM); c. 休眠模式未停用, 正向 PID 超驰选项关闭, 且当 250ms 计数器到期时, 正向 PID 尚未稳定: 系统转变为休眠模式。

[0171] 正常模式 (NM) — 电流感测块 (CUR_SNS) 和 ADC 得以启用。如果自校准未停用, 那么 ADC 使用最初两个样本来进行增益和偏移校准, 并在第三样本就绪时, 用信号通知 ADC 数据是好的。如果自校准被停用, 那么 ADC 用编程在指定寄存器中的值来执行增益和偏移校正, 并在第三样本就绪时, 用信号通知数据是好的。当 ADC 数据是好的时, 所述系统监视电流负载。以下相互排斥的条件 (其阈值可编程) 可发生: 1. 过电流条件: 系统设定过电流状态位。如果休眠模式未停用, 那么系统转变为休眠模式 (SM); 以及 2. 负载不足条件: 如果 LCSD_EN 引脚较高, 且休眠模式未停用, 那么系统转变为休眠模式 (SM); 以及 3. 低负载条件: 当系统检测到低负载条件时, 关断 SWR, 且当低负载条件平息时, 重新将 SWR 接通。

[0172] 休眠模式 (SM) — 系统停用 HF_OSC、CP、SWR、正向 PID、CUR_SNS 和 ADC。休眠模式还启动休眠计数器, 其持续时间是可编程的。默认休眠时间大约为 5 秒, 其可依据使用应用来调整。如果正向 PID 先前在进入休眠模式时尚未稳定, 那么系统保持在休眠模式。在此情况下, 可通过触发 EXT_RST 引脚而在 W1 中重启系统, 或通过去除电力来在 W0 中重启系统。

如果正向 PID 在进入休眠模式时是好的,那么当休眠计数器到期时,系统转变为 W1 状态。

[0173] 在所示出的实施方案中,通过经由电流感测放大器和 ADC 检视开关电容器电路的输出电流来实现正常操作模式与休眠操作模式之间的转变。另外,如果负载电流降低到所编程的数字阈值,那么控制状态机可停用 SWR 降压调节器。图 24 的图式中示出电流和对应模式转变的监视。

[0174] 参看图 21 和图 22,数字控制块 122 可,包括时钟产生器,其产生数字子系统所需的所有时钟。提供彼此异步的三个时钟域,低频时钟域、高频时钟域和 I2C 时钟域。

[0175] 模拟子系统到低频振荡器为数字子系统提供时钟,在所示出的实例中为 16kHz 时钟 (1f_clk)。除寄存器堆所使用的时钟之外,时钟产生器从 1f_clk 得出以下时钟: 1. sys_clk—具有 50% 工作周期的 8kHz 时钟,其对控制状态机进行计时。2. adc_gclk—sys_clk 的门控版本,其对 ADC 控制器进行计时。在休眠模式下,门控关闭此时钟。3. 1fdiv_clk—将用于模拟块中的具有 1kHz、2kHz 或 4kHz 的可编程频率且具有 50% 工作周期的经分频时钟。在休眠模式下,门控关闭此时钟。

[0176] 在模拟子系统中,可经由 TSTMD0 输入来旁路振荡器,以实现从 EXT_CLK 引脚施加 16kHz 时钟。

[0177] 模拟子系统的高频振荡器提供 1.6MHz、50% 工作周期时钟,其由时钟产生器进一步分频以产生 hfdiv_clk。hfdiv_clk 可经由寄存器堆来编程,以提供 100kHz、200kHz 和 400kHz 的频率。要针对时钟抖动 LFSR 以数字形式来使用 hfdiv_clk,且针对降压调节器和正向 PID 环路以模拟形式来使用 hfdiv_clk。当以模拟形式停用 HF 振荡器时,时钟在休眠模式下切断。

[0178] I2C 接口使用 SCLK 引脚处的时钟输入来控制 I2C 端口的操作。支持至多达 100Kbps 的数据速率。

[0179] 在所示出的实施方案中,数字控制块 122 还包括 ADC 控制器,其产生用于模拟子系统内的通用 12 位 ADC 的控制信号。数字控制块 122 还经由 ADC 多路复用器以及 CONTROL0 寄存器中的 ADC_MUX_SEL 寄存器来控制对到 ADC 的用于转换的输入的选择。ADC 输出格式为量值。当 ADC 首次被启用时,数字控制块执行自校准例程一次。数字控制块可以可配置地使用在自校准期间计算的增益和偏移校正值,或可使用写入到 ADC_GAIN 和 ADC_OFFSET 寄存器的增益和偏移校正值。

[0180] 在自校准例程期间,如下文所述来确定偏移和增益校正值。

[0181] 首先如下确定偏移:设定 ADC 输入多路复用器来选择 Reflo 参考电压。进行一次 ADC 转换。理想值将为 0。将 ADC 转换数据加载到本地 ADC 偏移校正寄存器中。

[0182] 接下来如下确定增益:设定 ADC 输入多路复用器来选择 Refhi 参考电压。进行一次 ADC 转换。理想值将为 4095。用 (ADC 转换数据 - 偏移校正)/4095 的结果来加载本地 ADC 增益校正寄存器。

[0183] 在自校准阶段之后,如下校正 ADC 转换值:经 ADC 校正的数据 = (ADC 转换数据 - 偏移校正)/4095。

[0184] 时钟抖动 LFSR 提供伪随机数字来实施 1.6MHz 时钟上的抖动以减轻 EMI。LFSR 为 12 位、最大序列、伽罗瓦 (Galois) 型 LFSR,其具有多项式 $x^{12}+x^6+x^4+x+1$ 。如下文的表中所示来产生抖动值。可用控制寄存器中的 dith_en 寄存器位来选择性地启用或停用时钟抖

动 LFSR。

[0185] 在一个实施方案中,特洛尼姆 PSSoC 数字控制块 122 可包括可配置递减计数器,其具有 0.512 秒到 16.384 秒的范围,以实施休眠定时器功能。步长为 512mS。计数器从时钟产生器块接收其时钟,在时钟产生器块处,所述时钟从 LF 振荡器时钟下分频。用在 SLEEP_CTRL 寄存器中编程的休眠_时间值来加载所述计数器。计数器将从此值开始倒计数,直到其达到零为止,此时其通知控制状态机休眠定时器已到期。

[0186] 图 25 是可结合特洛尼姆 PSSoC 106 使用的通信接口的示意性例示。图 26 是可结合特洛尼姆 PSSoC 106 使用的微处理器通信协议的示意性例示。在所示出的实施方案中,通信可为单向或双向的。特洛尼姆 PSSoC 106 含有一个或多个通信接口,此处描述为三个接口:1) 微处理器接口,2) 单或双通信/更新接口,用于编程值或将信息返回到状态机/微处理器,和 3) 测试/评估接口。对于某些产品来说,微处理器接口将用来与外部微处理器通信,通信/更新接口可更新微处理器或芯片内部的任何值。这允许产品可配置性,且允许实施用于特洛尼姆充电器的控制环路。对于特洛尼姆 PSSoC,这可为读取/写入或只写接口,即依据所确定的通信的类型(单向或多边),微处理器将或不能够从 PSSoC 读取。

[0187] 测试/评估接口将在制造测试环境下使用,且用于特洛尼姆 PSSoC 的台架评估。测试/评估接口将允许对芯片上寄存器的写入和读取存取。将使用升级、评估、健康检查和复位接口来重新编程芯片、改变其电压/电流输出,或改变控制逻辑的其它可重新编程的部分,包括阈值,以及运行扫描来帮助确定芯片是否有任何问题(健康检查)。

[0188] 通常,一次只能选择一个接口,但这可基于状态机或微处理器设定而改变。当“1”时,IF_SEL 输入引脚选择 I2C,且当“0”时,IF_SEL 输入引脚选择微处理器接口。

[0189] 微处理器通信接口。特洛尼姆 PSSoC 还可提供单线串行接口来支持 PSSoC 的可配置性。所述接口由单向或多向数据输入/输出组成。图 26 中示出协议。除非另有必要,否则所有包在结构和长度上都将是同质的。每一包将为某一数目个位。下文描述包字段。通过添加另一根线,可具有双通信接口,使得信息为多向的。

[0190] 为了支持可靠通信,所述数据可为按照 IEEE802.3 通信标准进行曼彻斯特(Manchester)编码的。接收器将接着使用过取样时钟来维持包上的位同步。位速率将为 600Kbps。传入数据将由是位速率的 16 倍的因子过取样。过取样时钟因此为 9.6MHz,且源自芯片上 RC 振荡器。

[0191] 启动:单个位,其值为信号线的非闲置状态。对于本申请,这将为“1”。R/W:用以指示读取或写入请求的单个位。当“0”时,将数据写入到选定的特洛尼姆寄存器。注意,特洛尼姆仅支持写入存取。Addr[4:0]:用来寻址特洛尼姆配置寄存器的 5 个位。数据[9:0]:将被写入到选定特洛尼姆寄存器的 10 个位。对于目标寄存器小于 10 个位的情况,将使数据右对齐。举例来说,当写入到八位寄存器时,数据[7:0]将被写入到所寻址的寄存器位置。闲置:单个位,其值为信号线的闲置状态。对于本申请,此将为“0”。

[0192] 数据以 MSB 首先传送。举例来说,主机在时间上先发射 Addr[4]。取决于编程,特洛尼姆实施方式将或支持主机对 ASIC 寄存器的读取操作。包括 R/W 位来用于未来扩展。

[0193] 图 27 是可包括在特洛尼姆 PSSoC 106 中的跨集成电路 136 的示意性例示。在所示出的实施方案中,特洛尼姆 PSSoC 106 含有 I2C 从属端口来支持装置的测试。可使用 I2C_

ADDR 引脚来配置 I2C 地址。将 I2C_ADDR 输入与 I2C 从属地址位进行比较。图 27 中示出特洛尼姆 I2C 总线协议。I2C 接口支持至多达 100Kbs 的位传送率。I2C 接口将 I2C SCLK 时钟输入进行完。

[0194] I2C 写入操作：特洛尼姆 PSSoC 支持向 I2C 从属端口上的特洛尼姆存储器映射的寄存器的写入。在接收到与特洛尼姆 I2C 地址匹配的 I2C 从属地址之后，图 27 中示出为字节 1 的下一字节将含有用于特洛尼姆寄存器堆地址的 5 位地址字段。特洛尼姆 PSSoC 仅支持每命令一个寄存器的存取。

[0195] I2C 读取操作：特洛尼姆 PSSoC 支持从 I2C 从属端口上的特洛尼姆存储器映射的寄存器的读取。读取操作需要两个 I2C 操作。第一，向 RDREQ 寄存器的 I2C 写入，其中字节 2 中的数据为要读取的寄存器的特洛尼姆存储器映射地址。接着，I2C 读取命令将读取所请求的寄存器。特洛尼姆仅支持每命令存取一个寄存器。

[0196] 注意，I2C 写入操作与更新 RDREQ 寄存器的时间之间存在延迟。这意味着在 I2C 写入操作之后，I2C 主机必须等待 400 微秒，之后进行 I2C 读取操作。此等待时间仅适用于 I2C 写入之后的第一 I2C 读取，以更新 RDREQ 寄存器。

[0197] 在特洛尼姆 PSSoC 的一个实施方案中，数字存储器具有智能，其中如果特洛尼姆 PSSoC 正为电视机供电，如果电视机从某一时间周期到另一时间周期未被使用，例如午夜到上午 7 点钟，持续固定的天数，那么特洛尼姆在这些时间期间将总是使自身处于休眠模式，以节约能源，且不重新参与唤醒序列的电流感测例程。

[0198] 在本发明的另一实施方案中，特洛尼姆 PSSoC 通过其 I2C 接口连接到无线（如 **BlueTooth®**）或电力线类型的通信协议和装置（外部、芯片上或模块上），以便接收对状态机或微处理器的指令。以此方式，可存在给予特洛尼姆的关于何时进入休眠模式、何时苏醒，以及复位、升级或改变其它前提条件（如过电压或 PWM 调解）的“实时”指令。以此方式，特洛尼姆 PSSoC 可具有对其控制机制的“实时”感测和切换，以实现不同等级的频率、速度或适应低电力情形，如在一些国家中，其中电网在大部分的时间期间通常欠压运行。在此情况下，特洛尼姆 PSSoC 可获得关于复位、操作或关断 / 重启的实时信息，包括来自其所有人，甚至通过使用家用通信技术内部的电池系统来自手机或平板计算机的实时命令。在此情况下，一人可能想要在离开时关断到由特洛尼姆 PSSoC 供电的特定电子设备或电子装置的电力，且这可通过经由无线或有线通信技术的通信接口来实现，从而通过特洛尼姆 PSSoC 中的 I2C 接口给出特定指令，指令其关断所述装置，且甚至预设所述装置应苏醒的时间。

[0199] 在本发明的另一实施方案中，且当用作充电器或恒定供应电力时，特洛尼姆 PSSoC 足够小，以配合到附接至电绳的壁式插座中，因此消除了对充电器“盒”或膝上型计算机“砖形物”的需要。

[0200] 在一个实施方案中，特洛尼姆 PSSoC 106 具有若干测试结构，以支持制造、编程、评估、升级、健康检查、通信、测试和台架评估。特洛尼姆 PSSoC 针对关键内部功能和控制信号的可控性和可观察性提供两个测试寄存器。TEST_CTRL0 寄存器向用户提供选择性地启用、停用或超驰特洛尼姆 PSSoC 中的个别模拟电路功能的控制的能力，以提供需要旁路控制状态机的替代控制方法。TEST_CTRL1 寄存器提供将内部模拟和数字信号多路复用到 ANATST 和 DIGTST 输出引脚以用于测试目的的能力。

[0201] 鉴于以上教导，本发明的许多修改和变化是可能的。在所附权利要求书的范围内，

可用于具体描述的方式不同的方式来实践本发明。

[0202] 图 30 是可结合特洛尼姆 PSSoC 106 使用的链接图。图 31 和图 32 是特洛尼姆 PSSoC 106 的额外示意性例示。图 33 是可结合特洛尼姆 PSSoC 106 使用的用于低电流检测和误差检测的算法的流程图。图 34 和图 35 是包括特洛尼姆 PSSoC 106 的电力电路 22 的示意性例示。在所示出的实施方案中,特洛尼姆 PSSoC 106 为高级电力控制器集成电路 (IC)。特洛尼姆 PSSoC 106 和对应的集成模块提供低成本、高效率途径来将典型的家用或商用电插座处存在的 AC 线电压转换为用于消费型电子应用的降低的经调节的 DC 电压。典型应用包括但不限于用于手机、平板计算机或其它手持式装置的充电系统、USB 电力转换、用于消费型、医疗和工业装置的电力供给,以及许多其它可能用途。

[0203] 通过上文所陈述的配置和特征,特洛尼姆 PSSoC 提供高效率、低噪声和低 EMI。另外,AC 到 DC、DC 到 DC 转换器具有高电力密度、低成本和电隔离。这些优点是从利用开关电容器电压击穿方案和一次侧感测 / 控制将原本离散的零件集成到芯片上来实现的。因此,特洛尼姆 PSSoC 的关键特征如下:支持较宽范围的可用 AC 输入电压和频率;可编程输出电压,以及通过自动设定以为适当操作配置输入电压来自动检测输入电压;用于 AC 到 DC、DC 到 DC 转换的高效开关电容器电路;实现高准确性的 PID (或类似) 调节控制环路;用于电流和温度监视的数字状态机;用于配置和控制的光电隔离的微处理器接口;以及用于制造测试的通信端口。

[0204] 特洛尼姆 PSSoC 的模拟和数字接口、输入和输出能够承受在典型操作范围之外的电压和电流。上述单元页可在较宽的温度范围内操作,且提供充足的抗 ESD 性。

[0205] 特洛尼姆 PSSoC 将输入和输出提供到外部世界和外部电路的接口。这些输入和输出包括但不限于:电力输入、电力输出、低电流关机启用输入、模式选择输入、需要外部电路的中间连接、测试连接、通信连接、电力输出、调节器输出、用于基于 PID 的 PWM 的连接、FET 驱动器输出以及反馈输入。

[0206] 特洛尼姆 PSSoC 是被设计来提供具有高效率和高准确性的输出电压调节的先进的电力控制器集成电路。特洛尼姆 PSSoC 的高级特征向用户提供可在各种各样的应用中使用多功能装置。对于特洛尼姆 PSSoC 来说,可编程输出电压是可能的,在多种电流负载条件下具有很少或没有效率损失。

[0207] 特洛尼姆 PSSoC 使用专有开关电容器电路系统来维持高效率,不管负载电压或电流如何。当负载不在汲取电流时,装置将进入低电流操作模式,以最小化保持清醒所需的传统的“吸血鬼”电流,以及按照负载来缩放活动子系统的数目,以便提供较宽负载范围上的高效率。

[0208] 特洛尼姆 PSSoC 的最高级框图在下文示出,且由以下主要电路块组成:高压多级 / 多分支开关电容器电压击穿电路;PID (或其它交换模式控制方案)、用于二次变压器的 PWM 控制的调节器控制块;电流和温度感测块;用于电压和电流监视的 ADC 或比较器;用于反馈控制的 DAC、PWM 或其它信号;用于电压和电流监视状态机的数字控制块;通信接口;以及用于芯片上电压和电流产生和其它电力要求的电力管理。

[0209] 电力管理。电力管理块将必要的电力轨和参考提供给 IC 的其余部分。所述其余部分由调压器、电流参考和电压参考组成。所述其余部分还包括 IC 使用所需的所有必要的缓冲和放大。所述电力管理系统还含有复位控制器,其管理所述系统在电力周期上的关断

和启动。

[0210] 开关电容器电压击穿电路。特洛尼姆 PSSoC 的开关电容器电压击穿电路用作近无损分压器。所述近无损分压器将 LINE_IN 引脚处存在的经整流的 DC 电压分压为 CP2_OUT 引脚处的降低的电压,以供外部变压器和二次电压控制环路使用。外部变压器可接着依据一次与二次绕组比使此电压进一步降低到所要应用电压,以及在需要时提供隔离。

[0211] 开关电容器电路被配置为具有多个并行分支的多个相同级的级联,如下文所示。基于电流感测放大器感测到的负载电流来将所述并行分支切入或切出所述电路。这使开关电容器电路能够在较宽的负载电流范围上维持高效率。在下面的图中,并行子系统的数目为 4,包括两个级。并行系统和转换级的数目可改变,使得所述系统为特定输入 / 输出电压比或电力要求而优化。

[0212] 所述开关电容器电路使用芯片上或芯片外反激电容器来最大化电力效率,且使用外部保持电容器来最小化电压纹波。这些电容器连接到分别为开关电容器电路的第 1 和第 2 级的输出的 CP1_OUT 和 CP2_OUT 引脚。所有级均由一个振荡器计时,或每一级可具有其自己的专用振荡器。开关电容器电路的每一分支可具有独立的启用。

[0213] 通过使用数 / 模转换器 (DAC),输出电压可在用于给定范围的具有高分辨率的应用的电压范围内编程。此 DAC 的数字控制使得多个电压能够在 CP2_OUT 引脚处被编程,以获得目标应用所需的所要最终输出电压。

[0214] 其它开关电容器电路级的开关电容器电路输出设定可由用户确定,或从测得的 AC 线 $V_{\text{输入}}$ 得出,使得可实现 $V_{\text{输入}}$ 与 $V_{\text{输出}}$ 之间的最佳比率。

[0215] 通过使用运算跨导放大器 (OTA) 来获得每一开关电容器电路级的调节。OTA 依据输出电压与输入参考电压之间的差异来调节施加到每一级中的反激电容器的电流。输入参考电压可取决于应用而编程、得出,或是固定的。

[0216] 可进行传入线的电压测量,以便优化开关电容器电路设定。此设定计算可在芯片上、芯片外或通过适当的芯片上电路在空中执行,使得每一开关电容器电路级的输出处于最优化的比率。

[0217] 电流感测放大器。特洛尼姆 PSSoC 中的电流感测放大器允许装置测量电流,作为反馈环路以及误差报告的一部分。电流可由 ADC 或通过具有不同阈值的一系列比较器来测量。

[0218] PID 控制环路。特洛尼姆 PSSoC 提供比例积分和差分 PID 环路或替代的 PWM 控制电路,以便驱动隔离变压器的一次侧,降压、升压或降压 - 升压电路。此电路是用来在必要时提供后调节和隔离。

[0219] 对 PID 环路的反馈可来自数字源,例如但不限于串行化 ADC 流或模拟信号,两者均取决于电路的输出。此反馈可提供关于经调节的输出电流或电压的信息。

[0220] 温度传感器。实现板上温度传感器,使得存在对过温情形的充足防护。采取的防御热损害的行动可包括下调输出电力,且完成输出的关断。

[0221] 控制电路。特洛尼姆 PSSoC 通过数字途径或通过模拟电路来提供控制。通过此控制电路,IC 能够设定和改变现有的控制阈值和控制点,以及启用 / 停用特定功能性。这在数字接口情形可通过寄存器或熔断器来完成,或在需要模拟设定的情况下,通过施加到模拟引脚的电压来完成。

[0222] 如果所述特征被启用,那么特洛尼姆 PSSoC 允许系统的输出被停用或下调。这可通过断开 PWM、开关电容器电路或通过下调任一或两个子系统而发生。可因误差检测或因低输出电流或输出电力情形而停用所述输出,所述情形例如在包括电池的所链接装置完成了对电池进行充电且特洛尼姆 PSSoC 正仅将电力提供给非电池充电功能性时发生。一旦特洛尼姆 PSSoC 已进入低电路关断状态,其就将间歇地将输出电力重新施加到最终装置,以便检查其现在是否需要高于某一阈值的电力,所述阈值指示电池现在需要进一步充电。可针对不同应用来调整处于断开状态所花费的时间。图 33 示出用于低电流检测和误差检测的算法的实例。

[0223] 特洛尼姆 PSSoC 提供到外部电路的多个接口,使得装置可控制和配置 IC。这些接口可包括但不限于 SPI、I2C、UART 或其它同步 / 异步串行流。还可实现到 NRZ 格式的替代编码,来优化外部电路的大小和零件计数。同样地,这些通信接口可连接到隔离装置,以便在需要的情况下实现来自所隔离区的通信。

[0224] 时钟产生器。特洛尼姆 PSSoC 可具有产生其自己的内部时钟的能力,其还可包括频率控制电路,包括但不限于内部 RC 振荡器、PLL、FLL、时钟分频器、VCO 和修整电路。另外,计时树可实施有意的时钟抖动或其它手段来改变时钟边缘放置,以便最小化计时在所辐射且进行的 EMI 的影响。

[0225] 模块描述。特洛尼姆 PSSoC 既定用作电力供应装置,其并入到接受 AC 电力输入、将此电力转换为 DC 电压且将此电力供应给外部装置的模块中。所述模块可采取许多形式,所述形式可包括到 ASIC 的输出的模拟或数字反馈,或 ASIC 可在无反馈的开环模式下操作。另外,模块电路可构造为使得可离散地监视和控制个别输出(在存在多个所连接输出的情况下)。取决于应用和调节要求,模块内的感测能力意在补充或代替 ASIC 所进行的测量。

[0226] 图 34 是包括具有隔离和离散输出感测的数字反馈模块的电力电路 22 的示意图。图 35 是包括具有反馈隔离的线性化的模拟反馈模块的电力电路 22 的示意性例示。这些反馈表示模拟反馈版本和数字反馈版本。这两个图还将隔离变压器指示为设计的一部分。取决于应用的要求,此组件可或可不包括在所述模块中。两个实例描述同步整流方案,然而,还可实现异步系统。

[0227] 数字反馈描述。数字反馈模块包括微控制器、独立 ADC 或二次 ASIC,以便监视输出电压,且允许在输出连接处进行非常精确的测量。这允许所述模块补偿可能导致输出电压的变化的组件损失、温度和其它变量。接着将此数据格式化,并将其发送回到 ASIC 以提供数字反馈流。还示出电流感测和输出启用晶体管,使得多个输出连接到所述模块,每一输出具有个别感测。以此方式,ASIC 描述中所描述的低电力切断功能性应被应用于个别负载,但电力是共享的。

[0228] 模拟反馈描述。如果出于成本或其它原因,希望使用模拟反馈系统,那么特洛尼姆 PSSoC 允许通过模拟反馈输入来实现此目的。在所示的实施方案中,穿过光电隔离 LED 的电流与输出电压成比例。所述电路被设计成使得档输出电压处于目标输出时,IC 上的模拟反馈引脚处的电压处于标称电压。电流监视由变压器的一次侧处的 IC 执行,且测量结果按变压器的匝数定量进行缩放。

[0229] 图 36 是可结合电力电路 22 使用的电平移位器电路的示意性例示。在一个实施方案中,开关电容器电压击穿电路 32 和降压调节器 34 依靠电平移位器,其可取静态 CMOS

电平数字信号以及将所述信号移位到各种电平的电压。完成此举来适当地驱动特洛尼姆 PSSoC 芯片外和特洛尼姆 PSSoC 芯片上的高压开关的栅极。电平移位器由具有静态 dc 电流偏置电流的差分对组成。所述差分对放大 CMOS 电平信号,且接着移位到较高轨。存在用户信号路径中的级联,以避免任何晶体管击穿。可经由 p 沟道开关来停用电平移位器,以避免任何静态电流耗用。一旦信号移位到另一轨,其就被进一步放大并转换为单端,且接着转换回到静态 CMOS 电平,来驱动高压开关。

[0230] 图 38 和 39 是电力电路 22 的额外示意性例示。在一个实施方案中,正向转换器变压器 102 可包括三次绕组 152(图 39 和图 40 中示出),其可用作用于电流感测的二次侧的复制品。举例来说,一些特洛尼姆 PSSoC 应用可在低电压下运行,且自驱动同步整流器可能不是可靠的解决方案。更多的栅极电压将确保稳健的系统。举例来说,将存在针对 1.8 伏 DC 输出的应用。假定 12:1 变压器和 43 伏 CP_DAC2 设定,3.6VDC 为二次绕组上的峰值电压。可使用 12:2 辅助绕组来为同步整流器 FET 产生 7.2 伏的栅极驱动。所述变压器设计可在二次侧上包括辅助绕组 152 来支持此要求。

[0231] 图 41 是包括 DC 到 DC 转换电路的电力电路 22 的示意图。在所示出的实施方案中,电力电路 22 包括开关电容器电压击穿电路 32,其用于接收 DC 输入电力信号,且产生具有较低电压电平的 DC 输出电力信号。在一个实施方案中,电力电路 22 还可包括与 SCVBC 32 并行耦合的开关模式降压调节器 34。高效开关电容器电压击穿电路 32 包括并行电耦合的一对反激电容器,以及电耦合到所述对反激电容器中的每一个的多个开关组合件。在一个实施方案中,所述电容器之间的栅极是共享的。可操作所述开关组合件来在充电阶段期间选择性地输入 DC 电力信号递送到所述对反激电容器中的每一个,且在具有比输入 DC 电力信号低的电压电平的放电阶段期间,选择性地输出 DC 电力信号递送到电子装置。至少一个开关组合件可包括 N-沟道 MOSFET 开关和电平移位器,其用于将控制信号递送到所述 N-沟道 MOSFET 开关。另外,迪克森电荷泵可耦合到所述电平移位器,以接收输入 DC 电力信号,且产生具有比所述输入 DC 信号高的电压电平的输出电力信号。将输出电力信号递送到电平移位器,来用于操作 N-沟道 MOSFET 开关(或关闭其它类型的 MOSFET)。另外,开关电容器电压击穿电路可包括控制电路,其包括:电压感测电路,用于感测输入 DC 电力信号的电压电平;以及增益控制器,其被配置来依据感测到的电压电平选择开关电容器电压击穿电路的增益设定,且依据选定的增益设定来操作所述多个开关组合件中的每一个。

[0232] 此书面描述使用实例来公开本发明,包括最佳模式,且还使所属领域的技术人员能够实践本发明,包括制造和使用任何装置或系统,以及执行任何所并入的方法。本发明的可取得专利的范围由所附权利要求书界定,且可包括所属领域的技术人员可以想到的其它实例。可从对图式、公开内容和所附权利要求书的研究获得本发明的其它方面和特征。可用与所附权利要求的范围内具体描述的方式不同的方式来实践本发明。还应注意,所附权利要求书内所列出的步骤和/或功能(不管步骤和/或功能在其中列出的次序如何)不限于任何特定操作次序。

[0233] 尽管本发明的各种实施方案的特定特征在一些图式中示出且在其它图式中未示出,但这仅仅是为了方便。根据本发明的原理,可结合任何其它图式的任何特征来参考和/或要求图式的任何特征。

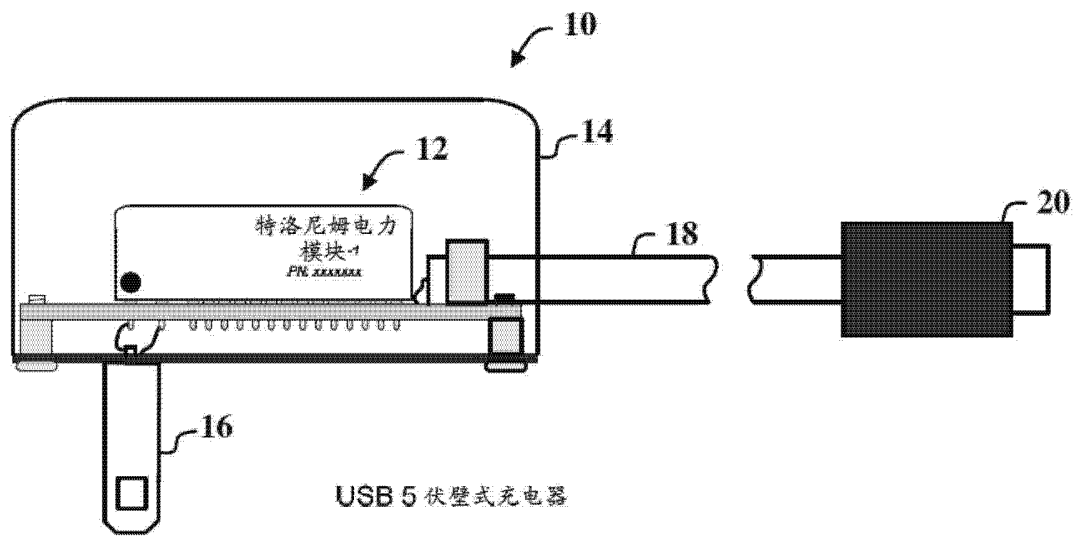


图 1

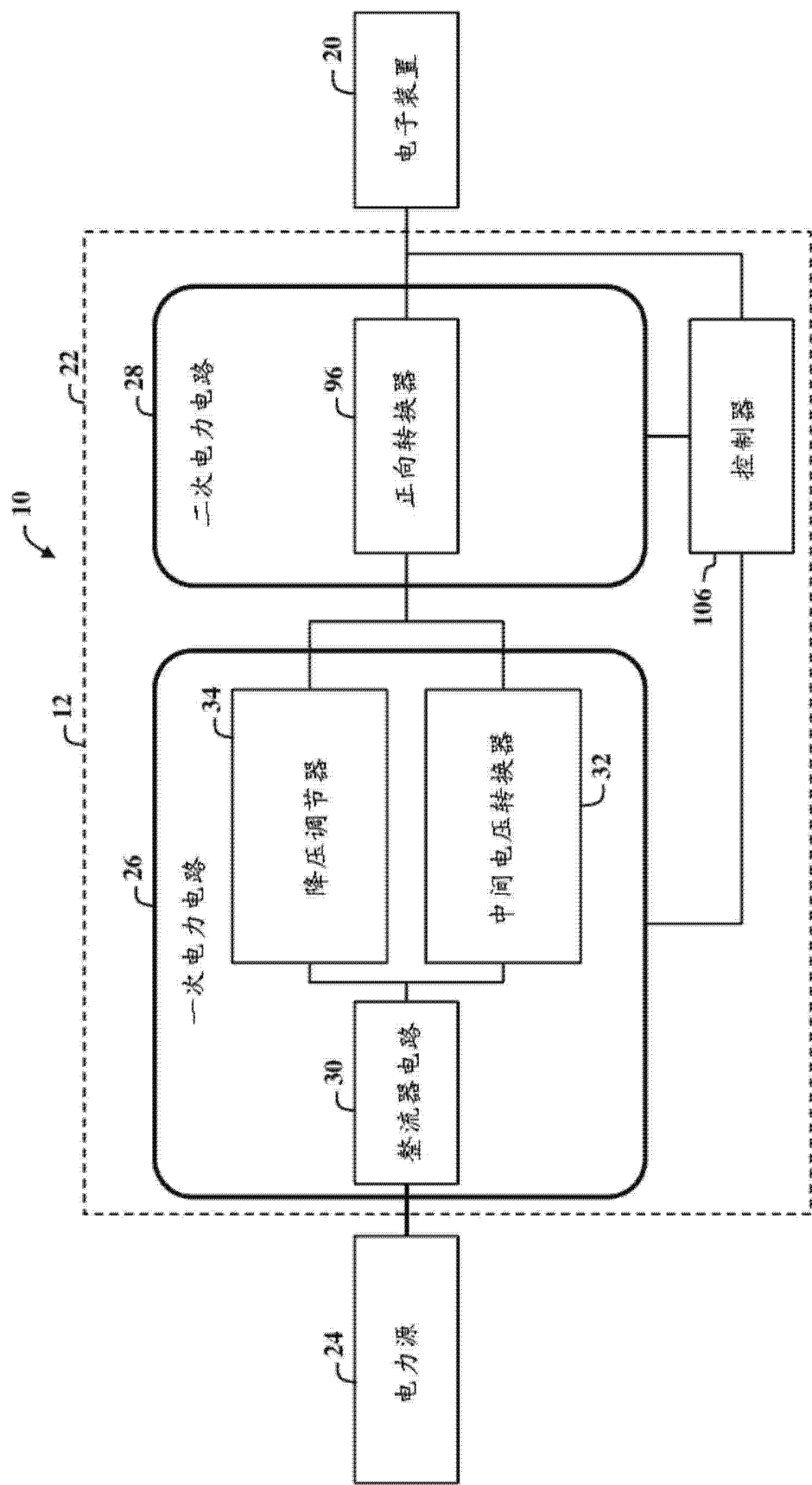


图 2

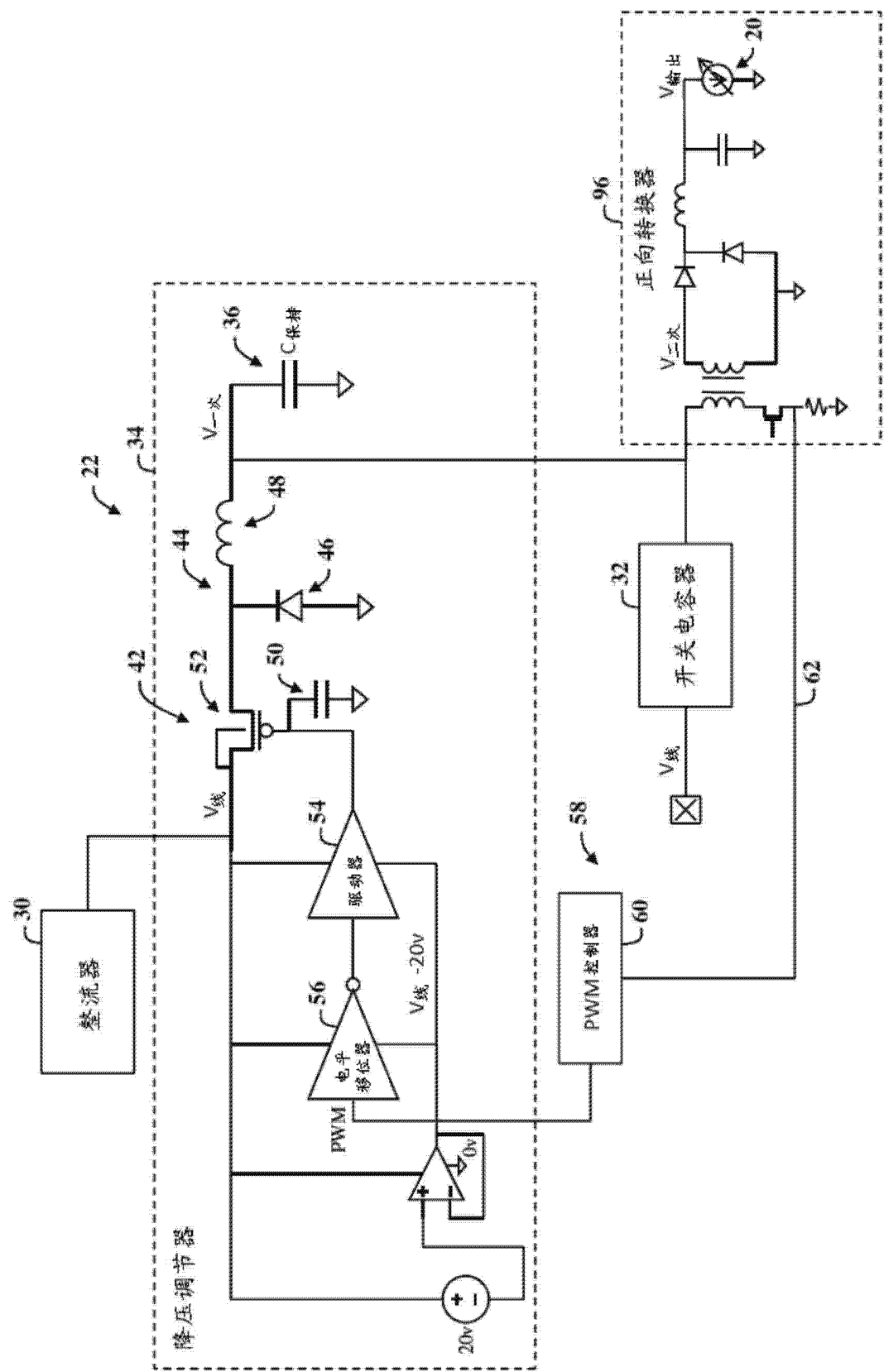


图 3

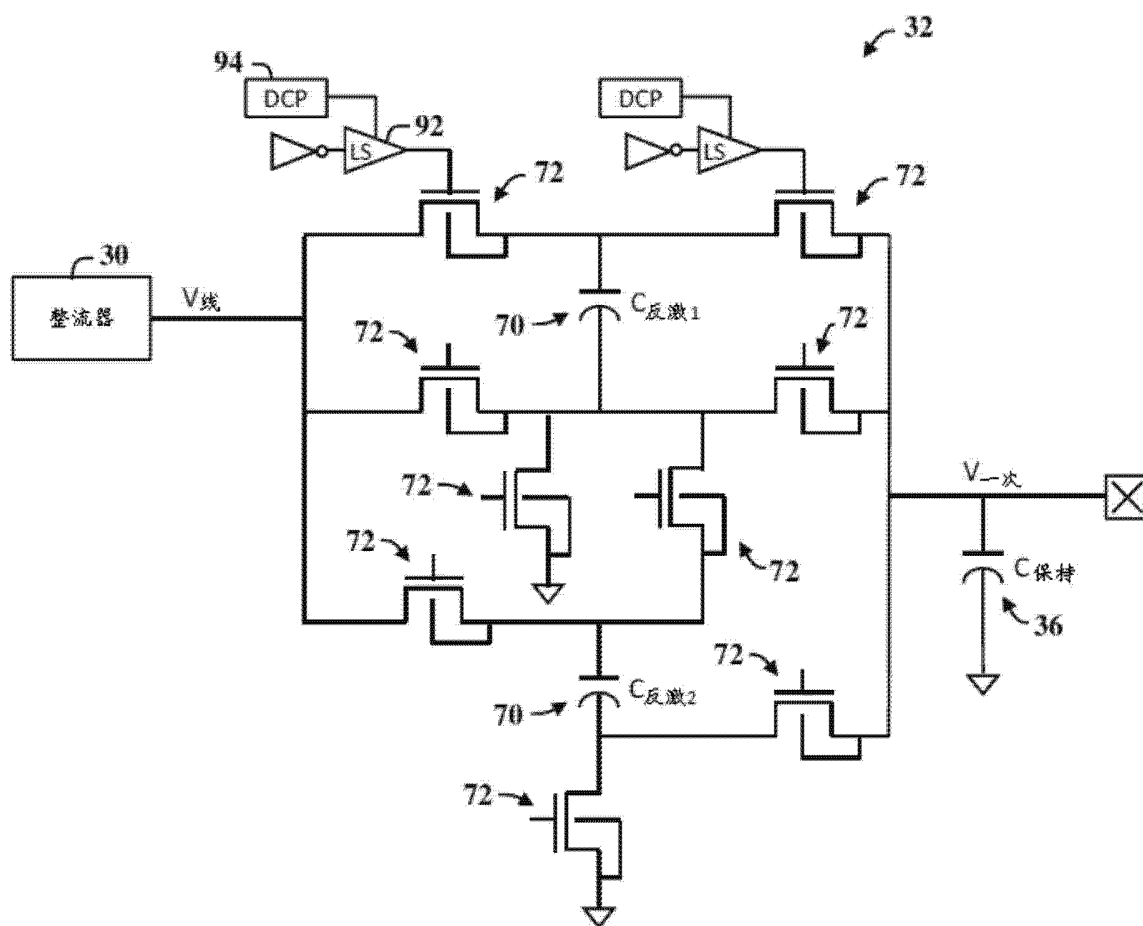


图 4

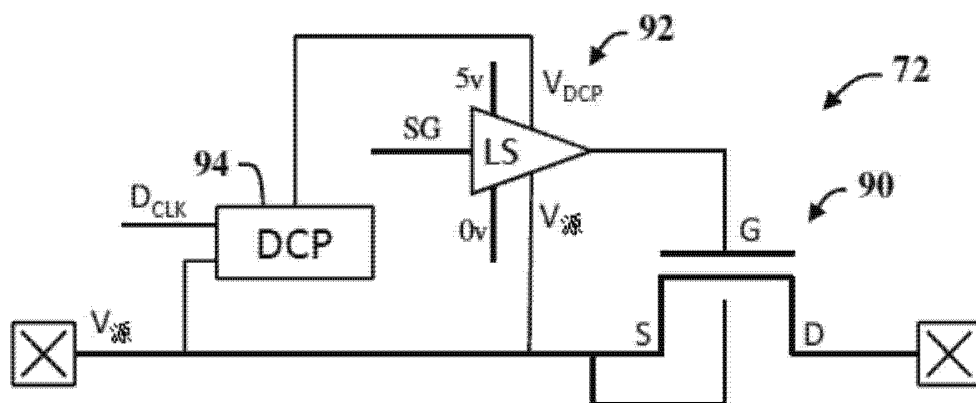


图 5

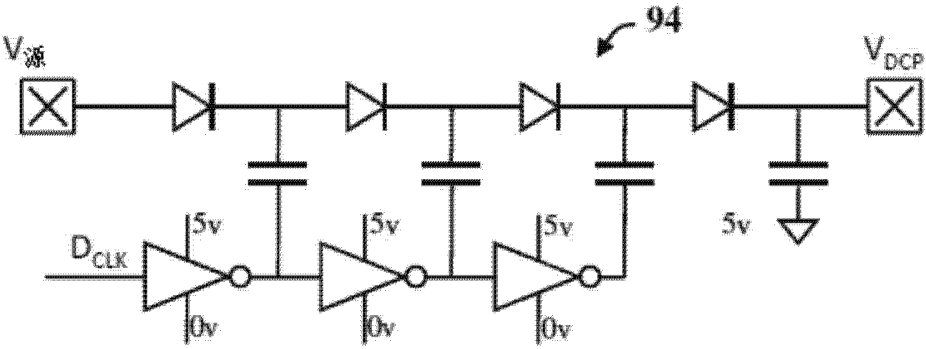


图 6

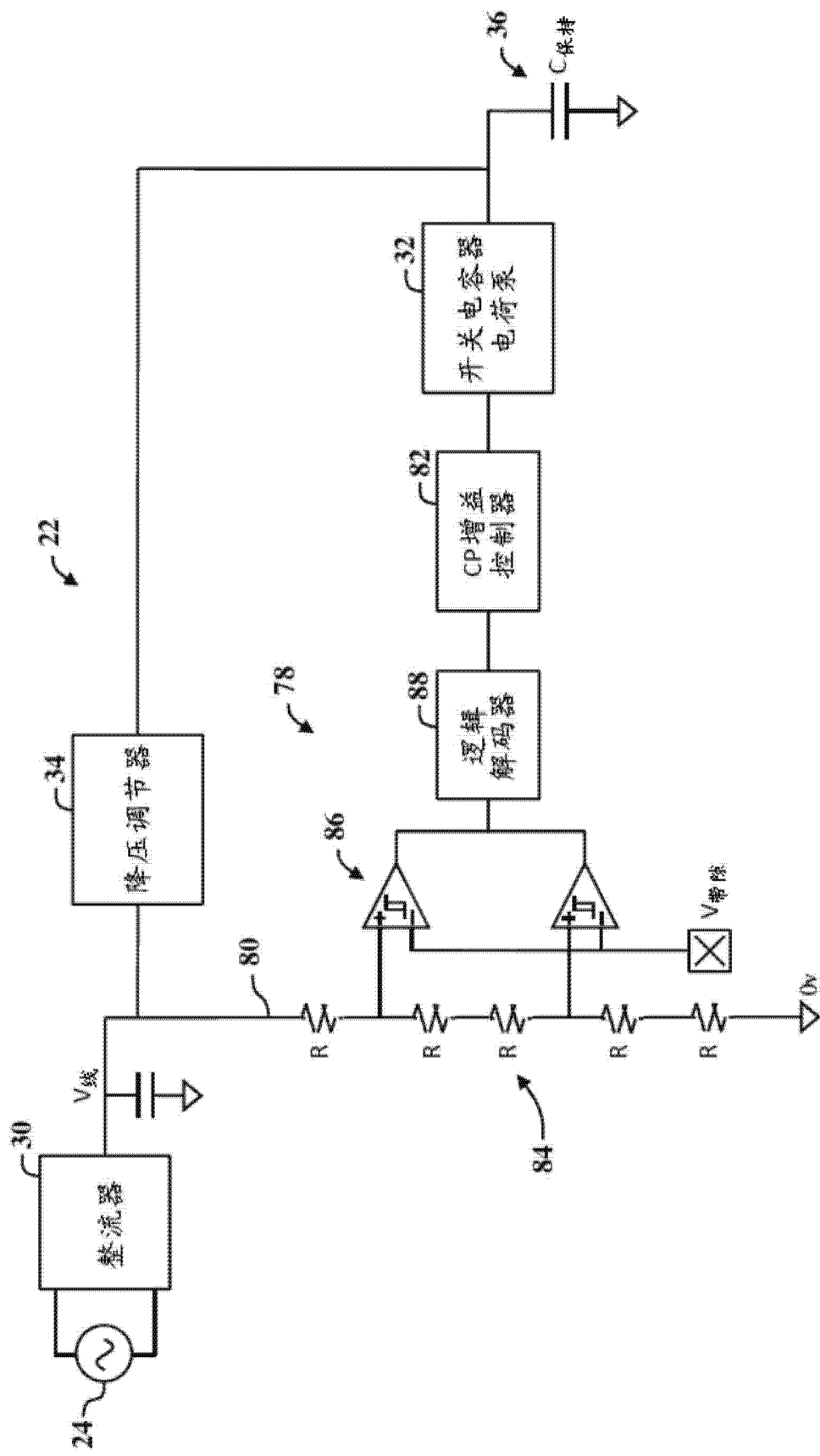


图 7

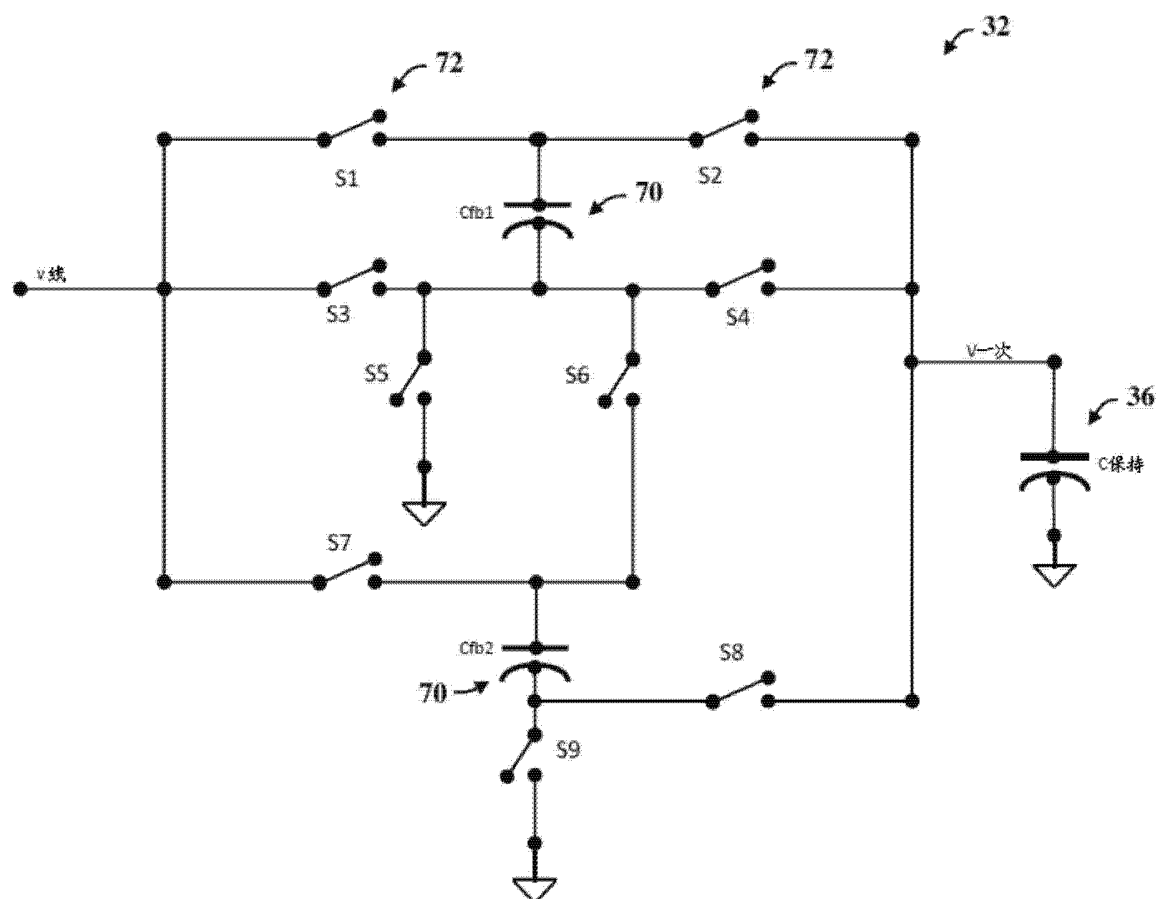


图 8

开关名称	阶段 1	阶段 2 G=1/2	阶段 2 G=2/3	阶段 2 G=1
S1	开	关	关	关
S2	关	开	开	开
S3	关	关	关	开
S4	开	关	关	关
S5	关	开	关	关
S6	关	关	开	关
S7	开	关	关	开
S8	开	关	关	关
S9	关	开	开	关

图 9

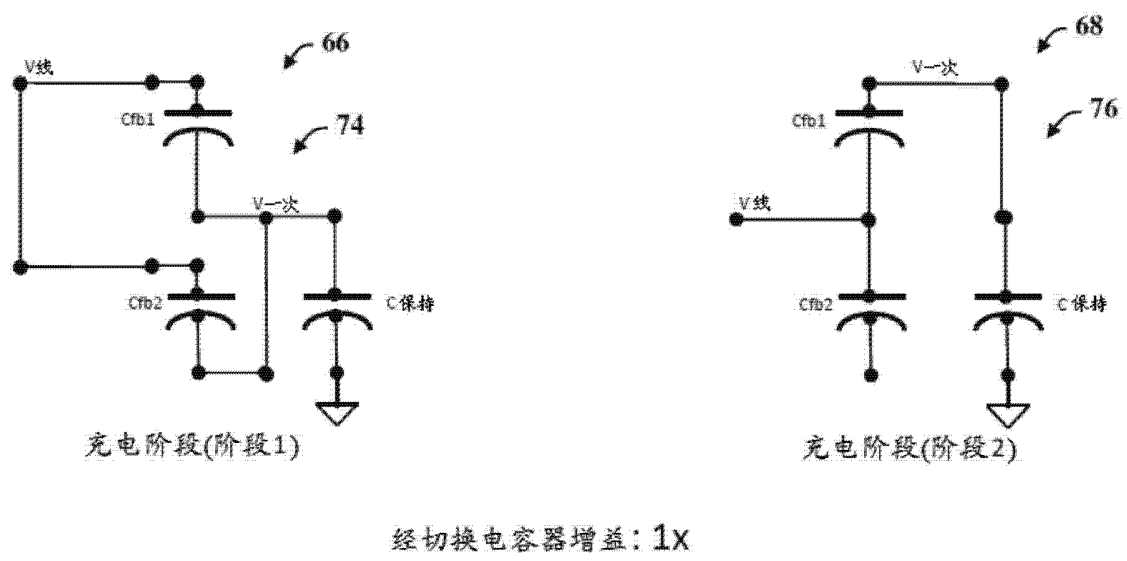


图 10

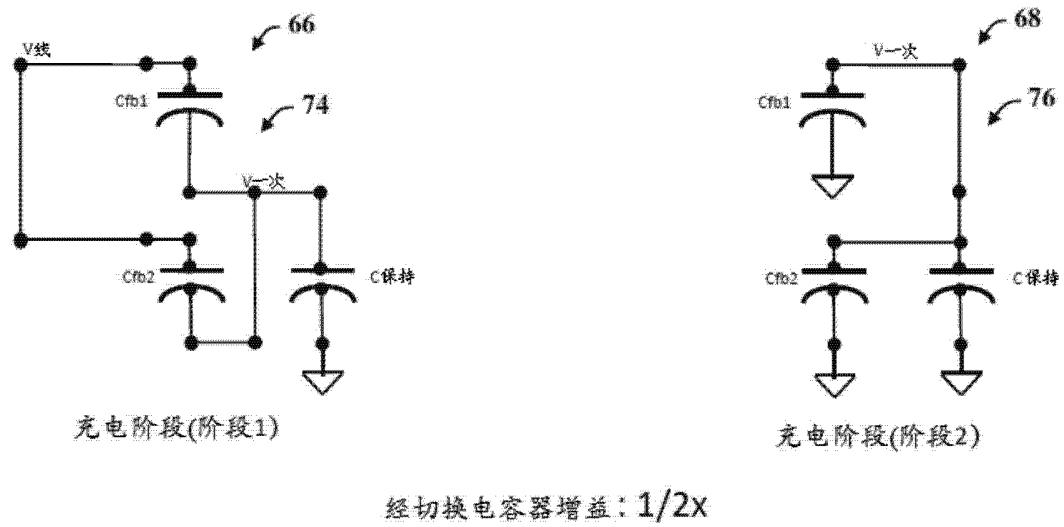


图 11

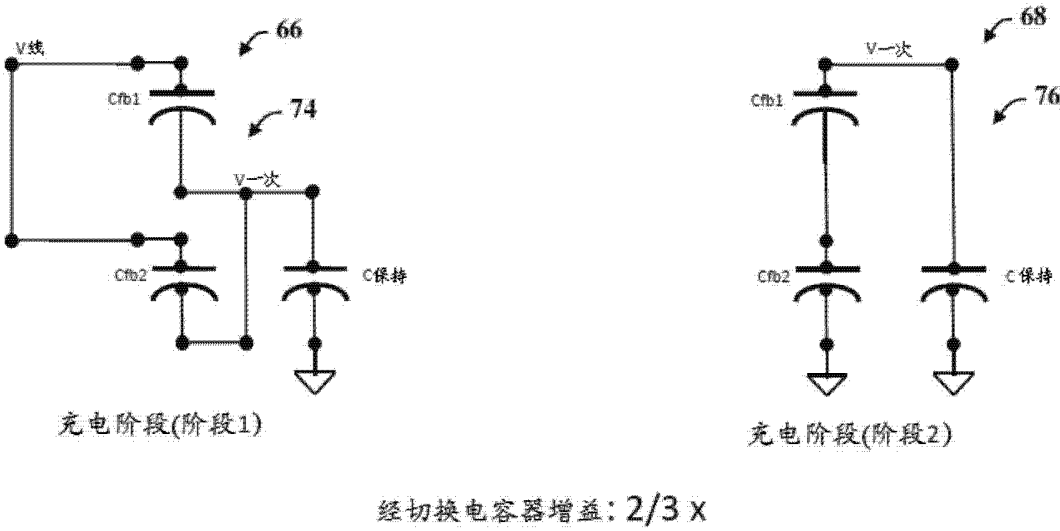


图 12

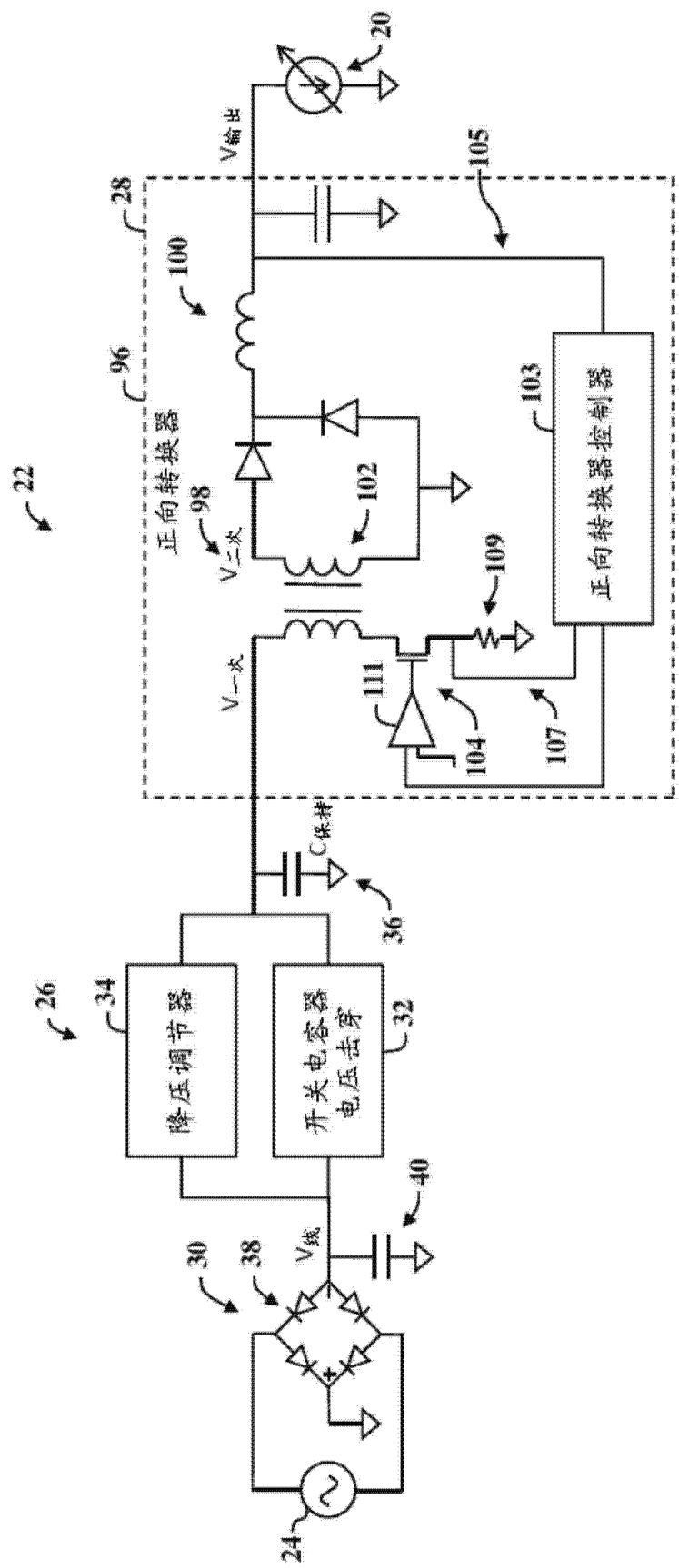


图 13

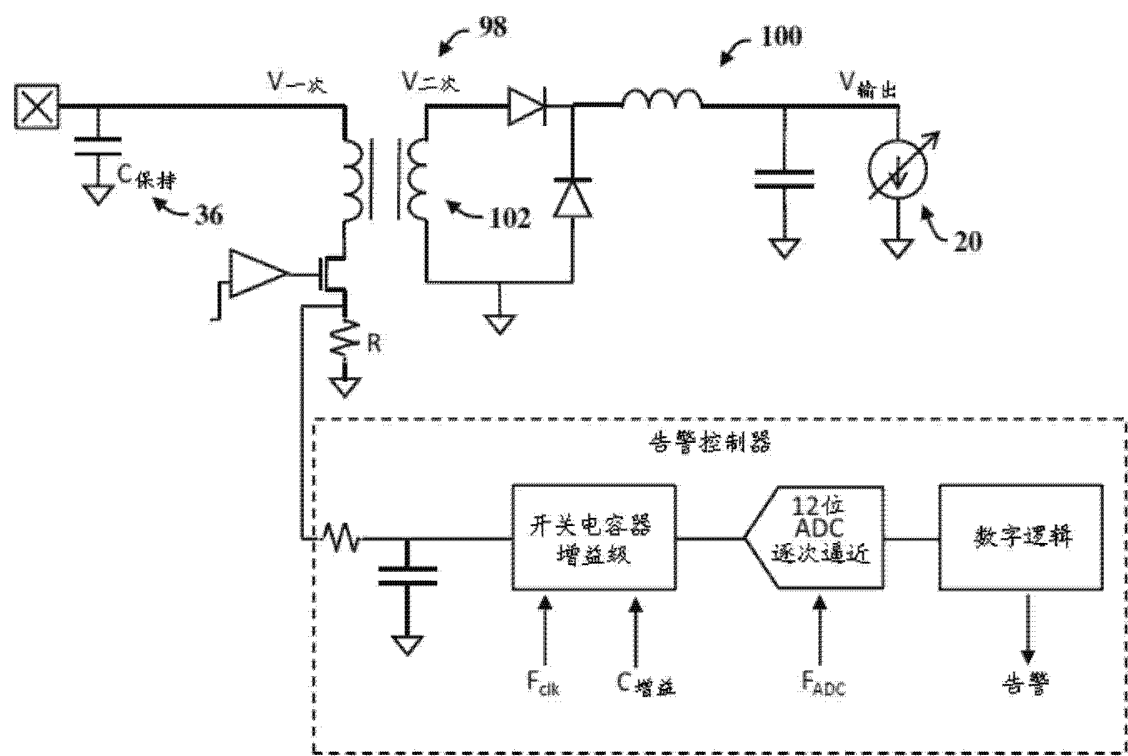


图 14

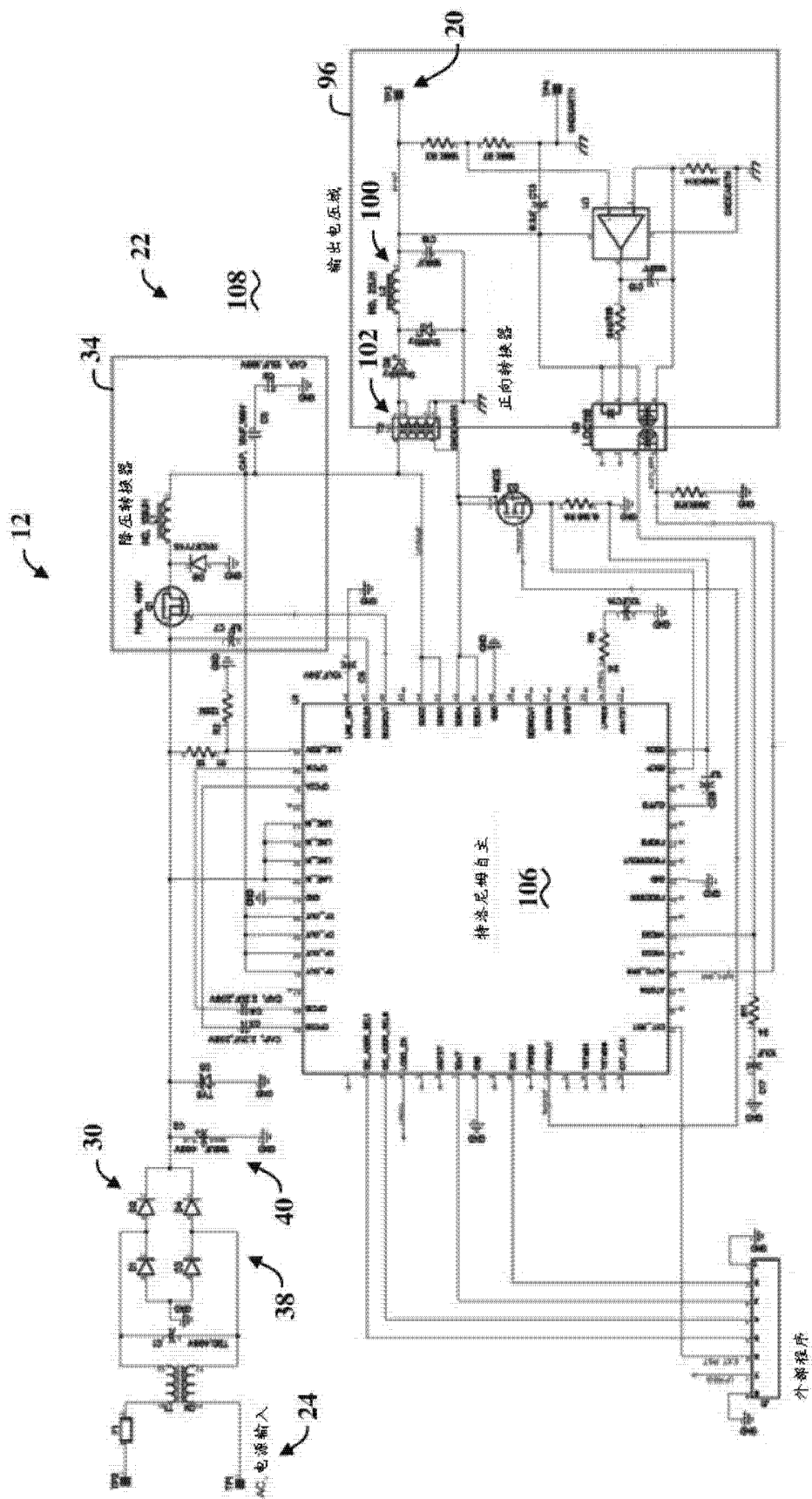


图 15

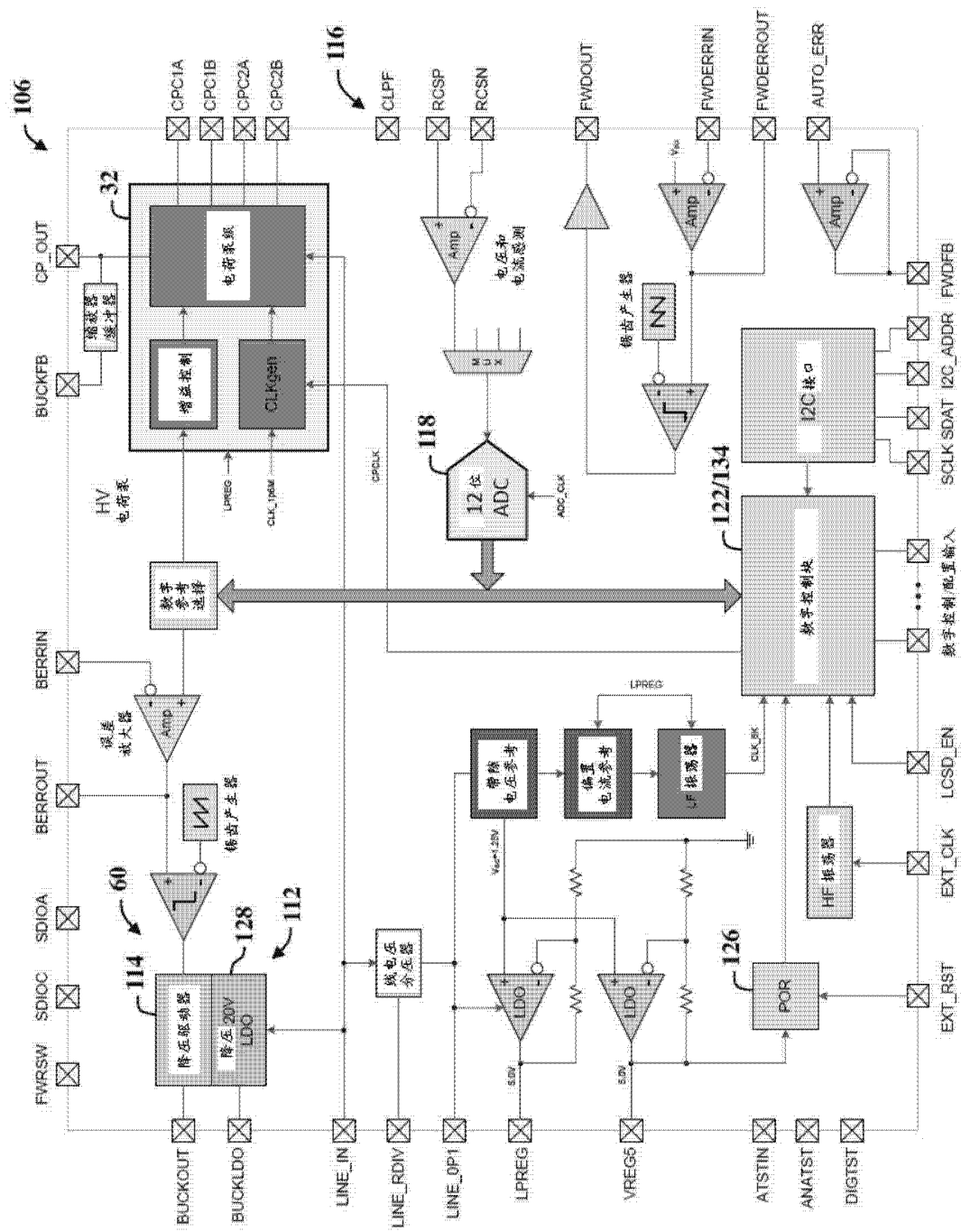


图 16

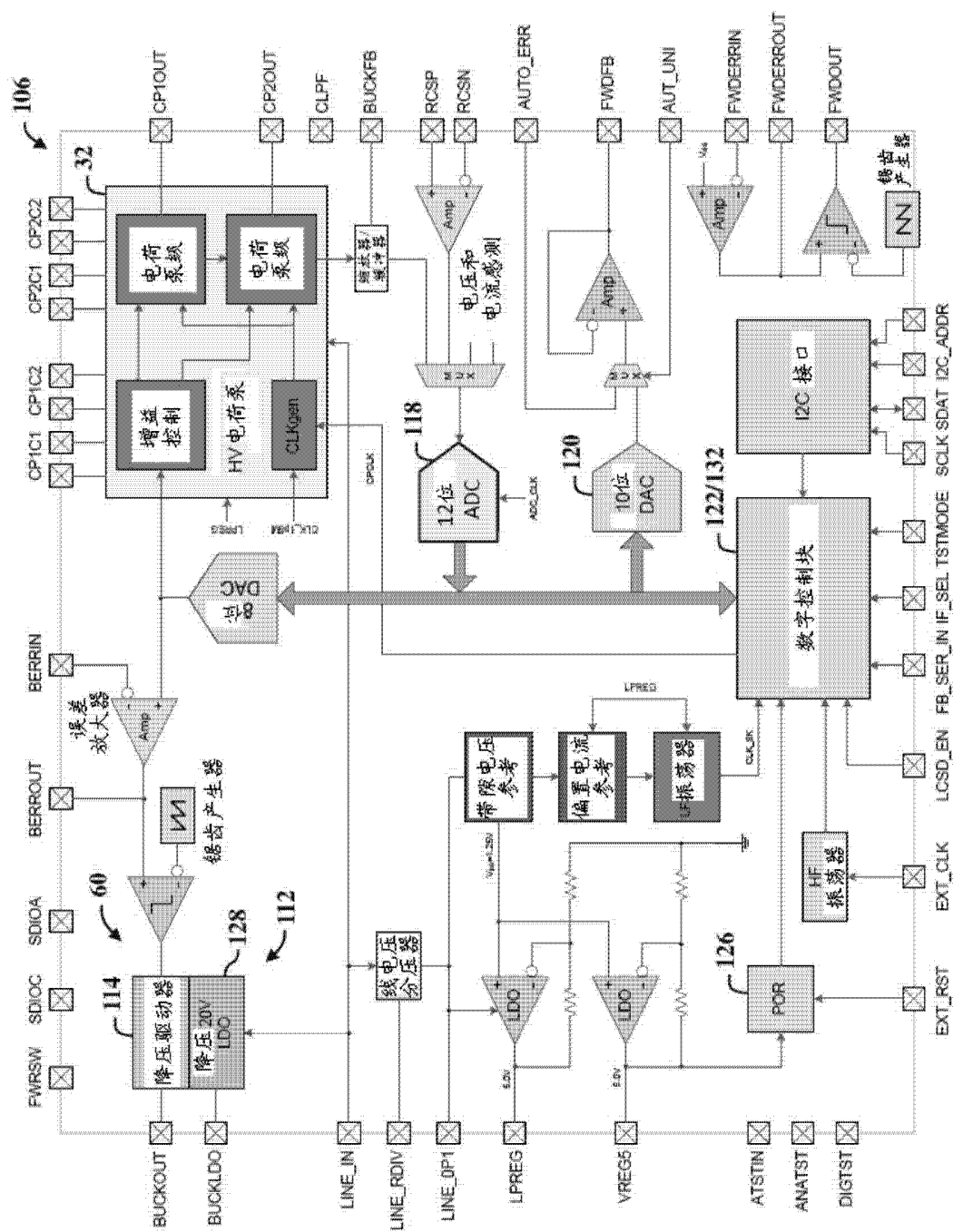


图 17A

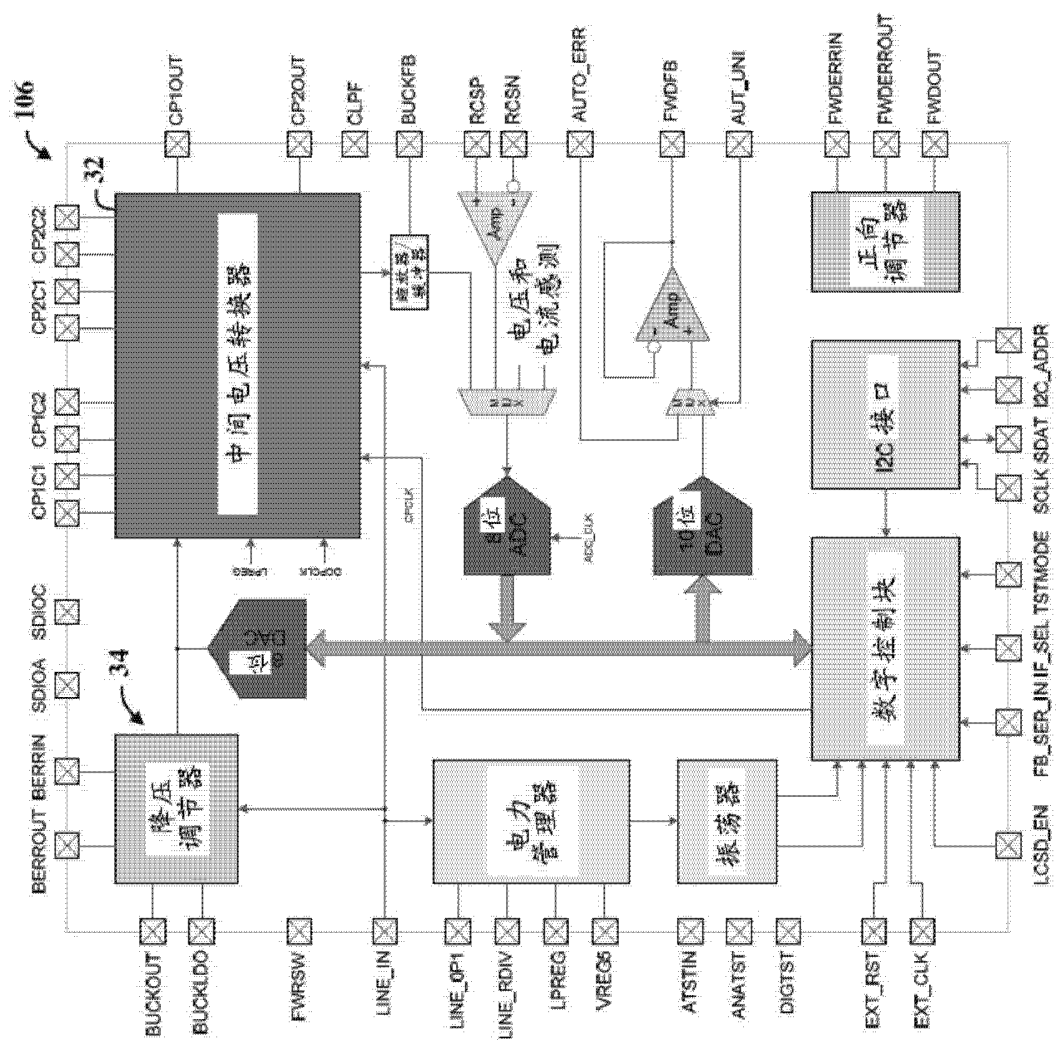


图 17B

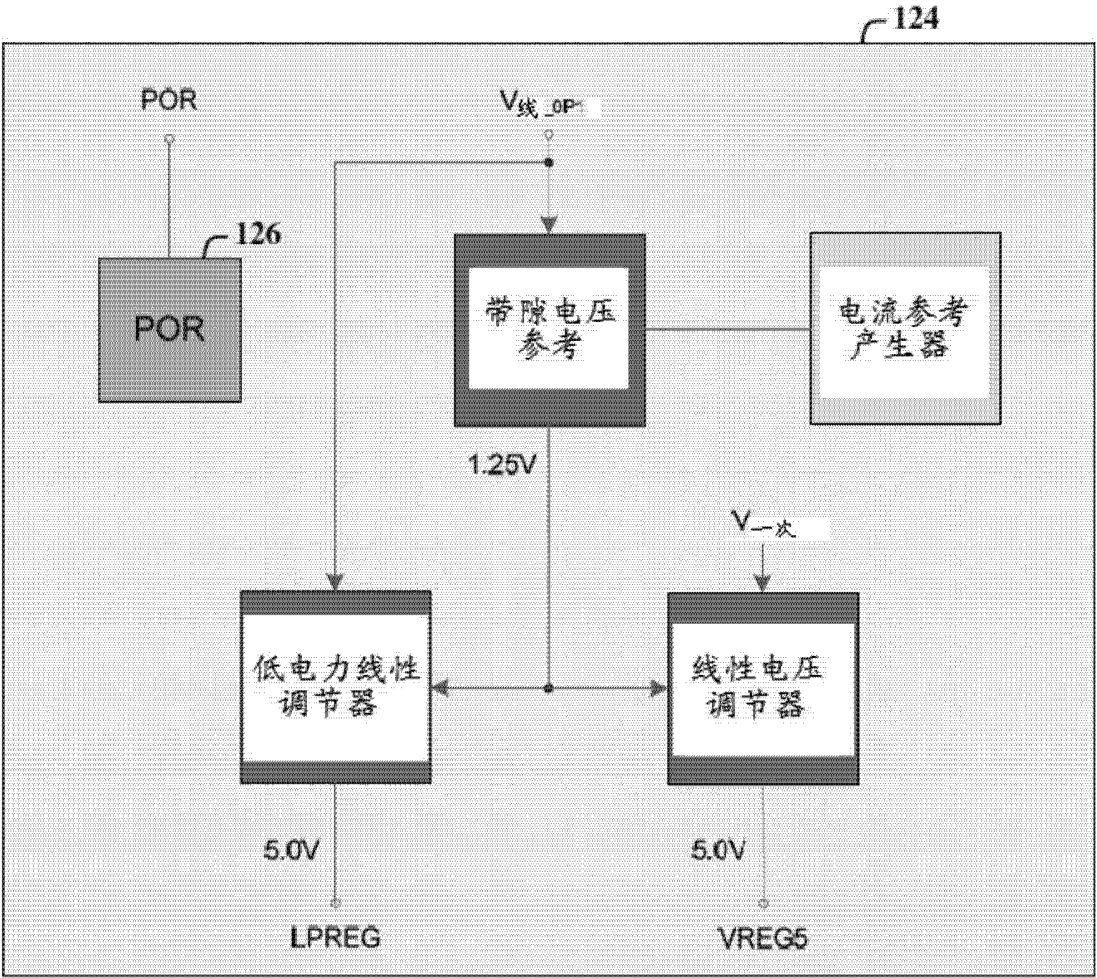
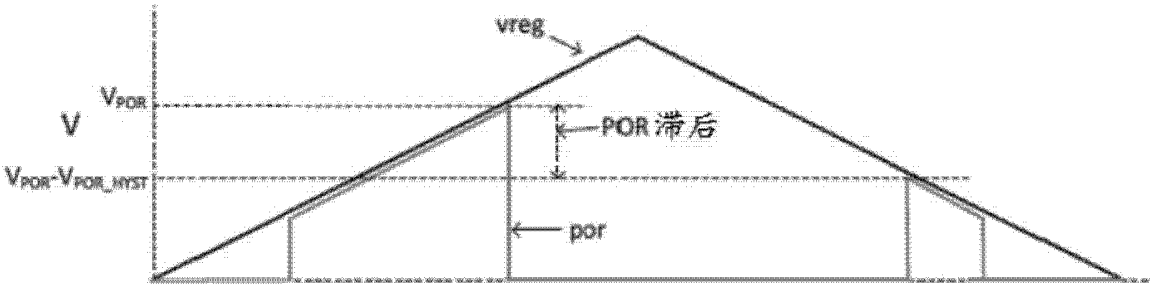


图 18



POR 阈值电压

图 19

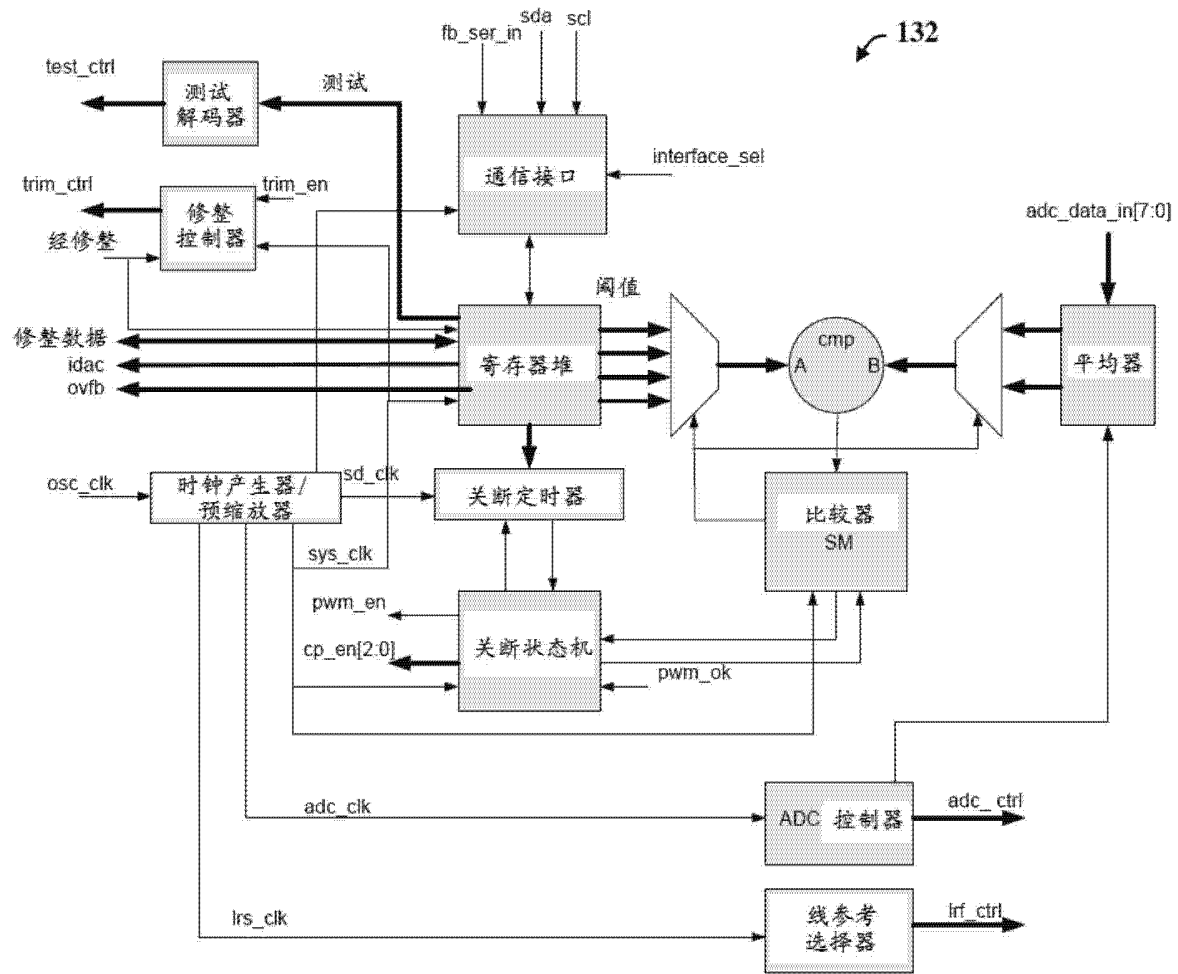


图 21

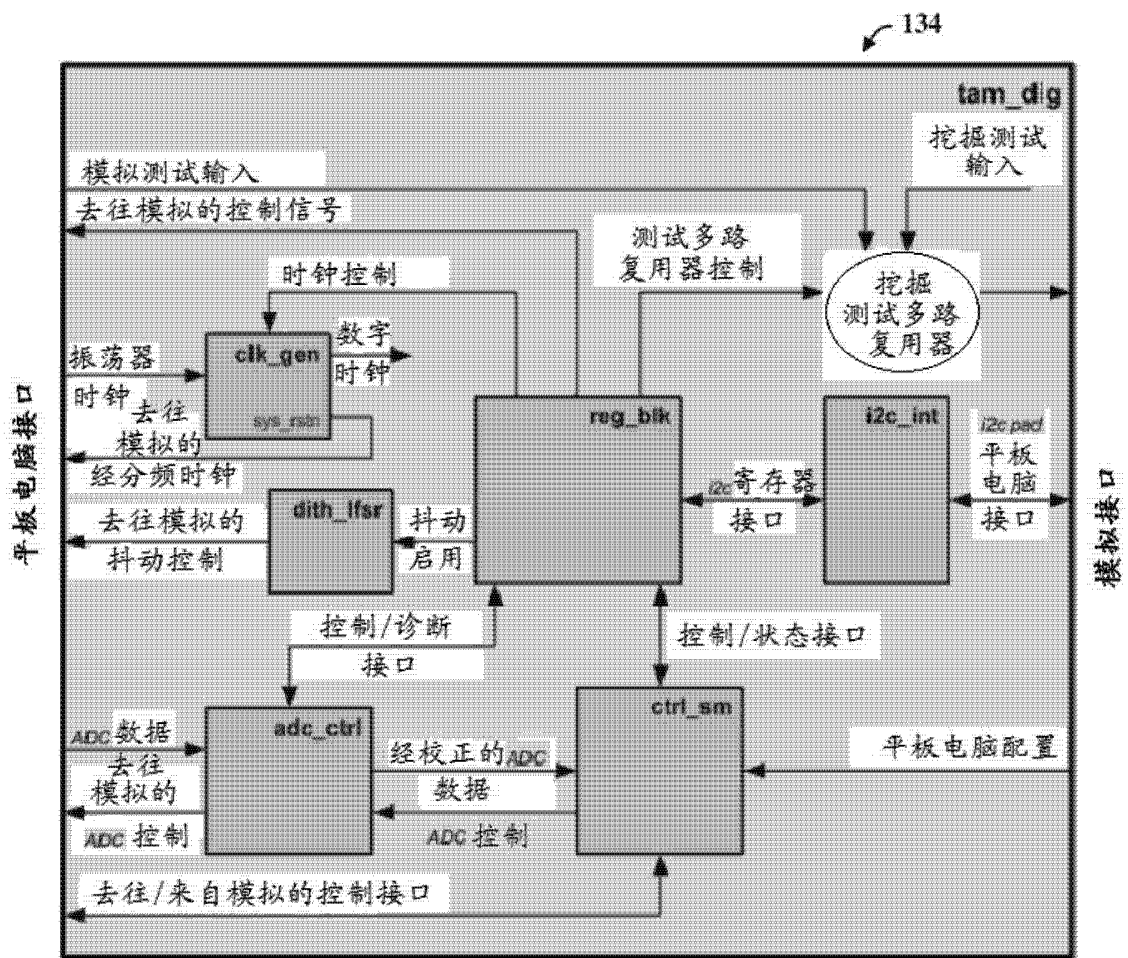


图 22

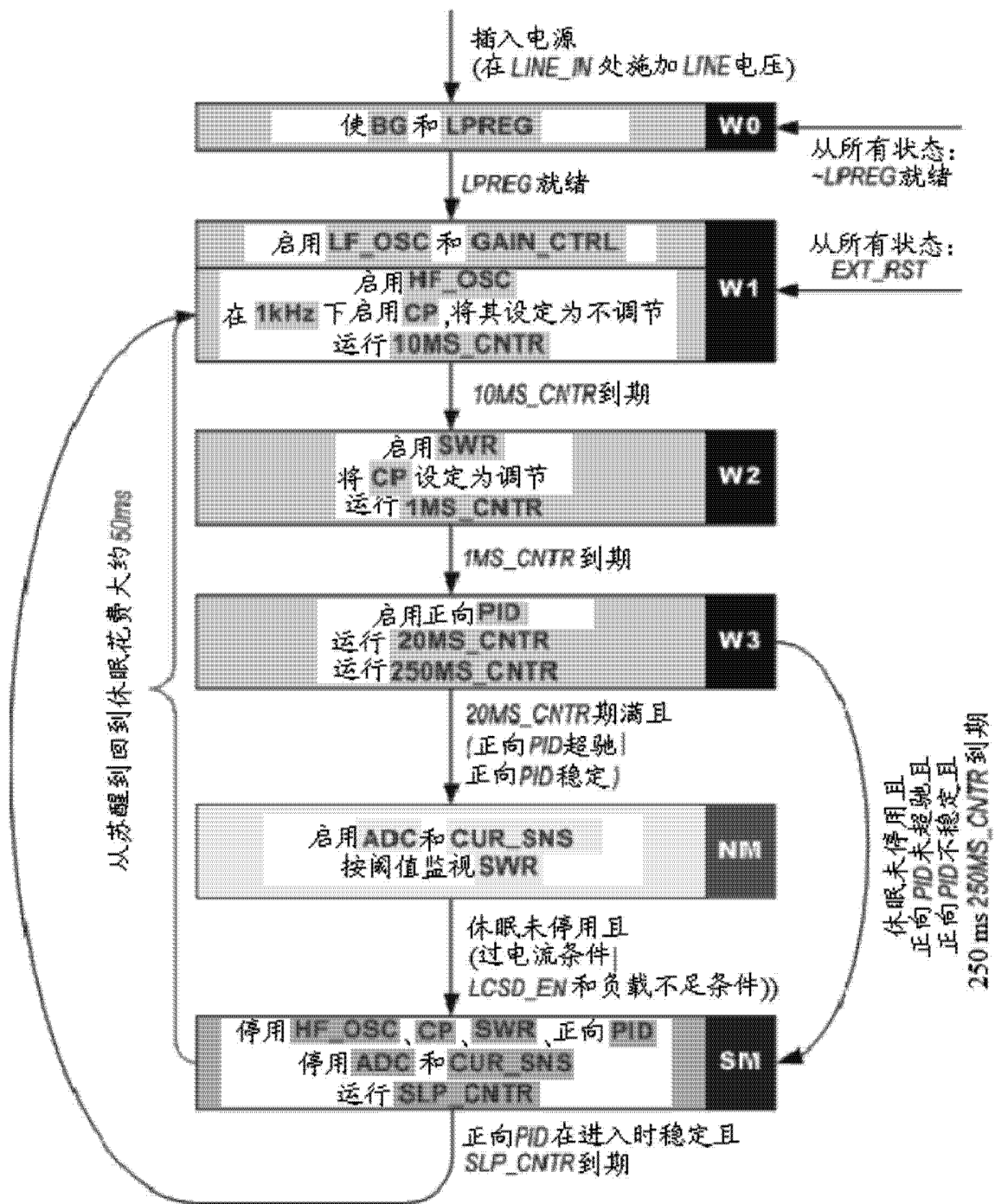


图 23

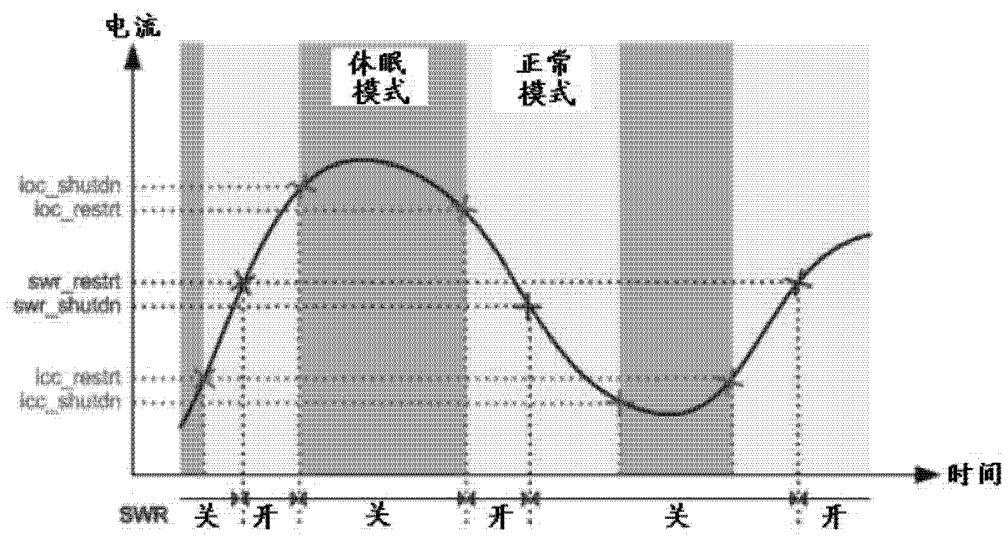


图 24

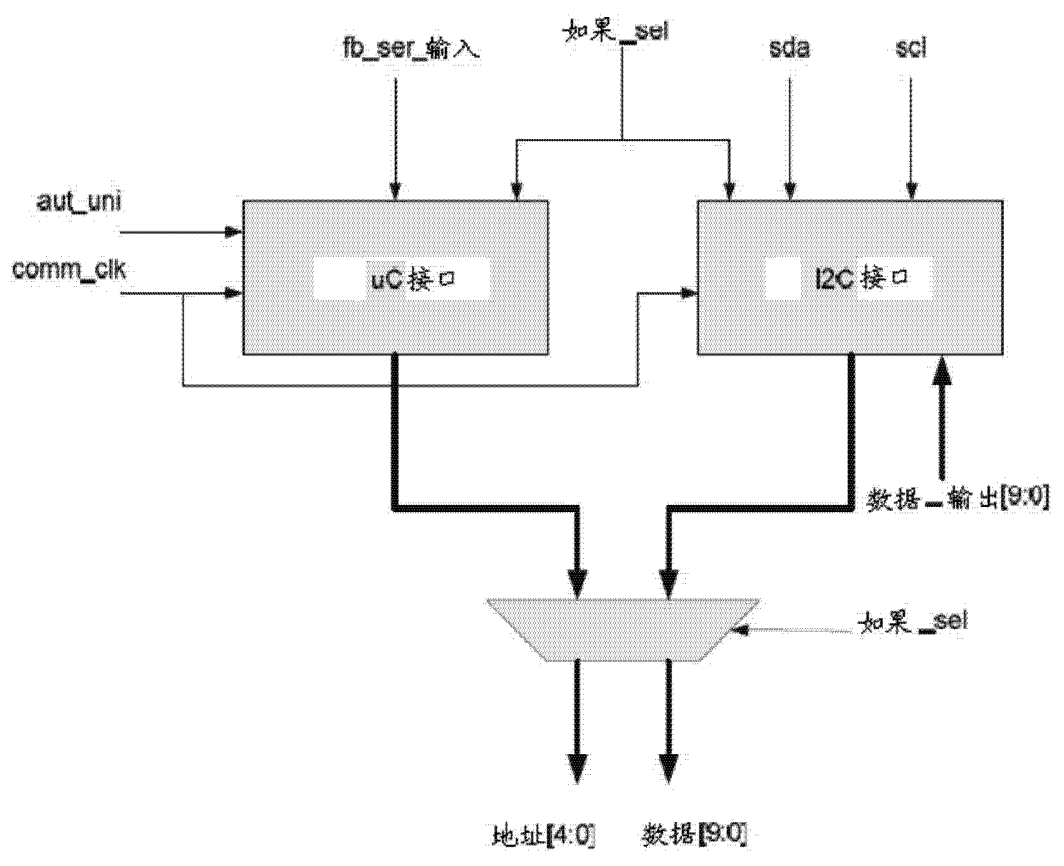


图 25

包格式

帧头	R/W	地址[4'0]	数据[9'0]	帧尾
----	-----	---------	---------	----

开始=非闲置状态
闲置=来自光学隔离器的不活动状态
对于读取, RW=1

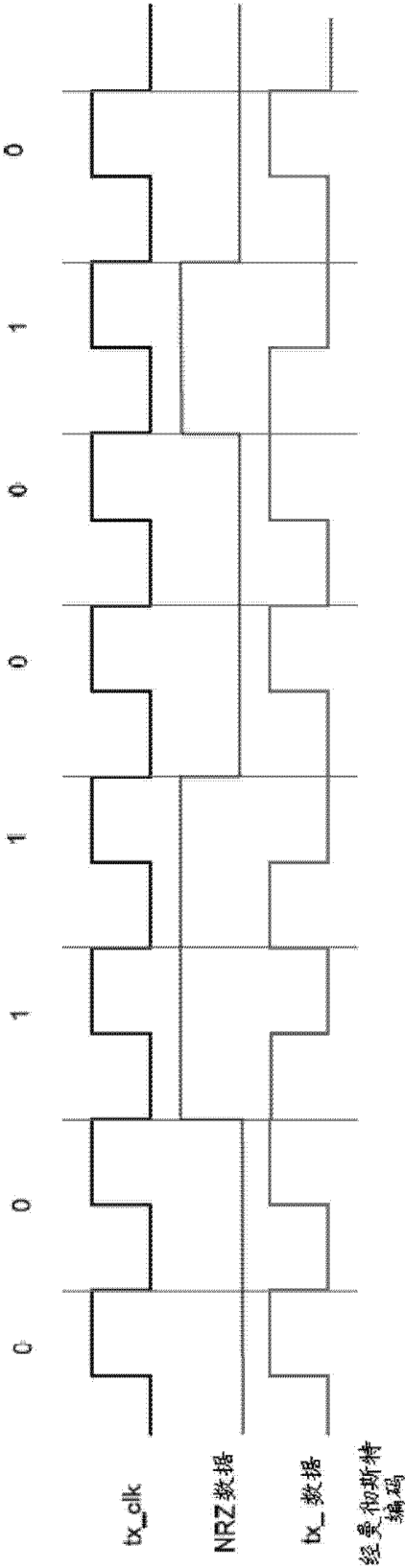


图 26

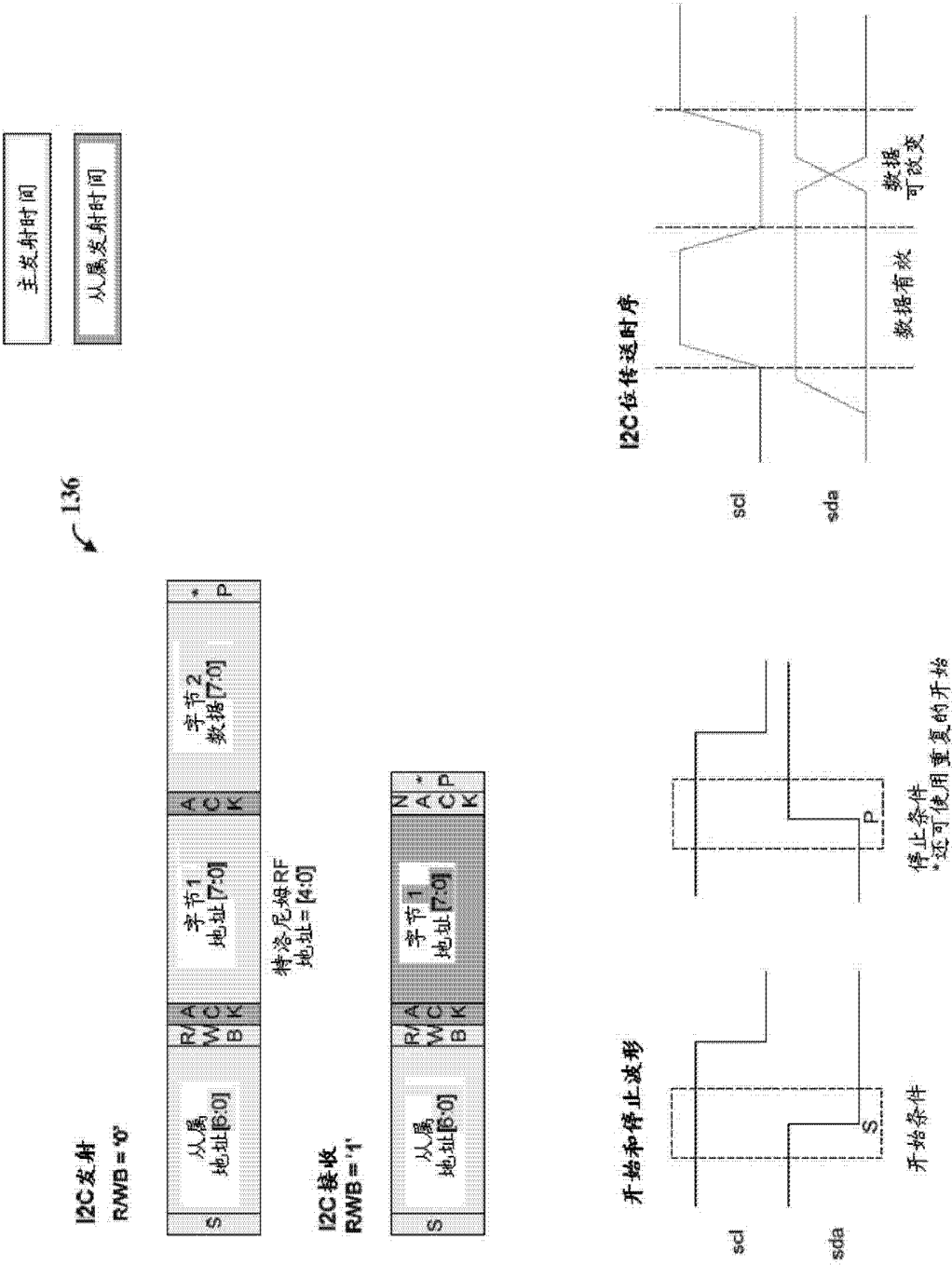


图 27

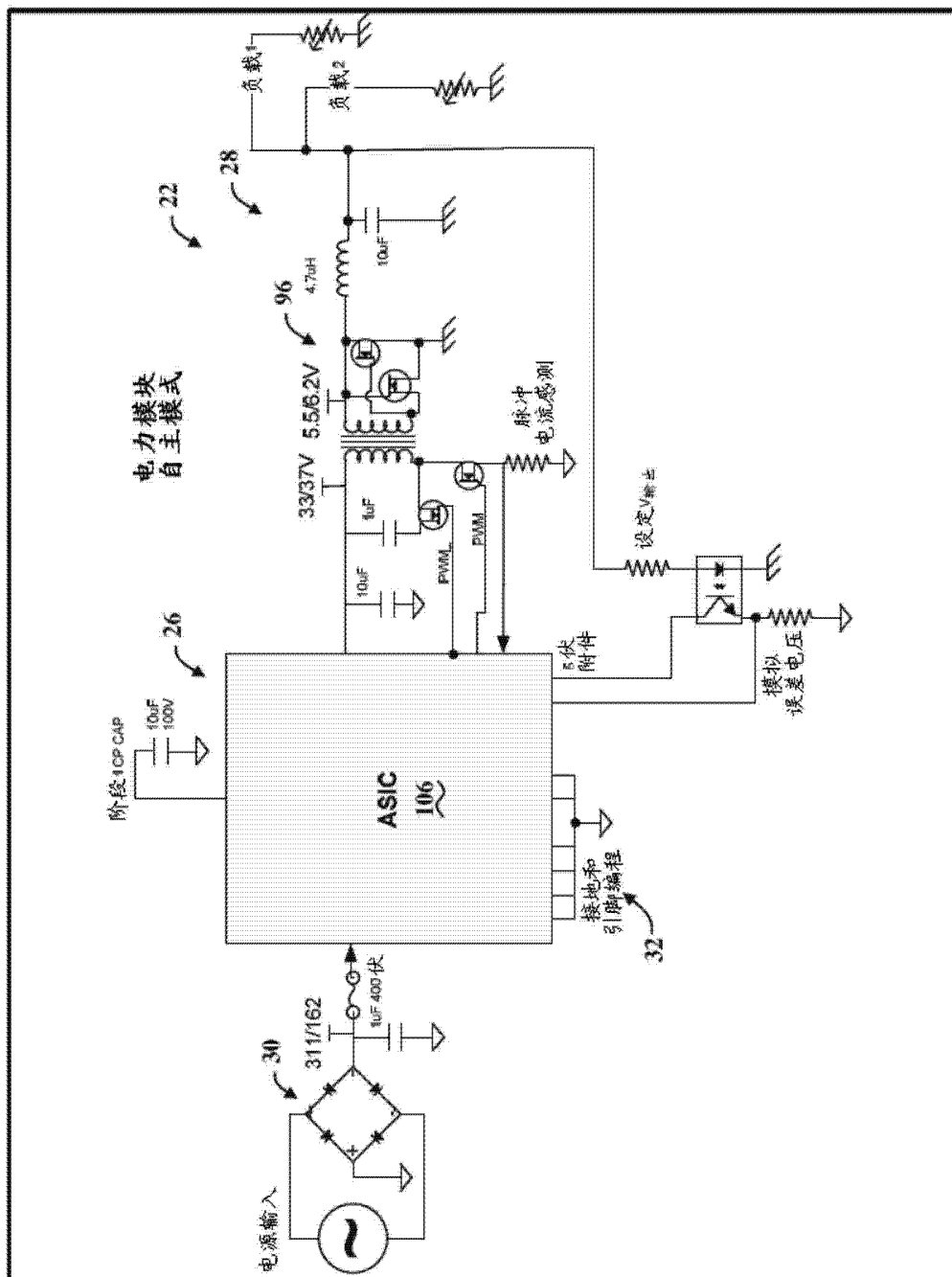


图 28

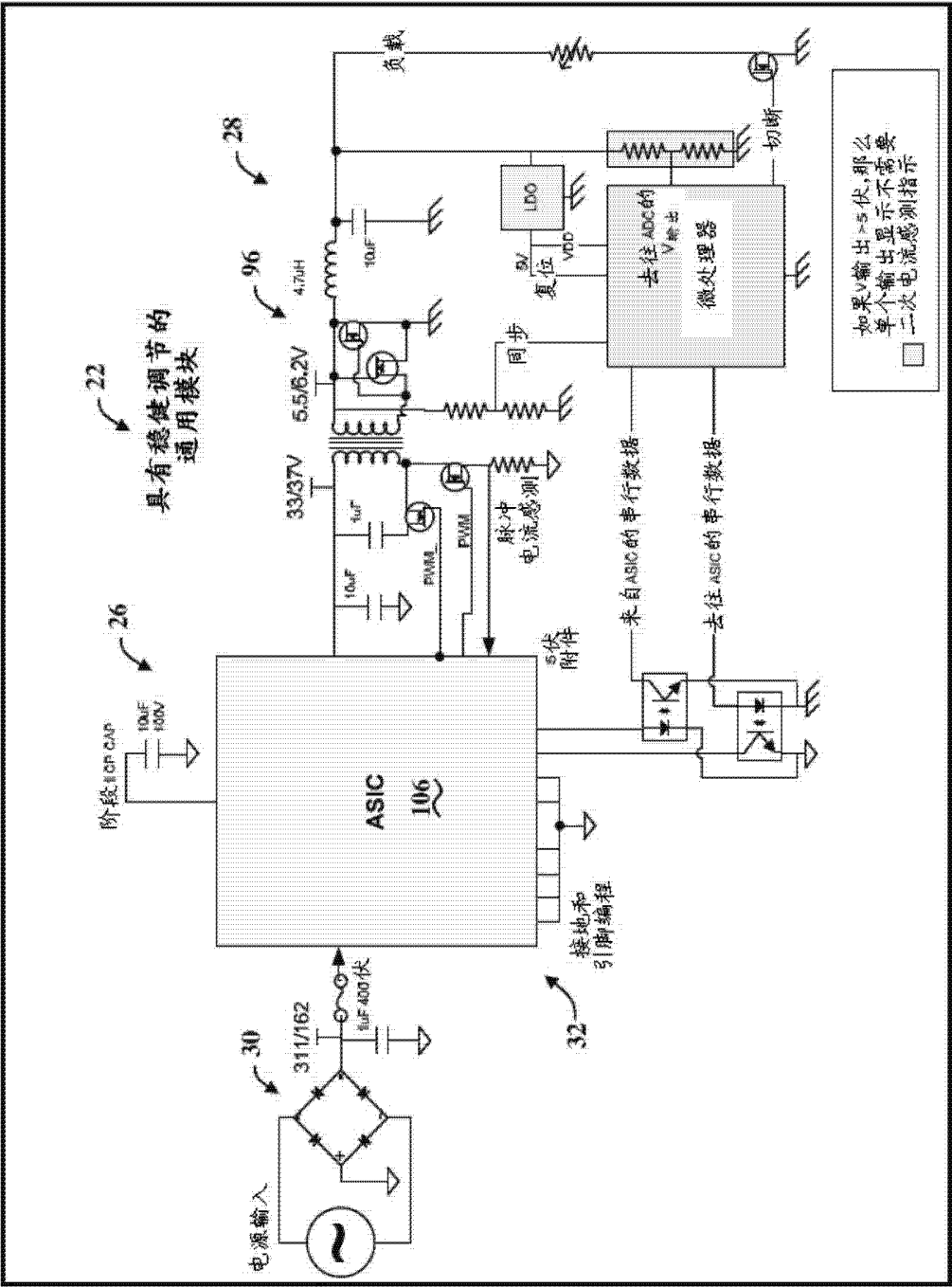


图 29

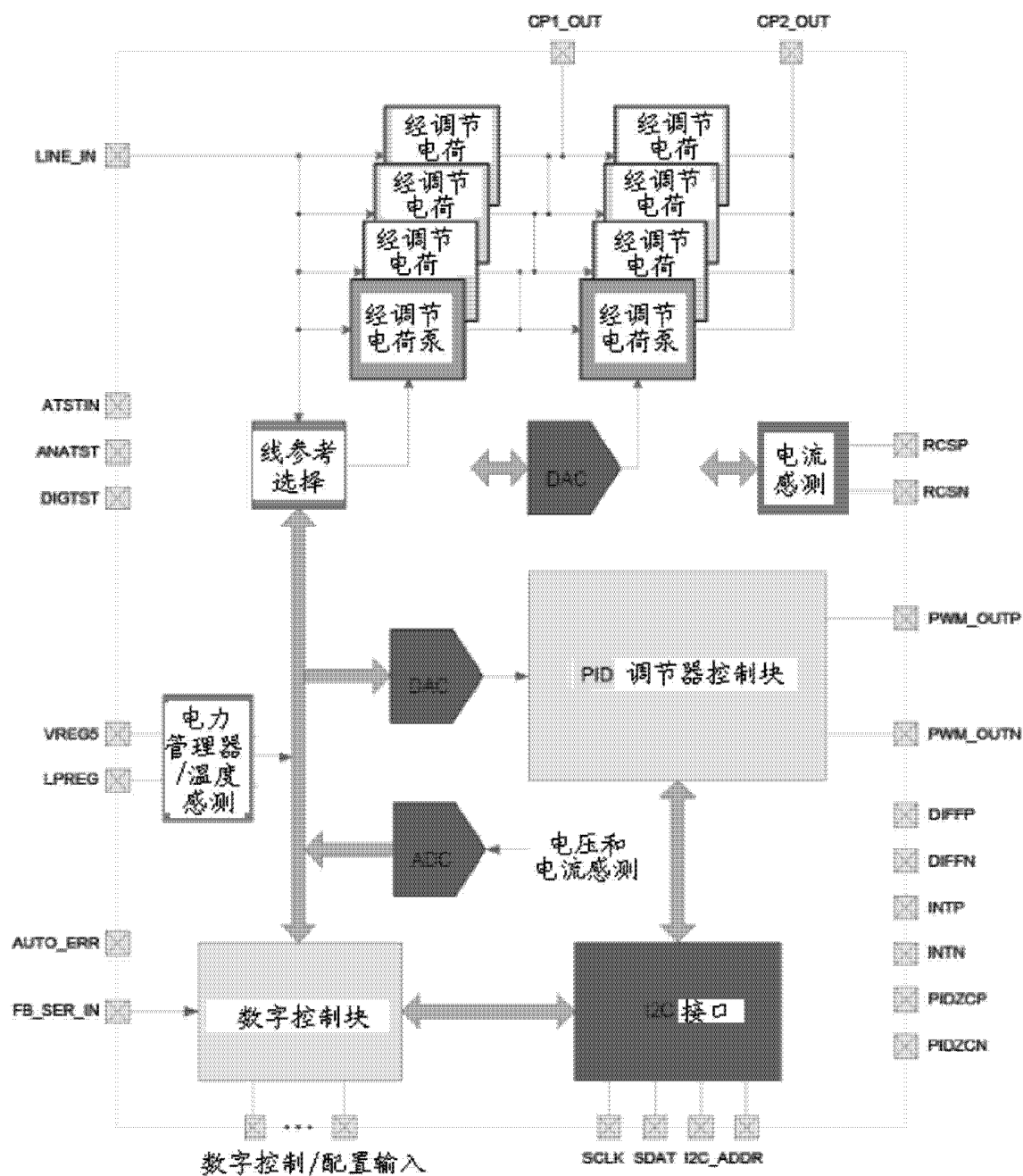


图 31

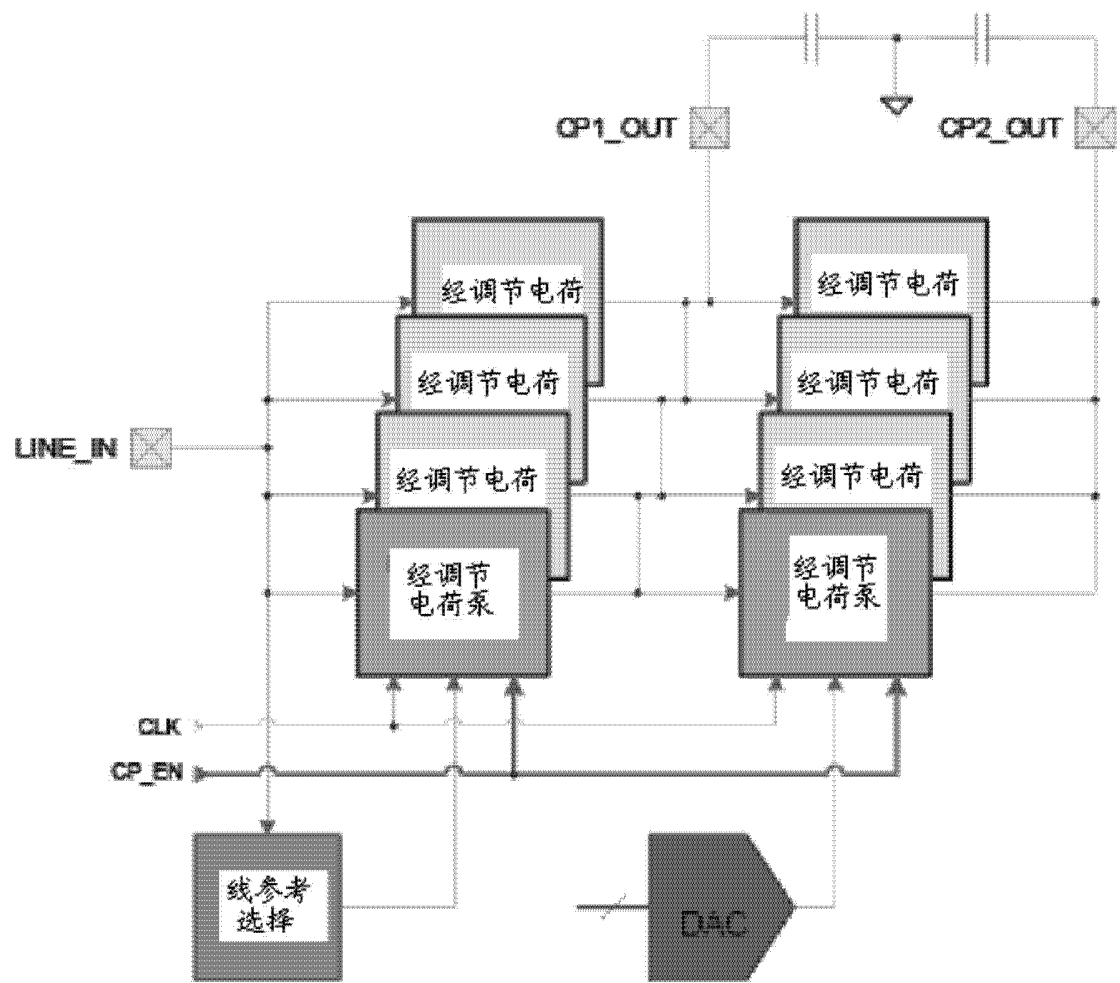


图 32

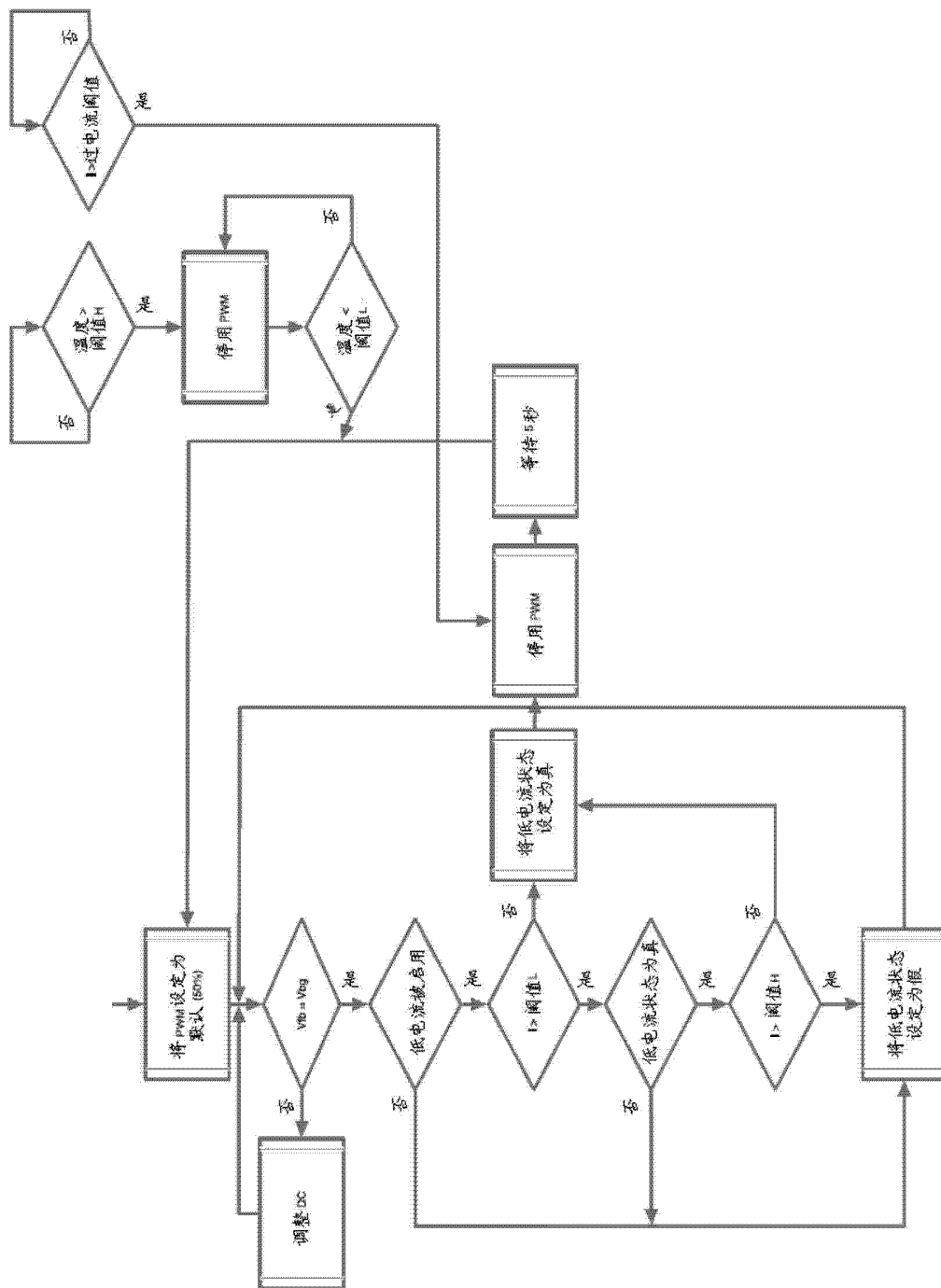


图 33

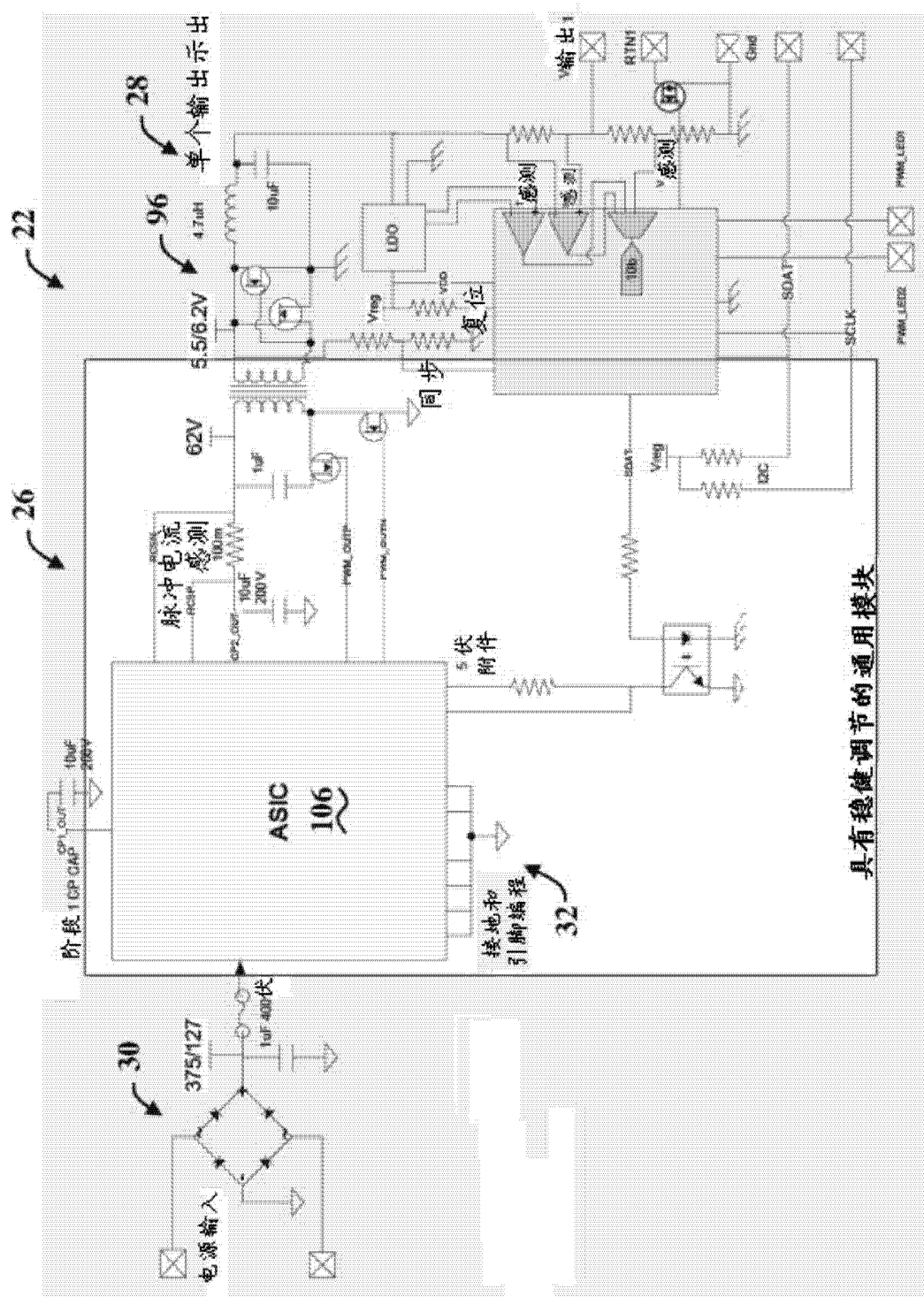


图 34

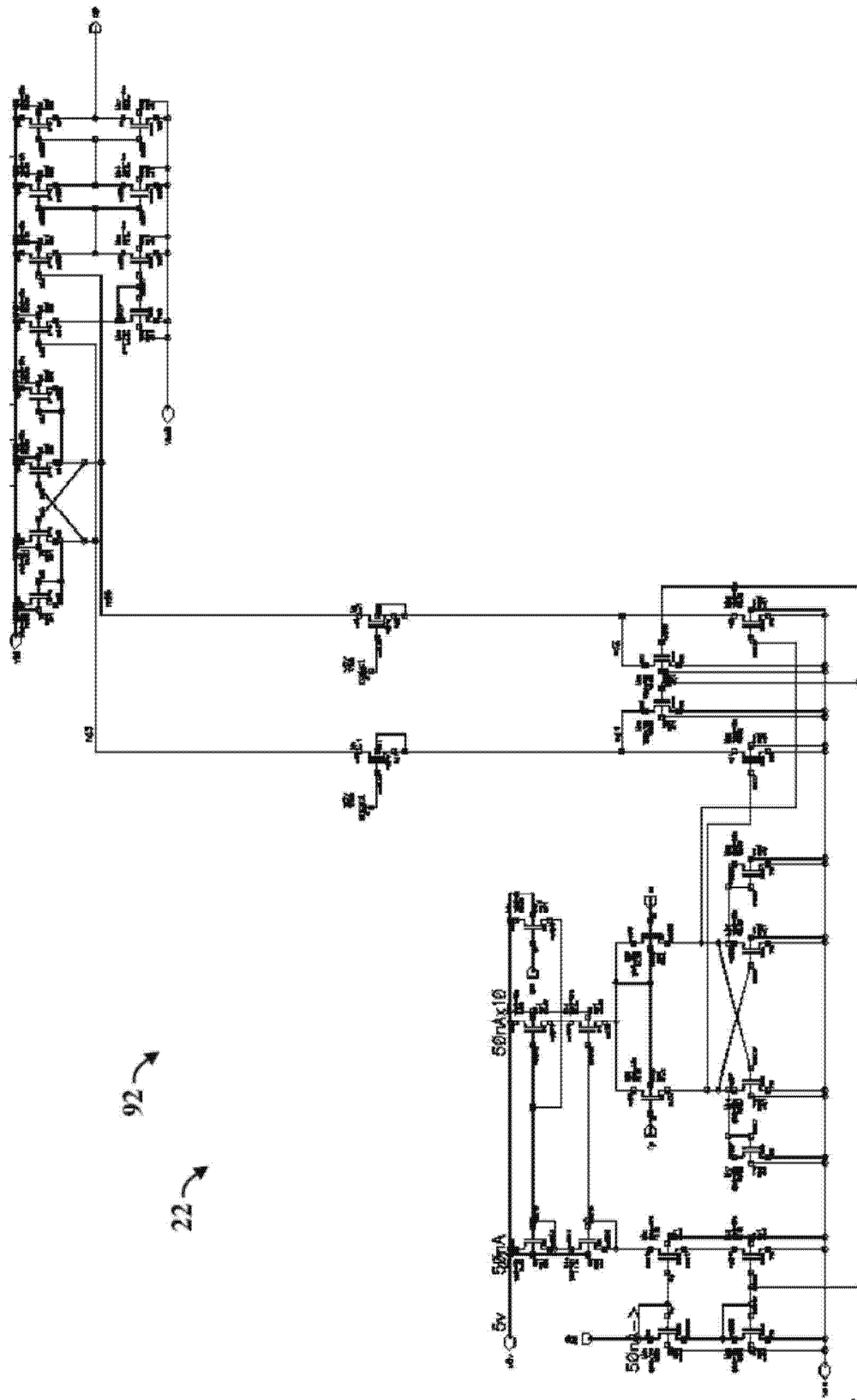


图 36

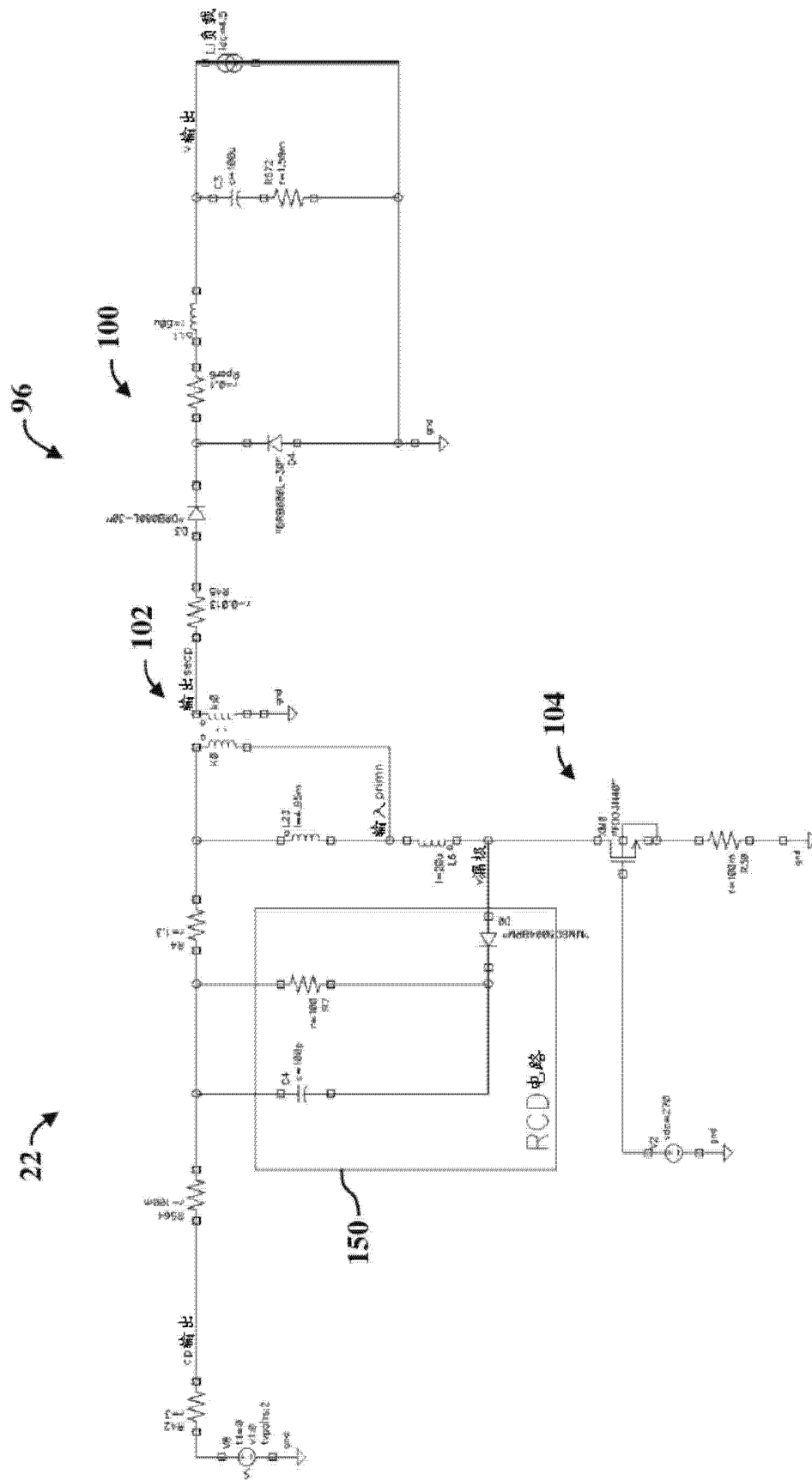


图 37

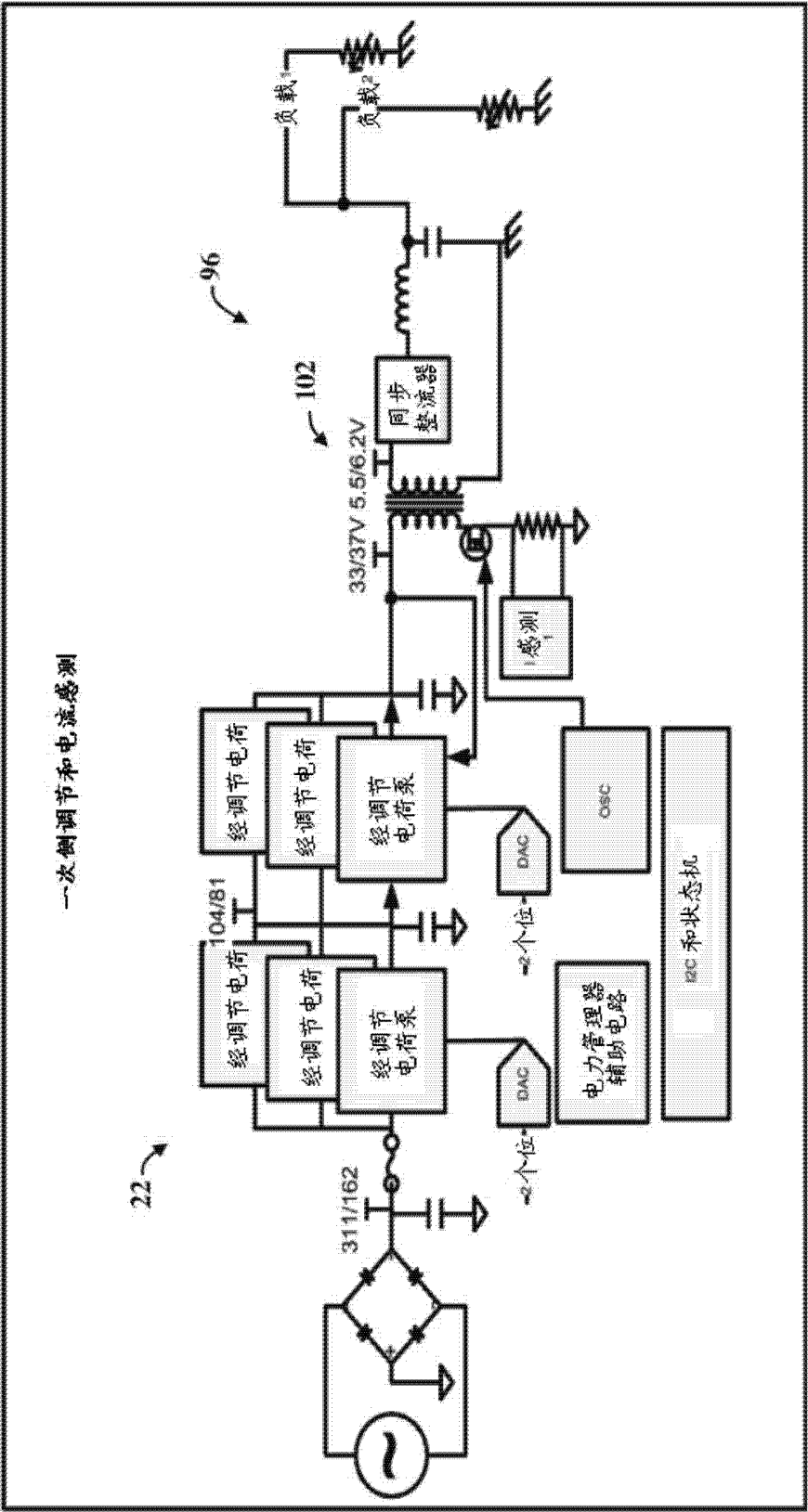


图 38

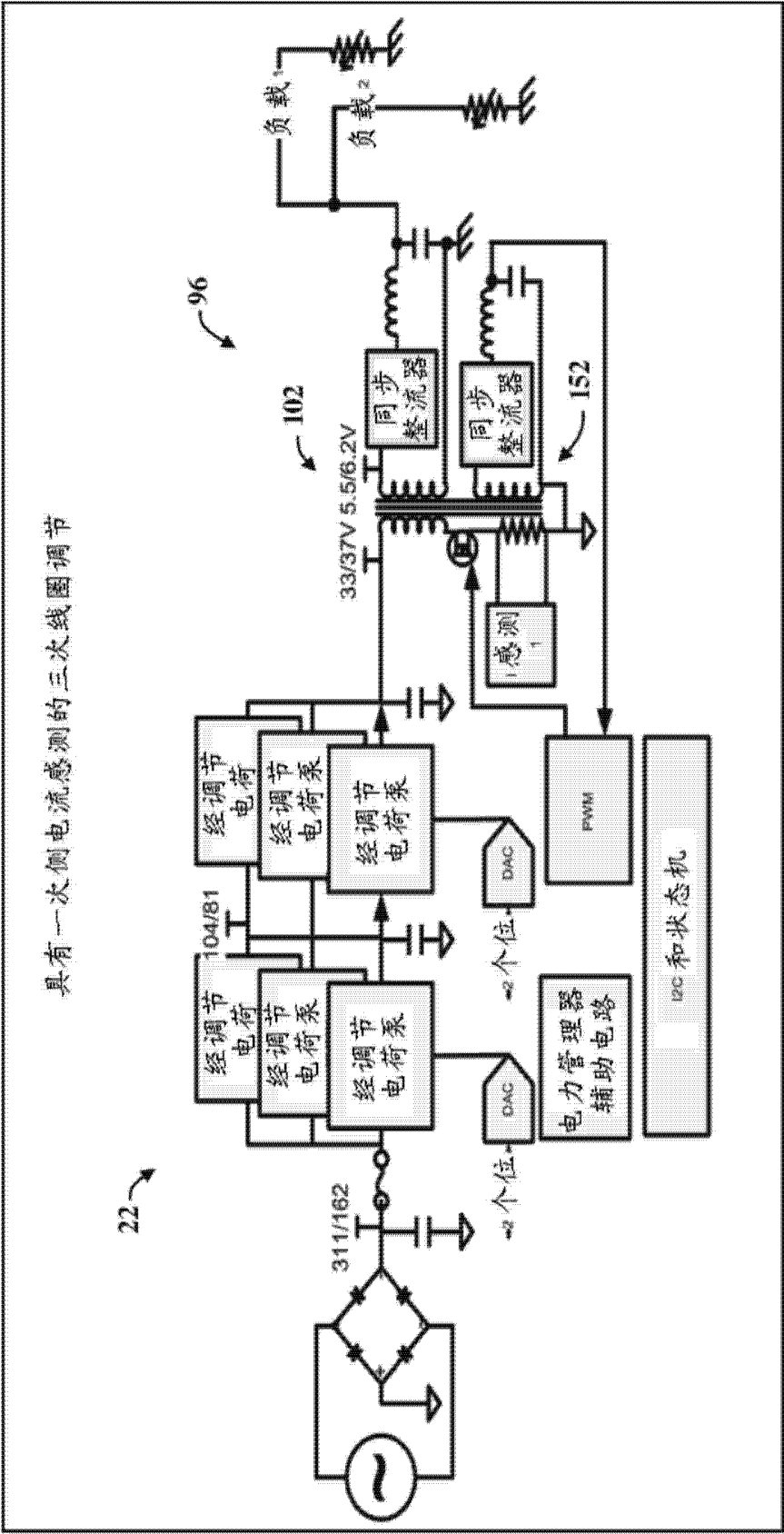


图 39

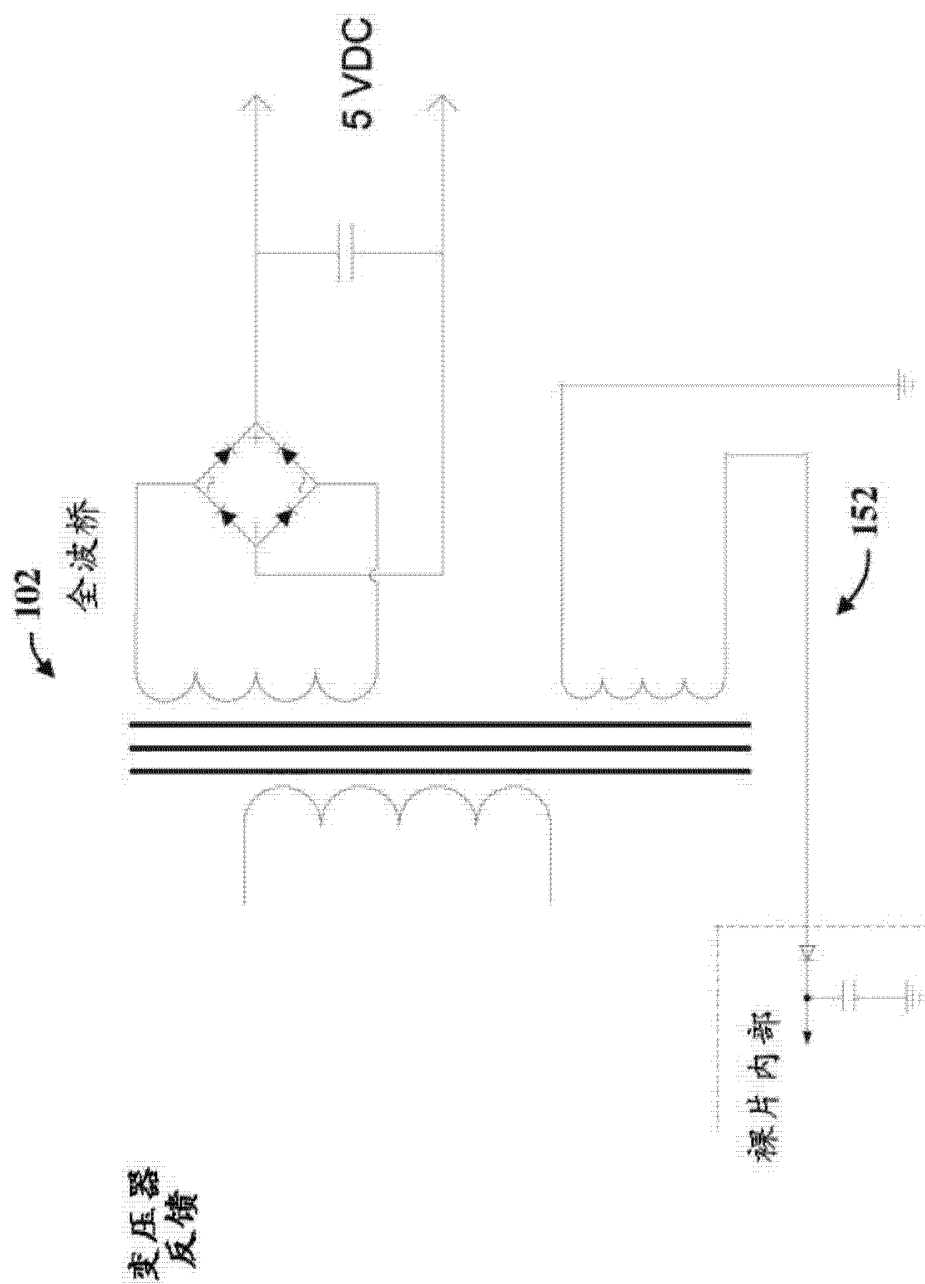


图 40

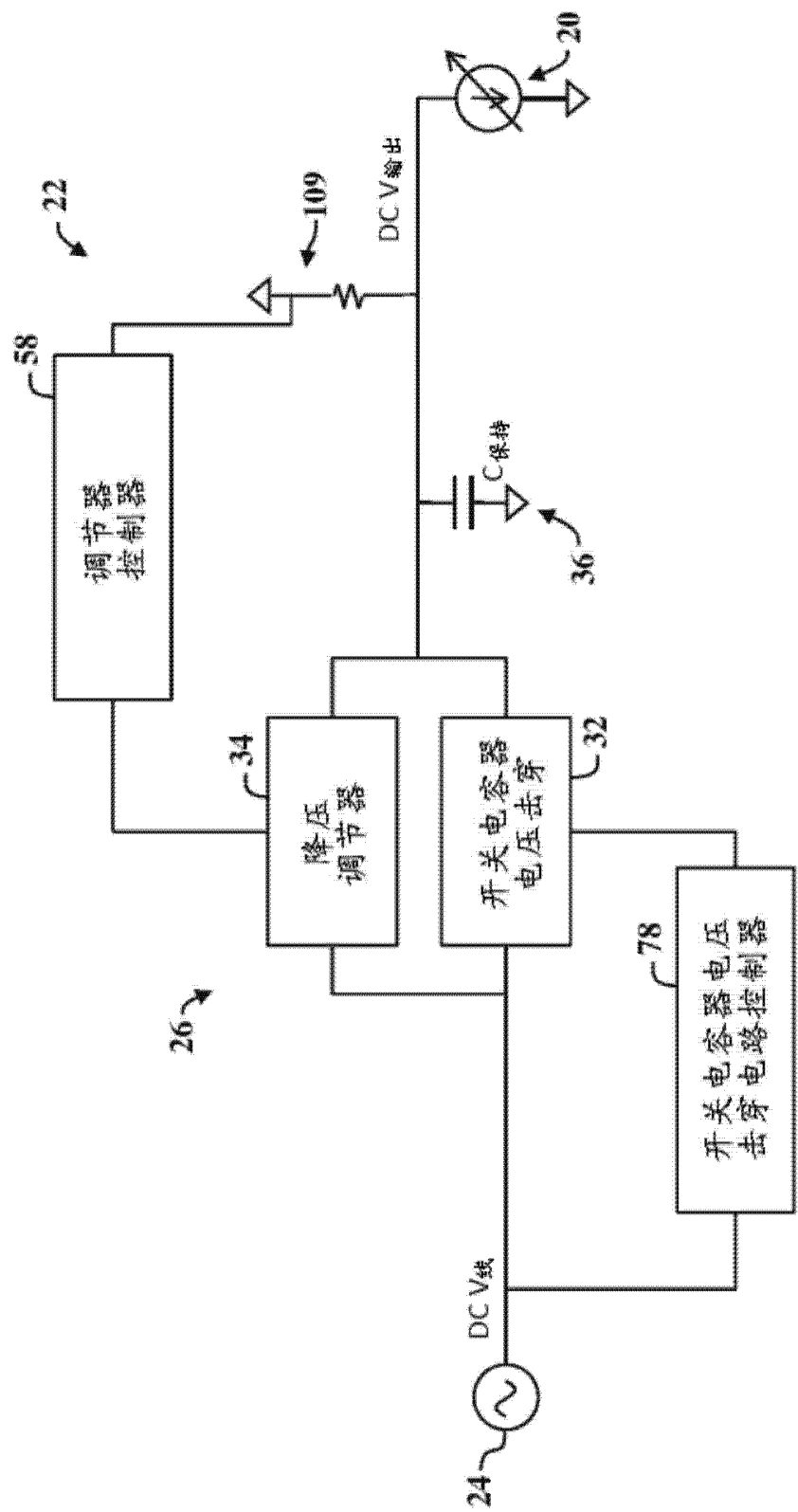


图 41