(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) **World Intellectual Property Organization**
International Bureau

(43) **International Publication Date**
27 August 2015 (27.08.2015)

WIPO | PCT

(10) **International Publication Number**
WO 2015/127014 A1

(51) **International Patent Classification**:
H04L 5/16 (2006.01) *H04B 1/44* (2006.01)

(21) **International Application Number**:
PCT/US2015/016512

(22) **International Filing Date**:
19 February 2015 (19.02.2015)

(25) **Filing Language**: English

(26) **Publication Language**: English

(30) **Priority Data**:
61/941,922 19 February 2014 (19.02.2014) US
14/311,355 23 June 2014 (23.06.2014) US

(63) **Related by continuation (CON) or continuation-in-part (CIP) to earlier application**:
US 14/311,355 (CON)
Filed on 23 June 2014 (23.06.2014)

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(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,

[Continued on next page]

(54) **Title**: CONTROL OF TX/RX MODE IN SERIAL HALF-DUPLEX TRANSCEIVER SEPARATELY FROM COMMUNICATING HOST

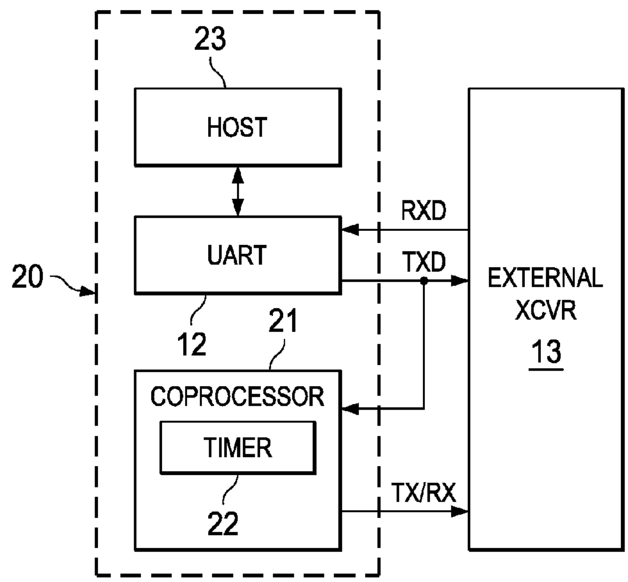

FIG. 2

(57) **Abstract**: In described examples, signaling (TX/RX) to control transmit/receive mode transitions of a serial half-duplex transceiver (13) coupled externally to an integrated circuit (20) is provided by the integrated circuit (20) separately (21) from a host processor (23) of the integrated circuit (20) with which the transceiver (13) communicates. This can avoid slow transceiver (13) turnaround times that may be associated with host processor (23) control of the mode transitions.

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SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

CONTROL OF TX/RX MODE IN SERIAL HALF-DUPLEX TRANSCEIVER SEPARATELY FROM COMMUNICATING HOST

[0001] This relates generally to communication by an integrated circuit, and more particularly to control of serial half-duplex communication by an integrated circuit.

BACKGROUND

[0002] Serial communication is common in industrial control applications. For example, serial half-duplex communication in accordance with RS-485 is widely used in automation systems. Applications such as factory automation systems often employ programmable logic controllers that use RS-485 for communication. Some systems are moving to Ethernet-based communication, but still require support for prevalent legacy systems. For example, RS-485 does not specify speed, format and protocol of the serial communication. Interoperability of devices from different manufacturers, even if similar, is not assured by merely complying with the signal level specifications.

[0003] An example of a conventional communication system using serial half-duplex communication is shown diagrammatically in FIG. 1, in which an integrated circuit 10 (e.g., a RISC microprocessor), including a host processor 11 and a universal asynchronous receiver/transmitter (UART) 12, cooperates with an external transceiver (XCVR) 13, such as a further integrated circuit. The UART 12 outputs to the transceiver 13 data TXD, which has been received from the host processor 11 and is transmitted by the transceiver onto a devices bus that has one or more connected devices, as shown diagrammatically at 14. Similarly, the UART 12 receives from the transceiver 13 data RXD, which has been received by the transceiver 13 from the devices bus 14. The UART 12 provides this received data to the host processor 11. The host processor 11 provides to the transceiver 13 control signaling TX/RX, which appropriately enables and disables transmit operation and receive operation of the transceiver 13.

[0004] A turn-around operation occurs when the host processor 11 (using the TX/RX signal) switches the transceiver 13 from a transmit (TX) mode to a receive (RX) mode, or vice versa. For example, for transition from TX mode to RX mode, turn-around time is the time required to transition the transceiver 13 from the TX mode (where transmit and receive operations of the transceiver 13 are respectively enabled and disabled) to the RX mode (where transmit and receive operations of the transceiver 13 are respectively disabled and enabled). This turn-around time begins when the last transmitted bit has completely traversed the transceiver 13.

[0005] For communication in many automation system applications, low latency (e.g., aggressively low latency) is important. For example, the turn-around from TX mode to RX mode should happen as soon as possible after the last transmitted bit has traversed the external transceiver (e.g., 13 in FIG. 1). Accordingly, the turn-around time from TX mode to RX mode should be as short as possible.

SUMMARY

[0006] In described examples, an integrated circuit apparatus includes a host processor and a UART. The UART is coupled for communication with the host processor and configured for serial half-duplex communication with a transceiver that is external to the apparatus. The transceiver assumes a transmit mode of operation and a receive mode of operation during the serial half-duplex communication. Also, the apparatus includes logic that is separate from the host processor, coupled to the UART, and responsive to operation of the UART for signaling to the transceiver respective indications of when to assume the transmit mode and when to assume the receive mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 diagrammatically shows a conventional communication system using serial half-duplex communication.

[0008] FIG. 2 diagrammatically shows a communication system according to example embodiments.

[0009] FIG. 3 shows operations that may be performed by the system of FIG. 2.

[0010] FIG. 4 diagrammatically shows a communication system according to further example embodiments.

[0011] FIG. 5 shows operations that may be performed by the system of FIG. 4.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0012] Depending on the software used in the host processor (such as shown at 11 in FIG. 1), the turn-around time associated with a transition from the TX mode to the RX mode of an external serial half-duplex transceiver (such as shown at 13 in FIG. 1) could have a negative impact on the receive capability of the communication link. If the turn-around time is too long, some of the incoming RX data will be missed. Some link protocols require the turn-around operation to occur within two bit times. In at least one example, for communication at 115.2k baud, a turn-around time of two bit times would be well within the commonly requested 130us.

[0013] Example embodiments control TX/RX mode transitions of the external transceiver separately from the host processor, thereby avoiding slow turn-around times that may be associated with host processor control of the TX/RX mode transitions. Some embodiments provide, on the same integrated circuit as the host processor, logic that is separate from the host processor and controls the TX/RX mode transitions.

[0014] FIG. 2 diagrammatically shows a communication system according to example embodiments. In the system of FIG. 2, a serial half-duplex UART 12 within an integrated circuit 20 interfaces communications between a host processor 23 of the integrated circuit 20 and an external transceiver 13 (an integrated circuit in some embodiments) that is coupled in turn to a devices bus (not explicitly shown in FIG. 2). However, in the system of FIG. 2, a coprocessor 21 (in integrated circuits such as 10 and 20 of FIGS. 1 and 2) is used for controlling transitions between the TX and RX modes of the transceiver 13. Thus, the host processor 23 of FIG. 2 does not control the TX/RX mode transitions, whereas the host processor 11 of FIG. 1 does control those transitions.

[0015] The coprocessor 21 controls the TX/RX mode transitions by exploiting knowledge of the timing and structure of serial data frames (also referred to as characters) transmitted at TXD by the UART 12. For example, frames transmitted at TXD usually begin with a start bit that is followed by a predetermined number of data bits (and one or more parity bits in some embodiments), which are in turn followed by one or more stop bits (usually one stop bit). In some embodiments, the frame contains eight data bits. The coprocessor 21 is coupled to the TXD output of the UART 12, and monitors the transmitted frame. Based on this monitoring of the transmitted frame, the coprocessor 21 outputs to the transceiver 13 signaling at TX/RX to indicate selection of the TX mode of the transceiver 13.

[0016] In the aforementioned frame monitoring, the coprocessor 21 monitors the TXD output of the UART 12 to detect occurrence of a start bit. Detection of the start bit triggers the coprocessor 21 to signal (at TX/RX) immediately for the TX mode of the transceiver 13 (e.g., TX enabled and RX disabled). In some embodiments, the TX or RX mode is selected by simply toggling a single digital signal that, depending on its logic level, enables TX while disabling RX, or vice versa. Detection of the start bit also triggers operation of a timer function at 22 in coprocessor 21. The total amount of time required to transmit a frame, which includes a start bit, multiple data (and optional parity) bits, and a stop bit, is known to the coprocessor 21. When triggered by start bit detection, the timer function 22 begins timing the frame transmission. When the timer function 22 indicates that the frame transmission time has elapsed, the coprocessor 21 signals the transceiver 13 for selection of the RX mode.

[0017] In some embodiments, the timer function 22 implements a delay time immediately after the frame transmission time has elapsed. The coprocessor 21 waits until the delay time expires, and then signals for the RX mode. The delay time helps ensure that the stop bit has completely traversed the transceiver 13 before the switch to RX mode occurs. Also, the coprocessor 21 continues to monitor the TXD output of the UART 12 during the delay time, thereby avoiding unnecessary toggling of the TX/RX select signal between frames in the event that a burst of consecutive frames is transmitted. Accordingly, the start bit of a second (or other subsequent) frame in a burst may be detected during the delay time, causing TX mode to remain selected. This operation can avoid a situation in which (a) a switch to RX mode occurs after completion of a frame in a burst, followed by (b) a switch right back to TX mode when the start bit of the next frame of the burst is detected. In various embodiments, the delay has various time durations, such as at least one bit transmission time (bit time), some fraction of a bit time, and combinations of at least one bit time and some fraction of a bit time.

[0018] In various embodiments, firmware for the coprocessor 21 provides configuration parameters including one or more of the total transmission time for a frame, the bit time (usually the same for all bits of a frame), the frame structure, and the delay time. In some embodiments, the use of the delay is an option. In such optional delay embodiments, the delay time parameter can be zero if the no-delay option is in effect.

[0019] The above-described use of the coprocessor 21 frees the host processor 23 from the task of switching the TX/RX mode of the transceiver 13. This is in contrast with conventional arrangements such as described above relative to FIG. 1, wherein the host processor performs the task of switching the TX/RX mode. The mode control by coprocessor 21 helps to avoid occurrences of excessive turn-around times that may be associated with host processor control.

[0020] FIG. 3 shows operations that may be performed according to example embodiments. In some embodiments, the system of FIG. 2 is capable of performing the operations of FIG. 3. At

31, monitoring for a start bit is shown. If a start bit is detected at 31, the TX mode is selected at 32, and a timer function begins at 33. When the timer expires at 34, a delay begins at 35. As shown at 36 and 37, monitoring for a start bit occurs at 36 during execution of the delay. If a start bit is detected at 36, operation proceeds to 32 where TX mode remains selected. If the delay time expires at 37 without detection of a start bit at 36, the RX mode is selected at 38, after which the next start bit is awaited at 31. Some embodiments do not implement the delay, while others implement it as an option. The broken line in FIG. 3 shows operation in no-delay embodiments, and in optional delay embodiments where the no-delay option is in effect. In both cases, the RX mode is selected at 38 immediately upon expiration of the timer at 34 as shown.

[0021] FIG. 4 diagrammatically shows a communication system according to further example embodiments. The system of FIG. 4 is generally similar to that of FIG. 2, except a coprocessor 41 within the integrated circuit 40 uses a line status register (LSR) 42 (conventionally available in the UART 12) to track progress of frame transmission on the TXD output of the UART 12. The LSR 42 conventionally indicates when transmit hold and shift registers of the UART 12 are empty, which is an indication that transmission of the frame is complete.

[0022] FIG. 5 shows further operations that may be performed according to example embodiments. In some embodiments, the system of FIG. 4 is capable of performing the operations of FIG. 5. At 51, monitoring for a start bit is shown. If a start bit is detected at 51, the TX mode is selected at 52, and the LSR is monitored starting at 53. When the LSR indicates at 54 that transmission is complete, the RX mode is selected at 55, after which the next start bit is awaited at 51.

[0023] The techniques described above relative to FIGS. 2-5 are easily scalable to accommodate multiple UARTs 12 in each of the integrated circuits 20 and 40, with multiple external transceivers 13 respectively coupled to the multiple UARTs. Such multiple UART/XCVR combinations are usually the case, such as in factory automation applications. The firmware for the coprocessor 21 or 41 provides configuration parameters to identify, for each of the multiple UART/XCVR combinations, which terminals of the integrated circuit are to be used by the coprocessor for monitoring the TXD output of the associated UART 12, and for outputting the TX/RX signal to the associated XCVR 13.

[0024] No interrupt processing is required on the host processor for TX/RX mode control in the above-described embodiments, so no impact exists on the host UART driver software operation. The firmware for the coprocessor may be loaded in conventional fashion by the host processor (e.g., a Linux or RTOS host processor driver) written for the operating system used on the host processor.

[0025] In some embodiments, the transceivers 13 are provided as RS-485 transceivers, such as the commercially available SN65HVD82 RS-485 transceiver. In some embodiments, the integrated circuits 20 and 40 are provided as RISC microprocessors, such as the commercially available AM335x/AM437x/AM57xx or similarly enabled microprocessors.

[0026] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An integrated circuit apparatus, comprising:

a host processor;

a universal asynchronous receiver/transmitter (UART) coupled for communication with the host processor and configured for serial half-duplex communication with a transceiver that is external to the apparatus, wherein the transceiver assumes a transmit mode of operation and a receive mode of operation during the serial half-duplex communication; and

logic that is separate from the host processor, coupled to the UART, and responsive to operation of the UART for signaling to the transceiver respective indications of when to assume the transmit mode and when to assume the receive mode.

2. The apparatus of claim 1, wherein the logic is configured to detect commencement and completion of a transmission from the UART to the transceiver.

3. The apparatus of claim 2, wherein the logic is responsive to detection of the commencement and detection of the completion for signaling the transceiver to assume the transmit mode and the receive mode, respectively.

4. The apparatus of claim 3, wherein the logic is configured to detect the commencement by monitoring for a start bit of the transmission.

5. The apparatus of claim 3, wherein the logic is configured to detect the completion by tracking elapsed time of the transmission.

6. The apparatus of claim 3, wherein the logic is configured to detect the completion by monitoring a transmit status indication provided by the UART.

7. The apparatus of claim 6, wherein the UART includes a status register that provides the transmit status indication.

8. The apparatus of claim 3, wherein the logic is configured to implement a delay between the detection of completion and the signaling the transceiver to assume the receive mode.

9. A communication system, comprising:

a transceiver configured to perform serial half-duplex communication during which the transceiver assumes a transmit mode of operation and a receive mode of operation; and

an integrated circuit including a host processor, a universal asynchronous receiver/transmitter (UART) coupled for communication with the host processor, and logic that is separate from the host processor and coupled to the UART;

wherein the transceiver is external to the integrated circuit and coupled to the UART and the logic;

wherein the UART is configured to cooperate with the transceiver to perform the serial half-duplex communication; and

wherein the logic is responsive to operation of the UART for signaling to the transceiver respective indications of when to assume the transmit mode and when to assume the receive mode.

10. The system of claim 9, wherein the logic is configured to detect commencement and completion of a transmission from the UART to the transceiver.

11. The system of claim 10, wherein the logic is responsive to detection of the commencement and detection of the completion for signaling the transceiver to assume the transmit mode and the receive mode, respectively.

12. The system of claim 11, wherein the logic is configured to detect the commencement by monitoring for a start bit of the transmission.

13. The system of claim 11, wherein the logic is configured to detect the completion by tracking elapsed time of the transmission.

14. The system of claim 11, wherein the logic is configured to detect the completion by monitoring a transmit status indication provided by the UART.

15. The system of claim 14, wherein the UART includes a status register that provides the transmit status indication.

16. The system of claim 11, wherein the logic is configured to implement a delay between the detection of completion and the signaling the transceiver to assume the receive mode.

17. A communication system, comprising:

a transceiver configured to perform serial half-duplex communication during which the transceiver assumes a transmit mode of operation and a receive mode of operation;

an integrated circuit including a host processor, a universal asynchronous receiver/transmitter (UART) coupled for communication with the host processor, and logic that is separate from the host processor and coupled to the UART;

wherein the transceiver is external to the integrated circuit and coupled to the UART and the logic;

wherein the UART is configured to cooperate with the transceiver to perform the serial half-duplex communication;

wherein the logic is responsive to operation of the UART for signaling to the transceiver respective indications of when to assume the transmit mode and when to assume the receive mode; and

at least one device coupled to the transceiver for communication with the host processor via the transceiver and the UART.

18. The system of claim 17, wherein the logic is configured to detect commencement and completion of a transmission from the UART to the transceiver.

19. The system of claim 18, wherein the logic is responsive to detection of the commencement and detection of the completion for signaling the transceiver to assume the transmit mode and the receive mode, respectively.

20. The system of claim 19, wherein the logic is configured to detect the commencement by monitoring for a start bit of the transmission, and to detect the completion by one of tracking elapsed time of the transmission and monitoring a transmit status indication provided by the UART.

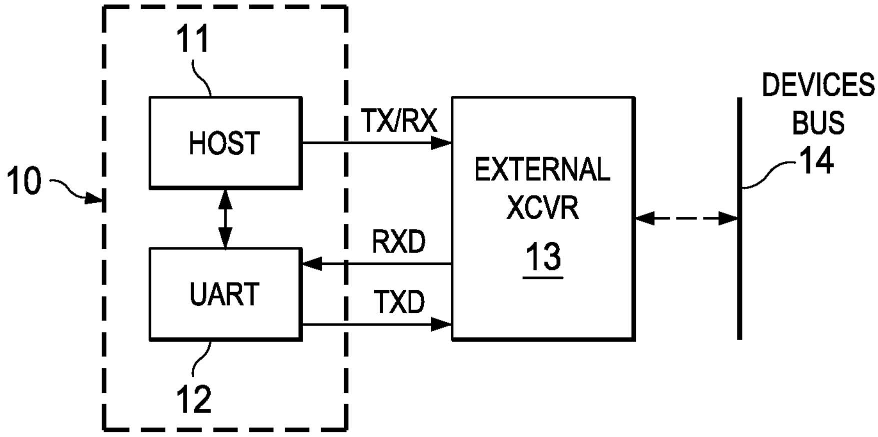


FIG. 1
(PRIOR ART)

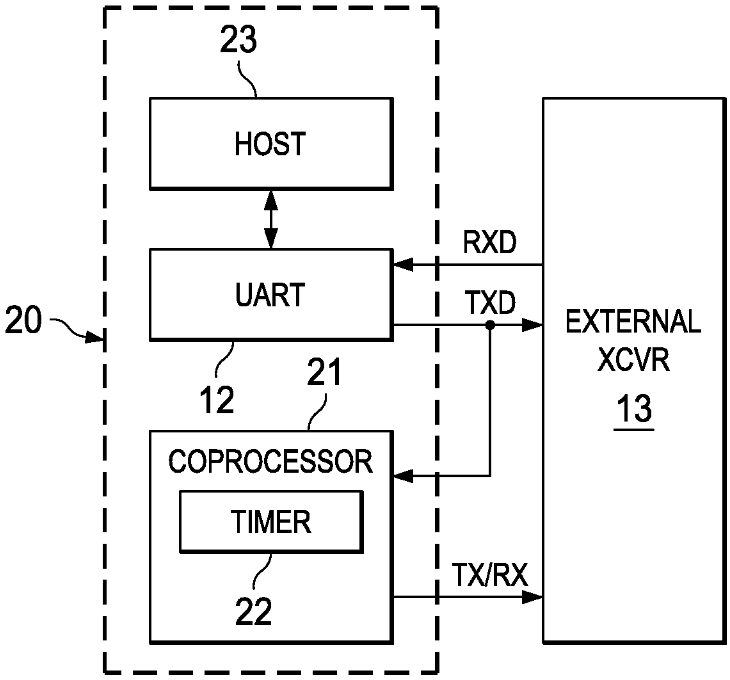
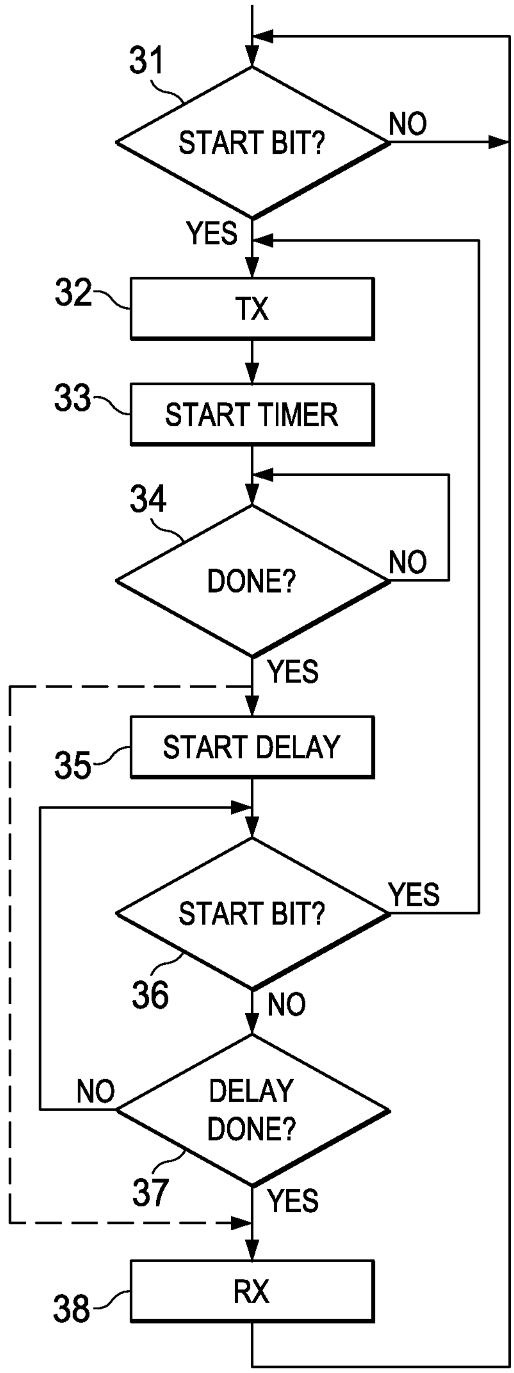


FIG. 2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34
DONE?
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START DELAY
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START BIT?
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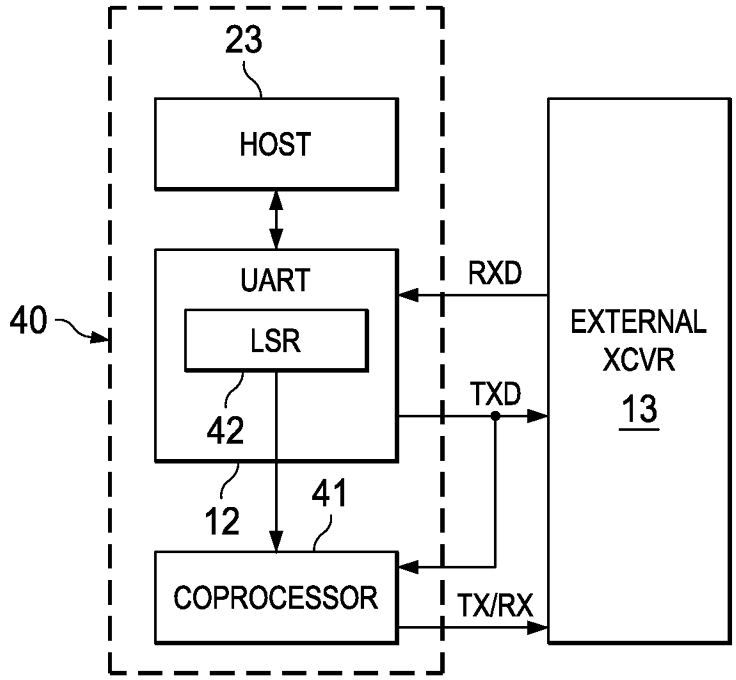
NO
NO
DELAY DONE?
37
YES
RX
38

FIG. 3


23
HOST
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LSR
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12
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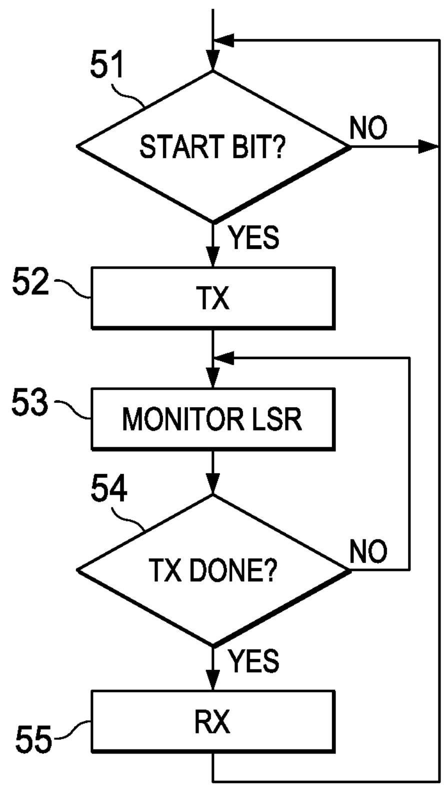
COPROCESSOR
RXD
TXD
TX/RX
EXTERNAL
XCVR
13

FIG. 4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55
RX

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2015/016512

A. CLASSIFICATION OF SUBJECT MATTER

H04L 5/16 *(2006.01)*
H04B 1/44 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04L 1/00-1/24, 5/00-5/26, H04B 1/00-1/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009/0213729 A1 (QUALCOMM INCORPORATION et al) 27.08.2009	1-20
A	US 6385210 B1 (Ford Global Technologies Inc) 07.05.2002	1-20
A	US 5953372 A (Standard Microsystems Corporation) 14.09.1999	1-20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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"&" document member of the same patent family

Date of the actual completion of the international search

28 May 2015 (28.05.2015)

Date of mailing of the international search report

10 June 2015 (10.06.2015)

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