

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
18 January 2007 (18.01.2007)

PCT

(10) International Publication Number
WO 2007/008934 A1

- (51) International Patent Classification:
H01L 29/786 (2006.01) **H01P 1/15** (2006.01)
- (21) International Application Number:
PCT/US2006/026965
- (22) International Filing Date: 11 July 2006 (11.07.2006)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/698,523 11 July 2005 (11.07.2005) US
11/484,370 10 July 2006 (10.07.2006) US
- (71) Applicant (for all designated States except US): **PEREGRINE SEMICONDUCTOR CORPORATION** [US/US]; 9450 Carroll Park Drive, San Diego, CA 92121 (US).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **BRINDLE, Christopher, N.** [US/US]; 13351 Silver Lake Drive, Poway, CA 92064 (US). **STUBER, Michael, A.** [US/US]; 7905 Vista Canela, Carlsbad, CA 92009 (US). **KELLY, Dylan, J.** [US/US]; 2677 Piantino Circle, San Diego,

CA 92108 (US). **KEMERLING, Clint, L.** [US/US]; 3658 Camino Marglesa, Escondido, CA 92025 (US). **IMTHURN, George, P.** [US/US]; 4650 Huggins Street, San Diego, CA 92122 (US). **WELSTAND, Robert, B.** [US/US]; 7365 Dancy Road, San Diego, CA 92126 (US). **BURGNER, Mark, L.** [US/US]; 4604 Brighton Avenue, San Diego, CA 92107 (US).

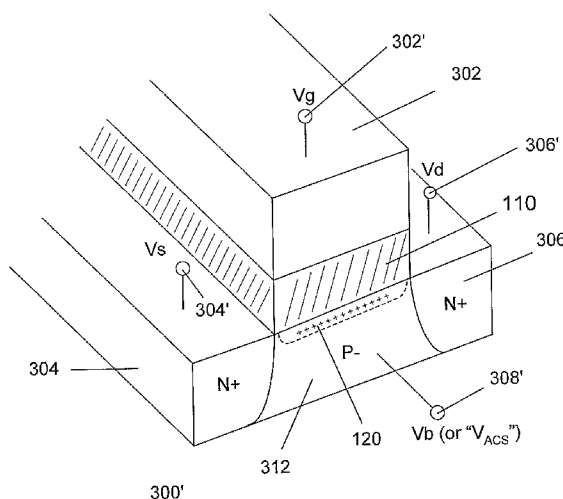
(74) Agent: **JAQUEZ, Martin, J.**; JAQUEZ & ASSOCIATES, 6265 Greenwich Drive, Suite 100D, San Diego, CA 92122 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),

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(54) Title: METHOD AND APPARATUS FOR USE IN IMPROVING LINEARITY OF MOSFETS USING AN ACCUMULATED CHARGE SINK



(57) Abstract: A method and apparatus for use in improving the linearity characteristics of MOSFET devices using an accumulated charge sink (ACS) are disclosed. The method and apparatus are adapted to remove, reduce, or otherwise control accumulated charge in SOI MOSFETs, thereby yielding improvements in FET performance characteristics. In one exemplary embodiment, a circuit having at least one SOI MOSFET is configured to operate in an accumulated charge regime. An accumulated charge sink, operatively coupled to the body of the SOI MOSFET, eliminates, removes or otherwise controls accumulated charge when the FET is operated in the accumulated charge regime, thereby reducing the nonlinearity of the parasitic off-state source-to-drain capacitance of the SOI MOSFET. In RF switch circuits implemented with the improved SOI MOSFET devices, harmonic and intermodulation distortion is reduced by removing or otherwise controlling the accumulated charge when the SOI MOSFET operates in an accumulated charge regime.

WO 2007/008934 A1



European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Method and Apparatus for use in Improving Linearity of MOSFETs Using an Accumulated Charge Sink

001 BACKGROUND

1. *Field*

5 **002** The present invention relates to metal-oxide-semiconductor (MOS) field effect transistors (FETs), and particularly to MOSFETs fabricated on Semiconductor-On-Insulator ("SOI") and Semiconductor-On-Sapphire ("SOS") substrates. In one embodiment, an SOI (or SOS) MOSFET is adapted to control accumulated charge and thereby improve linearity of circuit elements.

2. *Description of Related Art*

10 **003** Although the disclosed method and apparatus for use in improving the linearity of MOSFETs are described herein as applicable for use in SOI MOSFETs, it will be appreciated by those skilled in the electronic device design arts that the present teachings are equally applicable for use in SOS MOSFETs. In general, the present teachings can be used in the implementation of MOSFETs using any convenient semiconductor-on-insulator technology, including silicon-on-
15 insulator technology. For example, the inventive MOSFETs described herein can be implemented using compound semiconductors on insulating substrates. Such compound semiconductors include, but are not limited to, the following: Silicon Germanium (SiGe), Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN), Silicon Carbide (SiC), and II-VI compound semiconductors, including Zinc Selenide (ZnSe) and Zinc Sulfide (ZnS). The present teachings also may be used in
20 implementing MOSFETs fabricated from thin-film polymers. Organic thin-film transistors (OTFTs) utilize a polymer, conjugated polymers, oligomers, or other molecules to form the insulating gate dielectric layer. The present inventive methods and apparatus may be used in implementing such OTFTs.

25 **004** It will be appreciated by those skilled in the electronic design arts that the present disclosed method and apparatus apply to virtually any insulating gate technology, and to integrated circuits having a floating body. As those skilled in the art will appreciate, technologies are constantly being developed for achieving "floating body" implementations. For example, the inventors are aware of circuits implemented in bulk silicon wherein circuit implementations are used to "float" the body of the device. In addition, the disclosed method and apparatus can also be implemented using
30 silicon-on-bonded wafer implementations. One such silicon-on-bonded wafer technique uses "direct

silicon bonded" (DSB) substrates. Direct silicon bond (DSB) substrates are fabricated by bonding and electrically attaching a film of single-crystal silicon of differing crystal orientation onto a base substrate. The present disclosure therefore contemplates embodiments of the disclosed method and apparatus implemented in any of the developing floating body implementations. Therefore, references to and exemplary descriptions of SOI MOSFETs herein are not to be construed as limiting the applicability of the present teachings to SOI MOSFETs only. Rather, as described below in more detail, the disclosed method and apparatus find utility in MOSFETs implemented in a plurality of device technologies, including SOS and silicon-on-bonded wafer technologies.

005 As is well known, a MOSFET employs a gate-modulated conductive channel of n-type or p-type conductivity, and is accordingly referred to as an "NMOSFET" or "PMOSFET", respectively. FIGURE 1 shows a cross-sectional view of an exemplary prior art SOI NMOSFET 100. As shown in FIGURE 1, the prior art SOI NMOSFET 100 includes an insulating substrate 118 that may comprise a buried oxide layer, sapphire, or other insulating material. A source 112 and drain 116 of the NMOSFET 100 comprise N⁺ regions (*i.e.*, regions that are heavily doped with an "n-type" dopant material) produced by ion implantation into a silicon layer positioned above the insulating substrate 118. (The source and drain of PMOSFETs comprise P⁺ regions (*i.e.*, regions heavily doped with "p-type" dopant material)). The body 114 comprises a P⁻ region (*i.e.*, a region that is lightly doped with a "p-type" dopant), produced by ion implantation, or by dopants already present in the silicon layer when it is formed on the insulating substrate 118. As shown in FIGURE 1, the NMOSFET 100 also includes a gate oxide 110 positioned over the body 114. The gate oxide 110 typically comprises a thin layer of an insulating dielectric material such as SiO₂. The gate oxide 110 electrically insulates the body 114 from a gate 108 positioned over the gate oxide 110. The gate 108 comprises a layer of metal or, more typically, polysilicon.

006 A source terminal 102 is operatively coupled to the source 112 so that a source bias voltage "V_s" may be applied to the source 112. A drain terminal 106 is operatively coupled to the drain 116 so that a drain bias voltage "V_d" may be applied to the drain 116. A gate terminal 104 is operatively coupled to the gate 108 so that a gate bias voltage "V_g" may be applied to the gate 108.

007 As is well known, when a voltage is applied between the gate and source terminals of a MOSFET, a generated electric field penetrates through the gate oxide to the transistor body. For an enhancement mode device, a positive gate bias creates a channel in the channel region of the MOSFET body through which current passes between the source and drain. For a depletion mode device, a channel is present for a zero gate bias. Varying the voltage applied to the gate

modulates the conductivity of the channel and thereby controls the current flow between the source and drain.

008 For an enhancement mode MOSFET, for example, the gate bias creates a so-called "inversion channel" in a channel region of the body 114 under the gate oxide 110. The inversion channel comprises carriers having the same polarity (*e.g.*, "P" polarity (*i.e.*, hole carriers), or "N" polarity (*i.e.*, electron carriers) carriers) as the polarity of the source and drain carriers, and it thereby provides a conduit (*i.e.*, channel) through which current passes between the source and the drain. For example, as shown in the SOI NMOSFET 100 of FIGURE 1, when a sufficiently positive voltage is applied between the gate 108 and the source 112 (*i.e.* a positive gate bias exceeding a threshold voltage V_{th}), an inversion channel is formed in the channel region of the body 114. As noted above, the polarity of carriers in the inversion channel is identical to the polarity of carriers in the source and drain. In this example, because the source and drain comprise "n-type" dopant material and therefore have N polarity carriers, the carriers in the channel comprise N polarity carriers. Similarly, because the source and drain comprise "p-type" dopant material in PMOSFETs, the carriers in the channel of turned on (*i.e.*, conducting) PMOSFETs comprise P polarity carriers.

009 Depletion mode MOSFETs operate similarly to enhancement mode MOSFETs, however, depletion mode MOSFETs are doped so that a conducting channel exists even without a voltage being applied to the gate. When a voltage of appropriate polarity is applied to the gate the channel is depleted. This, in turn, reduces the current flow through the depletion mode device. In essence, the depletion mode device is analogous to a "normally closed" switch, while the enhancement mode device is analogous to a "normally open" switch. Both enhancement and depletion mode MOSFETs have a gate voltage threshold, V_{th} , at which the MOSFET changes from an off-state (non-conducting) to an on-state (conducting).

010 No matter what mode of operation an SOI MOSFET employs (*i.e.*, whether enhancement or depletion mode), when the MOSFET is operated in an off-state (*i.e.*, the gate voltage does not exceed V_{th}), and when a sufficient nonzero gate bias voltage is applied with respect to the source and drain, an "accumulated charge" may occur under the gate. The "accumulated charge", as defined in more detail below and used throughout the present application, is similar to the "accumulation charge" described in the prior art literature in reference to MOS capacitors. However, the prior art references describe "accumulation charge" as referring only to bias-induced charge existing under a MOS capacitor oxide, wherein the accumulation charge is of the same polarity as the majority carriers of the semiconductor material under the capacitor oxide. In contrast, and as described below in more detail, "accumulated charge" is used herein to refer to gate-bias induced carriers that may accumulate in the body of an off-state MOSFET, even if the majority carriers in the

body do not have the same polarity as the accumulated charge. This situation may occur, for example, in an off-state depletion mode NMOSFET, wherein the accumulated charge may comprise holes (*i.e.*, having P polarity) even though the body doping is N- rather than P-.

011 For example, as shown in FIGURE 1, when the SOI NMOSFET 100 is biased to
5 operate in an off-state, and when a sufficient nonzero voltage is applied to the gate 108, an accumulated charge 120 may accumulate in the body 114 underneath and proximate the gate oxide 110. The operating state of the SOI NMOSFET 100 shown in FIGURE 1 is referred to herein as an "accumulated charge regime" of the MOSFET. The accumulated charge regime is defined in more detail below. The causes and effects of the accumulated charge in SOI MOSFETs are now described
10 in more detail.

012 As is well known, electron-hole pair carriers may be generated in MOSFET
bodies as a result of several mechanisms (*e.g.*, thermal, optical, and band-to-band tunneling electron-hole pair generation processes). When electron-hole pair carriers are generated within an NMOSFET body, for example, and when the NMOSFET is biased in an off-state condition, electrons may be
15 separated from their hole counterparts and pulled into both the source and drain. Over a period of time, assuming the NMOSFET continues to be biased in the off-state, the holes (resulting from the separated electron-hole pairs) may accumulate under the gate oxide (*i.e.*, forming an "accumulated charge") underneath and proximate the gate oxide. A similar process (with the behavior of electrons and holes reversed) occurs in similarly biased PMOSFET devices. This phenomenon is now
20 described with reference to the SOI NMOSFET 100 of FIGURE 1.

013 When the SOI NMOSFET 100 is operated with gate, source and drain bias voltages that deplete the channel carriers in the body 114 (*i.e.*, the NMOSFET 100 is in the off-state), holes may accumulate underneath and proximate the gate oxide 110. For example, if the source bias voltage V_s and the drain bias voltage V_d are both zero (*e.g.*, connected to a ground contact, not
25 shown), and the gate bias voltage V_g comprises a sufficiently negative voltage with respect to ground and with respect to V_{th} , holes present in the body 114 become attracted to the channel region proximate the gate oxide 110. Over a period of time, unless removed or otherwise controlled, the holes accumulate underneath the gate oxide 110 and result in the accumulated charge 120 shown in FIGURE 1. The accumulated charge 120 is therefore shown as positive "+" hole carriers in FIGURE
30 1. In the example given, V_g is negative with respect to V_s and V_d , so electric field regions 122 and 124 may also be present.

Accumulated Charge Regime Defined

014 The accumulated charge is opposite in polarity to the polarity of carriers in the channel. Because, as described above, the polarity of carriers in the channel is identical to the polarity of carriers in the source and drain, the polarity of the accumulated charge 120 is also opposite to the polarity of carriers in the source and drain. For example, under the operating conditions described above, holes (having "P" polarity) accumulate in off-state NMOSFETs, and electrons (having "N" polarity) accumulate in off-state PMOSFETs. Therefore, a MOSFET device is defined herein as operating within the "accumulated charge regime" when the MOSFET is biased to operate in an off-state, and when carriers having opposite polarity to the channel carriers are present in the channel region. Stated in other terms, a MOSFET is defined as operating within the accumulated charge regime when the MOSFET is biased to operate in an off-state, and when carriers are present in the channel region having a polarity that is opposite the polarity of the source and drain carriers.

015 For example, and referring again to FIGURE 1, the accumulated charge 120 comprises hole carriers having P or "+" polarity. In contrast, the carriers in the source, drain, and channel (*i.e.*, when the FET is in the on-state) comprise electron carriers having N or "-" polarity. The SOI NMOSFET 100 is therefore shown in FIGURE 1 as operating in the accumulated charge regime. It is biased to operate in an off-state, and an accumulated charge 120 is present in the channel region. The accumulated charge 120 is opposite in polarity (P) to the polarity of the channel, source and drain carriers (N).

016 In another example, wherein the SOI NMOSFET 100 comprises a depletion mode device, V_{th} is negative by definition. According to this example, the body 114 comprises an N-region (as contrasted with the P-region shown in FIGURE 1). The source and drain comprise N⁺ regions similar to those shown in the enhancement mode MOSFET 100 of FIGURE 1. For V_s and V_d both at zero volts, when a gate bias V_g is applied that is sufficiently negative relative to V_{th} (for example, a V_g that is more negative than approximately -1 V relative to V_{th}), the depletion mode NMOSFET is biased into an off-state. If biased in the off-state for a sufficiently long period of time, holes may accumulate under the gate oxide and thereby comprise the accumulated charge 120 shown in FIGURE 1.

017 In other examples, V_s and V_d may comprise nonzero bias voltages. In some embodiments, V_g must be sufficiently negative to both V_s and V_d (in order for V_g to be sufficiently

negative to V_{th} , for example) in order to bias the NMOSFET in the off-state. Those skilled in the MOSFET device design arts shall recognize that a wide variety of bias voltages may be used to practice the present teachings. As described below in more detail, the present disclosed method and apparatus contemplates use in any SOI MOSFET device biased to operate in the accumulated charge regime.

018 SOI and SOS MOSFETs are often used in applications in which operation within the accumulated charge regime adversely affects MOSFET performance. As described below in more detail, unless the accumulated charge is removed or otherwise controlled, it detrimentally affects performance of SOI MOSFETs under certain operating conditions. One exemplary application, described below in more detail with reference to the circuits shown in FIGURES 2B and 5A, is the use of SOI MOSFETs in the implementation of radio frequency (RF) switching circuits. As described below with reference to FIGURES 2B and 5A in more detail, the inventors have discovered that unless the accumulated charge is removed or otherwise controlled, under some operating conditions, the accumulated charge adversely affects the linearity of the SOI MOSFET and thereby increases harmonic distortion and intermodulation distortion (IMD) caused by the MOSFET when used in the implementation of certain circuits. In addition, as described below in more detail, the inventors have discovered that removal or control of the accumulated charge improves the drain-to-source breakdown voltage (*i.e.*, the "BVDSS") characteristics of the SOI MOSFETs.

019 Therefore, it is desirable to provide techniques for adapting and improving SOI (and SOS) MOSFETs, and circuits implemented with the improved SOI MOSFETs, in order to remove or otherwise control the accumulated charge, and thereby significantly improve SOI MOSFET performance. It is desirable to provide methods and apparatus for use in improving the linearity characteristics in SOI MOSFETs. The improved MOSFETs should have improved linearity, harmonic distortion, intermodulation distortion, and BVDSS characteristics as compared with prior art MOSFETs, and thereby improve the performance of circuits implemented with the improved MOSFETs. The present teachings provide such novel methods and apparatus.

SUMMARY

020 Apparatuses and methods are provided to control accumulated charge in SOI MOSFETs, thereby improving nonlinear responses and harmonic and intermodulation distortion effects in the operation of the SOI MOSFETs.

5 **021** In one embodiment, a circuit having at least one SOI MOSFET is configured to operate in an accumulated charge regime. An accumulated charge sink (ACS), operatively coupled to the body of the SOI MOSFET, receives accumulated charge generated in the body, thereby reducing the nonlinearity of the net source-drain capacitance of the SOI MOSFET.

10 **022** In one embodiment, the ACS comprises a high impedance connection to the MOSFET body, with an exemplary impedance greater than 10^6 ohm.

BRIEF DESCRIPTION OF THE DRAWINGS

023 FIGURE 1 is a cross-sectional view of an exemplary prior art SOI NMOSFET.

024 FIGURE 2A is a simplified schematic of an electrical model showing the off-
5 state impedance characteristics of the exemplary prior art SOI NMOSFET of FIGURE 1.

025 FIGURE 2B is a schematic of an exemplary simplified RF switching circuit implemented using prior art SOI MOSFETs such as the prior art SOI NMOSFET of FIGURE 1.

026 FIGURES 3A and 3B are simplified schematic diagrams of a top view of an improved SOI NMOSFET adapted to control accumulated charge in accordance with the present
10 teachings.

027 FIGURE 3C is a cross-sectional perspective schematic of an improved SOI NMOSFET adapted to control accumulated charge showing gate, source, drain and accumulated charge sink (ACS) terminals.

028 FIGURE 3D is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge having an accumulated charge sink (ACS) electrically coupled
15 to a P+ region.

029 FIGURE 3E is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and showing a cross-sectional view line A-A' taken along approximately a center of the SOI NMOSFET.

030 FIGURE 3F is a cross-sectional view of the improved SOI NMOSFET of FIGURE 3E taken along the A-A' view line of FIGURE 3E.
20

031 FIGURE 3G is a cross-sectional view of the improved SOI NMOSFET of FIGURES 3A-3B.

032 FIGURE 3H is a simplified top view schematic of an SOI NMOSFET illustrating a region of increased threshold voltage that can occur in prior art MOSFETs and in some
25 embodiments of the improved SOI MOSFET due to manufacturing processes.

033 FIGURE 3I is a plot of inversion channel charge as a function of applied gate voltage when a region of increased threshold voltage is present in an SOI MOSFET.

034 FIGURE 3J is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and configured in a "T-gate" configuration.

035 FIGURE 3K is a simplified top view schematic of an improved SOI NMOSFET adapted to control accumulated charge and configured in an "H-gate" configuration.

5 036 FIGURE 4A is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge embodied as a four terminal device.

037 FIGURE 4B is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal.

10 038 FIGURE 4C is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal via a diode.

15 039 FIGURE 4D is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a control circuit.

040 FIGURE 4E is a simplified schematic of an exemplary RF switch circuit implemented using the four terminal ACC NMOSFET of FIGURE 4D, wherein the ACS terminal is driven by an external bias source.

20 041 FIGURE 4F is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a clamping circuit.

042 FIGURE 4G is a simplified schematic of an improved SOI NMOSFET adapted to control accumulated charge, embodied as a four terminal device, wherein an accumulated charge sink (ACS) terminal is coupled to a gate terminal via a diode in parallel with a capacitor.

25 043 FIGURE 4H shows plots of the off-state capacitance (C_{off}) versus applied drain-to-source voltages for SOI MOSFETs operated in the accumulated charge regime, wherein a first plot shows the off-state capacitance C_{off} of a prior art SOI MOSFET, and wherein a second plot shows the off-state capacitance C_{off} of the improved ACC SOI MOSFET made in accordance with the present teachings.

044 FIGURE 5A is a schematic of an exemplary prior art single pole, single throw (SPST) radio frequency (RF) switch circuit.

045 FIGURE 5B is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the gate of a shunting SOI NMOSFET is coupled to an accumulated charge sink (ACS) terminal.

046 FIGURE 5C is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the gate of a shunting SOI NMOSFET is coupled to an accumulated charge sink (ACS) terminal via a diode.

047 FIGURE 5D is a schematic of an RF switch circuit adapted for improved performance using accumulated charge control, wherein the accumulated charge sink (ACS) terminal is coupled to a control circuit.

048 FIGURE 6 is a schematic of an RF switch circuit including stacked MOSFETs, adapted for improved performance using accumulated charge control, wherein the accumulated charge sink (ACS) terminals of the shunting stacked MOSFETs are coupled to a control signal.

049 FIGURE 7 shows a flowchart of an exemplary method of improving the linearity of an SOI MOSFET device using an accumulated charge sink in accordance with the present disclosure.

050 FIGURE 8 shows a simplified circuit schematic of an exemplary embodiment of an RF switch circuit made in accordance with the present disclosure, wherein the RF switch circuit includes drain-to-source resistors between the drain and source of the ACC MOSFETs.

051 FIGURE 9 shows a simplified schematic of an exemplary single-pole double-throw (SPDT) RF switch circuit made in accordance with the present disclosure, wherein drain-to-source resistors are shown across the switching ACC SOI MOSFETs.

052 FIGURES 10-19 show exemplary performance results obtainable using the disclosed methods and apparatus for an exemplary single pole, six throw (SP6T) RF switch.

053 Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

054 As noted above, those skilled in the electronic device design arts shall appreciate that the teachings herein apply equally to NMOSFETs and PMOSFETs. For simplicity, the embodiments and examples presented herein for illustrative purposes include only NMOSFETs, unless otherwise noted. By making well known changes to dopants, charge carriers, polarity of bias voltages, *etc.*, persons skilled in the arts of electronic devices will easily understand how these embodiments and examples may be adapted for use with PMOSFETs.

Non-linearity and Harmonic Distortion Effects of Accumulated Charge in an SOI NMOSFET

055 As described above in the background, no matter what mode of operation the MOSFET employs (*i.e.*, enhancement mode or depletion mode), under some circumstances, when a MOSFET is operated in an off-state with a nonzero gate bias voltage applied with respect to the source and drain, an accumulated charge may occur under the gate. According to the present teachings, as described above when the MOSFET is in an off-state, and when carriers are present in the channel region having a polarity that is opposite the polarity of the source and drain carriers, the MOSFET is defined herein as operating in the accumulated charge regime.

056 According to the present teachings, the inventors have observed that, when used in certain circuit implementations, MOSFETs operating in the accumulated charge regime exhibit undesirable non-linear characteristics that adversely impact circuit performance. For example, as described below in more detail with reference to FIGURE 2A, the accumulated charge 120 (FIGURE 1) adversely affects the linearity of off-state SOI MOSFETs, and more specifically, it adversely affects the linearity of contributing capacitances to the drain-to-source capacitance (C_{ds}). For an SOI MOSFET operating in an off-state, C_{ds} is referred to as C_{off} . The contributing capacitances to C_{off} are described below in reference to FIGURE 2A for bias conditions wherein the gate bias V_g is provided by a circuit having an impedance that is large compared to the impedances of the contributing capacitances. As described below with reference to FIGURES 2B and 5A, this, in turn, adversely affects harmonic distortion, intermodulation distortion, and other performance characteristics of circuits implemented with the SOI MOSFETs. These novel observations, not taught or suggested by the prior art, may be understood with reference to the electrical model shown in FIGURE 2A.

057 FIGURE 2A is a simplified schematic of an electrical model 200 showing the off-state impedance (or conversely, conductance) characteristics of the exemplary prior art SOI NMOSFET 100 of FIGURE 1. More specifically, the model 200 shows the impedance characteristics from the source 112 to the drain 116 when the NMOSFET 100 is operated in the off-

state. Because the drain-to-source off-state impedance characteristic of the NMOSFET 100 is primarily capacitive in nature, it is referred to herein as the drain-to-source off-state capacitance (C_{off}). For the exemplary description herein, the gate 108 is understood to be biased at a voltage V_g by a circuit (not shown) that has an impedance that is large compared to the impedances of the contributing capacitances described in reference to FIGURE 2A. Persons skilled in the electronic arts will understand how this exemplary description may be modified for the case wherein the impedance of the circuit providing the V_g bias is not large compared to the impedances of the contributing capacitances.

058 As shown in FIGURE 2A, the junction between the source 112 and the body 114 (*i.e.*, a source-body junction 218) of the off-state NMOSFET 100 can be represented by a junction diode 208 and a junction capacitor 214, configured as shown. Similarly, the junction between the drain 116 and the body 114 (*i.e.*, the drain-body junction 220) of the off-state NMOSFET 100 can be represented by a junction diode 210 and a junction capacitor 216, configured as shown. The body 114 is represented simply as an impedance 212 that is present between the source-body junction 218 and the drain-body junction 220.

059 A capacitor 206 represents the capacitance between the gate 108 and the body 114. A capacitor 202 represents the capacitance between the source 112 and the gate 108, and another capacitor 204 represents the capacitance between the drain 116 and the gate 108. A substrate capacitance due to the electrical coupling between the source 112 and the drain 116 (through the insulating substrate 118 shown in FIGURE 1) is taken to be negligibly small in the exemplary description set forth below, and therefore is not shown in the electrical model 200 of FIGURE 2A.

060 As described above, when the NMOSFET 100 is in the off-state, and when the accumulated charge 120 (FIGURE 1) is not present in the body 114 (*i.e.*, the NMOSFET 100 is not operating within the accumulated charge regime), the body 114 is depleted of charge carriers. In this case the body impedance 212 is analogous to the impedance of an insulator, and the electrical conductance through the body 114 is very small (*i.e.*, the NMOSFET 100 is in the off-state). Consequently, the principal contributions to the drain-to-source off-state capacitance C_{off} are provided by the capacitors 202 and 204. The capacitors 202 and 204 are only slightly voltage dependent, and therefore do not significantly contribute to a nonlinear response that adversely affects harmonic generation and intermodulation distortion characteristics.

061 However, when the NMOSFET 100 operates within the accumulated charge regime, and the accumulated charge 120 is therefore present in the body 114, mobile holes comprising the accumulated charge produce p-type conductivity between the source-body junction

218 and the drain-body junction 220. In effect, the accumulated charge 120 produces an impedance between the source-body junction 218 and the drain-body junction 220 that is significantly less than the impedance between the junctions in the absence of the accumulated charge. If a V_{ds} voltage is applied between the drain 116 and the source 112, the mobile holes redistribute according to the electrical potentials that result within the body 114. DC and low-frequency current flow through the SOI NMOSFET 100 is prevented by the diode properties of the source-body junction 218 and the drain-body junction 220, as represented by the junction diodes 208 and 210, respectively. That is, because the junction diodes 208 and 210 are anti-series (*i.e.*, "back-to-back") in this case, no DC or low-frequency currents flow through the SOI NMOSFET 100. However, high-frequency currents may flow through the SOI NMOSFET 100 via the capacitances of the source-body junction 218 and the drain-body junction 220, as represented by the junction capacitors 214 and 216, respectively.

062 The junction capacitors 214 and 216 are voltage dependent because they are associated with junctions between n-type and p-type regions. This voltage dependence results from the voltage dependence of the width of the depletion region of the junction between the n-type and p-type regions. As a bias voltage is applied to the NMOSFET, the width of the depletion region of the junction between the n-type and p-type regions is varied. Because the capacitance of the junction depends on the width of the junction depletion region, the capacitance also varies as a function of the bias applied across the junction (*i.e.*, the capacitance is also voltage dependent).

063 Further, the capacitors 202 and 204 may also have a voltage dependence caused by the presence of the accumulated charge 120. Although the complex reasons for this voltage dependence are not described in detail herein, persons skilled in the arts of electronic devices shall understand that electric field regions (*e.g.*, electric field regions 122 and 124 described above with reference to FIGURE 1) may be affected by the response of the accumulated charge and its response to an applied V_{ds} , thereby causing a voltage dependence of capacitors 202 and 204. An additional nonlinear effect may occur due to a direct capacitance (not shown) between the source 112 and the drain 116. Although this direct capacitance would usually be expected to be negligible for most SOI MOSFETs, it may contribute for SOI MOSFETs having very short spacing between the source and drain. The contribution of this direct capacitance to C_{off} is also voltage-dependent in the presence of an accumulated charge, for reasons that are analogous to the voltage dependencies of the capacitors 202 and 204 as described above.

064 The voltage dependencies of the junction capacitors 214 and 216, the gate-to-source and gate-to-drain capacitors 202, 204, respectively, and the direct capacitance (not shown), cause nonlinear behavior in off-state capacitance C_{off} of the MOSFET when AC voltages are applied to the NMOSFET 100, thereby producing undesirable generation of harmonic distortions and

intermodulation distortion (IMD). The relative contributions of these effects are complex, and depend on fabrication processes, biases, signal amplitudes, and other variables. However, those skilled in the electronic device design arts shall understand from the teachings herein that reducing, removing, or otherwise controlling the accumulated charge provides an overall improvement in the nonlinear behavior of C_{off} . In addition, because the body impedance 212 is significantly decreased in the presence of the accumulated charge 120, the magnitude of C_{off} may be increased when the FET operates in the accumulated charge regime. Reducing, removing, or otherwise controlling the accumulated charge also mitigates this effect.

065 In addition, the accumulated charge does not accumulate in the body in an instant as soon as the FET transitions from an on-state (conducting state) to an off-state (non-conducting state). Rather, when the FET transitions from the on-state to the off-state, it begins to accumulate charge in the body of the MOSFET, and the amount of accumulated charge increases over time. The accumulation of the accumulated charge therefore has an associated time constant (*i.e.*, it does not instantly reach a steady-state level of accumulated charge). The accumulated charge accumulates slowly in the FET body. The depleted FET has a C_{off} associated with it which is increased with an increasing amount of accumulated charge. In terms of FET performance, as the C_{off} increases with an increasing amount of accumulated charge in the FET body, drift occurs in the FET insertion loss (*i.e.*, the FET becomes more "lossy"), isolation (the FET becomes less isolating) and insertion phase (delay in the FET is increased). Reducing, removing, or otherwise controlling the accumulated charge also mitigates these undesirable drift effects.

066 The inventors have observed that the nonlinear behavior of the MOSFET off-state capacitance C_{off} adversely affects the performance of certain circuits implemented with the prior art SOI MOSFETs. For example, when an RF switch is implemented using the prior art SOI MOSFETs, such as the prior art SOI NMOSFET 100 of FIGURE 1, the above-described non-linear off-state characteristics of the prior art MOSFETs adversely affect the linearity of the switch. As described below in more detail, RF switch linearity is an important design parameter in many applications. Improved switch linearity leads to improved suppression of harmonic and intermodulation (IM) distortion of signals processed by the switch. These improved switch characteristics can be critically important in some applications such as use in cellular communication devices.

067 For example, the well known GSM cellular communication system standard imposes stringent linearity, harmonic and intermodulation suppression, and power consumption requirements on front-end components used to implement GSM cell phones. One exemplary GSM standard requires that all harmonics of a fundamental signal be suppressed to below -30 dBm at

frequencies up to 12.75 GHz. If harmonics are not suppressed below these levels, reliable cell phone operation can be significantly adversely impacted (e.g., increased dropped calls or other communication problems may result due to harmonic and intermodulation distortion of the transmit and receive signals). Because the RF switching function is generally implemented in the cell phone front-end components, improvements in the RF switch linearity, harmonic and intermodulation suppression, and power consumption performance characteristics is highly desirable. A description of how the non-linear behavior of the off-state capacitance C_{off} of the prior art MOSFETs adversely affects these RF switch characteristics is now described with reference to FIGURE 2B.

Harmonic Distortion Effects on RF Switch Circuits Implemented using Prior Art SOI MOSFETs

068 FIGURE 2B illustrates an exemplary simplified RF switch circuit 250 implemented using prior art MOSFETs such as the prior art SOI NMOSFET 100 described above with reference to FIGURE 1. A detailed description of the operation and implementation of RF switch circuits is provided in commonly assigned U.S. Patent No. 6,804,502 which is hereby incorporated herein by reference in its entirety for its teachings on RF switch circuits. As shown in FIGURE 2B, the prior art RF switch 250 includes a single "pass" or "switching" MOSFET 254 operatively coupled to five shunting MOSFETs 260a-260e.

069 The MOSFET 254 acts as a pass or switching transistor and is configured, when enabled, to selectively couple an RF input signal (applied to its drain, for example) to an RF antenna 258 via a transmission path 256. The shunting MOSFETs, 260a-260e, when enabled, act to alternatively shunt the RF input signal to ground. As is well known, the switching MOSFET 254 is selectively controlled by a first switch control signal (not shown) coupled to its gate, and the shunting MOSFETs, 260a-260e are similarly controlled by a second switch control signal (not shown) coupled to their gates. The switching MOSFET 254 is thereby enabled when the shunting MOSFETs 260a-260e are disabled, and *vice versa*. As shown in the exemplary embodiment of the RF switch 250 of FIGURE 2B, the switching MOSFET 254 is enabled by applying a gate bias voltage of +2.5V (via the first switch control signal). The shunting MOSFETs 260a-260e are disabled by applying a gate bias voltage of -2.5V (via the second switch control signal).

070 When the switch 250 is configured in this state, the RF signal 252 propagates through the switching MOSFET 254, through the transmission path 256, and to the antenna 258. As described above with reference to FIGURE 2A, when the shunting MOSFETs 260a-260e comprise prior art SOI (or SOS) MOSFETs, such as the SOI NMOSFET 100 (FIGURE 1), an accumulated charge can occur in the SOI MOSFET bodies (i.e., when the SOI MOSFETs operate in the accumulated charge regime as described above). The accumulated charge can produce nonlinear

behavior in the off-state capacitance C_{off} of the SOI MOSFETs when AC voltages are applied to the MOSFETs.

071 More specifically, when the accumulated charge is present in the channel regions of the off-state SOI MOSFETs 260a-260e it responds to variations in the RF signals applied to their respective drains. As the time varying RF signal propagates along the transmission path 256, the RF signal applies time varying source-to-drain bias voltages to the SOI MOSFETs 260a-260e. The time varying source-to-drain bias voltages creates movement of the accumulated charge within the channel regions of the SOI MOSFETs 260-260e. The movement of the accumulated charge within the channel regions of the SOI MOSFETs causes variations in the drain-to-source off-state capacitance of the SOI MOSFETs 260a-260e. More specifically, the movement of the accumulated charge within the channel regions causes a voltage dependence of the drain-to-source off-state capacitance as described above with reference to FIGURE 2A. The voltage dependent variations in the off-state capacitance of the SOI MOSFETs 260a-260e is the dominant cause of harmonic distortion and IMD of the RF signal as it propagates through the RF switch 250.

072 As noted above, harmonic distortion and IMD of the RF signal is a major disadvantage of the prior art RF switch circuits implemented using the prior art SOI MOSFET devices. For many applications, harmonics and IMD of the RF signal must be suppressed to levels that heretofore have been difficult or impossible to achieve using prior art SOI MOSFET devices. In GSM devices, for example, at a maximum operating power of +35 dBm, prior art switches typically have only a 6 dB margin to the GSM third order harmonics suppression requirement of less than -30 dBm. Very low even order harmonic distortion is also desirable in GSM systems as the second order harmonic of the GSM transmit band also resides in the DCS receive band. Suppression of odd order (e.g., third order) harmonics of the RF signal, however, is desirable and improvements in that regard are needed.

073 In addition, as is well known, presence of an accumulated charge in the bodies of floating body (e.g., SOI) MOSFETs can also adversely affect the drain-to-source breakdown voltage (BVDSS) performance characteristics of the floating body MOSFETs. As is well known, floating-body FETs demonstrate drain-to-source breakdown voltage problems, also known as BVDSS, wherein the drain-to-source "punch-through" voltage is reduced by a parasitic bipolar action. The parasitic bipolar action is caused when holes are generated in the channel and the holes have nowhere to dissipate (i.e., because the body is floating, the holes have no means for escaping the body). As a consequence, the potential of the MOSFET body is increased, which effectively reduces the threshold voltage. In turn, this condition causes the MOSFET device to experience increased leakage, thereby

generating more holes in the body, and thereby exacerbating the BVDSS problem (as a result of this positive feedback condition).

074 The present disclosed method and apparatus for improving linearity of SOI (and SOS) MOSFET devices overcomes the above-described disadvantages of the prior art. Once the accumulated charge is recognized as a major source of harmonic distortion, IMD and compression/saturation in off-state SOI MOSFET devices, and in circuits (such as RF circuits) implemented with these devices, it becomes clear that reduction, removal, and/or control of the accumulated charge improves the harmonic suppression characteristics of these devices. In addition, reduction, removal, and/or control of the accumulated charge also improve the BVDSS performance characteristics by preventing the parasitic bipolar action from occurring. Improvements in BVDSS lead to consequent improvements in device linearity. Several exemplary structures and techniques for controlling the accumulated charge in SOI MOSFETs are described in detail in the next section.

Method and Apparatus for Improving the Linearity of MOSFETs Using Accumulated Charge Sinks (ACS) – Overview

075 As described below in more detail, the present disclosure describes methods and apparatuses for improving semiconductor device linearity (e.g., reducing adverse harmonic distortion and IMD effects) in SOI MOSFETs. In one exemplary embodiment, the method and apparatus improves the linearity and controls the harmonic distortion and IMD effects of the MOSFET devices by reducing the accumulated charge in the bodies of the MOSFET devices. In one embodiment, the present method and apparatus reduces or otherwise controls the accumulated charge in the MOSFET bodies using an accumulated charge sink (ACS) that is operatively coupled to the MOSFET body. In one embodiment, the present method and apparatus entirely removes all of the accumulated charge from the bodies of the MOSFET devices. In one described embodiment, the MOSFET is biased to operate in an accumulated charge regime, and the ACS is used to entirely remove, reduce, or otherwise control, the accumulated charge and thereby reduce harmonic distortions and IMD that would otherwise result. Linearity is also improved in some embodiments by removing or otherwise controlling the accumulated charge thereby improving the floating body MOSFET BVDSS characteristics.

076 As noted in the background section above, persons skilled in the electronic device design and manufacture arts shall appreciate that the teachings herein apply equally to MOSFETs fabricated on Semiconductor-On-Insulator ("SOI") and Semiconductor-On-Sapphire ("SOS") substrates. The present teachings can be used in the implementation of MOSFETs using any convenient semiconductor-on-insulator technology. For example, the inventive MOSFETs described herein can be implemented using compound semiconductors fabricated on insulating substrates, such

as GaAs MOSFETs. As noted above, the present method and apparatus may also be applied to silicon-germanium (SiGe) SOI MOSFETs. For simplicity, the embodiments and examples presented herein for illustrative purposes include only NMOSFETs, unless otherwise noted. By making well known changes to dopants, charge carriers, polarity of bias voltages, *etc.*, persons skilled in the electronic device design arts will easily understand how these embodiments and examples may be adapted for use with PMOSFETs.

077 As noted above, the present disclosure is particularly applicable to FETs and associated applications benefiting from a fully depleted channel when the FET is operated in the off-state, wherein an accumulated charge may result. The disclosed method and apparatus for use in improving the linearity of MOSFETs also finds applicability for use with partially depleted channels. As known to those skilled in the art, the doping and dimensions of the body vary widely. In an exemplary embodiment, the body comprises silicon having a thickness of approximately 100 angstroms to approximately 2,000 angstroms. In a further exemplary embodiment, dopant concentration within the FET bodies ranges from no more than that associated with intrinsic silicon to approximately 1×10^{18} active dopant atoms per cm^3 , resulting in fully-depleted transistor operation. In a further exemplary embodiment, dopant concentration within the FET bodies ranges from 1×10^{18} to 1×10^{19} active dopant atoms per cm^3 and/or the silicon comprising the body ranges from a thickness of 2000 angstroms to many micrometers, resulting in partially-depleted transistor operation. As will be appreciated by those skilled in the electronic design and manufacturing arts, the present disclosed method and apparatus for use in improving linearity of MOSFETs can be used in MOSFETs implemented in a wide variety of dopant concentrations and body dimensions. The present disclosed method and apparatus therefore is not limited for use in MOSFETs implemented using the exemplary dopant concentrations and body dimensions as set forth above.

078 According to one aspect of the present disclosure, accumulated charge within a FET body is reduced using control methodologies and associated circuitry. In one embodiment all of the accumulated charge is removed from the FET body. In other embodiments, the accumulated charge is reduced or otherwise controlled. In one embodiment, holes are removed from the FET body, whereas in another embodiment, electrons are removed from the FET body, as described below in more detail. By removing holes (or electrons) from the FET body using the novel and nonobvious teachings of the present disclosure, voltage induced variations in the parasitic capacitances of the off-state FETs are reduced or eliminated, thereby reducing or eliminating nonlinear behavior of the off-state FETs. In addition, as described above with reference to FIGURE 2A, because the body impedance is greatly increased when the accumulated charge is reduced or controlled, there is a beneficial overall reduction in the magnitude of the FET off-state capacitances. Also, as described

above, removing or otherwise controlling the accumulated charge in floating body MOSFETs improves the BVDSS characteristics of the FET and thereby improves the linearity of the floating body MOSFET.

079 Accumulated charge control not only facilitates a beneficial overall reduction in
5 the FET off-state capacitance C_{off} (as described above with reference to FIGURE 2A and below with
reference to FIGURE 4H), it also facilitates a reduction in C_{off} variations that can occur over time in
the presence of a time varying V_{ds} bias voltage. Thus, a reduction of undesirable harmonics
generation and intermodulation distortion in RF switch circuits is obtained using SOI MOSFETs
made in accordance with the present disclosure. Improved SOI MOSFET power handling, linearity,
10 and performance are achieved by devices made in accordance with the present teachings. While the
methods and apparatuses of the present disclosure are capable of fully removing accumulated charge
from the FET bodies, those skilled in the electronic device design arts shall appreciate that any
reduction of accumulated charge is beneficial.

080 Reductions in harmonics and intermodulation distortion are generally beneficial
15 in any semiconductor system, either bulk semiconductor or semiconductor-on-insulator (SOI)
systems. SOI systems include any semiconductor architecture employing semiconductor-containing
regions positioned above an underlying insulating substrate. While any suitable insulating substrate
can be used in a SOI system, exemplary insulating substrates include silicon dioxide (*e.g.*, a buried
oxide layer supported by a silicon substrate, such as that known as Separation by Implantation of
20 Oxygen (SIMOX)), bonded wafer (thick oxide), glass, and sapphire. As noted above, in addition to
the commonly used silicon-based systems, some embodiments of the present disclosure may be
implemented using silicon-germanium (SiGe), wherein the SiGe is used equivalently in place of Si.

081 A wide variety of ACS implementations and structures can be used to practice
the present disclosed method and apparatus. In accordance with one embodiment of the present
25 method and apparatus, an ACS is used to remove or otherwise control accumulated charge
(referenced as 120 in FIGURE 1 described above) from the MOSFETs when the MOSFETs are
configured to operate in the accumulated charge regime. By adapting the SOI (or SOS) MOSFETs in
accordance with the present teachings, improved Accumulated Charge Control (ACC) MOSFETs are
realized. The ACC MOSFETs are useful in improving performance of many circuits, including RF
30 switching circuits. Various characteristics and possible configurations of the exemplary ACC
MOSFETs are described in detail below with reference to FIGURES 3A-3K. This section also
describes how the exemplary ACS implementations of the present disclosure differ from the body
contacts of the prior art.

082 The ACC MOSFET is shown schematically embodied as a four-terminal device in FIGURE 4A. FIGURES 4B-4G show various exemplary simple circuit configurations that can be used in removing the accumulated charge from the ACC MOSFET when it operates in an accumulated charge regime. The operation of the simplified circuit configurations is described in more detail below with reference to FIGURES 4A-4G. The improvement in off-state capacitance C_{off} of the ACC MOSFETs, as compared with the off-state capacitance of the prior art SOI MOSFETs, is described below with reference to FIGURE 4H.

083 The operation of various exemplary RF switch circuits implemented using the ACC MOSFETs of the present disclosure is described below with reference to the circuit schematics of FIGURES 5B-5D. Further, an exemplary RF switch circuit using stacked ACC MOSFETs (for increased power handling) of the present disclosure is described below with reference to FIGURE 6. An exemplary method of improving the linearity of an SOI MOSFET using an accumulated charge sink (ACS) is described with reference to FIGURE 7. Finally, exemplary fabrication methods that may be used to manufacture the ACC MOSFET are described. The various exemplary ACS implementations and structures that can be used to practice the disclosed method and apparatus are now described with reference to FIGURES 3A-3K.

Controlling Accumulated Charge Using an Accumulated Charge Sink (ACS)

084 FIGURES 3A and 3B are simplified schematic diagrams of a top view of an Accumulated Charge Control (ACC) SOI NMOSFET 300 adapted to control accumulated charge 120 (FIGURE 1) in accordance with the present disclosure. In the exemplary embodiment, a gate contact 301 is coupled to a first end of a gate 302. A gate oxide (not shown in FIGURE 3A but shown in FIGURE 1) and a body 312 (shown in FIGURE 3B) are positioned under the gate 302. In the exemplary NMOSFET 300 shown, a source 304 and a drain 306 comprise N⁺ regions. In the exemplary embodiment, the ACC NMOSFET 300 includes an accumulated charge sink (ACS) 308 comprising a P- region. The ACS 308 is coupled to and is in electrical communication with the body 312 which also comprises a P- region. An electrical contact region 310 provides electrical connection to the ACS 308. In some embodiments, the electrical contact region 310 comprises a P⁺ region. As shown in FIGURE 3A, the electrical contact region 310 is coupled to and is in electrical communication with the ACS 308.

085 Those skilled in the arts of electronic devices shall understand that the electrical contact region 310 may be used to facilitate electrical coupling to the ACS 308 because in some embodiments it may be difficult to make a direct contact to a lightly doped region. In addition, in some embodiments the ACS 308 and the electrical contact region 310 may be coextensive. In

another embodiment, the electrical contact region 310 comprises an N+ region. In this embodiment, the electrical contact region 310 functions as a diode connection to the ACS 308, which prevents positive current flow into the ACS 308 (and also prevents positive current flow into the body 312) under particular bias conditions, as described below in more detail.

5 **086** FIGURE 3B is an alternative top view of the ACC SOI NMOSFET 300 of FIGURE 3A, illustrating the ACC NMOSFET 300 without its gate contact 301, gate 302, and gate oxide being visible. This view allows the body 312 to be visible. FIGURE 3B shows the coupling of the ACS 308 to one end of the body 312. In one embodiment, the body 312 and the ACS 308 comprise a combined P- region that may be produced by a single ion-implantation step. In another
10 embodiment, the body 312 and ACS 308 comprise separate P- regions that are coupled together.

087 As is well known to those skilled in the electronic device design arts, in other embodiments, the ACC NMOSFET 300 of FIGURES 3A and 3B can be implemented as an ACC PMOSFET simply by reversing the dopant materials used to implement the various FET component regions (*i.e.*, replace p-type dopant material with n-type dopant material, and *vice versa*). More
15 specifically, in an ACC PMOSFET, the source and drain comprise P+ regions, and the body comprises an N- region. In this embodiment, the ACS 308 also comprises an N- region. In some embodiments of the ACC PMOSFET, the electrical contact region 310 may comprise an N+ region. In other embodiments of the ACC PMOSFETs, the region 310 comprises a P+ region, which functions as a diode connection to the ACS 308 and thereby prevents current flow into the ACS 308
20 under particular bias conditions.

Prior Art Body Contacts Distinguished from the Disclosed ACS

088 According to the present disclosure, the ACS 308 used to implement ACC SOI MOSFETs includes novel features in structure, function, operation and design that distinguish it from the so-called "body contacts" (also sometimes referred to as "body ties", usually when the "body
25 contact" is directly connected to the source) that are well known in the prior art.

089 Exemplary references relating to body contacts used in prior art SOI MOSFETs include the following: (1) F. Hameau and O. Rozeau, Radio-Frequency Circuits Integration Using CMOS SOI 0.25 μ m Technology," 2002 RF IC Design Workshop Europe, 19 - 22 March 2002, Grenoble, France; (2) J. R. Cricci et al., "Silicon on Sapphire MOS Transistor," U. S. Patent No.
30 4,053,916, October 11, 1977; (3) O. Rozeau et al., "SOI Technologies Overview for Low-Power Low-Voltage Radio-Frequency Applications," Analog Integrated Circuits and Signal Processing, 25, pp. 93-114, Boston, MA, Kluwer Academic Publishers, Nov. 2000; (4) C. Tinella et al., "A High-

Performance CMOS-SOI Antenna Switch for the 2.5–5-GHz Band, "IEEE Journal of Solid-State Circuits, Vol. 38, No. 7, July, 2003; (5) H. Lee et al., "Analysis of body bias effect with PD-SOI for analog and RF applications," Solid State Electron., Vol. 46, pp. 1169–1176, 2002; (6) J.-H. Lee, et al., "Effect of Body Structure on Analog Performance of SOI NMOSFETs," Proceedings, 1998 IEEE International SOI Conference, 5-8 Oct. 1998, pp. 61 - 62; (7) C. F. Edwards, et al., The Effect of Body Contact Series Resistance on SOI CMOS Amplifier Stages," IEEE Transactions on Electron Devices, Vol. 44, No. 12, Dec. 1997 pp. 2290 - 2294; (8) S. Maeda, et al., Substrate-bias Effect and Source-drain Breakdown Characteristics in Body-tied Short-channel SOI MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 1, Jan. 1999 pp. 151 - 158; (9) F. Assaderaghi, et al., "Dynamic Threshold-voltage MOSFET (DTMOS) for Ultra-low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp. 414 - 422; (10) G. O. Workman and J. G. Fossum, "A Comparative Analysis of the Dynamic Behavior of BTG/SOI MOSFETs and Circuits with Distributed Body Resistance," IEEE Transactions on Electron Devices, Vol. 45, No. 10, Oct. 1998 pp. 2138 - 2145; and (11) T.-S. Chao, et al., "High-voltage and High-temperature Applications of DTMOS with Reverse Schottky Barrier on Substrate Contacts," IEEE Electron Device Letters, Vol. 25, No. 2, Feb. 2004, pp.86 - 88.

090 As described herein, applications such as RF switch circuits, may use SOI MOSFETs operated with off-state bias voltages, for which accumulated charge may result. The SOI MOSFETs are defined herein as operating within the accumulated charge regime when the MOSFETs are biased in the off-state, and when carriers having opposite polarity to the channel carriers are present in the channel regions of the MOSFETs. In some embodiments, the SOI MOSFETs may operate within the accumulated charge regime when the MOSFETs are partially depleted yet still biased to operate in the off-state. Significant benefits in improving nonlinear effects on source-drain capacitance can be realized by removing or otherwise controlling the accumulated charge according to the present teachings. In contrast to the disclosed techniques, none of the cited prior art teach or suggest ACS methods and apparatuses that are uniquely useful for removing or controlling accumulated charge. Nor are they informed regarding problems caused by the accumulated charge such as nonlinear effects on the off-state source-drain capacitance C_{off} . Consequently, the prior art body contacts described in the references cited above differ greatly (in structure, function, operation and design) from the ACSs described with reference to FIGURES 3A-4D.

091 In one example, the ACS 308 operates effectively to remove or otherwise control the accumulated charge from the SOI NMOSFET 300 using a high impedance connection to and throughout the body 312. High impedance ACSs may be used because the accumulated charge 120 is

primarily generated by phenomena (*e.g.*, thermal generation) that take a relatively long period of time to produce significant accumulated charge. For example, a typical time period for producing non-negligible accumulated charge when the NMOSFET operates in the accumulated charge regime is approximately a few milliseconds or greater. Such relatively slow generation of accumulated charge corresponds to very low currents, typically less than 100 nA/mm of transistor width. Such low currents can be effectively conveyed even using very high impedance connections to the body. According to one example, the ACS 308 is implemented with a connection having a resistance of greater than 10^6 ohms. Consequently, the ACS 308 is capable of effectively removing or otherwise controlling the accumulated charge 120 even when implemented with a relatively high impedance connection, relative to the low impedance prior art body contacts.

092 In stark contrast, the prior art teachings of body contacts described in the references cited above require low impedance (high efficiency) access to the body regions of SOI MOSFETs for proper operation (*see, e.g.*, references (3), (6), and (7) above). A principal reason for this requirement is that the prior art body contacts are primarily directed to reducing the adverse effects on SOI MOSFET functions caused by much faster and more effective electron-hole pair generation processes than occur when the FET is operated in the accumulated charge regime. For example, in some prior art MOSFETs not operated in the accumulated charge regime, electron-hole pair carriers are generated as a result of impact ionization. Impact ionization produces electron-hole pairs at a much faster rate than occurs when the FET is operated in the accumulated charge regime.

093 The relative rates for electron-hole pair generation by impact ionization versus the pair generation processes causing accumulated charge can be estimated from the roll-off frequencies for the two phenomena. For example, reference (3) cited above indicates roll-off frequencies for impact ionization effects in the range of 10^5 Hz. In contrast, a roll-off frequency for the accumulated charge effects has been observed to be in the range of 10^3 Hz or less, as indicated by recovery times for odd harmonics. These observations indicate that the ACS 308 can effectively control accumulated charge using an impedance that is at least 100 times larger than required of prior art body contacts used in controlling impact ionization charge, for example. Further, because impact ionization primarily occurs when the SOI MOSFET operates in an on-state, the effects of impact ionization can be amplified by on-state transistor operation. Low impedance body contacts to and throughout a body region is even more critical in these environments in order to control the effects of impact ionization under the on-state conditions.

094 In stark contrast, the ACS 308 of the present teachings removes or otherwise controls the accumulated charge only when the ACC SOI MOSFET operates in the accumulated charge regime. By definition, the FET is in the off-state in this regime, so there is no requirement to

remove impact ionization as amplified by an on-state FET. Therefore, a high impedance ACS 308 is perfectly adequate for removing the accumulated charge under these operating conditions. The prior art requirements for low impedance body connections results in numerous problems of implementation that are overcome by the present teachings, as described below in more detail.

5 **095** In addition, the ACS 308 may be implemented with much lower source-to-drain parasitic capacitance as compared to the body contacts of the prior art. The above-described low impedance connection to the SOI MOSFET body required of the prior art body contacts necessitates proximity of the contacts to the entire body. This may require a plurality body contact "fingers" that contact the body at different locations along the body. The low impedance connection to the body
10 also necessitates proximity of the prior art body contacts to the source and drain. Because of parasitic capacitances produced by such body contacts, the cited prior art references teach away from the use of such structures for many high frequency applications such as RF. In stark contrast, the ACS 308 of the present disclosure may be positioned a selected distance away from the source 304 and the drain 306, and the ACS 308 may also be coupled to the body 312 at a first distal end of the
15 body 312 (shown in FIGURES 3A and 3B). Arranged in this manner, the ACS 308 makes minimal contact (as compared to the prior art body contacts that may contact the body at many locations along the body) with the body 312. This configuration of the ACS 308 with the MOSFET eliminates or greatly reduces the parasitic capacitances caused by a more proximate positioning of the ACS 308 relative to the source, drain, and body. Further, the ACS 308 may be implemented in SOI MOSFETs
20 operated with a depleted channel. In general, the cited prior art references teach away from the use of body contacts for this environment (*see, e.g.,* reference (3), cited above).

096 Further, because impact ionization hole currents are much larger (in the range of 5,000 nA per mm body width) than for accumulated charge generation (less than approximately 100 nA per mm body width), the prior art does not teach how to effectively implement very large body
25 widths (*i.e.,* much greater than approximately 10 μm). In contrast, the ACS 308 of the present disclosed device may be implemented in SOI MOSFETs having relatively large body widths. This provides improvements in on-state conductance and transconductance, insertion loss and fabrication costs, particularly for RF switch devices. According to the prior art teachings cited above, larger body widths adversely affect the efficient operation of body contacts because their impedances are
30 necessarily thereby increased. Although the cited prior art suggests that a plurality of fingers may be used to contact the body at different locations, the plurality of fingers adversely affects parasitic source-to-drain capacitances, as described above.

097 For these reasons, and for the reasons described below in more detail, the present disclosure provides novel MOSFET devices, circuits and methods that overcome the limitations according to the prior art teachings as cited above.

098 FIGURE 3C is a cross-sectional perspective schematic of an ACC SOI NMOSFET 300' adapted to control accumulated charge in accordance with the disclosed method and apparatus. In the example shown in FIGURE 3C, the ACC NMOSFET 300' includes four terminals that provide electrical connection to the various FET component regions. In one embodiment, the terminals provide means for connecting external integrated circuit (IC) elements (such as metal leads, not shown) to the various FET component regions. Three of the terminals shown in FIGURE 3C are typically available in prior art FET devices. For example, as shown in FIGURE 3C, the ACC NMOSFET 300' includes a gate terminal 302' that provides electrical connection to the gate 302. Similarly, the ACC NMOSFET 300' includes source and drain terminals 304', 306' that provide electrical connection to the source 304 and drain 306, respectively. As is well known in the electronic design arts, the terminals are coupled to their respective FET component regions (*i.e.*, gate, drain and source) via so-called "ohmic" (*i.e.*, low resistance) contact regions. The manufacturing and structural details associated with the coupling of the various FET terminals to the FET component regions are well known in the art, and therefore are not described in more detail here.

099 As described above with reference to FIGURES 3A and 3B, the ACC NMOSFET 300' is adapted to control accumulated charge when the NMOSFET operates in the accumulated charge regime. To this end, in the exemplary embodiment shown in FIGURE 3C, the ACC NMOSFET 300' includes a fourth terminal that provides electrical connection to the body 312, and thereby facilitates reduction (or other control) of the accumulated charge when the FET 300' operates in the accumulated charge regime. More specifically, and referring again to FIGURE 3C, the ACC NMOSFET includes a "body" terminal, or Accumulated Charge Sink (ACS) terminal 308'. The ACS terminal 308' provides an electrical connection to the ACS 308 (not shown in FIGURE 3C, but shown in FIGURES 3A and 3B) and to the body 312. Although the ACS terminal 308' is shown in FIGURE 3C as being physically coupled to the body 312, those skilled in the electronic design arts shall understand that this depiction is for illustrative purposes only. The direct coupling of the ACS terminal 308' to the body 312 shown in FIGURE 3C illustrates the electrical connectivity (*i.e.*, not the physical coupling) of the terminal 308' with the body 312. Similarly, the other terminals (*i.e.*, terminals 302', 304' and 306') are also shown in FIGURE 3C as being physically coupled to their respective FET component regions. These depictions are also for illustrative purposes only.

0100 In most embodiments, as described above with reference to FIGURES 3A-3B, and described further below with reference to FIGURES 3D-3K, the ACS terminal 308' provides the electrical connection to the body 312 via coupling to the ACS 308 via the electrical contact region 310. However, the present disclosure also contemplates embodiments where the coupling of the ACS terminal 308' is made directly to the body 312 (*i.e.*, no intermediate regions exist between the ACS terminal 308' and the body 312).

0101 In accordance with the disclosed method and apparatus, when the ACC NMOSFET 300' is biased to operate in the accumulated charge regime (*i.e.*, when the ACC NMOSFET 300' is in the off-state, and there is an accumulated charge 120 of P polarity (*i.e.*, holes) present in the channel region of the body 312), the accumulated charge is removed or otherwise controlled via the ACS terminal 308'. When accumulated charge 120 is present in the body 312, the charge 312 can be removed or otherwise controlled by applying a bias voltage (V_b (for "body") or V_{ACS} (ACS bias voltage)) to the ACS terminal 308'. In general, the ACS bias voltage V_{ACS} applied to the ACS terminal 308' may be selected to be equal to or more negative than the lesser of the source bias voltage V_s and drain bias voltage V_d . More specifically, in some embodiments, the ACS terminal 308' can be coupled to various accumulated charge sinking mechanisms that remove (or "sink") the accumulated charge when the FET operates in the accumulated charge regime. Several exemplary accumulated charge sinking mechanisms and circuit configurations are described below with reference to FIGURES 4A-5D.

0102 Similar to the prior art NMOSFET 100 described above with reference to FIGURE 1, the ACC SOI NMOSFET 300' of FIGURE 3C can be biased to operate in the accumulated charge regime by applying specific bias voltages to the various terminals 302', 304', and 306'. In one exemplary embodiment, the source and drain bias voltages (V_s and V_d , respectively) are zero (*i.e.*, the terminals 304' and 306' are connected to ground). In this example, if the gate bias voltage (V_g) applied to the gate terminal 302' is sufficiently negative with respect to the source and drain bias voltages, and with respect to V_{th} (for example, if V_{th} is approximately zero, and if V_g is more negative than approximately -1 V), the ACC NMOSFET 300' operates in the off-state. If the ACC NMOSFET 300' continues to be biased in the off-state, the accumulated charge (holes) will accumulate in the body 312. Advantageously, the accumulated charge can be removed from the body 312 via the ACS terminal 308'. In some embodiments, as described below in more detail with reference to FIGURE 4B, the ACS terminal 308' is coupled to the gate terminal 302' (thereby ensuring that the same bias voltages are applied to both the gate (V_g) and the body (shown in FIGURE 3C as " V_b " or " V_{ACS} ").

0103 However, those skilled in the electronics design arts shall appreciate that a myriad of bias voltages can be applied to the four device terminals while still employing the techniques of the present disclosed method and apparatus. As long as the ACC SOI NMOSFET 300' is biased to operate in the accumulated charge regime, the accumulated charge can be removed or otherwise controlled by applying a bias voltage V_{ACS} to the ACS terminal 308', and thereby remove the accumulated charge from the body 312.

0104 For example, in one embodiment wherein the ACC NMOSFET 300' comprises a depletion mode device, V_{th} is negative by definition. In this embodiment if both the V_s and V_d bias voltages comprise zero volts (*i.e.*, both terminals tied to circuit ground node), and a gate bias V_g applied to the gate terminal 302' is sufficiently negative to V_{th} (for example, V_g is more negative than approximately -1 V relative to V_{th}), holes may accumulate under the gate oxide 110 thereby becoming the accumulated charge 120. In this example, in order to remove the accumulated holes (*i.e.*, the accumulated charge 120) from the FET body 312, the voltage V_{ACS} applied to the ACS 308 may be selected to be equal to or more negative than the lesser of V_s and V_d .

0105 In other examples, the source and drain bias voltages, V_s and V_d , respectively, may comprise voltage other than zero volts. According to these embodiments, the gate bias voltage V_g must be sufficiently negative to both V_s and V_d (in order for V_g to be sufficiently negative to V_{th} , for example) in order to bias the NMOSFET in the off-state. As described above, if the NMOSFET is biased in the off-state for a sufficiently long time period (approximately 1-2 ms, for example) an accumulated charge will accumulate under the gate oxide. In these embodiments, as noted above, in order to remove the accumulated charge 120 from the body 312, the ACS bias voltage V_{ACS} applied to the ACS terminal 308' may be selected to be equal to or more negative than the lesser of V_s and V_d .

0106 It should be noted that, in contrast to the examples described above, the prior art body contacts are implemented largely for purposes of mitigating the adverse effects caused by impact ionization. Consequently, the prior art body contacts are typically tied to the source of the MOSFET. In order to effectively control, reduce, or entirely remove the accumulated charge in an NMOSFET, V_{ACS} should, in the exemplary embodiments, be equal to or more negative than the lesser of V_s and V_d . Those skilled in the electronic device design arts shall appreciate that different V_s , V_d , V_g and V_{ACS} bias voltages may be used when the ACC MOSFET comprises a PMOSFET device. Because the prior art body contacts are typically tied to the source, this implementation cannot be effected using the prior art body contact approach.

0107 FIGURE 3D is a simplified schematic diagram of a top view of an ACC SOI NMOSFET 300" adapted to control accumulated charge 120 (FIGURE 1) in accordance with the present disclosure. FIGURE 3D shows the ACC NMOSFET 300" without its gate contact 301, gate 302, and gate oxide being visible. The ACC NMOSFET 300" of FIGURE 3D is very similar in design to the ACC NMOSFET 300 described above with reference to FIGURES 3A and 3B. For example, similar to the ACC NMOSFET 300, the ACC NMOSFET 300" includes a source 304 and drain 306 comprising N+ regions. The ACC NMOSFET 300" also includes an accumulated charge sink (ACS) 308 comprising a P- region. As shown in FIGURE 3D, the P- region that comprises the ACS 308 abuts (*i.e.*, is directly adjacent) the body 312, which also comprises a P- region. Similar to the ACC NMOSFET 300, the ACC NMOSFET 300" includes an electrical contact region 310 that provides electrical connection to the ACS 308. As noted above, in some embodiments, the electrical contact region 310 comprises a P+ region. In another embodiment, the electrical contact region 310 may comprise an N+ region (which thereby prevents positive current flow into the body 312 as noted above). As shown in FIGURE 3D, the electrical contact region 310 is formed in the ACC NMOSFET 300" directly adjacent the ACS 308. The ACC SOI NMOSFET 300" functions to control accumulated charge similarly to the operation of the ACC NMOSFETs described above with reference to FIGURES 3A-3C.

0108 FIGURE 3E is a simplified schematic diagram of a top view of an ACC SOI NMOSFET 300'" adapted to control accumulated charge in accordance with the present disclosure. The ACC NMOSFET 300'" is very similar in design and function to the ACC NMOSFETs described above with reference to FIGURES 3A-3D. FIGURE 3E shows a dashed cross-sectional view line A-A' taken along the approximate center of the NMOSFET 300'". This cross-sectional view is used herein to describe structural and performance characteristics of some exemplary prior art MOSFETs and some embodiments of the ACC NMOSFET that may occur as a result of the fabrication processes. Details of this cross-sectional view A-A' are now described with reference to FIGURE 3F.

0109 View line A-A' slices through the following component regions of the ACC NMOSFET 300'": the P+ electrical contact region 310, the ACS 308 (shown in FIGURE 3E, but not shown in FIGURE 3F), a P+ overlap region 310', a gate oxide 110, and a poly-silicon gate 302. In some embodiments, during the fabrication process, when the region 310 is doped with p-type dopant material, proximate the P- body region, some additional P+ doping may be implanted (*i.e.*, the p-type dopant material may overlap) into the P+ overlap region 310' of the poly-silicon gate 302. In some embodiments, such overlapping is performed intentionally to ensure that all of the gate oxide 110 is completely covered by the P+ region (*i.e.*, to ensure that no gap exists on the edge of the oxide 110

between the gate 302 and the P+ region 310). This, in turn, aids in providing a minimum impedance connection between the P+ region 310 and the body 312.

0110 Although the present teachings encompass such embodiments described above, those skilled in the electronic device design and manufacturing arts shall recognize that such low-resistance connections are not required. Therefore, disadvantages associated with the embodiment shown in FIGURE 3H, as described below in more detail, can be overcome by using other embodiments described herein (for example, the embodiments 300 and 300''' described below with reference to FIGURES 3G and 3J, respectively), in which gaps are intentionally implemented between the P+ region 310 and the body 312. In one exemplary embodiment, the P+ overlap region 310' overlaps the oxide 110 by approximately 0.2 – 0.7 microns. Those skilled in the MOSFET design and manufacturing arts shall appreciate that other overlap region dimensions can be used in practicing the present disclosed method and apparatus. In some embodiments, as shown in FIGURE 3F, for example, the remaining area over the gate oxide 110 and over the P- body is doped with n-type dopant material (*i.e.*, it comprises an N+ region).

0111 Referring again to FIGURE 3F, owing to the presence of the P+ overlap region 310' over the gate oxide 110, over the body 312, and proximate an edge 340 of the poly-silicon gate 302, an increased threshold voltage region is created in the NMOSFET 300'''. More specifically, due to the P+ doping (in the P+ overlap region 310') proximate the edge 340 of the gate 302 over the channel region of the body 312, a region of increased threshold voltage is formed in that region of the MOSFET 300'''. The effects of the region of increased threshold voltage are now described in more detail with reference to FIGURES 3H and 3I.

0112 FIGURE 3I shows a plot 380 of inversion channel charge versus applied gate voltage for an ACC NMOSFET. The plot 380 shown in FIGURE 3I illustrates one effect of the above-described increased threshold voltage that can occur in prior art MOSFETs, and in some embodiments of the present ACC NMOSFETs due to certain manufacturing processes. As described in more detail below, the increased threshold voltage region, shown in FIGURE 3H and described in more detail below, also occurs in prior art MOSFET designs due to the proximity of body ties to the FET body. As described below in more detail with reference to FIGURE 3J, for example, the present disclosed method and apparatus can be used to reduce or eliminate the region of increased threshold voltage found in some prior art SOI MOSFET designs.

0113 FIGURE 3H shows one embodiment of an ACC NMOSFET without its gate contact, gate, and gate oxide being visible. The MOSFET region of increased threshold voltage described above with reference to FIGURES 3E and 3F is shown in FIGURE 3H as occurring in the

region encompassed by the ellipse 307. As will be well understood by those skilled in the electronic design and manufacturing arts, for the reasons set forth above with reference to FIGURES 3E and 3F, due to the increased threshold voltage, the region 307 of the ACC MOSFET shown in FIGURE 3H effectively "turns on" after the rest of the ACC MOSFET channel region.

5 **0114** The increased threshold voltage can be reduced by reducing the size of the region 307. Eliminating the region 307 altogether eliminates the threshold voltage increase. Because the threshold voltage increase can increase harmonic and intermodulation distortion of the "on" state MOSFET, eliminating this effect improves MOSFET performance. The increased threshold voltage also has the detrimental effect of increasing the MOSFET on-resistance (*i.e.*, the resistance presented
10 by the MOSFET when it is in the on-state (conducting state), which detrimentally impacts the MOSFET insertion loss.

0115 In one exemplary embodiment, as shown, for example in the embodiments of the ACC NMOSFET 300 described above with reference to FIGURES 3A and 3B, and as described below in more detail with reference to the cross-sectional view of the ACC MOSFET 300 of
15 FIGURE 3G, the detrimental effects associated with threshold voltage increase are mitigated or overcome by positioning the P+ region 310 a selected distance away from an edge of the poly-silicon gate 302. This approach is shown both in the top view of the ACC MOSFET 300 of FIGURE 3A, and in the cross-sectional view of the ACC MOSFET 300 shown in FIGURE 3G. As shown in the cross-sectional view of the ACC MOSFET 300 of FIGURE 3G, the P+ region 310 does not extend all
20 the way to the edge 340 of the poly-silicon gate 302. This is in stark contrast to the embodiment 300" shown in FIGURE 3F, where the P+ region 310' extends all the way to the gate edge 340. By positioning the P+ region 310 a distance away from the gate edge 340 as shown in the embodiment 300 of FIGURE 3G, no P+ region is positioned proximate the poly-silicon gate 302 (*i.e.*, there is no P+ region present in the poly-silicon gate 302).

25 **0116** This configuration of the P+ region 310 eliminates or greatly reduces the problems associated with threshold voltage increase as described above. As described above with reference to FIGURES 3A and 3B, and with reference to the comparisons to the prior art body contact references, the relatively high impedance of the ACS 308 P- region (shown in FIGURE 3A) between the P+ region 310 and the gate 302 does not adversely affect the performance of the ACC
30 NMOSFET 300. As described above, the accumulated charge can be effectively removed even using a relatively high impedance ACS connection.

0117 In another exemplary embodiment, as described below with reference to FIGURE 3J, the threshold voltage increase is removed by positioning the P+ region 310 (and the

ACS 308) a distance away from the body 312. Because the electrical connectivity between the ACS 308 and the body 312 has relatively high impedance when the small region of P+ 310 is positioned a distance away from the body 312, this approach is never taught or suggested by the body contact prior art references (which require low impedance contacts as described above). This improved embodiment is described next with reference to FIGURE 3J.

0118 FIGURE 3J is a simplified top view schematic of another embodiment of an ACC SOI NMOSFET 300''' adapted to control accumulated charge and configured in a "T-gate" configuration. FIGURE 3J shows the ACC NMOSFET 300''' without its gate contact 301, gate 302, and gate oxide being visible. The gate (not shown in FIGURE 3J) and the body 312 are configured as "supporting" members of the "T-gate" configured ACC MOSFET 300''' (*i.e.*, they comprise the "bottom" portion of the "T-shaped" FET). These "supporting" members "support" the "supported" member of the T-gate configured MOSFET 300'', which comprises the ACS 308 as shown in FIGURE 3J (*i.e.*, the ACS 308 comprises the "top" portion of the "T-shaped" FET). As shown in FIGURE 3J, the ACC NMOSFET 300''' includes a small P+ region 310 conjoined to an ACS 308. As shown in FIGURE 3J, the P+ region 310 (and thus the ACS external electrical connection) is disposed a selected distance away from the body 312. The total impedance of the electrical connection from the body 312, through the ACS 308, and to the P+ region 310 is increased by positioning the P+ region 310 a selected distance away from the body 312. However, as described above, the present ACC NMOSFET 300''' works perfectly well to remove accumulated charge even using relatively high impedance ACS connections. For the reasons described above with reference to FIGURES 3A and 3B, due to the nature of the accumulated charge when the NMOSFET 300''' operates in the accumulated charge regime, the ACC NMOSFET 300''' does not require low impedance ACS electrical connections in order to remove accumulated charge from the body 312. Rather, an ACS connection of relatively large impedance may be used in practicing the present teachings, with corresponding improvements in NMOSFET performance as described above (*e.g.*, reductions in parasitic capacitance as compared with prior art low impedance body contacts). However, in other embodiments, if desired, a low impedance ACS connection may be used to practice the disclosed method and apparatus for use in improving linearity characteristics of SOI MOSFETs.

0119 Moreover, as described above with reference to FIGURE 3H, the embodiment of FIGURE 3J improves device performance owing to the fact that the small P+ region 310 is positioned a distance away from the body 312. Because the small P+ region 310 is positioned a distance away from the body 312, the threshold voltage increase is reduced or entirely eliminated, together with the consequent adverse performance effects described above.

0120 FIGURE 3K is a simplified top view schematic of another embodiment of an ACC SOI NMOSFET 300''' adapted to control accumulated charge and configured in an "H-gate" configuration. FIGURE 3K shows the ACC NMOSFET 300''' without its gate contact 301, gate 302, and gate oxide being visible. With the exception of some structural differences described herein, the ACC NMOSFET 300''' is very similar in design and function to the ACC NMOSFETs described above with reference to FIGURES 3A-3D and 3J. As shown in FIGURE 3K, the ACC NMOSFET 300''' includes two ACSs, 308 and 308'', disposed at opposite ends of the H-gate ACC NMOSFET 300'''. P+ regions 310 and 310'' are formed to abut their respective ACSs, 308 and 308'', and provide electrical contact thereto. In accordance with the disclosed method and apparatus, as described above, when the ACC NMOSFET 300''' is biased to operate in the accumulated charge regime, the accumulated charge is removed or otherwise controlled via the two ACSs 308 and 308''.

0121 It shall be understood by those skilled in the electronic device design arts that although the illustrated embodiment shows the ACSs 308 and 308'' extending approximately the entire width of the ACC NMOSFET 300''', the ACSs 308 and 308'' may also comprise much narrower (or wider) regions, and still function perfectly well to remove or otherwise control the accumulated charge. Also, in some embodiments, it is not necessary that the impedance of the ACS 308 matches the impedance of the ACS 308''. It will further be understood by the skilled person that the ACSs 308 and 308'' may comprise different sizes and configurations (*i.e.*, rectangular, square, or any other convenient shape), and may also be positioned at various distances away from the body 312 (*i.e.*, not necessarily the same distance away from the body 312). As described above with reference to FIGURE 3J, when the ACS 308 is positioned a selected distance away from the body 312, the problems associated with threshold voltage increase are reduced or eliminated.

Four-Terminal ACC MOSFET Devices – Simple Circuit Configurations

0122 The SOI NMOSFET 300 of FIGURES 3A and 3B may be implemented as a four terminal device, as illustrated schematically in FIGURE 4A. As shown in the improved ACC SOI NMOSFET 300 of FIGURE 4A, a gate terminal 402 is electrically coupled to the gate contact 301 (*e.g.*, FIGURE 3A) and is analogous to the gate terminal 302' shown in FIGURE 3C. The gate contact 301 is electrically coupled to the gate 302 (*e.g.*, FIGURES 3A and 3C). Similarly, a source terminal 404 is electrically coupled to the source 304 (*e.g.*, FIGURES 3A-3C) and is analogous to the source terminal 304' of FIGURE 3C. Similarly, a drain terminal 406 is electrically coupled to the drain 306 (*e.g.*, FIGURES 3A-3C) and is analogous to the drain terminal 306' of FIGURE 3C. Finally, the ACC NMOSFET 300 includes an ACS terminal 408 that is electrically coupled to the ACS 308 (*e.g.*, see FIGURES 3A-3B, and FIGURES 3D, 3J-3K) via the region 310. Those skilled in the electronic design and manufacturing arts shall understand that the region 310 may be used in

some embodiments to facilitate electrical coupling to the ACS 308 because, in some embodiments, it may be difficult to make a direct contact to a lightly doped region (*i.e.*, the ACS 308). The ACS terminal 408 is analogous to the ACS terminal 308' shown in FIGURE 3C.

0123 The ACC SOI NMOSFET 300 of FIGURE 4A may be operated using various techniques and implemented in various circuits in order to control accumulated charge present in the FET when it is operating in an accumulated charge regime. For example, in one exemplary embodiment as shown in FIGURE 4B, the gate and ACS terminals, 402 and 408, respectively, are electrically coupled together. In one embodiment of the simplified circuit shown in FIGURE 4B, the source and drain bias voltages applied to the terminals 404 and 406, respectively, may be zero. If the gate bias voltage (V_g) applied to the gate terminal 402 is sufficiently negative with respect to the source and drain bias voltages applied to the terminals 404 and 406, and with respect to the threshold voltage V_{th} , (for example, if V_{th} is approximately zero, and if V_g is more negative than approximately -1 V) the ACC NMOSFET 300 operates in the accumulated charge regime. As described above with reference to FIGURE 3C, for example, when the MOSFET operates in this regime, accumulated charge (holes) may accumulate in the body of the NMOSFET 300.

0124 Advantageously, the accumulated charge can be removed via the ACS terminal 408 by connecting the ACS terminal 408 to the gate terminal 402 as shown. This configuration ensures that when the FET 300 is in the off-state, it is held in the correct bias region to effectively remove or otherwise control the accumulated charge. As shown in FIGURE 4B, connecting the ACS terminal 408 to the gate ensures that the same bias voltages are applied to both the gate (V_g) and the body (shown in FIGURE 3C as " V_b " or " V_{ACS} "). Because the bias voltage V_{ACS} is the same as the gate voltage V_g in this embodiment, the accumulated charge is no longer trapped below the gate oxide (by attraction to the gate bias V_g) because it is conveyed to the gate terminal 402 via the ACS terminal 408. The accumulated charge is thereby removed from the body via the ACS terminal 408.

0125 In other exemplary embodiments, as described above with reference to FIGURE 3C, for example, V_s and V_d may comprise nonzero bias voltages. According to these examples, V_g must be sufficiently negative to both V_s and V_d in order for V_g to be sufficiently negative to V_{th} to turn the NMOSFET 300 off (*i.e.*, operate the NMOSFET 300 in the off-state). When so biased, as described above, the NMOSFET 300 may enter the accumulated charge regime and thereby have accumulated charge present in the body. For this example, the voltage V_{ACS} may also be selected to be equal to V_g by connecting the ACS terminal 408 to the gate terminal 402, thereby conveying the accumulated charge from the body of the ACC NMOSFET, as described above.

0126 In another exemplary embodiment, as described above, the ACC NMOSFET 300 comprises a depletion mode device. In this embodiment, the threshold voltage, V_{th} is, by definition, less than zero. For V_s and V_d both at zero volts, when a gate bias V_g sufficiently negative to V_{th} is applied to the gate terminal 402 (for example, V_g more negative than approximately -1 V relative to V_{th}), holes may accumulate under the gate oxide and thereby comprise an accumulated charge. For this example, the voltage V_{ACS} may also be selected to be equal to V_g by connecting the ACS terminal 408 to the gate terminal 402, thereby conveying the accumulated charge from the ACC NMOSFET as described above.

0127 In some embodiments of the improved ACC SOI NMOSFET 300, such as that described above with reference to FIGURE 4B, when the FET is biased on, diodes formed at the edge of the device (such as described above with reference to the interface between the ACS 308 and the drain 304 (and the source 306) as shown in FIGURE 3D) may become forward biased thereby allowing current to flow into the source and drain regions. In addition to wasting power, this may introduce nonlinearity into the NMOSFET. The nonlinearity results because the current that flows as a result of the forward biased interface diodes comprises nonlinear current. As V_{gs} and V_{gd} are reduced in that region of the device, the on resistance R_{on} at the edge of the device is increased. As is well known, and for the reasons set forth above, if the interface diodes formed at the edge of the device become forward biased, the device on-state characteristics are consequently dramatically adversely affected. Those skilled in the electronic device design arts shall understand that the configuration shown in FIGURE 4B limits application of a gate bias voltage V_{gs} to approximately 0.7 Volts. The simplified circuit shown in FIGURE 4C can be used to overcome these problems.

0128 Another exemplary simplified circuit using the improved ACC SOI NMOSFET 300 is shown in FIGURE 4C. As shown in FIGURE 4C, in this embodiment, the ACS terminal 408 may be electrically coupled to a diode 410, and the diode 410 may, in turn, be coupled to the gate terminal 402. This embodiment may be used to prevent a positive current flow into the MOSFET body 312 caused by a positive V_g -to- V_s (or, equivalently, V_{gs} , where $V_{gs} = V_g - V_s$) bias voltage, as may occur, for example, when the SOI NMOSFET 300 is biased into an on-state condition.

0129 As with the device shown in FIGURE 4B, when biased off, the ACS terminal voltage V_{ACS} comprises the gate voltage plus a voltage drop across the diode 410. At very low ACS terminal current levels, the voltage drop across the diode 410 typically also is very low (e.g., $\ll 500\text{mV}$, for example, for a typical threshold diode). The voltage drop across the diode 410 can be reduced to approximately zero by using other diodes, such as a 0Vf diode, for example. In one embodiment, reducing the voltage drop across the diode is achieved by increasing the diode 410

width. Additionally, maintaining the ACS-to-source or ACS-to-drain voltage (whichever bias voltage of the two bias voltages is lower) increasingly negative, also improves the linearity of the ACC MOSFET device 300.

0130 When the SOI NMOSFET 300 is biased in an on condition, the diode 410 is reverse-biased, thereby preventing the flow of positive current into the source and drain regions. The reverse-biased configuration reduces power consumption and improves linearity of the device. The circuit shown in FIGURE 4C therefore works well to remove accumulated charge from the ACC MOSFET body when the FET is in the off-state and is operated in the accumulated charge regime. It also permits almost any positive voltage to be applied to the gate voltage V_g . This, in turn, allows the ACC MOSFET to effectively remove accumulated charge when the device operates in the off-state, yet assume the characteristics of a floating body device when the device operates in the on-state.

0131 With the exception of the diode 410 used to prevent the flow of positive current into the ACS terminal 408, exemplary operation of the simplified circuit shown in FIGURE 4C is the same as the operation of the circuit described above with reference to FIGURE 4B.

0132 In yet another embodiment, the ACS terminal 408 may be coupled to a control circuit 412 as illustrated in the simplified circuit of FIGURE 4D. The control circuit 412 may provide a selectable ACS bias voltage V_{ACS} that selectively controls the accumulated charge (*i.e.*, the accumulated charge 120 described above with reference to FIGURE 1). As shown in FIGURE 4D, rather than having a local circuit provide the ACS bias voltage V_{ACS} (*e.g.*, as derived from the gate voltage V_g), in some embodiments the ACS bias voltage V_{ACS} is produced by a separate source that is independent of the ACC MOSFET device 300. In the case of a switch (as described below in more detail with reference to FIGURE 4E), the ACS bias voltage V_{ACS} should be driven from a source having a high output impedance. For example, such a high output impedance source can be obtained using a large series resistor in order to ensure that the RF voltage is divided across the MOSFET and that the ACS bias voltage V_{ACS} has $V_{ds}/2$ "riding" on it, similarly to the gate voltage. This approach is described in more detail below with reference to FIGURE 4E.

0133 It may be desirable to provide a negative ACS bias voltage V_{ACS} to the ACS terminal 408 when the SOI NMOSFET 300 is biased into an accumulated charge regime. In this exemplary embodiment, the control circuit 412 may prevent positive current flow into the ACS terminal 408 by selectively maintaining an ACS bias voltage V_{ACS} that is consistently negative with respect to both the source and drain bias voltages. In particular, the control circuit 412 may be used to apply an ACS bias voltage that is equal to or more negative than the lesser of V_s and V_d . By

application of such an ACS bias voltage, the accumulated charge is thereby removed or otherwise controlled.

0134 In the exemplary embodiment of the simplified circuit shown in FIGURE 4D, the source and drain bias voltages applied to the terminals 404 and 406, respectively, may be zero. If the gate bias voltage (V_g) applied to the gate terminal 402 is sufficiently negative with respect to the source and drain bias voltages applied to the terminals 404 and 406, and with respect to V_{th} , (for example, if V_{th} is approximately zero, and if V_g is more negative than approximately -1 V) the ACC NMOSFET 300 operates in the accumulated charge regime, and the accumulated charge (holes) may accumulate in the body of the ACC NMOSFET 300. Advantageously, the accumulated charge can be removed via the ACS terminal 408 by connecting the ACS terminal 408 to the control circuit 412 as shown. In order to ensure that the accumulated charge is conveyed from the body of the ACC NMOSFET 300, the ACS bias voltage V_{ACS} that is applied to the ACS terminal 408 should be equal to or more negative than the gate voltage and more negative than the lesser of V_s and V_d . Because the accumulated charge 120 is conveyed to the bias voltage V_{ACS} applied to the ACS terminal 408 by the control circuit 412, the accumulated charge does not remain trapped under the gate oxide due to attraction to the gate bias voltage V_g .

0135 In other embodiments, V_s and V_d may comprise bias voltages that are other than zero. According to these examples, V_g must be sufficiently negative to both V_s and V_d in order for V_g to be sufficiently negative to V_{th} , in order to bias the NMOSFET 300 in the off-state. This allows the accumulation of accumulated charge under the gate oxide. For this example, the ACS bias voltage V_{ACS} may be selected to be equal to or more negative than the lesser of V_s and V_d by connecting the ACS terminal 408 to the control circuit 412 to provide selected ACS bias voltages, thereby conveying the accumulated charge from the ACC NMOSFET 300.

0136 In other embodiments, if the ACC NMOSFET 300 of FIGURE 4D comprises a depletion mode device, V_{th} is, by definition, less than zero. For V_s and V_d both at zero volts, when a gate bias V_g sufficiently negative to V_{th} is applied (for example, V_g more negative than approximately -1 V relative to V_{th}), holes may accumulate under the gate oxide. For this example, the ACS bias voltage V_{ACS} that is applied to the ACS terminal 408 may also be selected to be equal to or more negative than the lesser of V_s and V_d by connecting the ACS terminal 408 to the control circuit 412 and thereby provide the desired ACS bias voltages V_{ACS} that are necessary to remove the accumulated charge from the ACC NMOSFET 300.

0137 As described above, in one embodiment, instead of having the control circuit 412 provide a bias to the ACS terminal 408 as shown in FIGURE 4D, the ACS terminal 408 can be

driven by a separate bias source circuit, as shown, for example, in the embodiment of FIGURE 4E. In one exemplary circuit implementation, as exemplified in the circuit of FIGURE 4E, in an RF switch circuit, the separate V_{ACS} source has a high output impedance element 403 which ensures that the RF voltage is divided across the ACC NMOSFET 300, and which further ensures that the voltage applied to the ACS terminal 408 has $V_{ds}/2$ applied thereon, similar to the voltage V_{gs} that is applied to the gate terminal 402. In one exemplary embodiment, an inverter 405 is configured in series with the high output impedance element 403 and supplied by GND and $-V_{DD}$. In one exemplary embodiment, $-V_{DD}$ is readily derived from a convenient positive voltage supply. It could, however, comprise an even more negative voltage for improved linearity (*i.e.*, it can be independent of the gate voltage).

0138 In another embodiment, the circuit shown in FIGURE 4C can be modified to include a clamping circuit configured in series with an ACS terminal 408. Such an exemplary embodiment is shown in FIGURE 4F. Under certain operating conditions, current that flows out of the ACC NMOSFET 300, conveying the accumulated charge from the body of the ACC NMOSFET 300, via the ACS terminal 408 is sufficiently high such that it causes problems in the biasing circuitry (*i.e.*, under some conditions the ACS current is so high that the biasing circuitry cannot adequately sink the current flowing out of the body of the ACC NMOSFET 300). As shown in the circuit of FIGURE 4F, one exemplary embodiment solves this problem by interrupting the flow of ACS current out of the body of the ACC NMOSFET 300, and thereby returning the ACC NMOSFET 300 to a floating body condition.

0139 In one exemplary circuit, as shown in FIGURE 4F, a depletion-mode FET 421 is configured in series between the ACS terminal 408 and a diode 410. In this exemplary circuit, the depletion-mode FET 421 includes a gate terminal that is electrically connected to the FET's source terminal. In this configuration, the depletion-mode FET 421 functions to clip or limit the current that flows from the ACS terminal 408 when the ACC MOSFET operates in the accumulated charge regime. More specifically, the depletion-mode FET 421 enters saturation upon reaching a predefined threshold. The current leaving the body of the ACC MOSFET is thereby limited by the saturation current of the FET 421. In some embodiments, the predefined saturation threshold may optionally be adjusted to change the point at which clamping occurs, such as by selecting a higher threshold voltage, which results in a lower maximum current and earlier clamping.

0140 In some embodiments, such as for example in an RF switch circuit, the gate terminal 402 and the ACS terminal 408 follow V_{ds} at half the rate ($V_{ds}/2$) of V_{ds} . At high V_{ds} excursions, V_{gs} may approach the threshold voltage V_{th} , resulting in increased I_{ds} leakage current. In some cases, such a leakage current exits the ACS terminal 408 and can overwhelm associated

circuitry (e.g., a negative voltage generator). Hence, the circuit shown in FIGURE 4F solves or otherwise mitigates these problems. More specifically, by coupling the FET 421 in series between the ACS terminal 408 and the diode 410, the current that exits the ACS terminal 408 is limited to the saturation current of the FET 421.

5 **0141** In yet another exemplary embodiment, the simplified circuit shown in FIGURE 4C can be modified to include an AC shorting capacitor placed in parallel with the diode 410. The simplified circuit of FIGURE 4G can be used to compensate for certain undesirable nonlinearities present in a full circuit application. In some embodiments, due to parasitics present in the MOSFET layout, nonlinearity characteristics existing in the diode 410 of FIGURE 4C may introduce
10 undesirable nonlinearities in a full circuit implementation. As the diode is in place to provide DC bias conditions and is not intended to have any AC signals across it, it may be desirable in some embodiments to take steps to mitigate the effects of any AC signal present across the diode 410.

0142 As shown in the simplified circuit of FIGURE 4G, the circuit of FIGURE 4C has been modified to include an AC shorting capacitor 423 wherein the AC shorting capacitor 423 is
15 configured in parallel across the diode 410. The AC shorting capacitor 423 is placed in parallel with the diode 410 to ensure that nonlinearities of the diode 410 are not excited by an AC signal. In some exemplary circuits, such as in an RF switch, the AC shorting capacitor 423 does not impact the higher level full circuit, as the gate terminal 402 and the ACS terminal 408 typically have the same AC signal applied (*i.e.*, AC equipotential).

20 **0143** In some circuit embodiments, body nodes of a multi-finger FET implementation may be connected to one another (using, for example, metal or silicon), overlapping the source fingers. On another side of the FET implementation, gate nodes may be are connected to one another (using, for example, metal or silicon) overlapping the drain fingers. As a result of this FET implementation, additional capacitance may result between the source and body (S-B), and further
25 additional capacitance may result between the drain and gate (D-G). These additional capacitances may degrade the symmetry of the intrinsic device. Under AC excitation, this results in the gate terminal following the drain terminal more closely, and the body terminal following the source terminal more closely, which effectively creates an AC signal across the diode 410, which can excite nonlinearities of the diode 410 as described above. Using the exemplary embodiment shown in
30 FIGURE 4G, parasitic nonlinear excitation due to the overlapping fingers is mitigated.

Improved C_{off} Performance Characteristics of ACC MOSFETs made in Accordance with the Present Disclosed Method and Apparatus

0144 FIGURE 4H is a plot 460 of the off-state capacitance (C_{off}) versus an applied drain-to-source voltage of an SOI MOSFET when an AC signal is applied to the MOSFET (the plot 460 is relevant to an exemplary 1 mm wide MOSFET, though similar plots result using wider and narrower devices). In one embodiment, a gate voltage equals $-2.5 \text{ Volts} + V_d/2$, and V_s equals 0. A first plot 462 shows the off-state capacitance C_{off} of a typical prior art NMOSFET operating within the accumulated charge regime and thereby having an accumulated charge as described above with reference to FIGURE 1. As shown in FIGURE 4H, the off-state capacitance C_{off} shown in plot 462 of the prior art FET is voltage-dependent (*i.e.*, it is nonlinear) and peaks when $V_d = 0 \text{ Volts}$. A second plot 464 illustrates the off-state capacitance C_{off} of an improved ACC SOI MOSFET made in accordance with the present teachings, wherein the accumulated charge is conveyed from the ACC MOSFET, thereby reducing, controlling and/or eliminating the accumulated charge from the ACC MOSFET body. As shown in FIGURE 4H, the off-state capacitance C_{off} shown in plot 464 of the ACC SOI MOSFET is not voltage-dependent (*i.e.*, it is linear).

0145 As described above with reference to FIGURE 2A, by controlling, reducing or eliminating the accumulated charge, the impedance 212 of the NMOSFET body 312 (FIGURE 3C, and shown as the MOSFET body 114 in the electrical model of FIGURE 2A) is increased to a very large value. This increase in the impedance 212 of the MOSFET body reduces the contribution to C_{off} caused by the impedance of the junctions 218 and 220 (FIGURE 2A), thereby reducing the overall magnitude of C_{off} and the nonlinear effects associated with the impedances of the junctions 218 and 220. Plot 464 illustrates how the present teachings advantageously reduce both the nonlinearity and overall magnitude of the off-state capacitance C_{off} of the MOSFET. The reduced nonlinearity and magnitude of the off-state capacitance C_{off} improves the performance of circuits using MOSFETs operating in an accumulated charge regime, such as RF switching circuits. Exemplary RF switching circuits implemented with the ACC MOSFETs described above with reference to FIGURES 4A-4G are now described with reference to FIGURES 5A-5D.

Exemplary Improved Performance RF Switch Implementations using ACC SOI MOSFETs in Accordance with the Present Teachings

0146 FIGURE 5A shows a schematic diagram of a single pole, single throw (SPST) RF switch circuit 500 in accordance with prior art. The RF switch circuit 500 is one example of a general class of well-known RF switch circuits. Similar RF switch circuits are described in the following co-pending and commonly assigned U. S. Applications and Patent: Provisional Application No. 60/651,736, filed February 9, 2005, entitled "UNPOWERED SWITCH AND

BLEEDER CIRCUIT;" Application No. 10/922,135, filed August 18, 2004, pending, which is a continuation application of Application No. 10/267,531, filed October 8, 2002, which issued October 12, 2004 as U.S. Patent 6,804,502, entitled "SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS". Application No. 10/267,531, filed October 8, 2002, which issued
5 October 12, 2004 as U.S. Patent 6,804,502 claims the benefit of U.S. Provisional Application No. 60/328,353, filed October 10, 2001. All of the above-cited applications and issued patent set forth above are hereby incorporated by reference herein as if set forth in full for their teachings on RF switch circuits including SOI MOSFET switch circuits.

0147 Referring again to FIGURE 5A, a switching SOI NMOSFET 506 is adapted to
10 receive an RF input signal "RFin" at an input terminal 502. The switching SOI MOSFET 506 is electrically coupled to selectively couple the RFin input signal to an output terminal 504 (*i.e.*, thereby convey an RF output signal Rfout at the output terminal 504). In the exemplary embodiment, the switching SOI NMOSFET 506 is controlled by a first control signal C1 that is conveyed by a control line 512 through a gate resistor 510 (optionally included for suppression of parasitic RF coupling).
15 The control line 512 is electrically coupled to a control circuit 520, which generates the first control signal C1.

0148 Referring again to FIGURE 5A, a shunting SOI NMOSFET 508 is adapted to
20 receive the RF input signal RFin at its drain terminal, and to selectively shunt the input signal RFin to ground via an optional load resistor 518. The shunting SOI NMOSFET 508 is controlled by a second control signal C1x which is conveyed by a control line 516 through a gate resistor 514 (optionally included for suppression of parasitic RF coupling and for purposes of voltage division). The control line 516 is electrically coupled to the control circuit 520, which generates the second control signal C1x.

0149 The terms "switching" and "shunting", as pertains to the transistors shown in
25 FIGURE 5A and also described below with reference to the RF switch circuits of FIGURES 5B-5D, 6, 8, and 9, are used interchangeably herein with the terms "switch" and "shunt", respectively. For example, the switching transistor 506 (and all of its analogous switching transistors described below in FIGURES 5B-5D, 6, 8, and 9) is also referred to herein as the "switch" transistor. Similarly, the shunting transistor 508 (and all of its analogous shunting transistors described below in FIGURES
30 5B-5D, 6, 8, and 9) is also referred to herein as the "shunt" transistor. The terms "switch" and "switching" (and similarly the terms "shunt" and "shunting"), when used to describe the RF switch circuit transistors, are used interchangeably herein. Further, as described below in more detail with reference to FIGURE 6, those skilled in the RF switching design and fabrication arts shall recognize that although the switch and shunt transistors are shown in FIGURES 5A-5D and FIGURE 9 as

comprising a single MOSFET, it shall be understood that they may comprise transistor groupings comprising one or more MOSFET transistors.

0150 It will also be appreciated by those skilled in RF switch circuits that all of the exemplary switch circuits may be used "bi-directionally," wherein the previously described input ports function as output ports, and *vice versa*. That is, although an exemplary RF switch may be described herein as having one or more input ports (or nodes) and one or more output ports (or nodes), this description is for convenience only, and it will be understood that output ports may, in some applications, be used to input signals, and input ports may, in some applications, be used to output signals. The RF switch circuits described with reference to FIGURES 2B, 4E, 5A-5D, 6, 8 and 9 are described herein as having "input" and "output" ports (or "nodes") that input and output RF signals, respectively. For example, as described below in more detail with reference to FIGURE 9, RF input node 905 and RF input node 907 are described below as inputting RF signals RF1 and RF2 respectively. RFC common port 903 is described below as providing an RF common output signal. Those skilled in the RF switch circuit design arts shall recognize that the RF switch is bidirectional, and that the previously described input ports function perfectly well as output ports, and *vice versa*. In the example of the RF switch of FIGURE 9, the RFC common port can be used to input an RF signal which is selectively output by the RF nodes 905 and 907.

0151 Referring again to FIGURE 5A, the first and second control signals, C1 and C1x, respectively, are generated so that the switching SOI NMOSFET 506 operates in an on-state when the shunting SOI NMOSFET 508 operates in an off-state, and *vice versa*. These control signals provide the gate bias voltages V_g to the gate terminals of the NMOSFETs 506 and 508. When either of the NMOSFETs 506 or 508 is biased to select the transistor off-state, the respective V_g must comprise a sufficiently large negative voltage so that the respective NMOSFET does not enter, or approach, an on-state due to the time varying applied voltages of the RF input signal R_{Fin} . The maximum power of the RF input signal R_{Fin} is thereby limited by the maximum magnitude of the gate bias voltage V_g (or, more generally, the gate-to-source operating voltage, V_{gs}) that the SOI NMOSFETs 506 and 508 can reliably sustain. For RF switching circuits such as those exemplified herein, the magnitude of $V_{gs(max)} = |V_g| + |V_{ds(max)}/2|$, where $V_{ds} = V_d - V_s$, and $V_{ds(max)}$ comprises the maximum V_{ds} due to the high-power input signal voltage levels associated with the RF input signal R_{Fin} .

0152 Exemplary bias voltages for the switching and shunting SOI NMOSFETs 506 and 508, respectively, may include the following: with V_{th} approximately zero volts, V_g , for the on-state, of +2.5 V, and V_g , for the off-state, of - 2.5 V. For these bias voltages, the SOI NMOSFETs may eventually operate in an accumulated charge regime when placed into their off-states. In particular, and as described above with reference to FIGURE 2B, when the switching NMOSFET 506

is in the on-state, and the shunting NMOSFET 508 is biased in the off-state, the output signal RFout may become distorted by the nonlinear behavior of the off capacitance C_{off} of the shunting NMOSFET 508 caused by the accumulated charge. Advantageously, the improved ACC MOSFETs made in accordance with the present teachings can be used to improve circuit performance, especially as it is adversely affected by the accumulated charge.

0153 FIGURE 5B is a schematic of an improved RF circuit 501 adapted for higher performance using the present accumulated charge reduction and control techniques. The switch circuit 501 differs from the prior art circuit 500 (FIGURE 5A) in that the shunting NMOSFET 508 is replaced by a shunting ACC NMOSFET 528 made in accordance with the present teachings. The shunting ACC NMOSFET 528 is analogous to the ACC NMOSFET described above with reference to FIGURES 4A and 4B. Similarly, the gate, source, drain and ACC terminals of the shunting ACC NMOSFET 528 are analogous to the respective terminals of the ACC NMOSFET 300. With the exception of the improved switch performance afforded by the improved shunting ACC NMOSFET 528, the operation of the RF switch circuit 501 is very similar to the operation of the RF switch circuit 500 described above with reference to FIGURE 5A.

0154 Exemplary bias voltages for the switching NMOSFET 526 and the shunting ACC NMOSFET 528 may include: with V_{th} approximately zero, V_g , for the on-state, of +2.5 V, and V_g , for the off-state, of - 2.5 V. For these bias voltages, the SOI NMOSFETs may operate in an accumulated charge regime when placed into the off-state. However, when the switching NMOSFET 526 is in the on-state and the shunting ACC NMOSFET 528 is in the off-state, the output signal RFout at the output terminal 505 will not be distorted by nonlinear behavior of the off-state capacitance C_{off} of the improved shunting ACC NMOSFET 528 due to the accumulated charge. When the shunting ACC NMOSFET 528 operates in the accumulated charge regime, the accumulated charge is removed via the ACS terminal 508'. More specifically, because the gate terminal 502' of the shunting ACC NMOSFET 528 is connected to the ACS terminal 508', the accumulated charge is removed or otherwise controlled as described above in reference to the simplified circuit of FIGURE 4B. The control of the accumulated charge improves performance of the switch 501 by improving the linearity of the off transistor, shunting ACC NMOSFET 528, and thereby reducing the harmonic and intermodulation distortion of the RF output signal Rfout generated at the output terminal 505.

0155 FIGURE 5C is a schematic of another embodiment of an improved RF switch circuit 502 adapted for higher performance using the accumulated charge control techniques of the present disclosure. The switch circuit 502 differs from the prior art circuit 500 (FIGURE 5A) in that the NMOSFET 508 is replaced by an ACC NMOSFET 528 made in accordance with the present teachings. The ACC NMOSFET 528 is analogous to the ACC NMOSFET 300 described above with

reference to FIGURES 4A and 4C. Similarly, the gate, source, drain and ACC terminals of the ACC NMOSFET 528 are analogous to the respective terminals of the ACC NMOSFETs 300 described above with reference to FIGURE 4A and 4C. With the exception of the improved switch performance afforded by the improved ACC NMOSFET 528, the operation of the switch circuit 502 is very similar to the operations of the switch circuits 500 and 501 described above with reference to FIGURES 5A and 5B, respectively.

0156 Exemplary bias voltages for the NMOSFET 526 and the ACC NMOSFET 528 may include the following: with V_{th} approximately zero volts, V_g , for the on-state, of +2.5 V, and V_g , for the off-state, of - 2.5 V. For these bias voltages, the SOI NMOSFETs 526, 528 may operate in an accumulated charge regime when placed into an off-state. However, when the NMOSFET 526 is in the on-state and the ACC NMOSFET 528 is in the off-state, the output signal RF_{out} will not be distorted by nonlinear behavior of the off-state capacitance C_{off} of the ACC NMOSFET 528 due to the accumulated charge. Because the gate terminal 502' of the ACC NMOSFET 528 is connected to the ACS terminal 508' via a diode 509, the accumulated charge is entirely removed, reduced or otherwise controlled, as described above with reference to FIGURE 4C. Similar to the improved switch 501 described above with reference to FIGURE 5B, control of the accumulated charge improves performance of the switch 502 by improving the linearity of the off transistor, 528, and thereby reducing the harmonic and intermodulation distortion of the RF output signal RF_{out} output of the RF output terminal 505. Connection of the diode 509 as shown may be desired in some embodiments for suppression of positive current flow into the ACC NMOSFET 528 when it is biased into an on-state, as described above with reference to FIGURE 4C.

0157 FIGURE 5D is a schematic of another embodiment of an improved RF switch circuit 503 adapted for higher performance using the present accumulated charge control techniques. The switch circuit 503 differs from the prior art circuit 500 (FIGURE 5A) in that the NMOSFET 508 of FIGURE 5A is replaced by an ACC NMOSFET 528 made in accordance with the present teachings. The ACC NMOSFET 528 is analogous to the ACC NMOSFET described above with reference to FIGURES 4A and 4D. With the exception of the improved switch performance afforded by the improved ACC NMOSFET 528, the operation of the switch circuit 503 is very similar to the operations of the switch circuits 500, 501 and 502 described above with reference to FIGURES 5A-5C, respectively.

0158 Exemplary bias voltages for the NMOSFET 526 and the ACC NMOSFET 528 may include the following: with V_{th} approximately zero volts, V_g , for the on-state, of +2.5 V, and V_g , for the off-state, of - 2.5 V. For these bias voltages, the SOI NMOSFETs 526, 528 may operate in an accumulated charge regime when placed into the off-state. However, when the NMOSFET 526 is in

the on-state and the ACC NMOSFET 528 is in the off-state, the output signal RFout produced at the output terminal 505 will not be distorted by the nonlinear behavior of the off-state capacitance C_{off} of the ACC NMOSFET 528 due to the accumulated charge. When the NMOSFET 528 operates in the accumulated charge regime, the accumulated charge is removed via the ACS terminal 508'. More specifically, because the ACS terminal 508' of the ACC NMOSFET 528 is electrically coupled to the control circuit 520 via the control line 517 (*i.e.*, controlled by the control signal "C2" as shown), the accumulated charge can be eliminated, reduced or otherwise controlled by applying selected bias voltages to the ACS terminal 508' as described above with reference to FIGURE 4D. Those skilled in the arts of electronic circuit design shall understand that a wide variety of bias voltage signals can be applied to the ACS terminal for the purpose of reducing or otherwise controlling the accumulated charge. The specific bias voltages may be adapted for use in a particular application. The control of the accumulated charge improves performance of the switch 503 by improving the linearity of the off-state transistor, 528, and thereby reducing the harmonic and intermodulation distortion of the RF output signal Rfout generated at the output terminal 505.

0159 In the circuits described above with respect to FIGURES 5B-5D, the switching SOI MOSFETs 526 are shown and described as implemented using SOI MOSFETs of the prior art (*i.e.*, they do not comprise ACC MOSFETs and therefore do not have an ACS terminal). Those skilled in the electronic device design arts shall understand and appreciate that in other embodiments of the disclosed method and apparatus, the prior art switching SOI MOSFETs 526 may be replaced, as desired or required, by ACC SOI MOSFETs made in accordance with the present disclosure. For example, in some embodiments of RF switches implemented using the ACC MOSFET of the present teachings, the RF switch comprises a single-pole double-throw RF switch. In this embodiment, the switching SOI MOSFETs (*e.g.*, analogous to the switching SOI MOSFETs 526 described above with reference to FIGURES 5B-5D) may comprise ACC SOI MOSFETs. Such an implementation prevents nonlinear behavior of the off-state switching SOI MOSFETs (which is turned off when it is not selected as an input "pole") from detrimentally affecting the output of the RF signal as switched through the selected "pole". Implementation of the RF switches using switching ACC MOSFETs reduces the magnitude, drift, and voltage dependency of the off capacitance C_{off} of the switching transistors. Consequently, and as described above in more detail, the switch performance characteristics, such as its isolation, insertion loss and drift characteristics, are also improved. This implementation is described in more detail below with reference to the RF switch circuit shown in FIGURE 9. Many other examples will be apparent to those skilled in the arts of electronic circuits.

0160 For example, as set forth above, although the exemplary RF switches have been described as being implemented using ACC SOI NMOSFET devices, they can also be implemented

using ACC SOI PMOSFET devices. Further, although single-pole single-throw, and single-pole double-throw RF switches have been described above as examples of RF switches implemented in accordance with the present teachings, the present application encompasses any variation of single-pole multi-throw, multi-pole single-throw, and multi-pole multi-throw RF switch configurations.

5 Those skilled in the RF switch design and fabrication arts shall recognize and appreciate that the present teachings can be used in implementing any convenient RF switch configuration design.

Exemplary RF Switch Implementation using Stacked Transistors

0161 In the exemplary embodiments of RF switch circuits described above, the switch circuits are implemented using a single SOI NMOSFET (*e.g.*, the single SOI NMOSFET 506 of FIGURE 5A, and the single SOI NMOSFET 526 of FIGURES 5B - 5D) that selectively couples or blocks (*i.e.*, electrically opens the circuit connection) the RF input signal to the RF output. Similarly, in the exemplary embodiments described above with reference to FIGURES 5A-5D, a single SOI NMOSFET (*e.g.*, the single SOI NMOSFET 508 of FIGURE 5A, and ACC SOI NMOSFET 528 of FIGURES 5B-5D) is used to shunt (FET in the on-state) or block (FET in the off-state) the RF input signal to ground. Commonly assigned U.S. Patent 6,804,502, entitled "SWITCH CIRCUIT AND METHOD OF SWITCHING RADIO FREQUENCY SIGNALS", issued October, 12, 2004, describes RF switch circuits using SOI NMOSFETs implemented with stacked transistor groupings that selectively couple and block RF signals.

0162 One example of how stacked NMOSFETs may be implemented in accordance with the teachings of the present disclosure is illustrated in FIGURE 6. An RF switch circuit 600 is analogous to the RF switch circuit 503 of FIGURE 5D, wherein the single SOI NMOSFET 526 is replaced by a stack of SOI NMOSFETs 602, 604 and 606. Similarly, the single ACC SOI NMOSFET 528 is replaced by a stack of ACC SOI NMOSFETs 620, 622 and 624. The control signal C2 is provided to the ACS terminals of the ACC SOI NMOSFETs 620, 622 and 624 via optional resistors 626, 628, and 630, respectively. The resistors 626, 628, and 630 may optionally be included in order to suppress parasitic RF signals between the stacked ACC SOI NMOSFETs 620, 622, and 624, respectively. The RF switch circuit 600 operates analogously to the operation of the RF switch circuit 503 described above with reference to FIGURE 5D.

0163 Three stacked ACC SOI NMOSFETs are shown in each ACC NMOSFET stack in the exemplary stacked RF switch circuit 600 of FIGURE 6. A plurality of three ACC NMOSFETs is shown for illustrative purposes only, however, those skilled in the integrated circuit design arts will understand that an arbitrary plurality may be employed according to particular circuit requirements such as power handling performance, switching speed, *etc.* A smaller or larger plurality of stacked ACC NMOSFETs may be included in a stack to achieve a desired operating performance.

0164 Other stacked RF switch circuits, adapted for accumulated charge control, analogous to the circuits described above with reference to FIGURES 5B-5D, may also be employed. Implementations of such circuits shall be obvious from the teachings above to those skilled in the electronic device design arts, and therefore are not described further herein. Moreover, it shall be obvious to those skilled in the electronic device design arts that, although a symmetrically stacked

(i.e., having an equal number of shunting and switching transistors) RF switch is shown in the stacked RF switch of FIGURE 6, the present inventive ACC method and apparatus is not so limited. The present teachings can be applied in implementing both symmetrically and asymmetrically stacked (having an unequal number of shunting and switching transistors) RF switches. The designer will readily understand how to use the ACC MOSFETs of the present disclosure in implementing asymmetrical, as well as symmetrical, RF switch circuits.

Exemplary Method of Operation

0165 FIGURE 7 illustrates an exemplary method 700 of improving the linearity of an SOI MOSFET having an accumulated charge sink (ACS) in accordance with the present disclosure. The method 700 begins at a STEP 702, whereat an ACC SOI MOSFET having an ACS terminal is configured to operate in a circuit. The ACS terminal may be operatively coupled to the gate of the SOI MOSFET (as described above with reference to FIGURES 4B, 4C, 5B and 5C), or to a control circuit (as described above with reference to FIGURES 4D and 5D). In other embodiments, the ACS terminal may be operatively coupled to any convenient accumulated charge sinking mechanism, circuit, or device as is convenient to the circuit or system designer. The method then proceeds to a step 704.

0166 At the STEP 704, the ACC SOI MOSFET is controlled, at least part of the time, so that it operates in an accumulated charge regime. In most embodiments, as described above, the ACC MOSFET is operated in the accumulated charge regime by applying bias voltages that place the FET in an off-state condition. In one exemplary embodiment, the ACC SOI MOSFET comprises an ACC SOI NMOSFET that is configured as part of a shunting circuit of an RF switch. According to this exemplary embodiment, the SOI NMOSFET may be operated in an accumulated charge regime after the shunting circuit is placed into an off-state by applying a negative bias voltage to the gate terminal of the ACC NMOSFET.

0167 The method then proceeds to a STEP 706, whereat the accumulated charge that has accumulated in the channel region of the ACC MOSFET is removed or otherwise controlled via the ACS terminal. In this embodiment, the accumulated charge is conveyed to another circuit terminal and is thereby reduced or otherwise controlled. One such exemplary circuit terminal that can be used to convey the accumulated charge from the MOSFET body comprises a gate terminal of the ACC MOSFET (*see, e.g.*, the description above with reference to FIGURES 4B, 4C, 5B and 5C). Another exemplary circuit terminal that can be used to remove or otherwise control the accumulated charge comprises the terminal of a control circuit (*see, e.g.*, FIGURES 4D and 5D). As described in more detail above, removing or otherwise controlling the accumulated charge in the ACC MOSFET

body improves the linearity of the off-state ACC MOSFET, which reduces the harmonic distortion and IMD of signals affected by the ACC MOSFET, and which, in turn, improves circuit and system performance. In RF switch circuits, improvements (in both linearity and magnitude) are made to the off capacitance of shunting ACC MOSFET devices, which, in turn, improves the performance of the RF switch circuits. In addition to other switch performance characteristics, the harmonic and intermodulation distortions of the RF switch are reduced using the ACC method and apparatus of the present teachings.

0168 FIGURES 8 and 9 show schematics of additional exemplary embodiments of RF switching circuits made in accordance with the disclosed method and apparatus for use in improving linearity of MOSFETs having an ACS. As described in more detail below with reference to FIGURES 8 and 9, in some exemplary embodiments of RF switch circuits made in accordance with the present disclosure, it may be desirable to include drain-to-source resistors, R_{ds} , and thereby improve some switch performance characteristics when the switch is used in a particular application. These exemplary RF switch circuits are now described in more detail.

Exemplary RF Switch Implementations using Stacked Transistors having Source to Drain Resistors

0169 FIGURE 8 shows one exemplary embodiment of an RF switch circuit 800 made in accordance with the present disclosure. As shown in FIGURE 8, some embodiments of RF switches made in accordance with the present disclosure may include drain-to-source (R_{ds}) resistors electrically connected to the respective sources and drains of the ACC MOSFETs. For example, the exemplary switch 800 of FIGURE 8 includes drain-to-source R_{ds} resistors 802, 804, and 806 electrically connected to the respective sources and drains of the shunting ACC SOI NMOSFETs 620, 622, and 624, respectively. Motivation for use of the drain-to-source R_{ds} resistors is now described.

0170 As shall be appreciated by skilled persons from the present teachings, removal of the accumulated charge via the ACS terminal causes current to flow from the body of the ACC SOI MOSFET. For example, when a hole current flows from the body of an ACC SOI MOSFET via the ACS, an equal electron current flows to the FET source and/or drain. For some circuits (e.g., the RF switch circuit of FIGURE 8), the sources and/or drains of the ACC SOI NMOSFETs are connected to other SOI NMOSFETs. Because off-state SOI NMOSFETs have a very high impedance (e.g., in the range of 1 Gohm for a 1 mm wide SOI NMOSFET), even a very small drain-to-source current (e.g., in the range of 1 nA) can result in an unacceptably large drain-to-source voltage V_{ds} across the ACC SOI NMOSFET in satisfaction of Kirchhoff's well known current and voltage laws. In some

embodiments, such as that shown in the RF switch circuits of FIGURES 8 and 9, such resultant very large drain-to-source voltages V_{ds} undesirably impacts reliability and linearity of the ACC SOI NMOSFET. The drain-to-source resistors R_{ds} provide a path between the ACC FET drain and source whereby currents associated with controlling the accumulated charge may be conducted away from the sources and drains of ACC SOI NMOSFETs when implemented in series with high impedance elements such as other ACC SOI NMOSFETs.

0171 Exemplary operating voltages for the NMOSFETs 602-606 of FIGURE 8, and the ACC NMOSFETs 620-624, may include the following: V_{th} approximately zero volts, V_g , for the on-state, of +2.5 V, and V_g , for the off-state, of - 2.5 V. In an exemplary embodiment, the ACC SOI NMOSFET 622 of FIGURE 8 may have a width of 1mm, and an electron-hole pair generation rate for accumulated charge producing a current of 10 pA/ μ m for operation in the accumulated charge regime. For the electron current supplied equally by the source and drain, and an impedance of the ACC SOI NMOSFETs 620 and 622 on the order of 1 Gohm, then an unacceptable bias of - 5 V would result on the source and drain of the ACC SOI NMOSFET 622 without the presence of R_{ds} resistors 802 and 806. This bias voltage would also be applied to the interior nodes of the ACC SOI NMOSFETs 620 and 624.

0172 Even currents smaller than the exemplary currents may produce adverse effects on the operation of the RF switching circuit 800 by reducing V_{gs} and/or V_{gd} of the ACC SOI MOSFETs 620-624 in the off-state, thereby reducing the power handling capability and reliability of the circuit by increasing leakage (e.g., when either V_{gs} or V_{gd} approaches V_{th}), by increasing hot-carrier damage caused by excess leakage, *etc.* Linearity of the MOSFETs is also degraded by reducing V_{gs} and/or V_{gd} when either value approaches V_{th} .

0173 Exemplary values for the R_{ds} resistors 802 to 806 may be selected in some embodiments by selecting a value approximately equal to the resistance of the gate resistors 632-636 divided by the number of ACC SOI NMOSFETs in the stack (in the exemplary embodiment, there are three ACC FETs in the stack). More generally, the value of the R_{ds} resistors may be equal to the gate resistor value divided by the number of ACC SOI NMOSFETs in the stack. In one example, a stack of eight ACC SOI NMOSFETs may have gate resistors of 80 kohm and R_{ds} resistors of 10 kohm.

0174 In some embodiments, the R_{ds} resistors may be selected so that they do not adversely affect switch performance characteristics, such as, for example, the insertion loss of the switch 800 due to the off-state ACC SOI NMOSFETs. For example, for a net shunt resistance greater than 10 kohm, the insertion loss is increased by less than 0.02 dB.

0175 In other embodiments, the R_{ds} resistors may be implemented in circuits comprising a single ACC SOI MOSFET (as contrasted with the stacked shunting configuration exemplified in FIGURE 8 by the shunting ACC FETs 620, 622 and 624). For example, such circuits may be desirable if there are other high-impedance elements configured in series with an ACC SOI MOSFET that may cause a significant bias voltage to be applied to the source or drain as a result of the current flow created when removing or otherwise controlling accumulated charge. One exemplary embodiment of such a circuit is shown in FIGURE 9.

0176 FIGURE 9 shows an exemplary single-pole double-throw (SPDT) RF switch circuit 900 made in accordance with the present teachings. As shown in FIGURE 9, a DC blocking capacitor 904 is connected to a first RF input node 905 that receives a first RF input signal RF1. Similarly, a DC blocking capacitor 906 is connected to a second RF input node 907 that receives a second RF input signal RF2. Further, a DC blocking capacitor 902 is electrically connected to an RF common output node 903 that provides an RF common output signal (RFC) selectively conveyed to the node RFC 903 by the switch circuit 900 from either the first RF input node 905 or the second RF input node 907 (*i.e.*, RFC either outputs RF1 or RF2, depending upon the operation of the switch as controlled by the control signals C1 and C1x described below in more detail).

0177 A first control signal C1 is provided to control the operating states of the ACC SOI NMOSFETs 526 and 528' (*i.e.*, C1 selectively operates the FETs in the on-state or the off-state). Similarly, a second control signal C1x is provided to control the operating states of the ACC SOI NMOSFETs 528 and 526'. As is well known, and as described for example in the above incorporated commonly assigned U.S. Patent No. 6,804,502, the control signals C1 and C1x are generated so that the ACC SOI NMOSFETs 526 and 528' are in an on-state when the ACC SOI NMOSFETs 528 and 526' are in an off-state, and *vice versa*. This configuration allows the RF switch circuit 900 to selectively convey either the signal RF1 or RF2 to the RF common output node 903.

0178 A first ACS control signal C2 is configured to control the operation of the ACS terminals of the SOI NMOSFETs 526 and 528'. A second ACS control signal C2x is configured to control the ACS terminals of the ACC SOI NMOSFETs 528 and 526'. The first and second ACS control signals, C2 and C2x, respectively, are selected so that the ACSs of the associated and respective NMOSFETs are appropriately biased in order to eliminate, reduce, or otherwise control their accumulated charge when the ACC SOI NMOSFETs operate in an accumulated charge regime.

0179 As shown in the RF switch circuit 900 of FIGURE 9, in some embodiments, an R_{ds} resistor 908 is electrically connected between the source and drain of the switching ACC NMOSFET 526. Similarly, in some embodiments, an R_{ds} resistor 910 is electrically connected

between the source and drain of the switching ACC NMOSFET 526'. According to this example, the circuit 900 is operated so that either the shunting ACC NMOSFET 528 or the shunting ACC NMOSFET 528' operate in an on-state at any time (*i.e.*, at least one of the input signals RF1 at the node 905 or RF2 at the node 907 is always conveyed to the RFC node 903), thereby providing a low-impedance path to ground for the node 905 or 907, respectively. Consequently, either the R_{ds} resistor 908 or the R_{ds} resistor 910 provides a low-impedance path to ground from the RF common node 903, thereby preventing voltage bias problems caused as a result of ACC current flow into the nodes 903, 905 and 907 that might otherwise be caused when using the DC blocking capacitors 902, 904 and 906.

Additional Exemplary Benefits Afforded by the ACC MOSFETs of the Present Disclosure

0180 As described above, presence of the accumulated charge in the bodies of the SOI MOSFETs can adversely affect the drain-to-source breakdown voltage (BVDSS) performance characteristics of the floating body MOSFETs. This also has the undesirable effect of worsening the linearity of off-state MOSFETs when used in certain circuits such as RF switching circuits. For example, consider the shunting SOI NMOSFET 528 shown in FIGURE 9. Further consider the case wherein the shunting NMOSFET 528 is implemented with a prior art SOI NMOSFET, rather than with the ACC NMOSFET made in accordance with the present teachings. Assume that the RF transmission line uses a 50-ohm system. With small signal inputs, and when the NMOSFET 528 operates in an off-state, the prior art off-state shunting NMOSFET 528 may introduce harmonic distortion and/or intermodulation distortion in the presence of multiple RF signals. This will also introduce a noticeable loss of signal power.

0181 When sufficiently large signals are input that cause the NMOSFET 528 to enter a BVDSS regime, some of the RF current is clipped, or redirected through the NMOSFET 528 to ground, resulting in a loss of signal power. This current "clipping" causes compression behavior that can be shown, for instance, in a RF switch "Pout vs. Pin" plot. This is frequently characterized by P1dB, wherein the insertion loss is increased by 1.0 dB over the small-signal insertion loss. This is an obvious indication of nonlinearity of the switch. In accordance with the present disclosed method and apparatus, removing, reducing or otherwise controlling the accumulated charge increases the BVDSS point. Increases to the BVDSS point of the NMOSFET 528 commensurately increases the large-signal power handling of the switch. As an example, for a switch, doubling the BVDSS voltage of the ACC NMOSFET increases the P1dB point by 6 dB. This is a significant accomplishment as compared with the prior art RF switch designs.

0182 In addition, as described above in more detail, presence of the accumulated charge in SOI MOSFET body adversely impacts the magnitude of C_{off} and also takes time to form when the FET is switched from an on-state to an off-state. In terms of switch performance, the nonlinearity of C_{off} adversely impacts the overall switch linearity performance (as described above), and the magnitude of C_{off} adversely affects the small-signal performance parameters such as insertion loss, insertion phase (or delay), and isolation. By reducing the magnitude of C_{off} using the present disclosed method and apparatus, the switch (implemented with ACC MOSFETs) has reduced insertion loss due to lowered parasitic capacitance, reduced insertion phase (or delay), again due to lowered parasitic capacitance, and increased isolation due to less capacitive feedthrough.

0183 The ACC MOSFET also improves the drift characteristic of SOI MOSFETs as pertains to the drift of the small-signal parameters over a period of time. As the SOI MOSFET takes some time to accumulate the accumulated charge when the switch is off, the C_{off} capacitance is initially fairly small. However, over a period of time while operated in the accumulated charge regime, the off-state capacitance C_{off} increases toward a final value. The time it takes for the NMOSFET to reach a full accumulated charge state depends on the electron-hole pair (EHP) generation mechanism. Typically, this time period is on the order of approximately hundreds of milliseconds for thermal EHP generation at room temperature, for example. During this charge-up time period, the insertion loss and insertion phase increase. Also, during this time period, the isolation decreases. As is well known, these are undesirable phenomena in standard SOI MOSFET devices. These problems are alleviated or otherwise mitigated using the ACC NMOSFETs and related circuits described above.

0184 In addition to the above-described benefits afforded by the disclosed ACC MOSFET method and apparatus, the disclosed techniques also allow the implementation of SOI MOSFETs having improved temperature performance, improved sensitivity to V_{dd} variations, and improved sensitivity to process variations. Other improvements to the prior art SOI MOSFETs afforded by the present disclosed method and apparatus will be understood and appreciated by those skilled in the electronic device design and manufacturing arts.

Exemplary Fabrication Methods

0185 In one embodiment of the present disclosure, the exemplary RF switches described above may be implemented using a fully insulating substrate semiconductor-on-insulator (SOI) technology. Also, as noted above, in addition to the commonly used silicon-based systems, some embodiments of the present disclosure may be implemented using silicon-germanium (SiGe), wherein the SiGe is used equivalently in place of silicon.

0186 In some exemplary embodiments, the MOSFET transistors of the present disclosure may be implemented using "Ultra-Thin-Silicon (UTSi)" (also referred to herein as "ultrathin silicon-on-sapphire") technology. In accordance with UTSi manufacturing methods, the transistors used to implement the inventive methods disclosed herein are formed in an extremely thin layer of silicon in an insulating sapphire wafer. The fully insulating sapphire substrate enhances the performance characteristics of the inventive RF circuits by reducing the deleterious substrate coupling effects associated with non-insulating and partially insulating substrates. For example, insertion loss improvements may be realized by lowering the transistor on-state resistances and by reducing parasitic substrate conductance and capacitance. In addition, switch isolation is improved using the fully insulating substrates provided by UTSi technology. Owing to the fully insulating nature of silicon-on-sapphire technology, the parasitic capacitance between the nodes of the RF switches is greatly reduced as compared with bulk CMOS and other traditional integrated circuit manufacturing technologies.

0187 Examples of and methods for making silicon-on-sapphire devices that can be implemented in the MOSFETs and circuits described herein, are described in U.S. Patent Nos. 5,416,043 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); 5,492,857 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,572,040 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,596,205 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,600,169 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); 5,663,570 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,861,336 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,863,823 ("Self-aligned edge control in silicon on insulator"); 5,883,396 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"); 5,895,957 ("Minimum charge FET fabricated on an ultrathin silicon on sapphire wafer"); 5,920,233 ("Phase locked loop including a sampling circuit for reducing spurious side bands"); 5,930,638 ("Method of making a low parasitic resistor on ultrathin silicon on insulator"); 5,973,363 ("CMOS circuitry with shortened P-channel length on ultrathin silicon on insulator"); 5,973,382 ("Capacitor on ultrathin semiconductor on insulator"); and 6,057,555 ("High-frequency wireless communication system on a single ultrathin silicon on sapphire chip"). All of these referenced patents are incorporated herein in their entirety for their teachings on ultrathin silicon-on-sapphire integrated circuit design and fabrication.

0188 Similarly to other bulk and SOI CMOS processes, an SOS enhancement mode NMOSFET, suitable for some embodiments of the present disclosure, may, in some embodiments, be

fabricated with a p-type implant into the channel region with n-type source and drain regions, and may have a threshold voltage of approximately + 500 mV. The threshold voltage is directly related to the p-type doping level, with higher doping resulting in higher thresholds. Similarly, the SOS enhancement mode PMOSFET may, in some exemplary embodiments, be implemented with an n-type channel region and p-type source and drain regions. Again, the doping level defines the threshold voltage with higher doping resulting in a more negative threshold.

0189 In some exemplary embodiments, an SOS depletion-mode NMOSFET, suitable for some embodiments of the present disclosure, may be fabricated by applying the p-type channel-implant mask to the n-type transistor, resulting in a structure that has n-type channel, source, and drain regions and a negative threshold voltage of approximately - 500 mV. Similarly, in some exemplary embodiments, a suitable depletion-mode PMOSFET may be implemented by applying the n-type channel-implant mask to the p-type transistor, resulting in a structure that has p-type channel, source, and drain regions and a positive threshold voltage of approximately + 500 mV.

0190 As noted in the background section above, the present ACC MOSFET apparatus can also be implemented using any convenient semiconductor-on-insulator technology, included, but not limited to, silicon-on-insulator, silicon-on-sapphire, and silicon-on-bonded wafer technology. One such silicon-on-bonded wafer technique uses "direct silicon bonded" (DSB) substrates. Direct silicon bond (DSB) substrates are fabricated by bonding and electrically attaching a film of single-crystal silicon of differing crystal orientation onto a base substrate. Such implementations are available from the Silicon Genesis Corporation headquartered in San Jose, California. As described at the Silicon Genesis Corporation website (publicly available at "www.sigen.com"), silicon-on-bonded wafer techniques include the so-called NanoCleave™ bonding process which can be performed at room temperature. Using this process, SOI wafers can be formed with materials having substantially different thermal expansion coefficients, such as in the manufacture of Germanium-on-Insulator wafers (GeOI). Exemplary patents describing silicon-on-bonded wafer implementations are as follows: US Pat. No. 7,056,808, issued June 6, 2006 to Henley, et al.; US Pat. No. 6,969,668, issued November 29, 2005 to Kang, et al.; US Pat. No. 6,908,832, issued June 21, 2005 to Farrens et al.; US Pat. No. 6,632,724, issued Oct. 14, 2003 to Henley, et al. and US Pat. No. 6,790,747, issued September 14, 2004 to Henley, et al. All of the above-cited patents are incorporated by reference herein for their teachings on techniques and methods of fabricating silicon devices on bonded wafers.

0191 A reference relating to the fabrication of enhancement-mode and depletion-mode transistors in SOS is "CMOS/SOS/LSI Switching Regulator Control Device," Orndorff, R. and Butcher, D., Solid-State Circuits Conference, Digest of Technical Papers, 1978 IEEE International,

Volume XXI, pp. 234-235, February 1978. The "Orndorff" reference is hereby incorporated in its entirety herein for its techniques on the fabrication of enhancement-mode and depletion-mode SOS transistors.

Exemplary Results

5 **0192** Exemplary results that can be obtained using the disclosed method and apparatus for use in improving the linearity of MOSFETs are shown in FIGURES 10-19. The measured results are provided for a single pole, six throw (SP6T) RF switch. Those skilled in the art of RF switch circuit design shall understand that the results can be extended to any practical RF switch configuration, and therefore are not limited to the exemplary SP6T switch for which results are
10 shown.

0193 FIGURES 10-15 show harmonic performance versus Input Power for prior art devices and for ACC MOSFET devices made in accordance with the present disclosed method and apparatus. Switch circuits implemented with the ACC MOSFET of the disclosed method and apparatus have a third harmonic response that rises at a 3:1 slope (cube of the input) versus input
15 power on the log scale. Those skilled in the electronic device design arts shall appreciate that no input-power dependent dynamic biasing occurs with the improved RF switch designs made in accordance with the present disclosure. In contrast, prior art floating body FET harmonics disadvantageously do not follow a 3:1 slope. This is disadvantageous for small-signal third-order distortions such as IM3.

20 **0194** As shown in FIGURES 10-19, at a GSM maximum input power of +35 dBm, the 3fo is improved by 14 dB. This is shown in detail in FIGURE 11. Improvements in third order harmonic distortion is also applicable to all odd order responses, such as, for example, 5th order responses, 7th order responses, *etc.*

0195 Similar to 3fo, the second order response of the improved ACC MOSFET-
25 implemented RF switch follows a 2:1 slope (square of the input) whereas the prior art RF switch does not. This results in improved 2fo and IM2 performance at low input power, and roughly the same performance at +35 dBm.

0196 FIGURES 14 and 15 treat the performance under non 50-ohm loads. In this case, the load represents a 5:1 mismatch wherein the load impedance can be of any convenient value that
30 results in a reflection coefficient magnitude of 2/3. In the case of SOI MOSFETs, reflection coefficients that result in higher voltages cause the most severe problems. At 5:1 VSWR, the voltage

can be 1.667 X higher. Those skilled in the art may view this similarly by sweeping the input power up to higher voltages which equate to the mismatch conditions.

0197 FIGURES 10-19 illustrate that the improved RF switch, implemented with ACC MOSFETs made in accordance with the present disclosed method and apparatus, has improved large voltage handling capabilities as compared to the prior art RF switch implementations. As shown in FIGURES 10-19, the harmonics are approximately 20 dB at the worst mismatch phase angle. Transient harmonics are also shown. Those skilled in the art shall observe that the standard SP6T switch 3fo overshoots by several dB before reaching a final value. The improved SP6T switch made in accordance with the present disclosed method and apparatus does not exhibit such a time-dependency.

0198 FIGURE 16 shows insertion loss performance results achieved using the improved SP6T RF switch of the present teachings. It can be observed that the improved SP6T switch has slightly improved insertion loss (IL) performance characteristics. FIGURE 17 shows that isolation is also slightly improved using the present improved SP6T RF switch.

0199 FIGURE 18 shows IM3 performance which is a metric of the slightly nonlinear behavior of the RF switch. The IM3 performance is shown versus phase again due to a load mismatch in the system under test. As can be observed by reviewing FIGURE 18, the performance of the improved SP6T RF switch is improved by approximately 27 dB.

0200 Finally, FIGURE 19 is a summary table which also includes IM2 data. FIGURE 19 shows almost 20 dB improvement for a low frequency blocker and 11 dB for a high frequency blocker. In one exemplary application wherein the SP6T may be used, all IM products must fall below -105 dBm. The improved SP6T switch is the only RF switch manufactured at the time of filing the present application meeting this requirement.

0201 A number of embodiments of the present inventive concept have been described. Nevertheless, it will be understood that various modifications may be made without departing from the scope of the inventive teachings. For example, it should be understood that the functions described as being part of one module may in general be performed equivalently in another module. Also, as described above, all of the RF switch circuits can be used in bi-directionally, with output ports used to input signals, and *vice versa*. Furthermore, the present inventive teachings can be used in the implementation of any circuit that will benefit from the removal of accumulated charge from MOSFET bodies. The present teachings will also find utility in circuits wherein off-state transistors

must withstand relatively high voltages. Other exemplary circuits include DC-to-DC converter circuits, power amplifiers, and similar electronic circuits.

0202 Accordingly, it is to be understood that the concepts described herein are not to be limited by the specific illustrated embodiments, but only by the scope of the appended claims.

CLAIMS

What is claimed is:

1. An accumulated charge control (ACC) floating body MOSFET (ACC MOSFET), adapted to control nonlinear response of the MOSFET when the MOSFET is operated in an accumulated charge regime, comprising:
 - a) a MOSFET having a floating body, wherein the floating body MOSFET selectively operates in the accumulated charge regime, and wherein accumulated charge is present in the body of the floating body MOSFET when the MOSFET operates in the accumulated charge regime; and
 - b) an accumulated charge sink (ACS) operatively coupled to the body of the MOSFET, wherein the ACS removes or otherwise controls the accumulated charge in the MOSFET body.
2. The ACC MOSFET of Claim 1, wherein the MOSFET includes a gate, drain, source, and a gate oxide layer positioned between the gate and the body, and wherein the MOSFET operates in the accumulated charge regime when the MOSFET is operated in an off-state (non-conducting state), and wherein charge accumulates within the body in a region proximate the gate oxide.
3. The ACC MOSFET of Claim 2, wherein the MOSFET body includes a channel region including a gate modulated conductive channel between the source and the drain, and wherein the source, drain and channel have carriers of identical polarity when the MOSFET is operated in an on-state (conducting state), and wherein the MOSFET operates in the accumulated charge regime when the MOSFET is biased to operate in the off-state and when the accumulated charge has a polarity that is opposite to the polarity of the source, drain and channel carriers.
4. The ACC MOSFET of Claim 3, wherein the MOSFET comprises an NMOSFET device, and wherein the accumulated charge comprises holes having "P" polarity.
5. The ACC MOSFET of Claim 3, wherein the MOSFET comprises a PMOSFET device, and wherein the accumulated charge comprises electrons having "N" polarity.
6. The ACC MOSFET of Claim 4, wherein the MOSFET comprises an enhancement mode NMOSFET device.
7. The ACC MOSFET of Claim 4, wherein the MOSFET comprises a depletion mode NMOSFET device.

8. The ACC MOSFET of Claim 5, wherein the MOSFET comprises an enhancement mode PMOSFET device.
9. The ACC MOSFET of Claim 5, wherein the MOSFET comprises a depletion mode PMOSFET device.
10. The ACC MOSFET of Claim 1, wherein the MOSFET is fabricated in a semiconductor-on-insulator technology.
11. The ACC MOSFET of Claim 1, wherein the MOSFET is fabricated on a semiconductor-on-sapphire substrate.
12. The ACC MOSFET of Claim 10, wherein the semiconductor-on-insulator technology comprises silicon-germanium (SiGe) fabricated on an insulating substrate.
13. The ACC MOSFET of Claim 10, wherein the semiconductor-on-insulator technology comprises gallium arsenide (GaAs) fabricated on an insulating substrate.
14. The ACC MOSFET of Claim 1, wherein the MOSFET is fabricated in a semiconductor-on-bonded wafer technology.
15. The ACC MOSFET of Claim 14, wherein the MOSFET is fabricated on direct silicon bond substrates by bonding and electrically attaching a film of single-crystal silicon onto a base insulating substrate.
16. The ACC MOSFET of Claim 1, wherein the MOSFET has an inherent linearity characteristic, and wherein the linearity of the ACC MOSFET is improved by removing or otherwise reducing the accumulated charge from the MOSFET body.
17. The ACC MOSFET of Claim 15, wherein the MOSFET produces harmonic distortion and intermodulation (IMD) effects when implemented in a selected circuit, and wherein the improved linearity of the ACC MOSFET achieved by removing or otherwise reducing the accumulated charge also improves the harmonic distortion and IMD effects, and wherein removing or otherwise reducing the accumulated charge also improves power handling and voltage tolerances associated with the ACC MOSFET.
18. The ACC MOSFET of Claim 2, wherein the MOSFET has an inherent drain-to-source breakdown voltage (BVDSS) characteristic, and wherein the BVDSS characteristic of the ACC MOSFET is improved by removing or otherwise reducing the accumulated charge from the MOSFET body.

19. The ACC MOSFET of Claim 2, wherein the MOSFET has a drain-to-source off-state capacitance (C_{off}) when operated in the off-state (non-conducting state), and wherein the off-state capacitance (C_{off}) exhibits improved linearity characteristics by removing or otherwise reducing the accumulated charge from the MOSFET body.

20. The ACC MOSFET of Claim 19, wherein the off-state capacitance (C_{off}) has an inherent magnitude, and wherein the magnitude of the off-state capacitance (C_{off}) is decreased by removing or otherwise reducing the accumulated charge from the MOSFET body.

21. The ACC MOSFET of Claim 19, wherein the off-state capacitance (C_{off}) varies over time in a presence of a time varying drain-to-source bias voltage (V_{ds}), and wherein the variations of C_{off} over time are reduced by removing or otherwise reducing the accumulated charge from the MOSFET body.

22. The ACC MOSFET of Claim 19, wherein the off-state capacitance (C_{off}) varies over time as the accumulated charge accumulates in the MOSFET body, and wherein the variations of C_{off} over time are reduced by removing or otherwise reducing the accumulated charge from the MOSFET body.

23. The ACC MOSFET of Claim 1, wherein the ACS has an impedance greater than approximately 10^6 ohms.

24. The ACC MOSFET of Claim 1, wherein the ACS has an impedance less than approximately 10^6 ohms.

25. The ACC MOSFET of Claim 1, wherein the ACC MOSFET has an inherent power handling capability, and wherein the ACC MOSFET is capable of processing input signals having increased power levels by removing or otherwise reducing the accumulated charge from the MOSFET body.

26. An accumulated charge control floating body MOSFET (ACC MOSFET) adapted to control charge accumulated in the body of the MOSFET when the MOSFET is operated in an accumulated charge regime, comprising:

a) a gate, drain, source, floating body, and a gate oxide layer positioned between the gate and the floating body, wherein the ACC MOSFET operates in the accumulated charge regime when the MOSFET is operated in an off-state (non-conducting state) and charge accumulates within the body in a region proximate and underneath the gate oxide layer; and

b) a first accumulated charge sink (ACS) positioned proximate a first distal end of the floating body, wherein the ACS is in electrical communication with the floating body, and wherein the ACS removes or otherwise controls the accumulated charge in the ACC MOSFET body.

27. The ACC MOSFET of Claim 26, wherein the ACC MOSFET further comprises an electrical contact region positioned proximate to and in electrical communication with the first ACS, wherein the electrical contact region facilitates electrical coupling to the first ACS.

28. The ACC MOSFET of Claim 27, wherein the ACC MOSFET comprises an ACC NMOSFET, and wherein the source and drain both comprise N⁺ doped regions, the floating body and the first ACS both comprise P⁻ doped regions, and the electrical contact region comprises a P⁺ doped region.

29. The ACC MOSFET of Claim 27, wherein the ACC MOSFET comprises an ACC NMOSFET, and wherein the source and drain both comprise N⁺ doped regions, the floating body and the first ACS both comprise P⁻ doped regions, and the electrical contact region comprises an N⁺ doped region that acts as a diode connection to the first ACS thereby inhibiting positive current flow into the first ACS and into the floating body under selected bias voltage conditions.

30. The ACC MOSFET of Claim 27, wherein the ACC MOSFET comprises an ACC PMOSFET, and wherein the source and drain both comprise P⁺ doped regions, the floating body and the ACS both comprise N⁻ doped regions, and the electrical contact region comprises an N⁺ doped region.

31. The ACC MOSFET of Claim 27, wherein the ACC MOSFET comprises an ACC PMOSFET, and wherein the source and drain both comprise P⁺ doped regions, the floating body and the ACS both comprise N⁻ doped regions, and the electrical contact region comprises an P⁺ doped region that acts as a diode connection to the ACS thereby inhibiting positive current flow into the ACS and into the floating body under selected bias voltage conditions.

32. The ACC MOSFET of Claim 27, wherein the electrical contact region and the ACS are coextensive.

33. The ACC MOSFET of Claim 28, wherein the floating body and the ACS comprise a combined P⁻ doped region that may be fabricated in a single ion-implementation manufacturing step.

34. The ACC MOSFET of Claim 28, wherein the floating body and the ACS comprise separate P⁻ doped regions that are coupled together.

35. The ACC MOSFET of Claim 27, wherein the MOSFET body includes a channel region including a gate modulated conductive channel between the source and the drain, and wherein the

source, drain and channel have carriers of identical polarity when the ACC MOSFET is operated in an on-state (conducting state), and wherein the ACC MOSFET operates in the accumulated charge regime when the MOSFET is biased to operate in the off-state and when the accumulated charge has a polarity that is opposite to the polarity of the source, drain and channel carriers.

36. The ACC MOSFET of Claim 35, wherein the ACC MOSFET comprises an NMOSFET device, and wherein the accumulated charge comprises holes having "P" polarity.

37. The ACC MOSFET of Claim 35, wherein the MOSFET comprises a PMOSFET device, and wherein the accumulated charge comprises electrons having "N" polarity.

38. The ACC MOSFET of Claim 35, wherein the ACC MOSFET has a depleted or partially depleted channel region.

39. The ACC MOSFET of Claim 26, wherein the ACS has an impedance greater than approximately 10^6 ohms.

40. The ACC MOSFET of Claim 26, wherein the ACS has an impedance less than approximately 10^6 ohms.

41. The ACC MOSFET of Claim 26, wherein the ACS is positioned a selected distance away from the source and drain thereby reducing parasitic capacitance effects associated with the ACS.

42. The ACC MOSFET of Claim 26, wherein the ACS is coupled to the body at the first distal end of the floating body thereby reducing parasitic capacitance effects associated with the coupling of the ACS to the floating body.

43. The ACC MOSFET of Claim 26, wherein the floating body has a width exceeding approximately 10 μm .

44. The ACC MOSFET of Claim 26, wherein the ACC MOSFET includes a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS.

45. The ACC MOSFET of Claim 44, wherein the gate, drain, source and ACS terminals are coupled to their respective regions via low resistance contact regions.

46. The ACC MOSFET of Claim 44, wherein the ACC MOSFET is biased to operate in the accumulated charge regime by applying selected bias voltages to the source, drain and gate terminals,

and wherein accumulated charge is removed or otherwise controlled by coupling the ACS terminal to an accumulated charge sinking mechanism.

47. The ACC MOSFET of Claim 46, wherein the accumulated charge is removed or otherwise controlled by applying a selected bias voltage V_{ACS} to the ACS terminal when the ACC MOSFET operates in the accumulated charge regime.

48. The ACC MOSFET of Claim 47, wherein the ACC MOSFET comprises a depletion mode NMOSFET device, and wherein V_{ACS} is selected to be equal to or more negative than the lesser of the source bias voltage and the drain bias voltage.

49. The ACC MOSFET of Claim 27, wherein the electrical contact region is positioned a selected distance away from the source, drain and body, thereby reducing parasitic capacitance effects associated with the ACS.

50. The ACC MOSFET of Claim 35, further including a contact region overlap region positioned proximate a distal edge of the gate over the channel region of the body and over the gate oxide layer, wherein the overlap region ensures that all of the gate oxide layer is completely covered with dopant material that is the same as dopant material used to form the electrical contact region.

51. The ACC MOSFET of Claim 50, wherein the electrical contact region is positioned a selected distance away from the distal edge of the gate thereby reducing or eliminating a region of increased threshold voltage in the MOSFET associated with the proximity of the overlap region to the distal edge of the gate.

52. The ACC MOSFET of Claim 26, wherein the ACC MOSFET comprises a "T-gate" configured ACC MOSFET, and wherein the floating body forms a supporting member of the "T-gate" configured MOSFET and the first ACS forms a supported member of the "T-gate" configured MOSFET, and wherein the first ACS is positioned along the first distal end of the floating body and is in contact with at least some portion of the floating body.

53. The ACC MOSFET of Claim 52, wherein the ACC MOSFET further comprises an electrical contact region positioned proximate and in electrical communication with the ACS, wherein the electrical contact region facilitates electrical coupling to the ACS.

54. The ACC MOSFET of Claim 53, wherein the ACS has an impedance greater than approximately 10^6 ohms.

55. The ACC MOSFET of Claim 53, wherein the ACS has an impedance less than approximately 10^6 ohms.

56. The ACC MOSFET of Claim 26, wherein the ACC MOSFET comprises an "H-gate" configured ACC MOSFET, wherein the H-gate configured MOSFET includes the first and a second ACS positioned proximate the first and a second distal end of the floating body, respectively, and wherein the first and second ACSs are positioned on opposite ends of the floating body, and wherein the first ACS has an associated and respective first electrical contact region positioned proximate thereto and in electrical communication therewith, and wherein the second ACS has an associated and respective second electrical contact region positioned proximate thereto and in electrical communication therewith, and wherein the first and second ACSs are in electrical communication with the floating body.

57. The ACC MOSFET of Claim 56, wherein the ACC MOSFET has a width, and wherein the first and second ACSs extend approximately the entire width of the ACC MOSFET.

58. The ACC MOSFET of Claim 57, wherein the first and second ACSs extend beyond the width of the ACC MOSFET.

59. The ACC MOSFET of Claim 57, wherein the first and second ACSs do not extend to the width of the ACC MOSFET.

60. The ACC MOSFET of Claim 56, wherein the first and second ACSs have identical impedances.

61. The ACC MOSFET of Claim 60, wherein the impedances of the first and second ACSs differ from one another.

62. The ACC MOSFET of Claim 56, wherein the first electrical contact region is positioned a first selected distance away from the floating body, and wherein the second electrical contact region is positioned a second selected distance away from the floating body.

63. The ACC MOSFET of Claim 62, wherein the first and second selected distances are identical.

64. The ACC MOSFET of Claim 62, wherein the first and second selected distances differ from one another.

65. The ACC MOSFET of Claim 56, wherein the ACSs are approximately rectangular.

66. The ACC MOSFET of Claim 56, wherein the ACSs are approximately circular.

67. The ACC MOSFET of Claim 56, wherein the ACSs are approximately square.

68. A four-terminal accumulated charge control floating body MOSFET (ACC MOSFET) device, adapted to control charge accumulated in the body of the MOSFET when the MOSFET is operated in an accumulated charge regime, comprising:

a) a gate, drain, source, floating body, and a gate oxide layer positioned between the gate and the floating body, wherein the ACC MOSFET operates in the accumulated charge regime when the MOSFET is operated in an off-state (non-conducting state) and charge accumulates within the body in a region proximate and underneath the gate oxide layer;

b) an accumulated charge sink (ACS) positioned proximate a distal end of the floating body, wherein the ACS is in electrical communication with the floating body; and

c) a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS;

wherein the charge accumulated in the body is controlled or removed from the body via the ACS terminal when the MOSFET operates in the accumulated charge regime.

69. The four-terminal ACC MOSFET of Claim 68, wherein the gate and ACS terminals are electrically coupled together.

70. The four-terminal ACC MOSFET of Claim 69, wherein the accumulated charge is removed from the body via the ACS and gate terminals when the ACC MOSFET device is biased to operate in the accumulated charge regime.

71. The four-terminal ACC MOSFET of Claim 69, wherein a diode is coupled between the gate and ACS terminals such that the diode prevents positive current flow into the ACC MOSFET body when the MOSFET is operated in an on-state (conducting state) condition and the diode is reverse-biased.

72. The four-terminal ACC MOSFET of Claim 71, wherein the diode has an associated voltage drop across the diode, and wherein the voltage drop across the diode may be selectively reduced by increasing a width of the diode.

73. The four-terminal ACC MOSFET of Claim 68, wherein the ACS terminal is coupled to an accumulated charge sinking mechanism.

74. The four-terminal ACC MOSFET of Claim 73, wherein the ACS accumulated charge sinking mechanism comprises a control circuit adapted to control or remove the accumulated charge from the body when the ACC MOSFET operates in the accumulated charge regime.

75. The four-terminal ACC MOSFET of Claim 73, wherein the accumulated charge sinking mechanism produces a selectable accumulated charge sink bias voltage (V_{ACS}), and wherein the V_{ACS} is selected such that the accumulated charge is removed from the body when the ACC MOSFET operates in the accumulated charge regime.

76. The four-terminal ACC MOSFET of Claim 75, wherein the accumulated charge sink bias voltage V_{ACS} is driven by a source having a relatively high impedance.

77. The four-terminal ACC MOSFET of Claim 76, wherein the accumulated charge sink bias voltage V_{ACS} is driven by a source having an impedance greater than approximately 10^6 ohms.

78. The four-terminal ACC MOSFET of Claim 75, wherein the gate, drain and source have associated and respective gate (V_g), drain (V_d) and source (V_s) bias voltages, and wherein the ACS bias voltage V_{ACS} is selected to be equal to or more negative than the lesser of both V_s and V_d , thereby conveying the accumulated rhetorical charge from the body when the MOSFET operates in the accumulated charge regime.

79. The four-terminal ACC MOSFET of Claim 68, wherein the gate and ACS terminals are electrically coupled together via a clamping circuit configured in series between the ACS and gate terminals.

80. The four-terminal ACC MOSFET of Claim 79, wherein the clamping circuit limits the flow of current from the ACS terminal during the accumulated charge regime thereby ensuring that the accumulated charge is controlled or removed from the MOSFET body during the accumulated charge regime.

81. The four-terminal ACC MOSFET of Claim 79, wherein the clamping circuit comprises a depletion-mode MOSFET configured in series between the ACS terminal and the gate terminal.

82. The four-terminal ACC MOSFET of Claim 81, wherein the depletion-mode MOSFET has a selected saturation current, and wherein the saturation current limits the flow of current from the ACS terminal during the accumulated charge regime.

83. The four-terminal ACC MOSFET of Claim 82, wherein the depletion-mode MOSFET enters saturation upon reaching a predefined threshold, and wherein the saturation current is selected by setting the threshold to a desired value.

84. The four-terminal ACC MOSFET of Claim 81, wherein the clamping circuit further comprises a diode configured in series with the depletion-mode MOSFET.

85. The four-terminal ACC MOSFET of Claim 71, further comprising an AC shorting capacitor coupled in parallel across the diode, wherein the AC shorting capacitor ensures that nonlinearity characteristics of the diode are not excited when AC signals present across the diode.

86. An RF switch circuit for switching RF signals, comprising:

- a) a first RF port capable of outputting or receiving a first RF signal;
- b) a second RF port capable of outputting or receiving a second RF signal;
- c) a switch transistor grouping having a first node coupled to the first RF port and a second node coupled to the second RF port, wherein the switch transistor grouping is controlled by a first switch control signal (C1); and
- d) a shunt transistor grouping having a first node coupled to the first RF port and a second node coupled to ground, wherein the shunt transistor grouping is controlled by a second switch control signal (C1x), and wherein the shunt transistor grouping comprises one or more ACC MOSFETs defined by Claim 2;

and wherein when the first switch control signal C1 is enabled, the switch transistor grouping is enabled and the shunt transistor grouping is disabled thereby electrically coupling the first RF port to the second RF port, and wherein when the second switch control signal C1x is enabled, the shunt transistor grouping is enabled while the switch transistor grouping is disabled thereby shunting the first RF port to ground.

87. The RF switch of Claim 86, wherein the switch transistor grouping comprises a single MOSFET, and wherein the shunt transistor grouping comprises a single ACC MOSFET.

88. The RF switch of Claim 86, wherein the switch transistor grouping comprises a plurality of MOSFETs arranged in a stacked configuration, and wherein the shunt transistor grouping comprises a plurality of ACC MOSFETs arranged in a stacked configuration.

89. The RF switch of Claim 88, wherein the switch transistor grouping comprises a first number of MOSFETs arranged in a stacked configuration, and wherein the shunt transistor grouping comprises a second number of ACC MOSFETs arranged in a stacked configuration, and wherein the first number and the second number differ from one another.

90. The RF switch of Claim 86, wherein the ACC MOSFET includes a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS, and wherein the gate and ACS terminals are electrically coupled together and also coupled to the second switch control signal C1x, and wherein the accumulated charge is removed from the body of the ACC MOSFET through the ACS and gate terminals.

91. The RF switch of Claim 90, wherein the switch transistor grouping comprises a single MOSFET, and wherein the shunt transistor grouping comprises a single ACC MOSFET.

92. The RF switch of Claim 90, wherein the switch transistor grouping comprises a plurality of MOSFETs arranged in a stacked configuration, and wherein the shunt transistor grouping comprises a plurality of ACC MOSFETs arranged in a stacked configuration.

93. The RF switch of Claim 90, wherein the RF switch exhibits harmonic distortion, intermodulation distortion (IMD) and linearity performance characteristics under operation, and wherein the RF switch is capable of processing RF signals of a selected power level, and wherein the harmonic distortion, IMD, linearity characteristics, and power level processing of the RF switch are improved by removal or control of the accumulated charge from the body of the shunt transistor grouping.

94. The RF switch of Claim 93, wherein the harmonic and intermodulation distortion of an RF output signal is reduced or eliminated by the removal or control of the accumulated charge from the body of the shunt transistor grouping.

95. The RF switch of Claim 90, wherein a diode is coupled between the gate and ACS terminals such that the diode prevents positive current flow into the ACC MOSFET body when the ACC MOSFET is enabled and the diode is reverse-biased, and wherein the ACS terminal is coupled to the second switch control signal C1x via the diode, and wherein the accumulated charge is removed from the body of the ACC MOSFET through the ACS terminal.

96. The RF switch of Claim 95, wherein the switch transistor grouping comprises a single MOSFET, and wherein the shunt transistor grouping comprises a single ACC MOSFET.

97. The RF switch of Claim 85, wherein the switch transistor grouping comprises a plurality of MOSFETs arranged in a stacked configuration, and wherein the shunt transistor grouping comprises a plurality of ACC MOSFETs arranged in a stacked configuration.

98. The RF switch of Claim 86, wherein the ACC MOSFET includes a gate terminal electrically coupled to the gate, a drain terminal electrically coupled to the drain, a source terminal electrically coupled to the source, and an ACS terminal electrically coupled to the ACS, and wherein the ACS terminal is electrically coupled to an accumulated charge sinking mechanism, and wherein the sinking mechanism comprises a control circuit adapted to control or remove the accumulated charge from the body when the shunt transistor grouping operates in the accumulated charge regime.

99. The RF switch of Claim 98, wherein the switch transistor grouping comprises a single MOSFET, and wherein the shunt transistor grouping comprises a single ACC MOSFET.

100. The RF switch of Claim 98, wherein the switch transistor grouping comprises a plurality of MOSFETs arranged in a stacked configuration, and wherein the shunt transistor grouping comprises a plurality of ACC MOSFETs arranged in a stacked configuration.

101. The RF switch of Claim 98, wherein the ACS terminal of the shunt transistor grouping is coupled to a third switch control signal (C2), and wherein the shunt transistor grouping is enabled by the second switch control signal C1x while the switch transistor grouping is disabled thereby shunting the first RF port to ground, and wherein the accumulated charge is removed from the body of the ACC MOSFET when the shunt transistor grouping is disabled.

102. The RF switch of Claim 95, wherein the RF switch exhibits harmonic distortion, intermodulation distortion (IMD) and linearity performance characteristics under operation, and wherein the RF switch is capable of processing RF signals of a selected power level, and wherein the harmonic distortion, IMD, linearity characteristics, and power level processing of the RF switch are improved by removal or control of the accumulated charge from the body of the shunt transistor grouping.

103. The RF switch of Claim 98, wherein the RF switch exhibits harmonic distortion, intermodulation distortion (IMD) and linearity performance characteristics under operation, and wherein the RF switch is capable of processing RF signals of a selected power level, and wherein the harmonic distortion, IMD, linearity characteristics, and power level processing of the RF switch are improved by removal or control of the accumulated charge from the body of the shunt transistor grouping.

104. The RF switch of Claim 90, wherein the switch transistor grouping comprises one or more ACC MOSFETs defined by Claim 2.

105. The RF switch of Claim 95, wherein the switch transistor grouping comprises one or more ACC MOSFETs defined by Claim 2.

106. The RF switch of Claim 98, wherein the switch transistor grouping comprises one or more ACC MOSFETs defined by Claim 2.

107. The RF switch of Claim 90, wherein the RF switch comprises a single-pole, multi-throw switch.

108. The RF switch of Claim 95, wherein the RF switch comprises a single-pole, multi-throw switch.

109. The RF switch of Claim 98, wherein the RF switch comprises a single-pole, multi-throw switch.

110. The RF switch of Claim 90, wherein the RF switch comprises a multi-pole, single-throw switch.

111. The RF switch of Claim 95, wherein the RF switch comprises a multi-pole, single-throw switch.

112. The RF switch of Claim 98, wherein the RF switch comprises a multi-pole, single-throw switch.

113. The RF switch of Claim 90, wherein the RF switch comprises a multi-pole, multi-throw switch.

114. The RF switch of Claim 95, wherein the RF switch comprises a multi-pole, multi-throw switch.

115. The RF switch of Claim 98, wherein the RF switch comprises a multi-pole, multi-throw switch.

116. A method of controlling the linearity characteristics of a floating body MOSFET, wherein the floating body MOSFET includes an accumulated charge sink (ACS) operatively coupled to the body of the MOSFET and adapted to remove or otherwise control accumulated charge that accumulates in the MOSFET body when the MOSFET is operated in a off-state (non-conducting state), comprising:

- a) configuring the floating body MOSFET to operate in a selected circuit;
- b) biasing the floating body MOSFET to operate in an accumulated charge regime; and
- c) removing or otherwise controlling the accumulated charge.

117. The method of Claim 116, wherein the step b) of biasing the MOSFET to operate in the accumulated charge regime comprises biasing the MOSFET into the off-state.

118. The RF switch of Claim 90, wherein the ACC MOSFET further includes a drain-to-source resistor (R_{ds}) electrically coupled between the drain and source of the ACC MOSFET.

119. The RF switch of Claim 118, wherein the drain-to-source resistor (R_{ds}) provides a path between the ACC MOSFET drain and source whereby current associated with controlling the accumulate

charge is conducted away from the source and drain when the ACC MOSFET is configured in series with other high impedance elements.

120. The RF switch of Claim 119, wherein the gate of the ACC MOSFET is coupled to a gate resistor, and wherein the drain-to-source resistor (R_{ds}) has an impedance approximately equal to the impedance of the gate resistor.

121. The RF switch of Claim 92, wherein the ACC MOSFETs further include a plurality of drain-to-source resistors (R_{ds}) associated with and respective to each of the stacked ACC MOSFETs, on a one-to-one basis, wherein each of the drain-to-source resistors are electrically coupled between the drain and source of each of their associated and respective ACC MOSFETs, and wherein the gates of each of the respective ACC MOSFETs are coupled to associated and respective gate resistors, and wherein the drain-to-source resistors (R_{ds}) of each associated and respective ACC MOSFET in the stack has an impedance approximately equal to the impedance of its associated and respective gate resistor divided by a number of ACC MOSFETs in the stack.

122. An RF switch circuit for switching RF signals, comprising:

- a) a first RF port capable of receiving or outputting a first RF signal (RF1);
- b) a second RF port capable receiving or outputting a second RF signal (RF2);
- c) an RF common port;
- d) a first switch transistor grouping having a first node coupled to the first RF port and a second node coupled to the RF common port, wherein the first switch transistor grouping is controlled by a first switch control signal (C1);
- e) a second switch transistor grouping having a first node coupled to the second RF port and a second node coupled to the RF common port, wherein the second switch transistor grouping is controlled by a second switch control signal (C1x);
- f) a first shunt transistor grouping having a first node coupled to the second RF port and a second node coupled to ground, wherein the first shunt transistor grouping is controlled by the first switch control signal C1; and
- g) a second shunt transistor grouping having a first node coupled to the first RF port and a second node coupled to ground, wherein the second shunt transistor grouping is controlled by the second switch control signal C1x,

wherein, when C1 is enabled, the first switch and first shunt transistor groupings are enabled while the second switch and shunt transistor groupings are disabled, thereby electrically coupling the first RF port with the RF common port and shunting the second RF port to ground, and wherein when C1 is disabled and C1x is enabled, the second switch and shunt transistor groupings are enabled while the first switch and shunt transistor groupings are disabled, thereby electrically coupling the second

RF port with the RF common port and shunting the first RF port to ground, and wherein the switch and shunt transistor groupings comprise one or more ACC MOSFETs defined by Claim 1.

123. The RF switch of Claim 122, wherein each of the ACC MOSFETs include an ACS terminal in electrical communication with their respective and associated ACSs, and wherein the ACS terminals of each of the ACC MOSFETs are controlled by a sinking mechanism, and wherein the sinking mechanism removes accumulated charge from the ACC MOSFET bodies when the ACC MOSFETs operate in the accumulated charge regime.

124. The RF switch of Claim 123, wherein the RF switch exhibits harmonic distortion, intermodulation distortion (IMD) and linearity performance characteristics under operation, and wherein the RF switch is capable of processing RF signals of a selected power level, and wherein the harmonic distortion, IMD, linearity characteristics, and power level processing of the RF switch are improved by removal or control of the accumulated charge from the bodies of the ACC MOSFETs.

125. The RF switch of Claim 123, wherein the ACC MOSFETs inherent drain-to-source breakdown voltage (BVDSS) characteristics, and wherein the BVDSS characteristics of the ACC MOSFETs are improved by removing or otherwise reducing the accumulated charge from the MOSFET bodies.

126. The RF switch of Claim 123, wherein the RF switch exhibits small-signal performance characteristics including insertion loss, insertion phase (delay), and isolation, and wherein the small-signal performance characteristics of the RF switch are improved by removal and control of the accumulated charge from the ACC MOSFET bodies.

127. The RF switch of Claim 123, wherein the RF switch includes associated temperature performance characteristics, and wherein the temperature performance characteristics of the RF switch are improved by removal and control of the accumulated charge from the ACC MOSFET bodies, and wherein the RF switch also exhibits decreased sensitivity to Vdd and fabrication process variations.

128. The RF switch of Claim 122, wherein the RF switch comprises a single-pole, multi-throw switch.

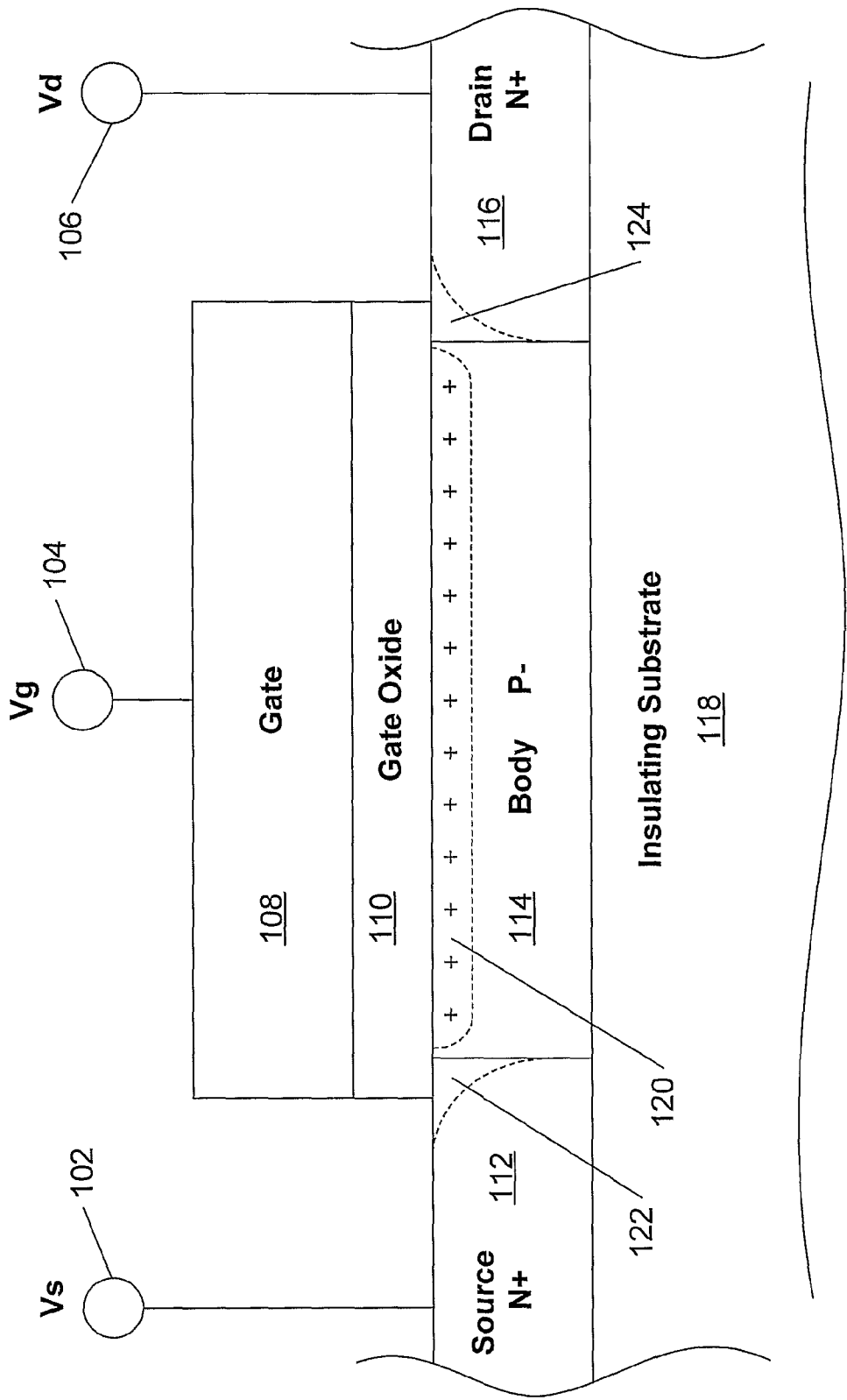
129. The RF switch of Claim 122, wherein the RF switch comprises a multi-pole, single-throw switch.

130. The RF switch of Claim 122, wherein the RF switch comprises a multi-pole, multi-throw switch.

131. The ACC MOSFET of Claim 1, wherein the MOSFET is fabricated in a silicon-on-insulator technology.

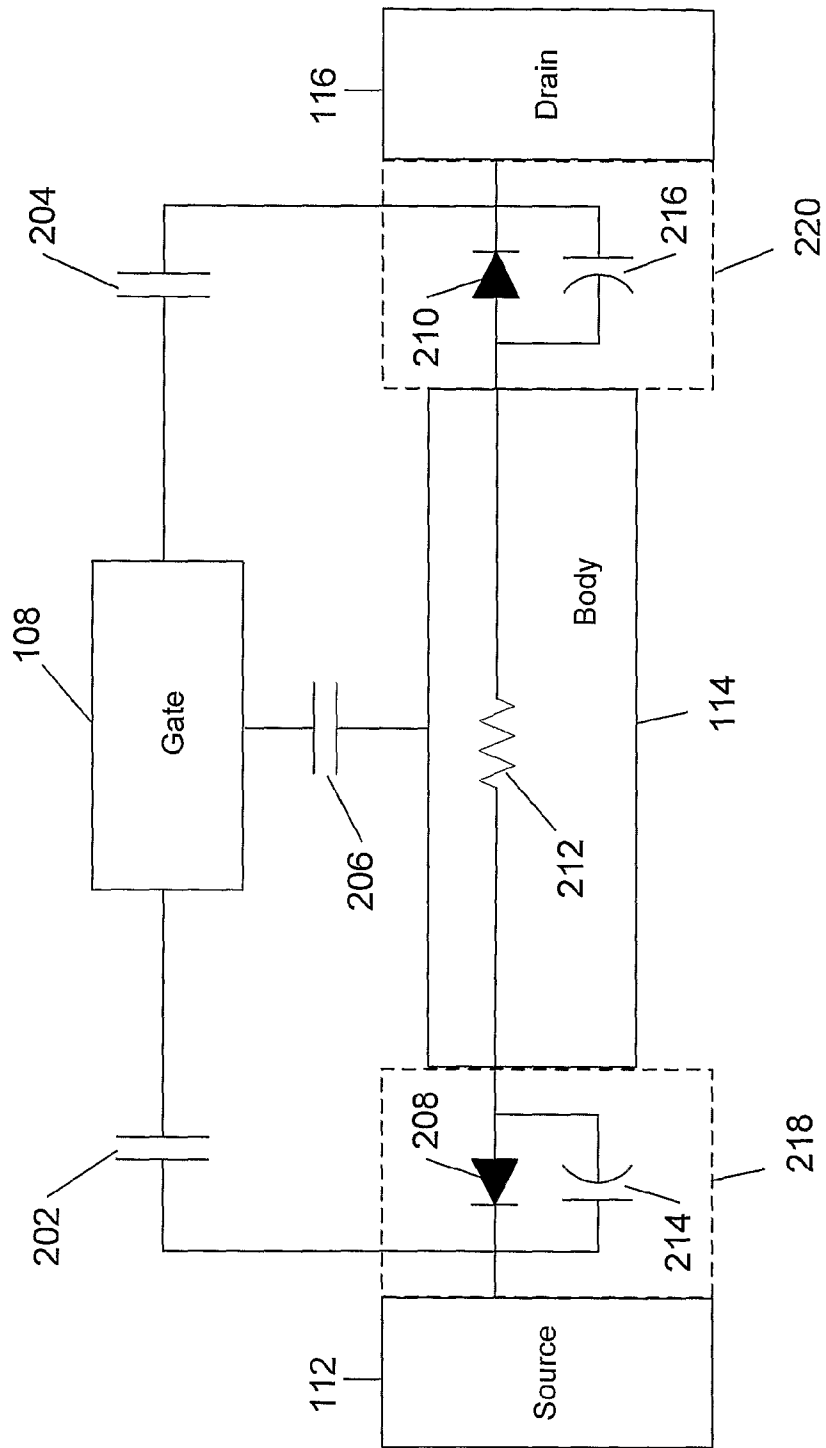
132. The RF switch of Claim 86, wherein the RF switch exhibits harmonic distortion, intermodulation distortion (IMD) and linearity performance characteristics under operation, and wherein the RF switch is capable of processing RF signals of a selected power level, and wherein the harmonic distortion, IMD, linearity characteristics, and power level processing of the RF switch are improved by removal or control of the accumulated charge from the body of the shunt transistor grouping.

133. The RF switch of Claim 86, wherein the RF switch comprises a single-pole, multi-throw switch.



100

Figure 1 (Prior Art)



200

Figure 2A

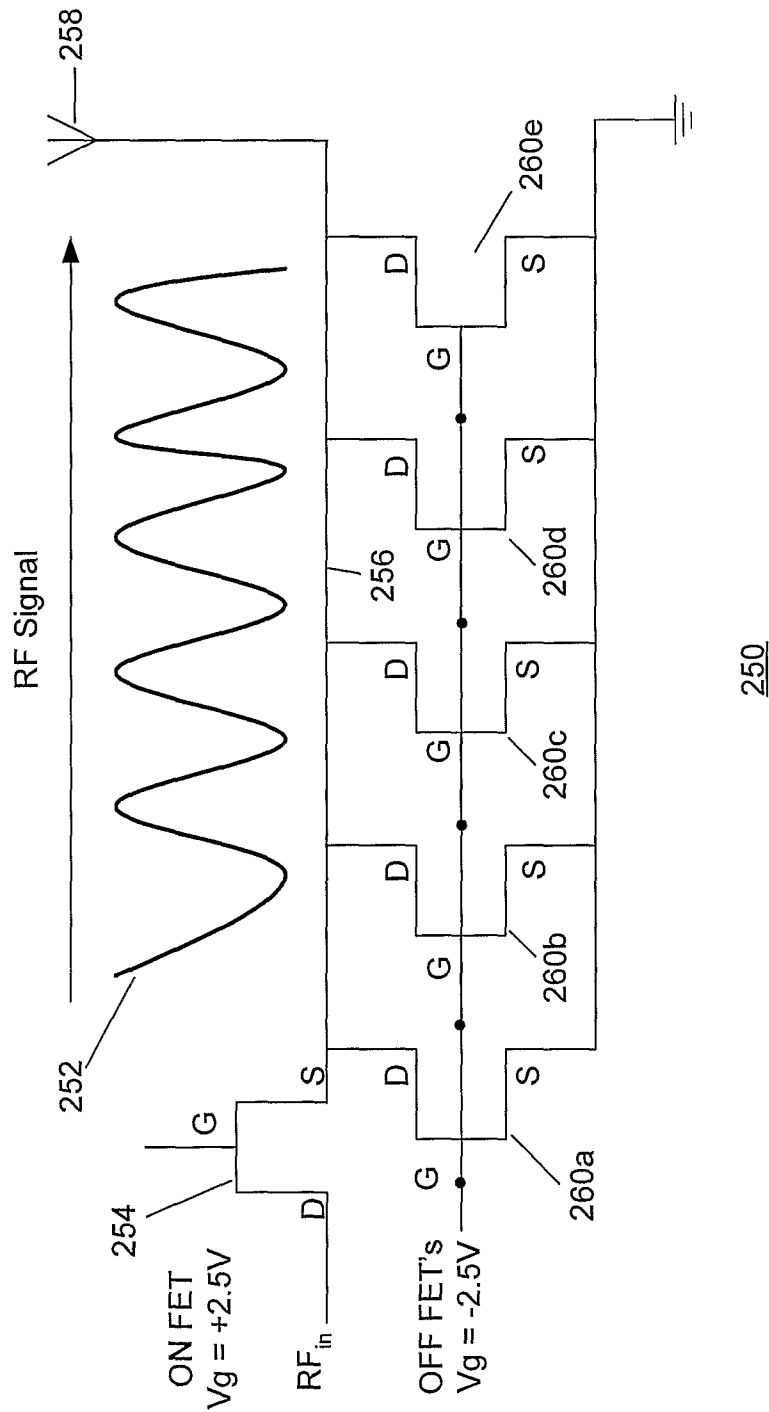
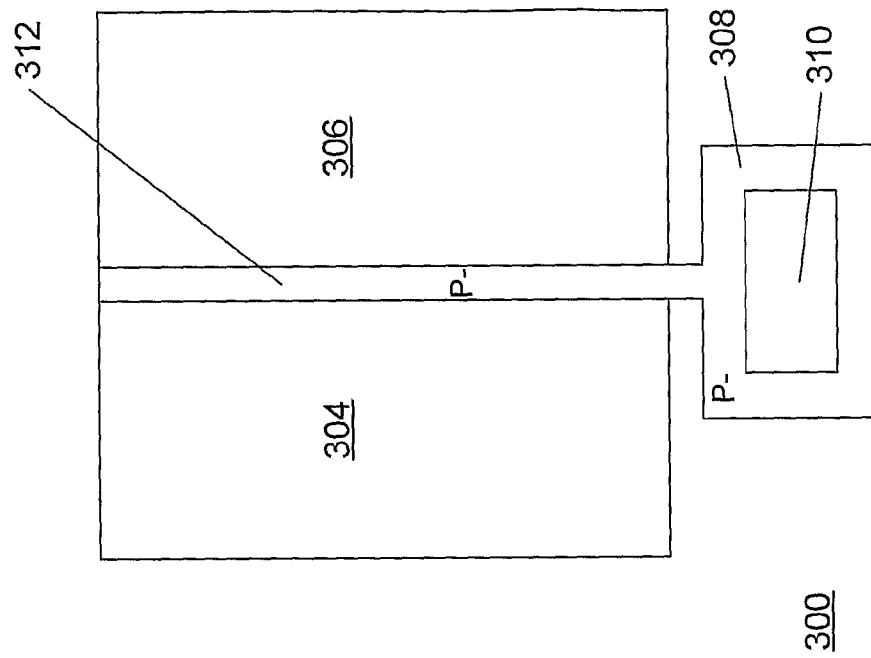
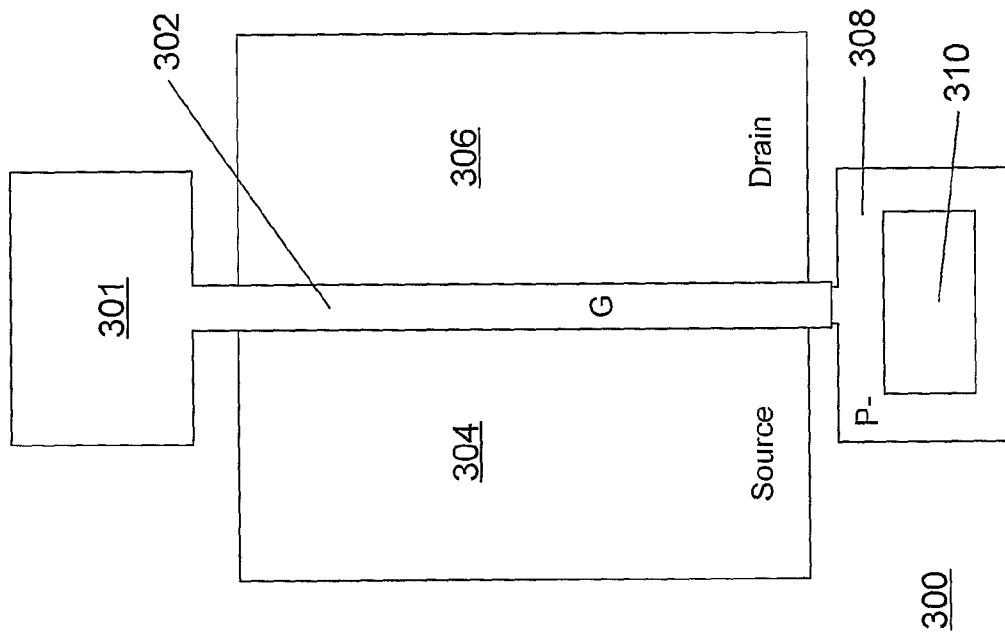


FIGURE 2B



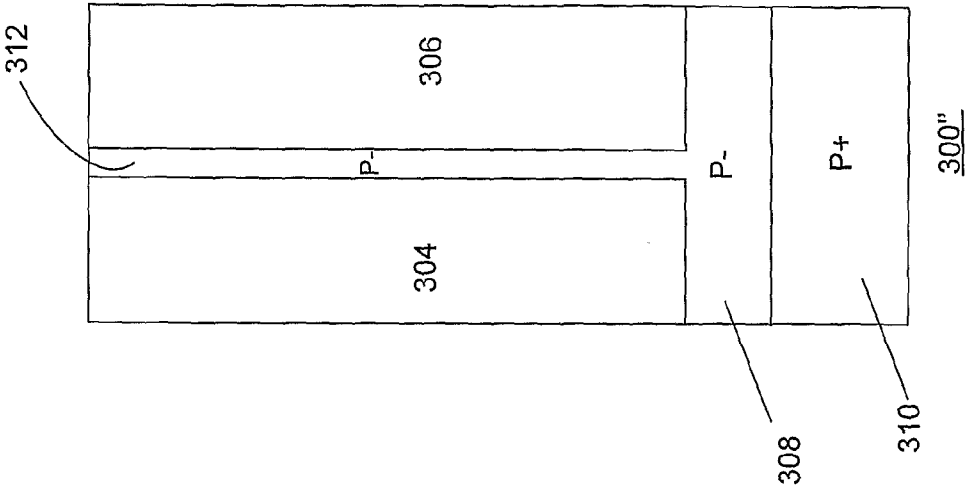


Figure 3D

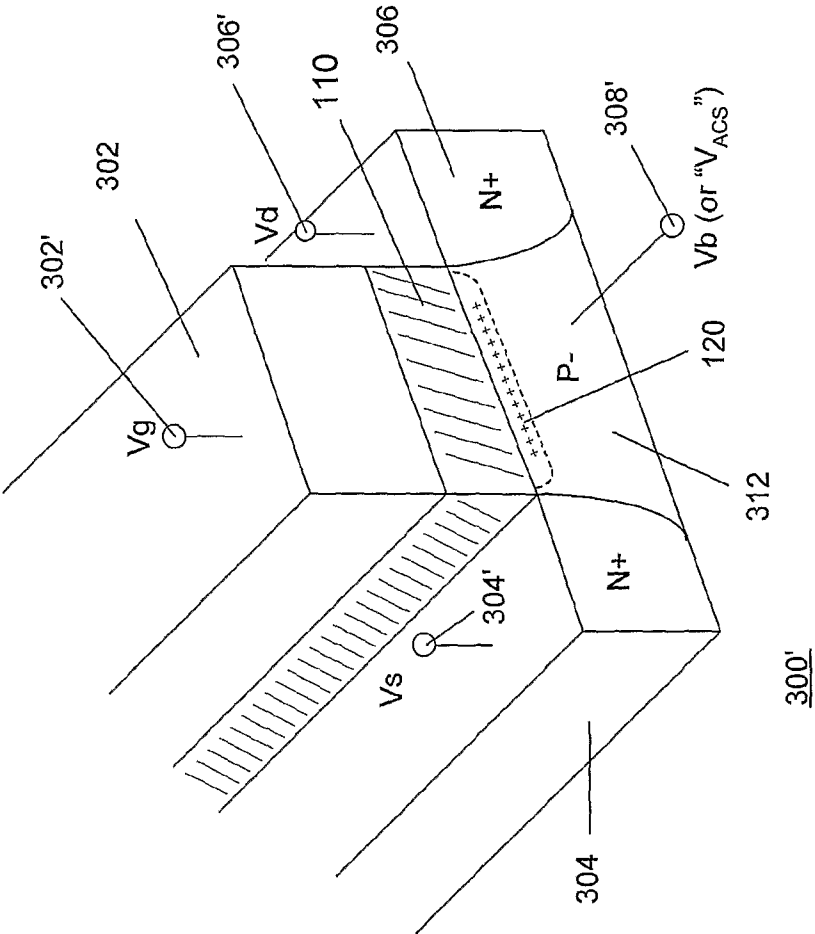


Figure 3C

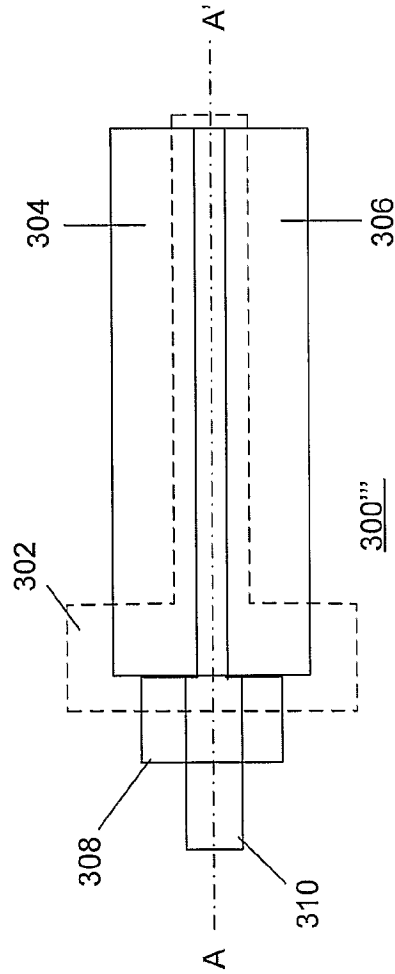


Figure 3E

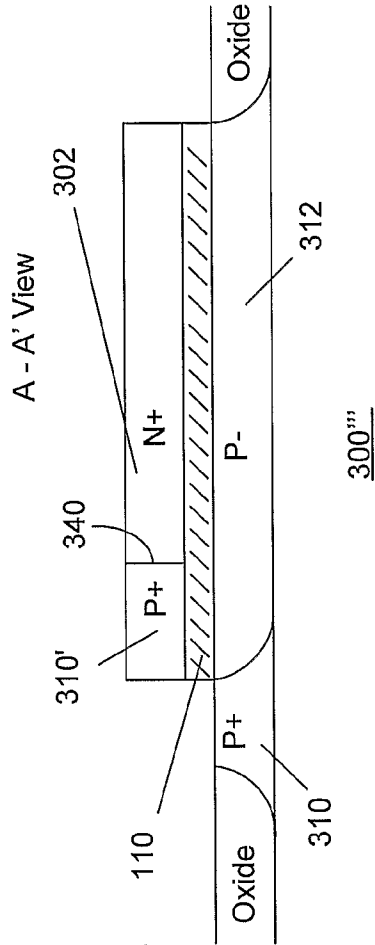


Figure 3F

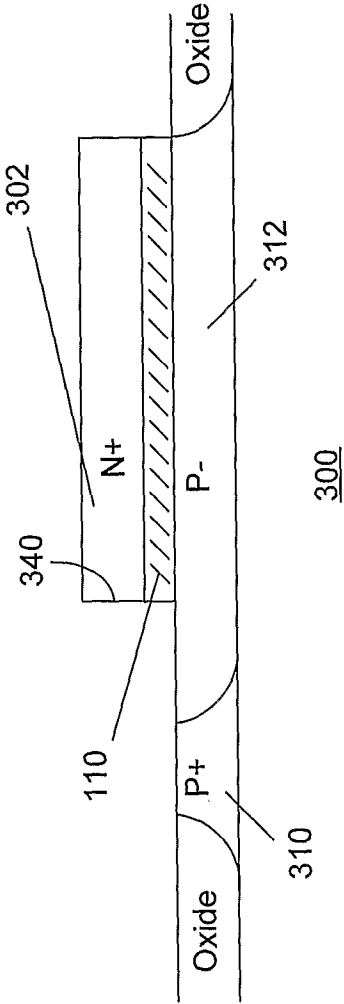


Figure 3G

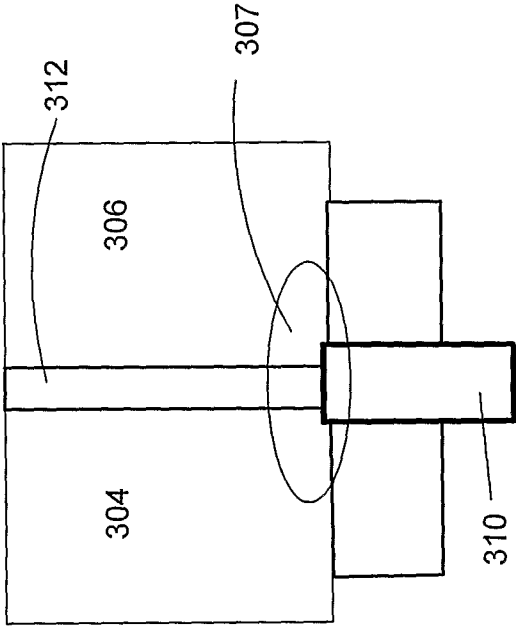
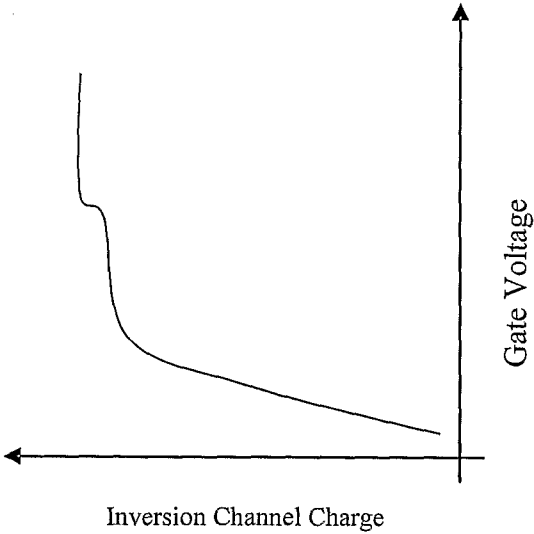


Figure 3H



380

Figure 3I

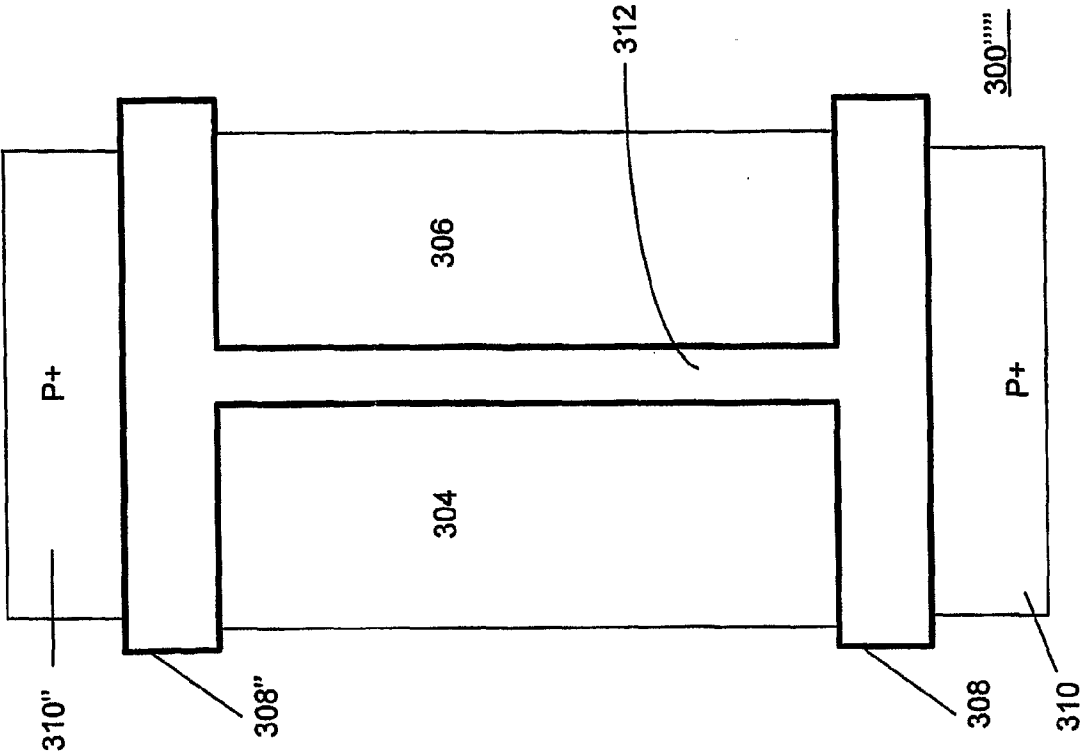


Figure 3J

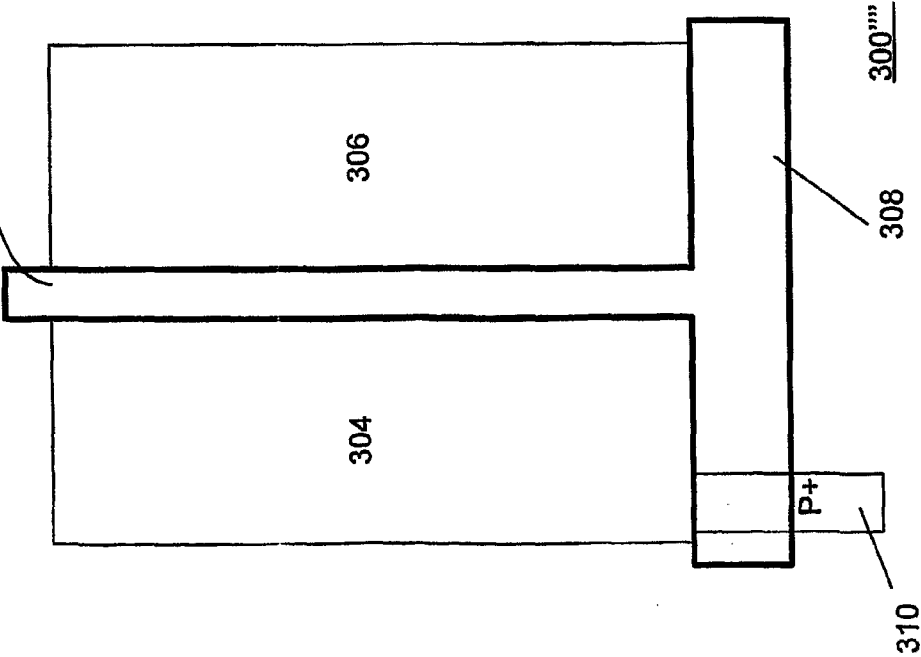


Figure 3K

Figure 4A

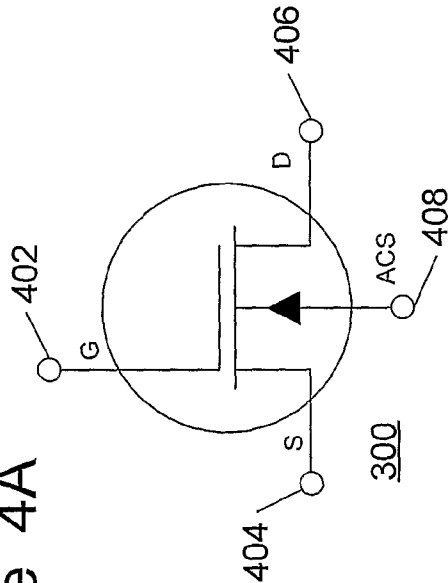


Figure 4B

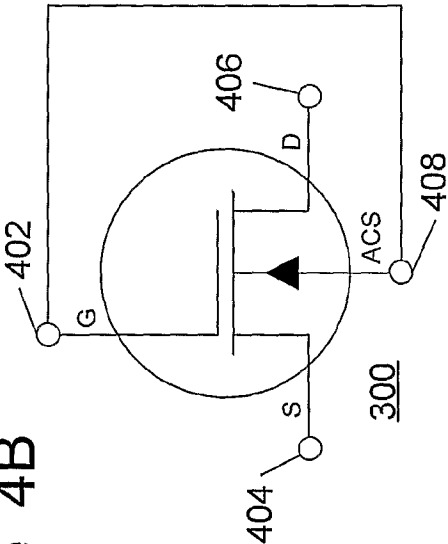


Figure 4C

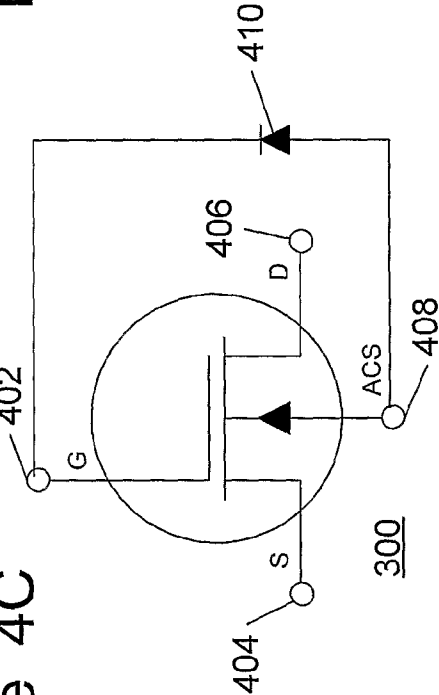
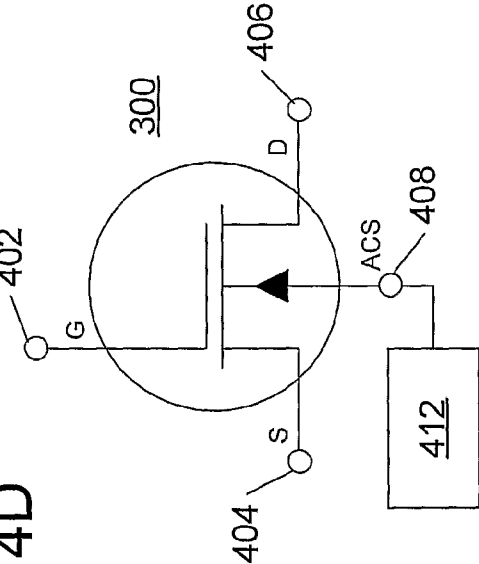


Figure 4D



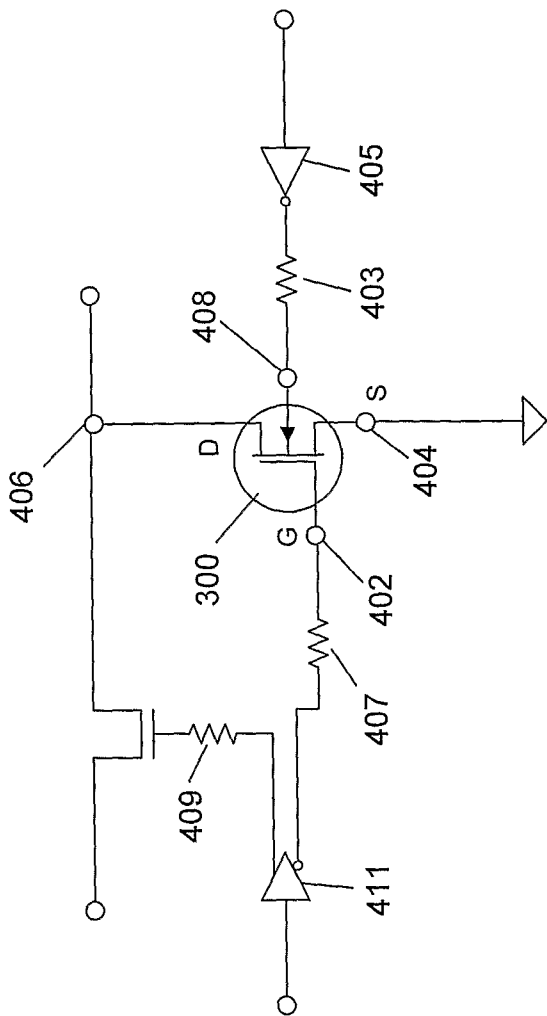


Figure 4E

Figure 4G

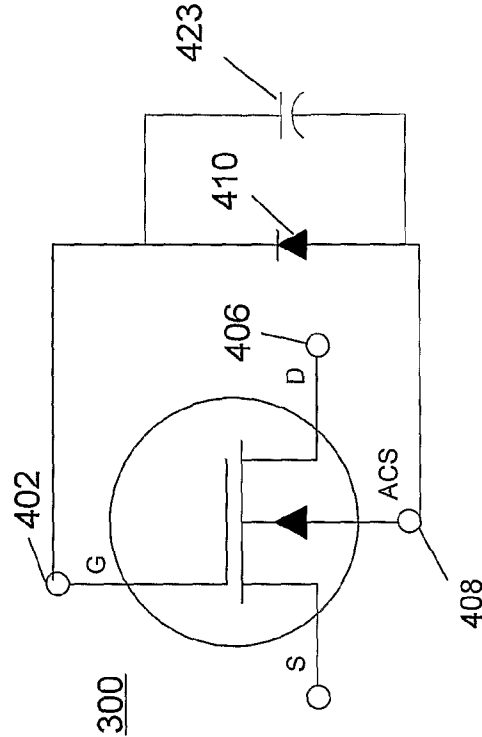
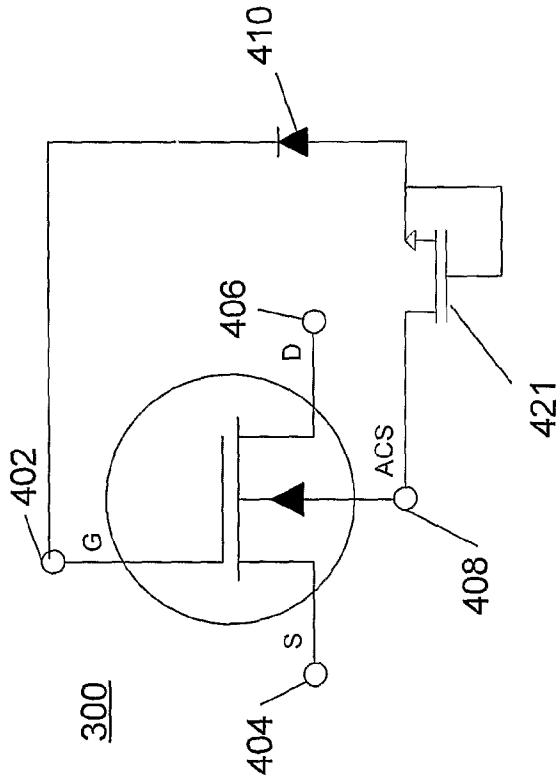


Figure 4F



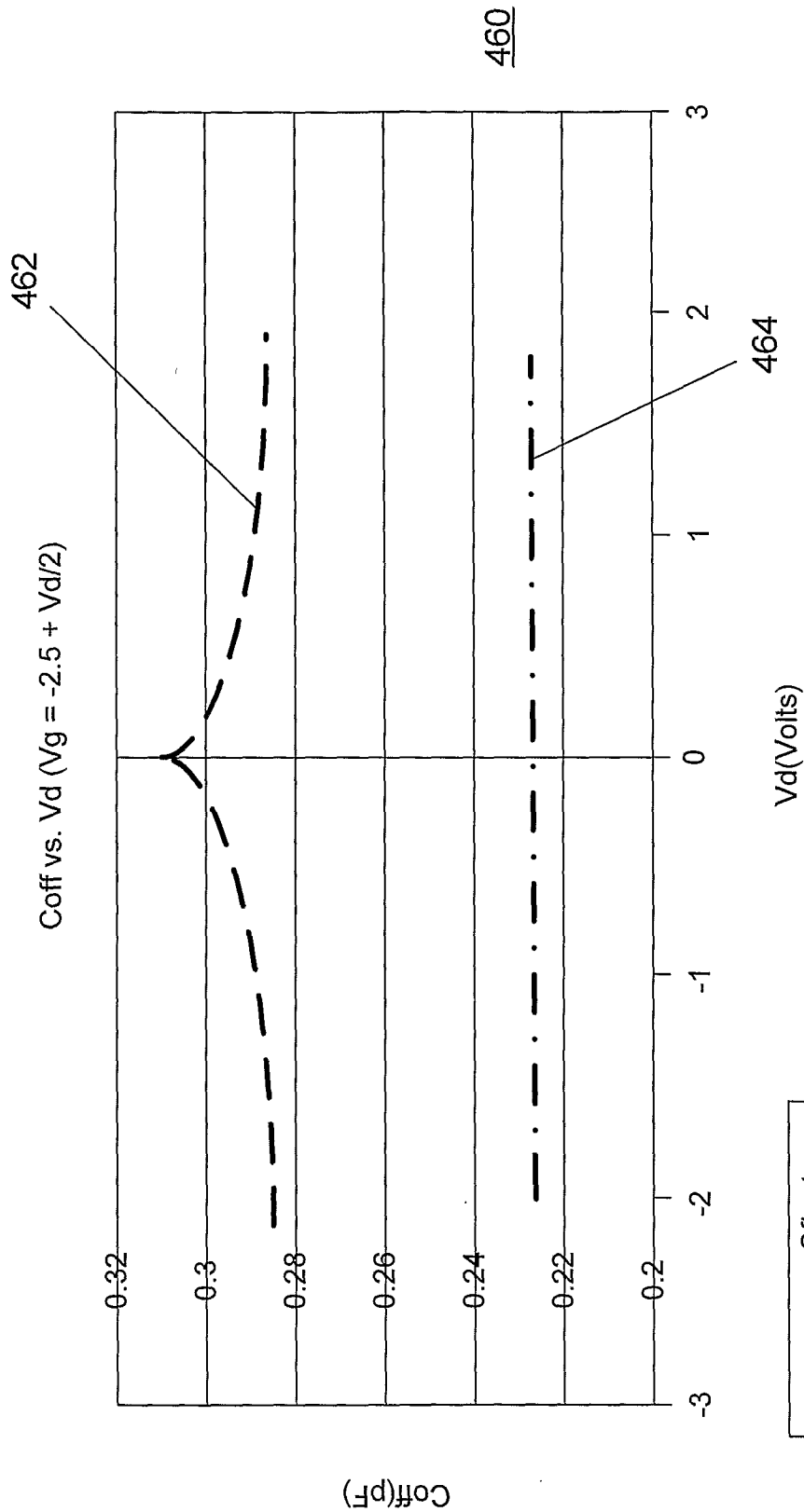


Figure 4H

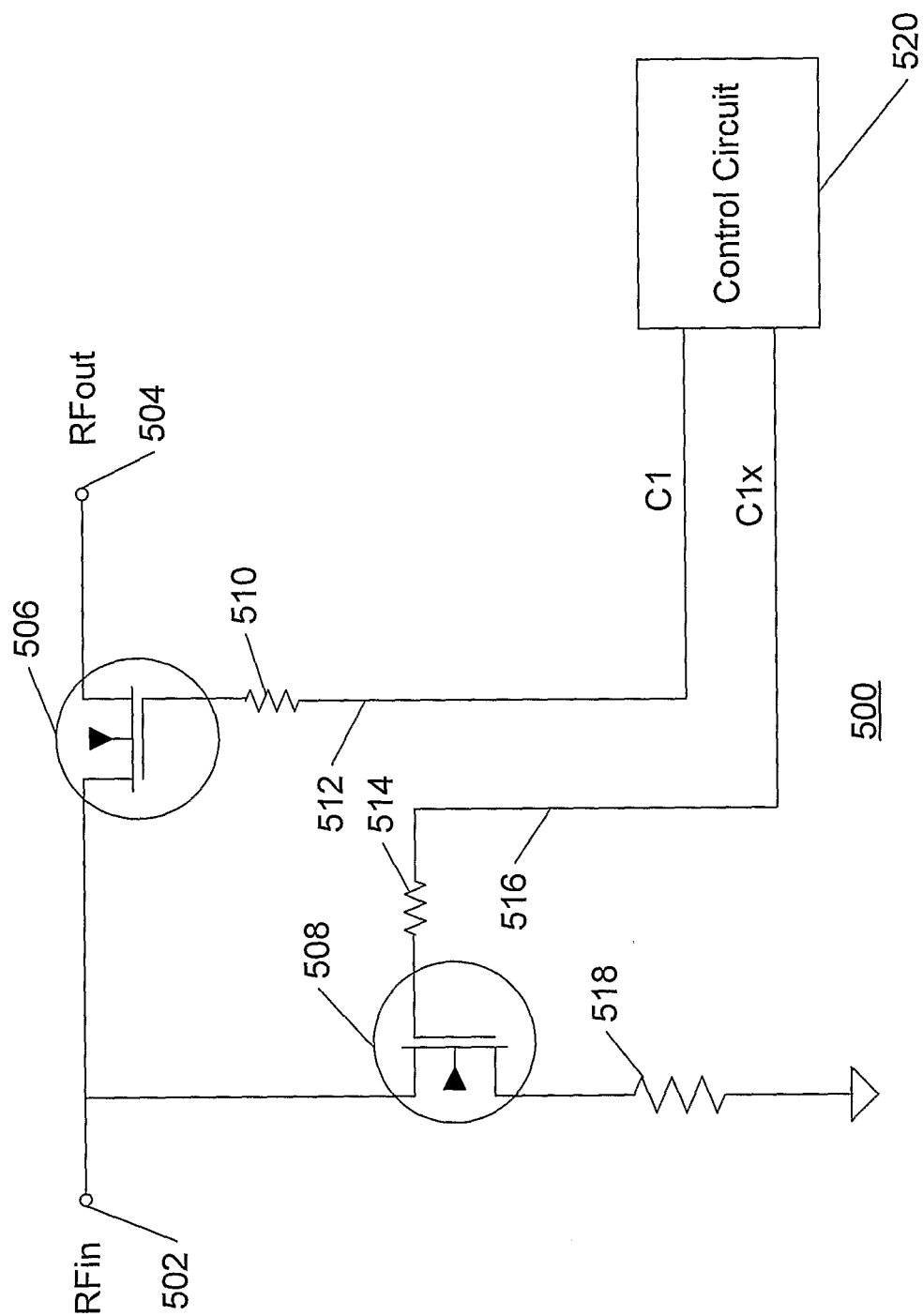


Figure 5A

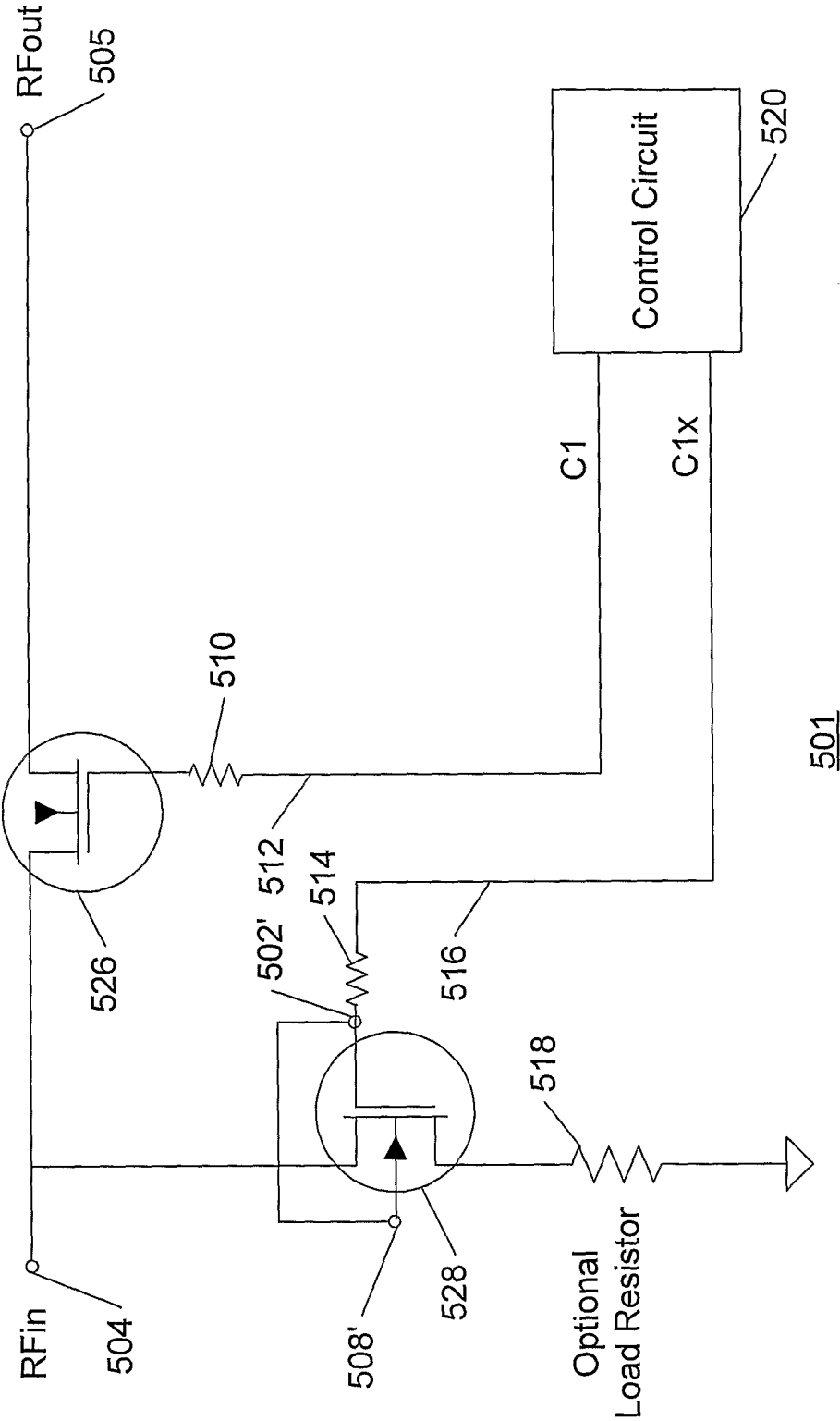


Figure 5B

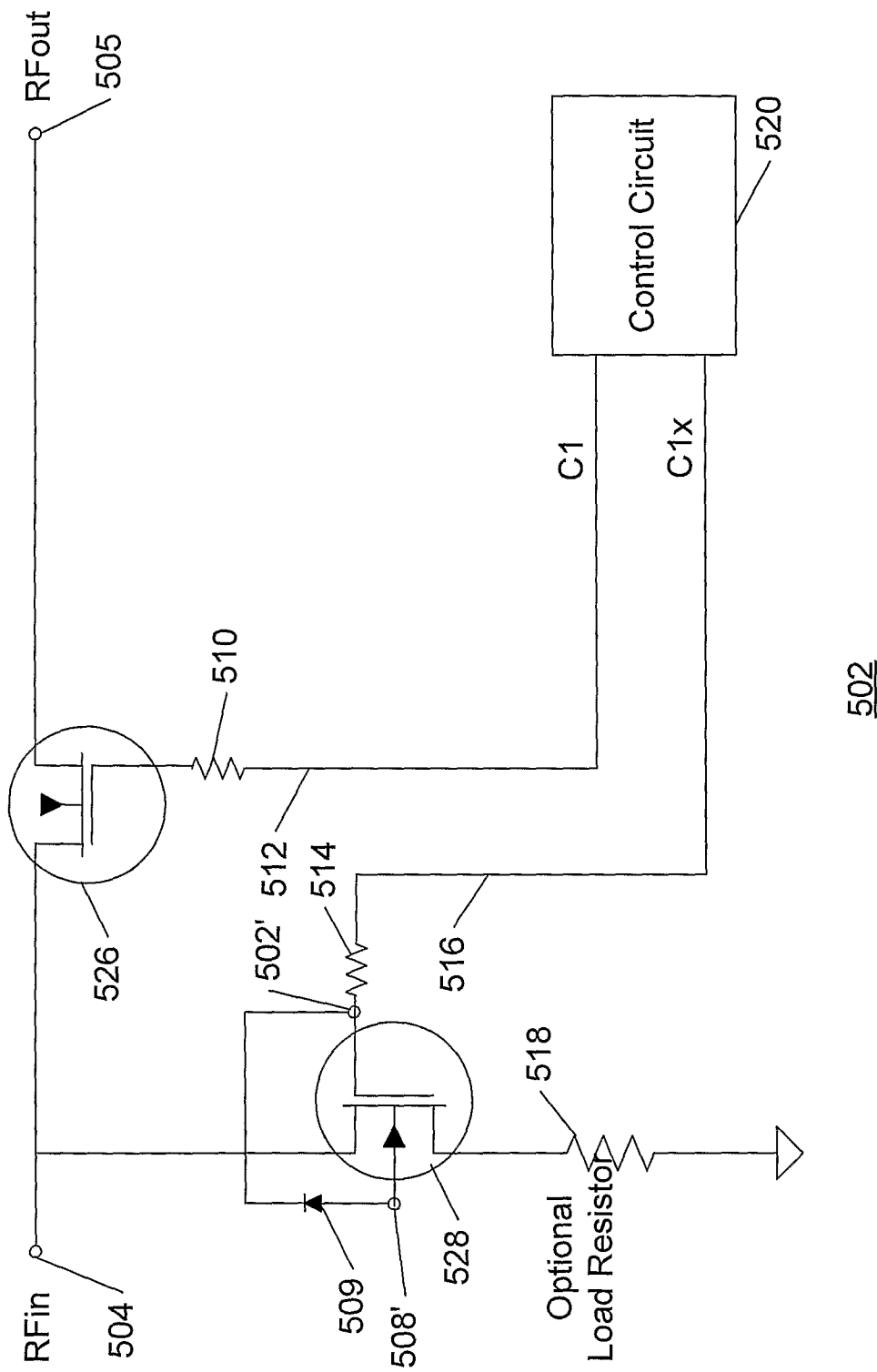


Figure 5C

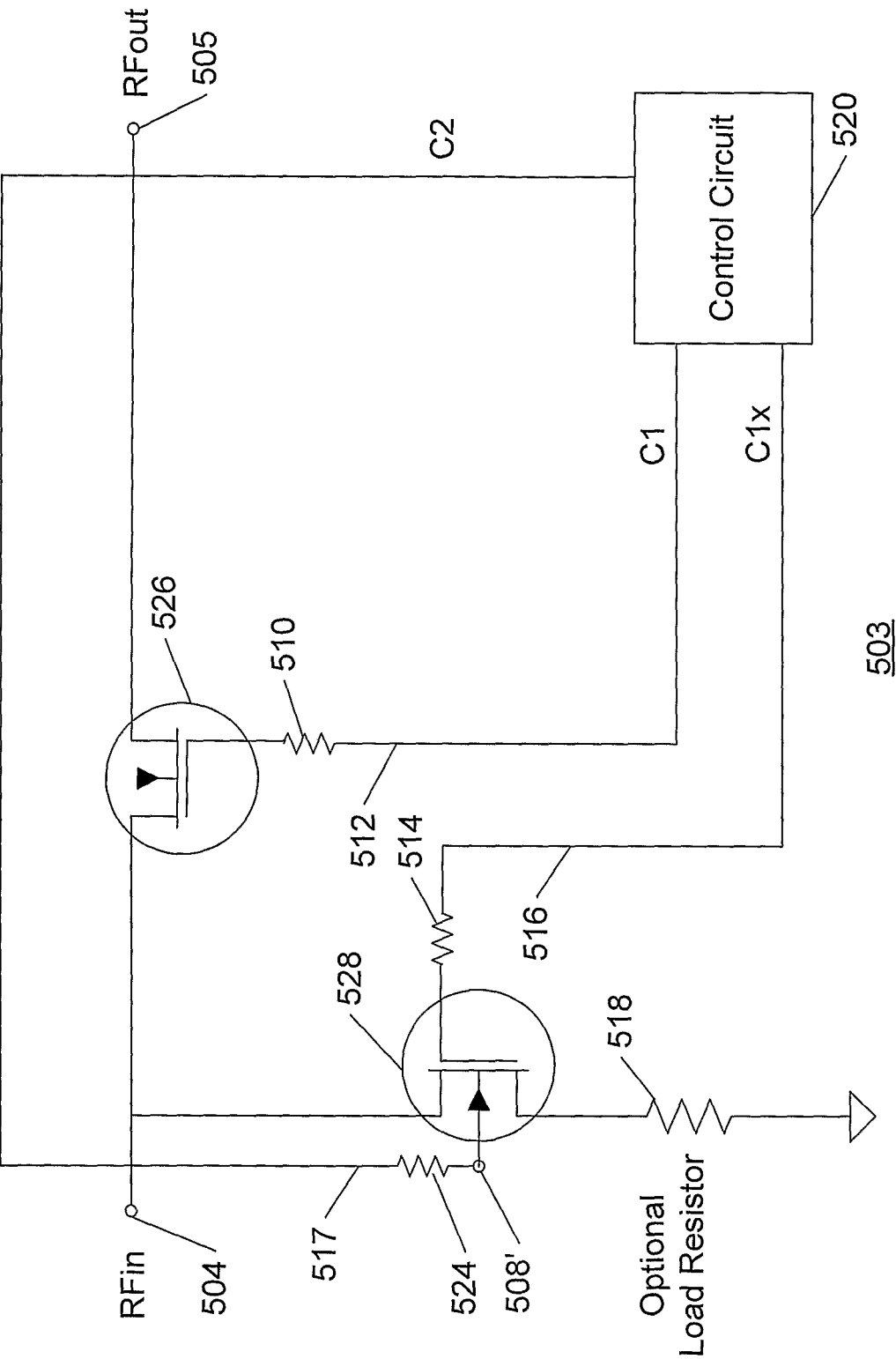


Figure 5D

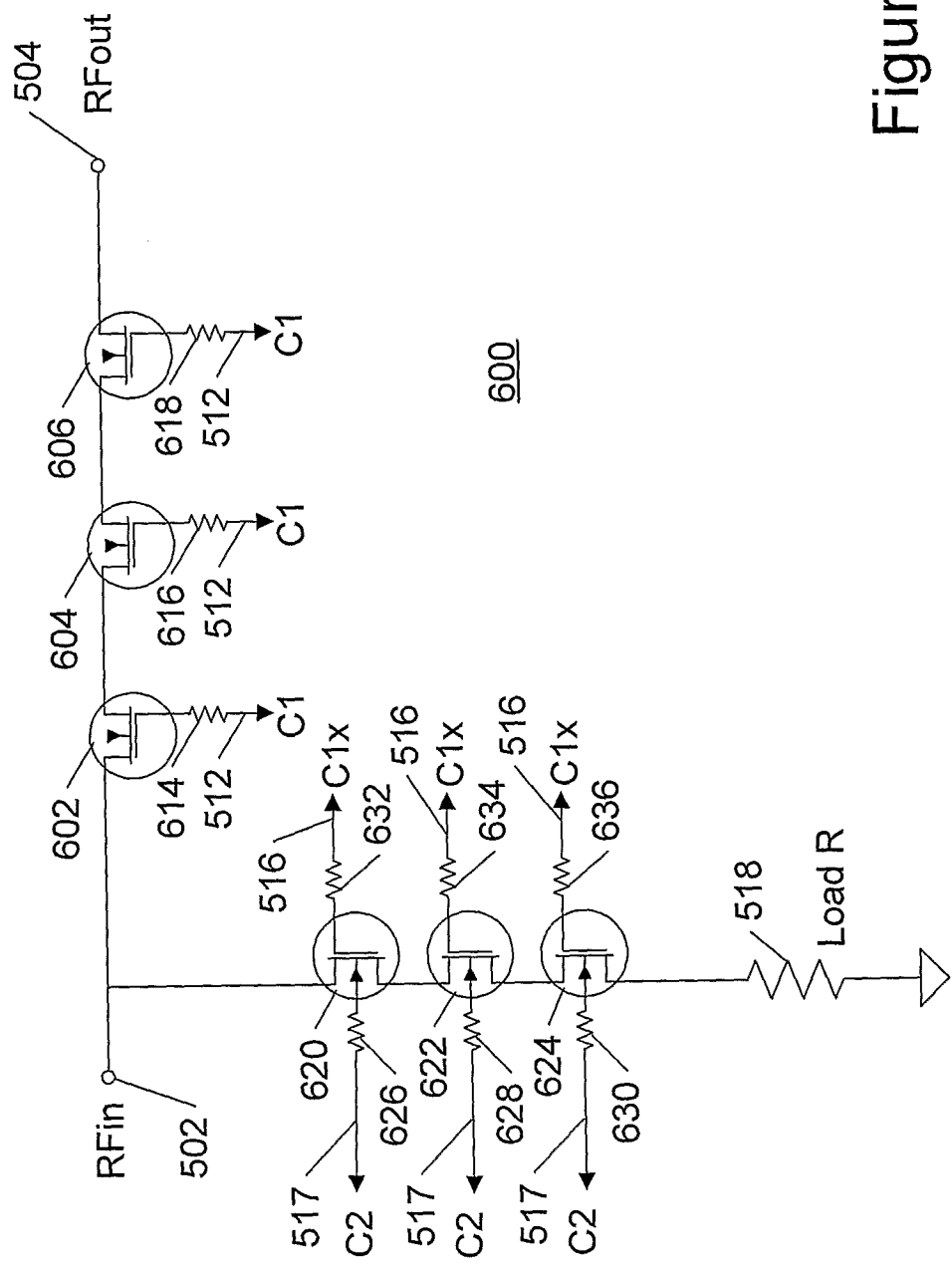


Figure 6

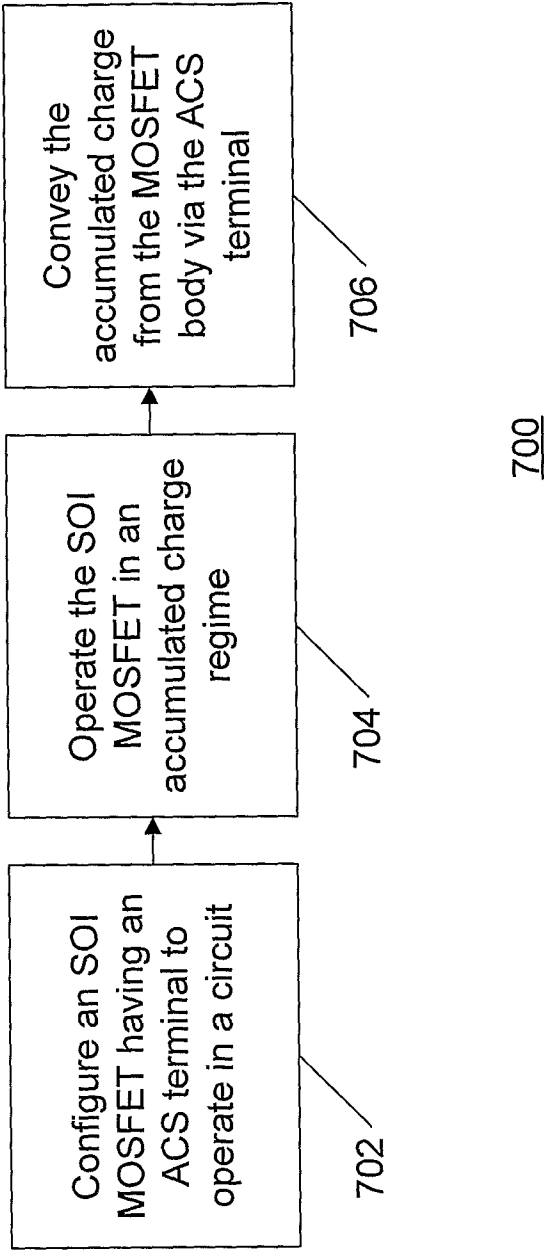


Figure 7

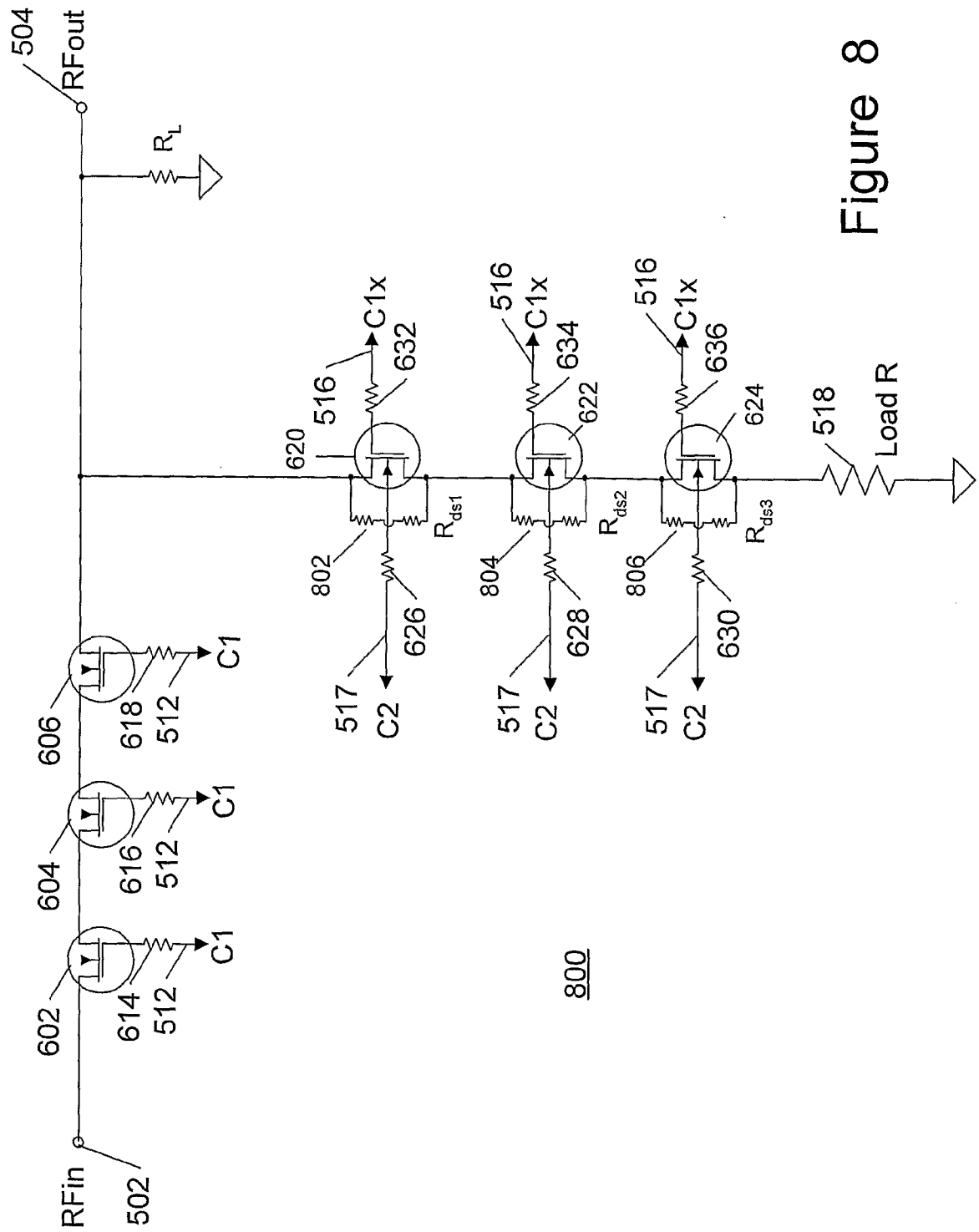


Figure 8

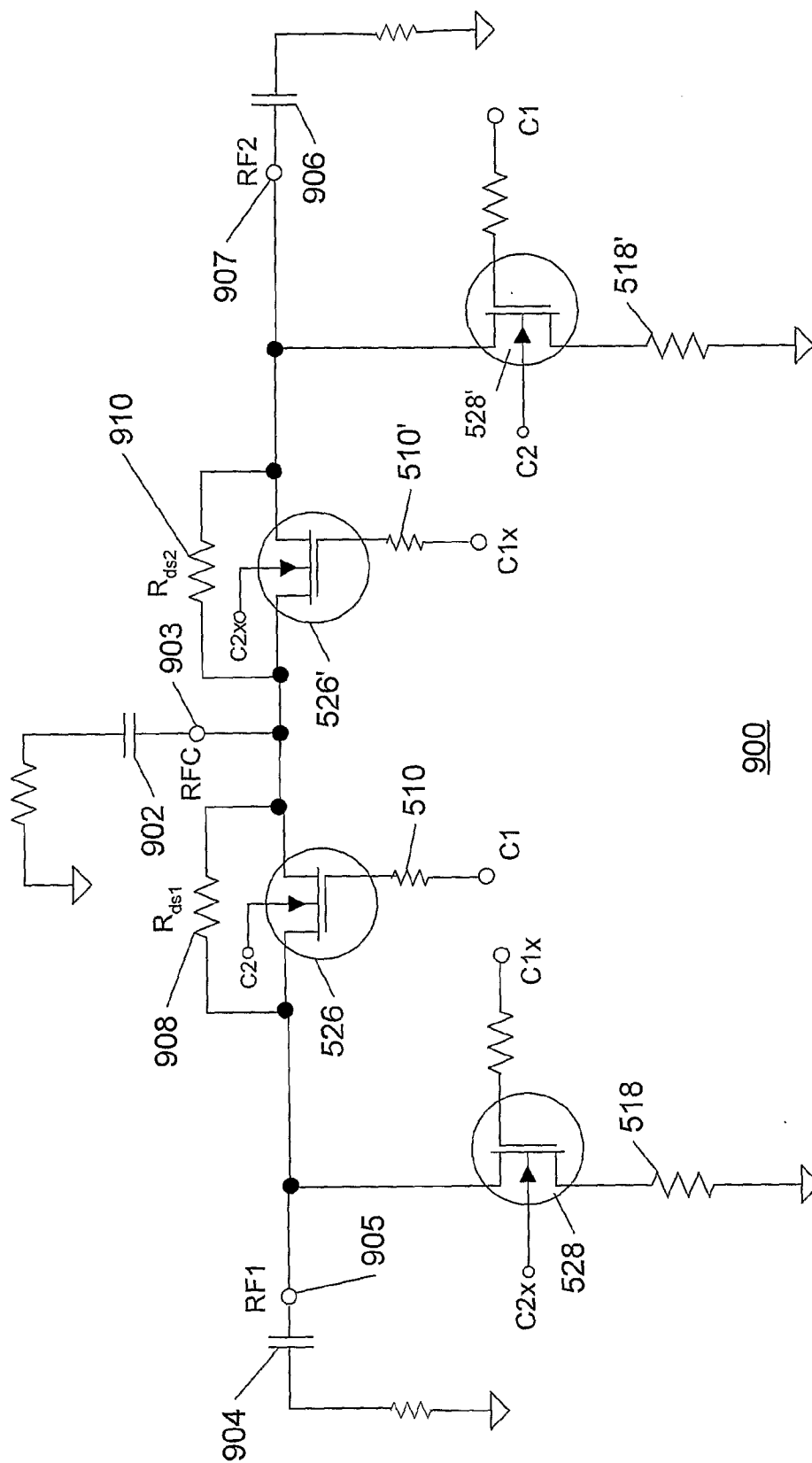
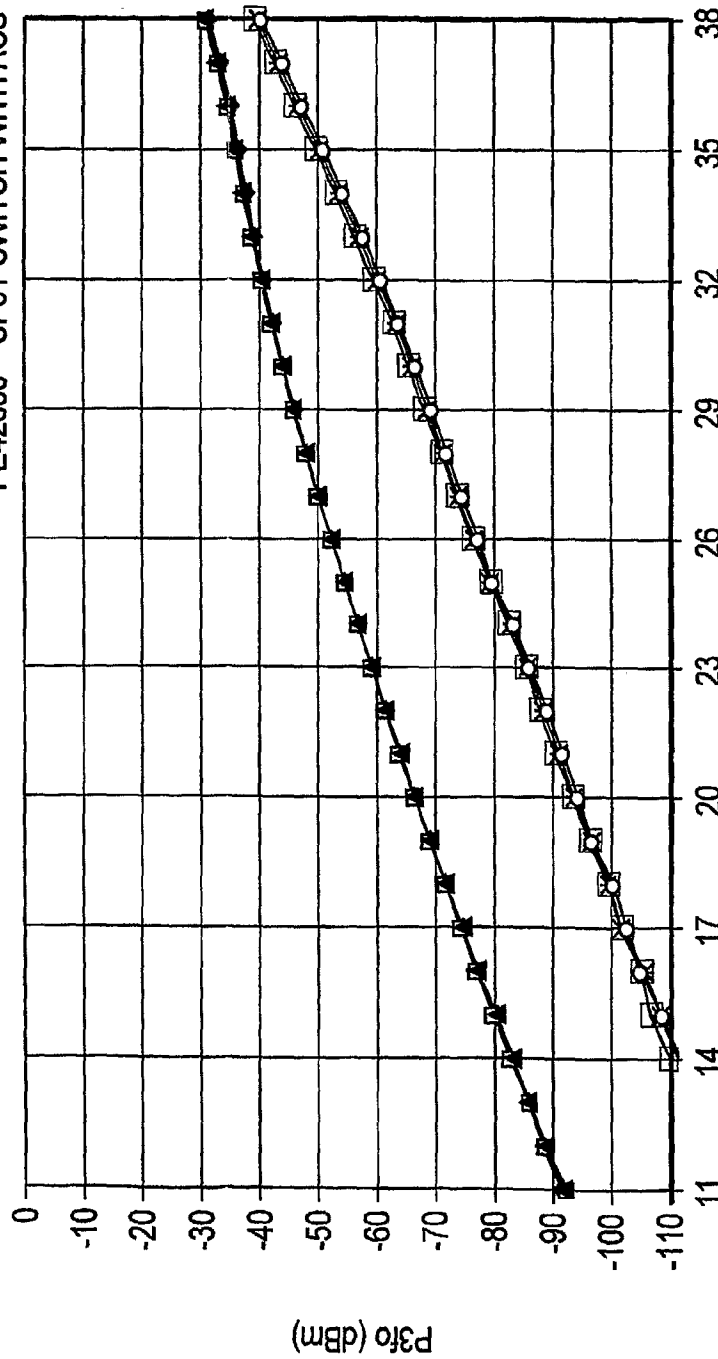


Figure 9

3f_o HARMONIC PERFORMANCE VS INPUT POWER

PE42663 = SP6T SWITCH WITHOUT ACS
PE42660 = SP6T SWITCH WITH ACS



TEMP = 25° C
V_{dd} = 2.6 V
F_o = 900 MHz
RF PULSE WIDTH = 2ms
50 Ω LOAD ALL OTHER PORTS

INPUT POWER (dBm)

PE42660 TAKEN TO 41
dBm INPUT POWER
WITH NO DAMAGE TO
THE DEVICE

—◆— PE4263 (2.65) —□— PE4263 (2.75) —▲— PE4263 (2.85)
—□— PE42660 (2.65) —*— PE42660 (2.75) —○— PE42660 (2.85)

FIG. 10

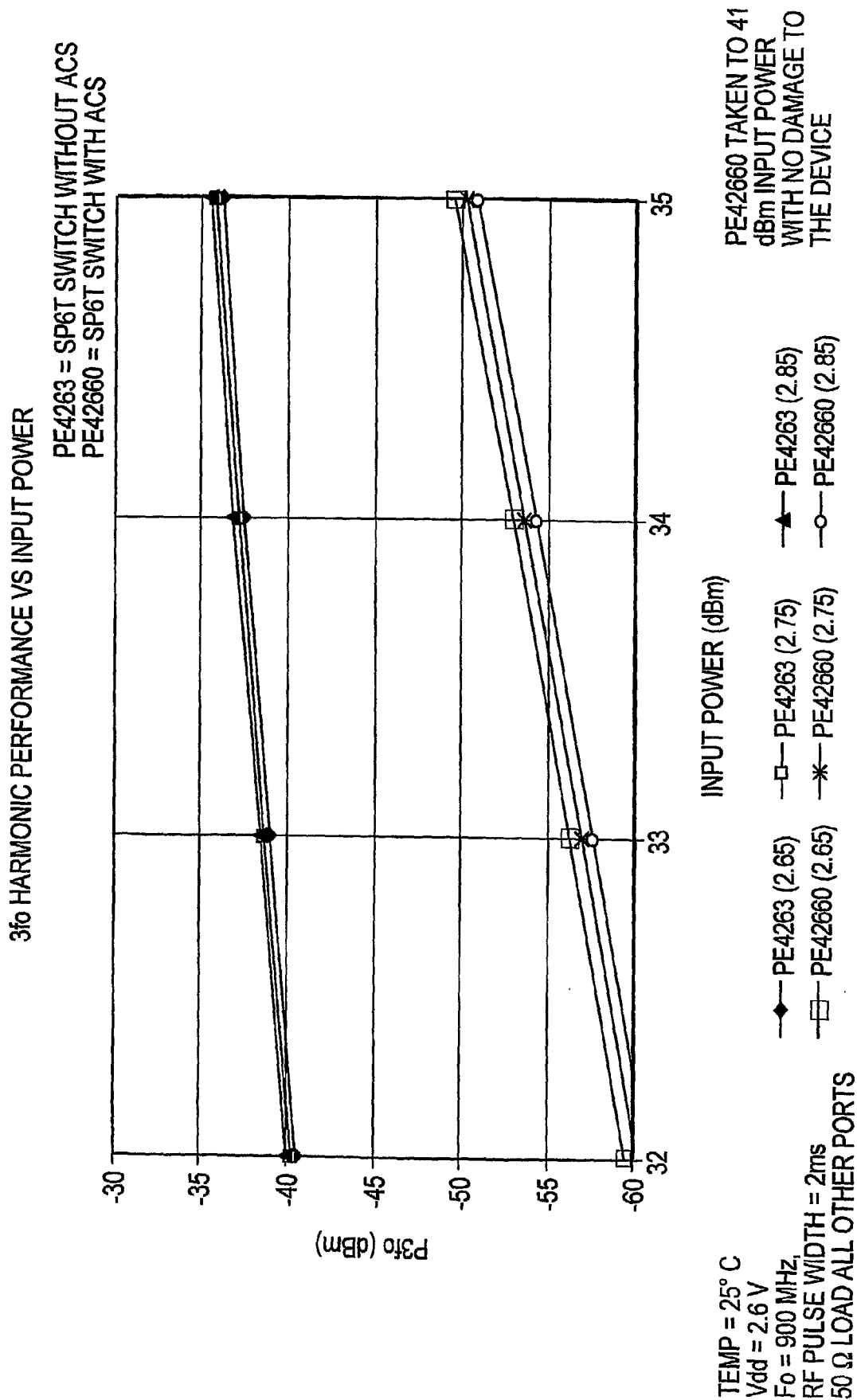


FIG. 11

2f_o HARMONIC PERFORMANCE VS INPUT POWER
 PE4263 = SP6T SWITCH WITHOUT ACS
 PE42660 = SP6T SWITCH WITH ACS

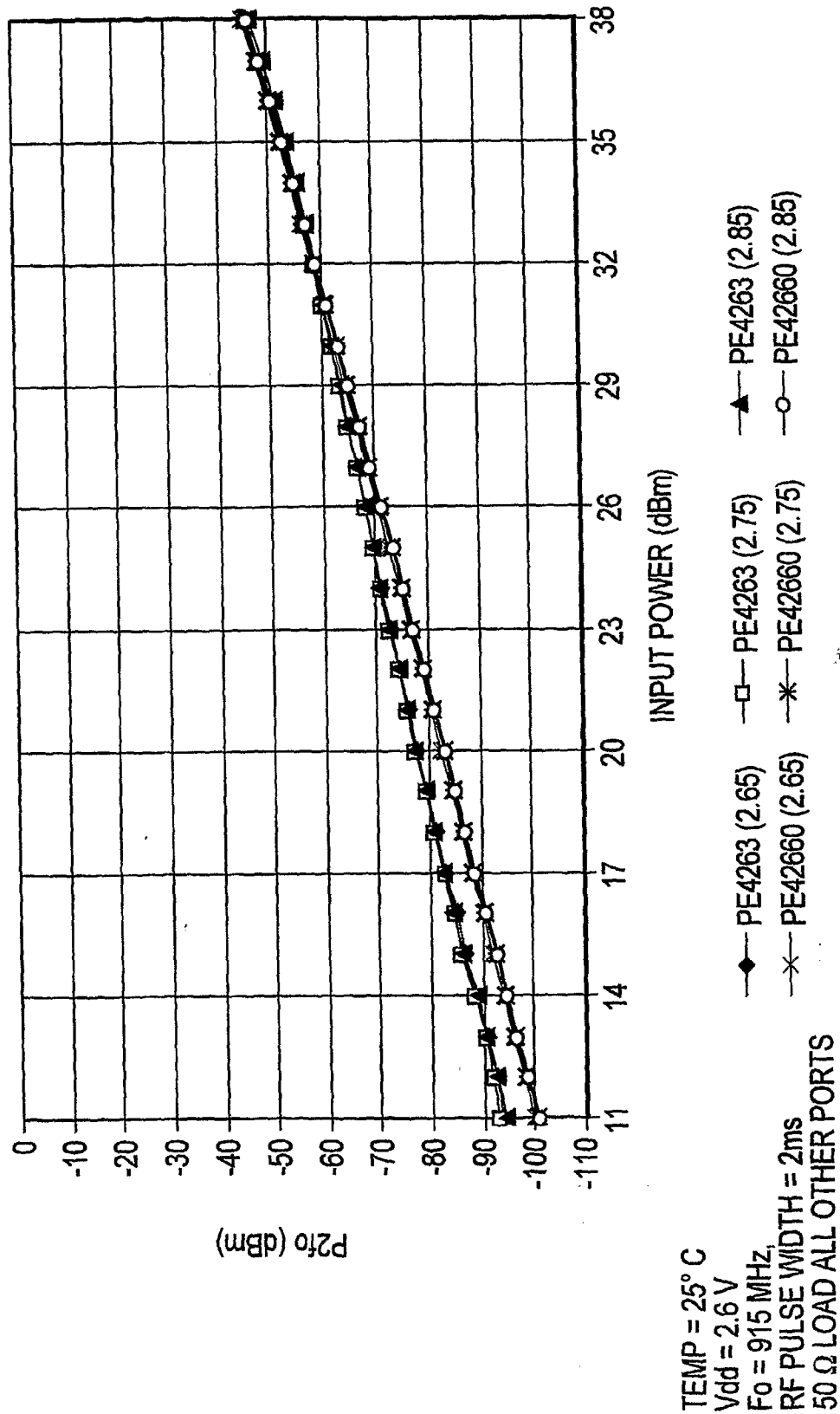
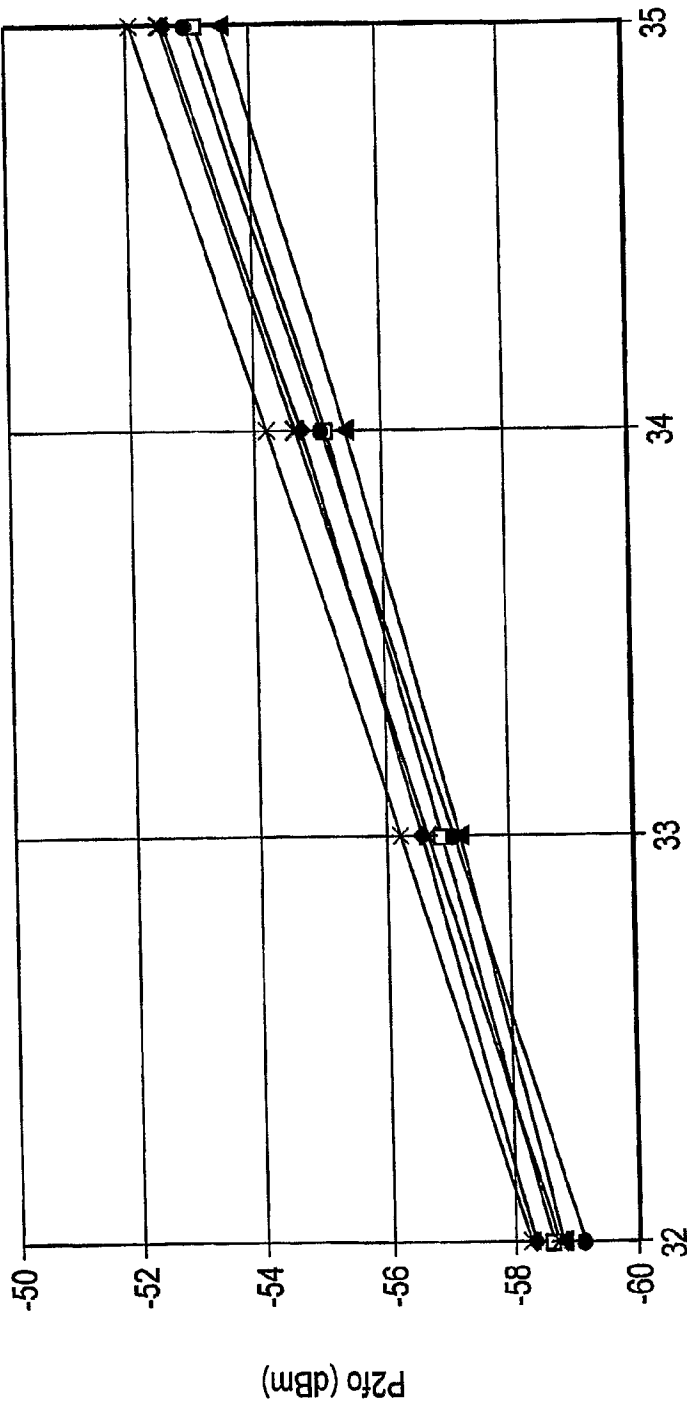


FIG. 12

2fo HARMONIC PERFORMANCE VS INPUT POWER
PE42663 = SP6T SWITCH WITHOUT ACS
PE42660 = SP6T SWITCH WITH ACS



TEMP = 25° C
Vdd = 2.6 V
Fo = 915 MHz,
RF PULSE WIDTH = 2ms
50 Ω LOAD ALL OTHER PORTS

- ◆ PE42663 (2.65)
- PE42663 (2.75)
- ▲ PE42663 (2.85)
- ✱ PE42660 (2.65)
- ✱ PE42660 (2.75)
- PE42660 (2.85)

FIG. 13

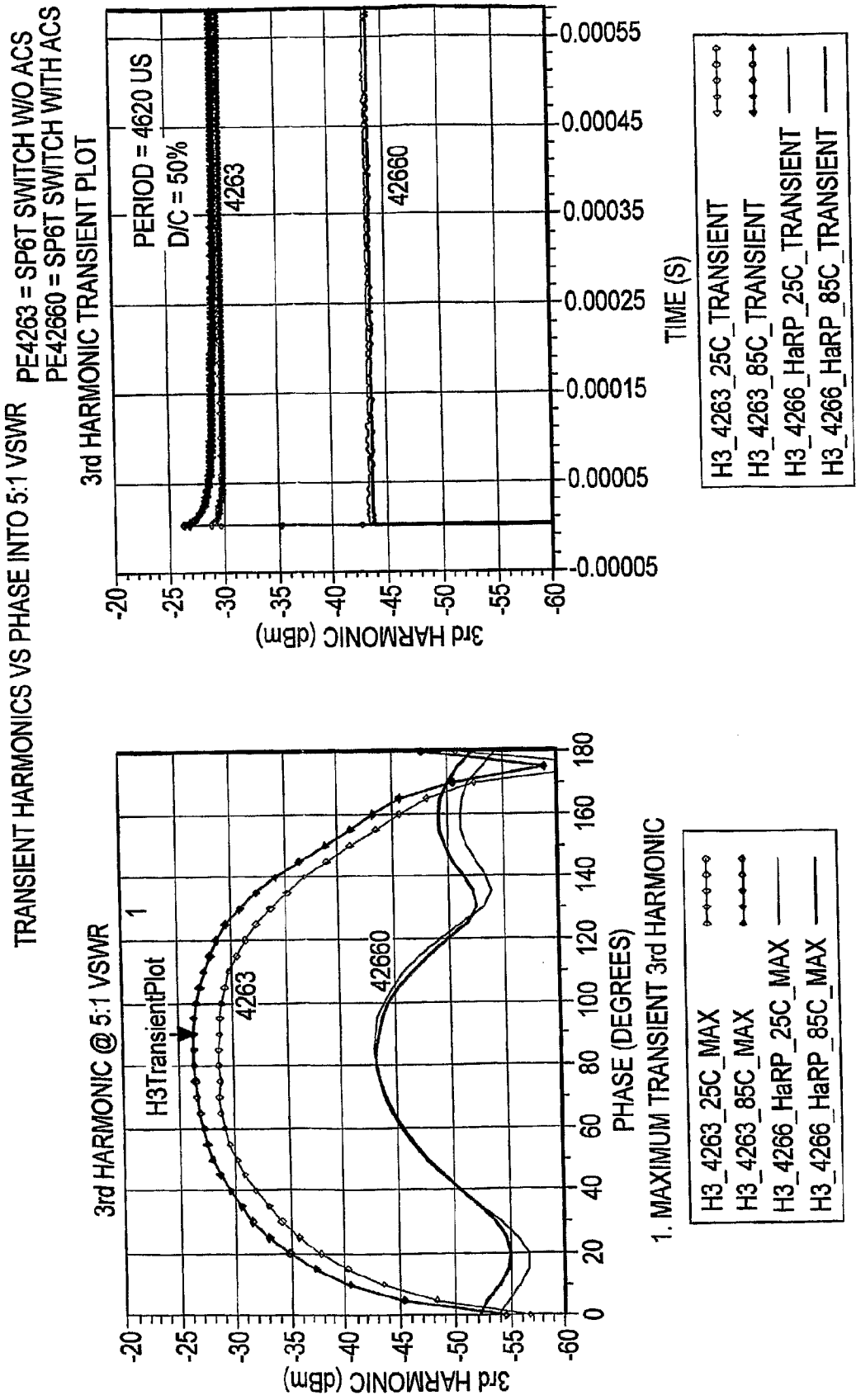


FIG. 14

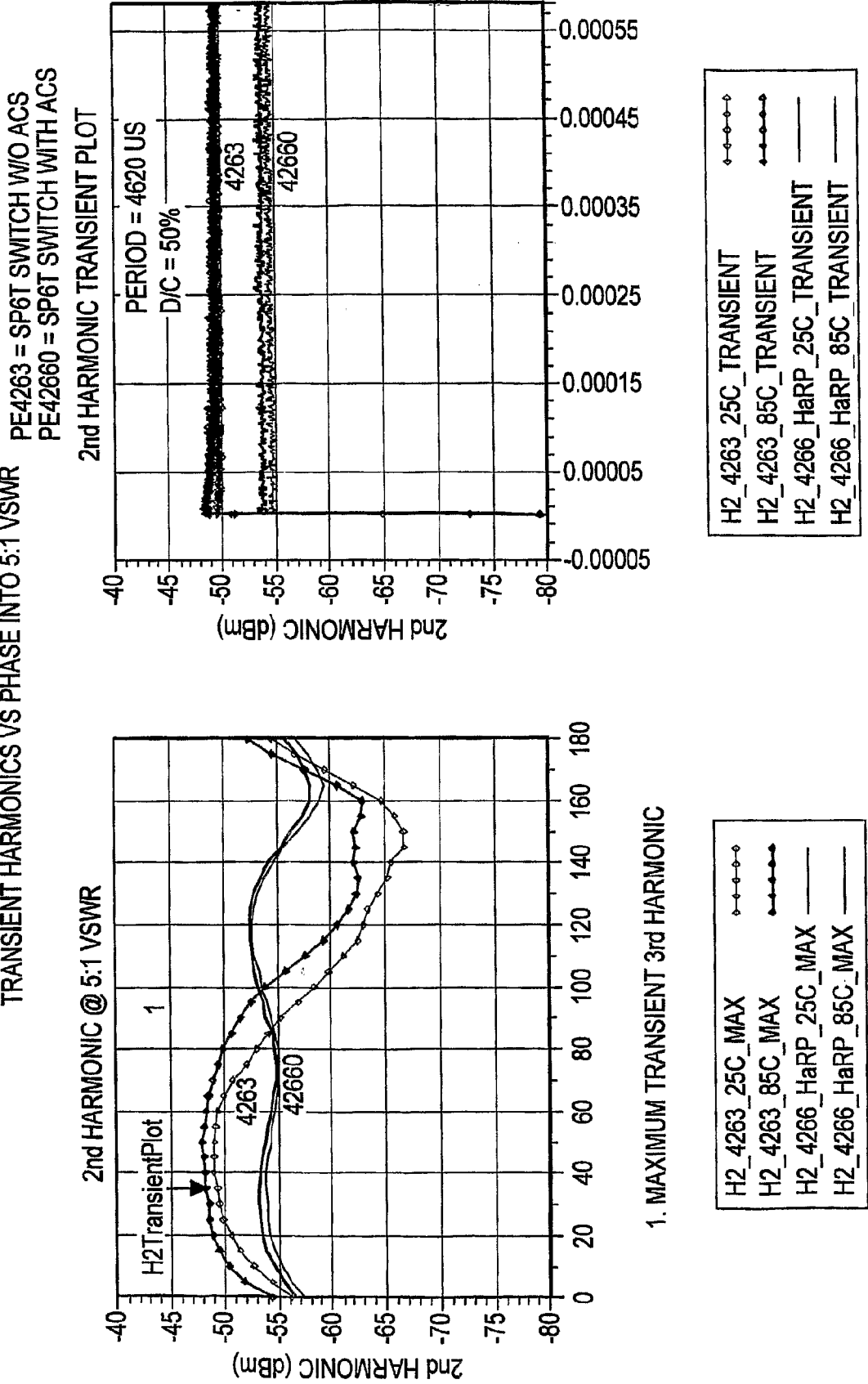


FIG. 15

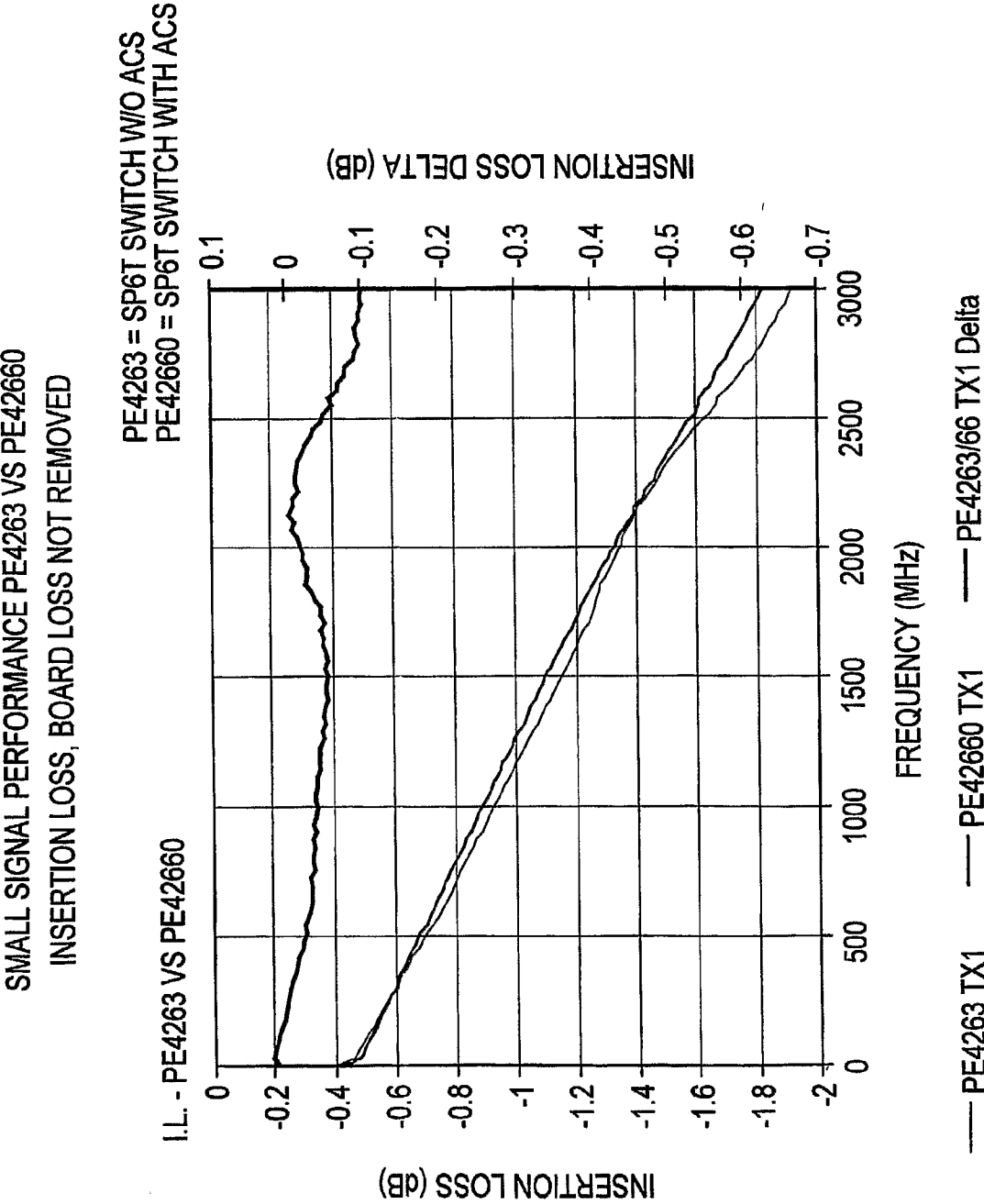


FIG. 16

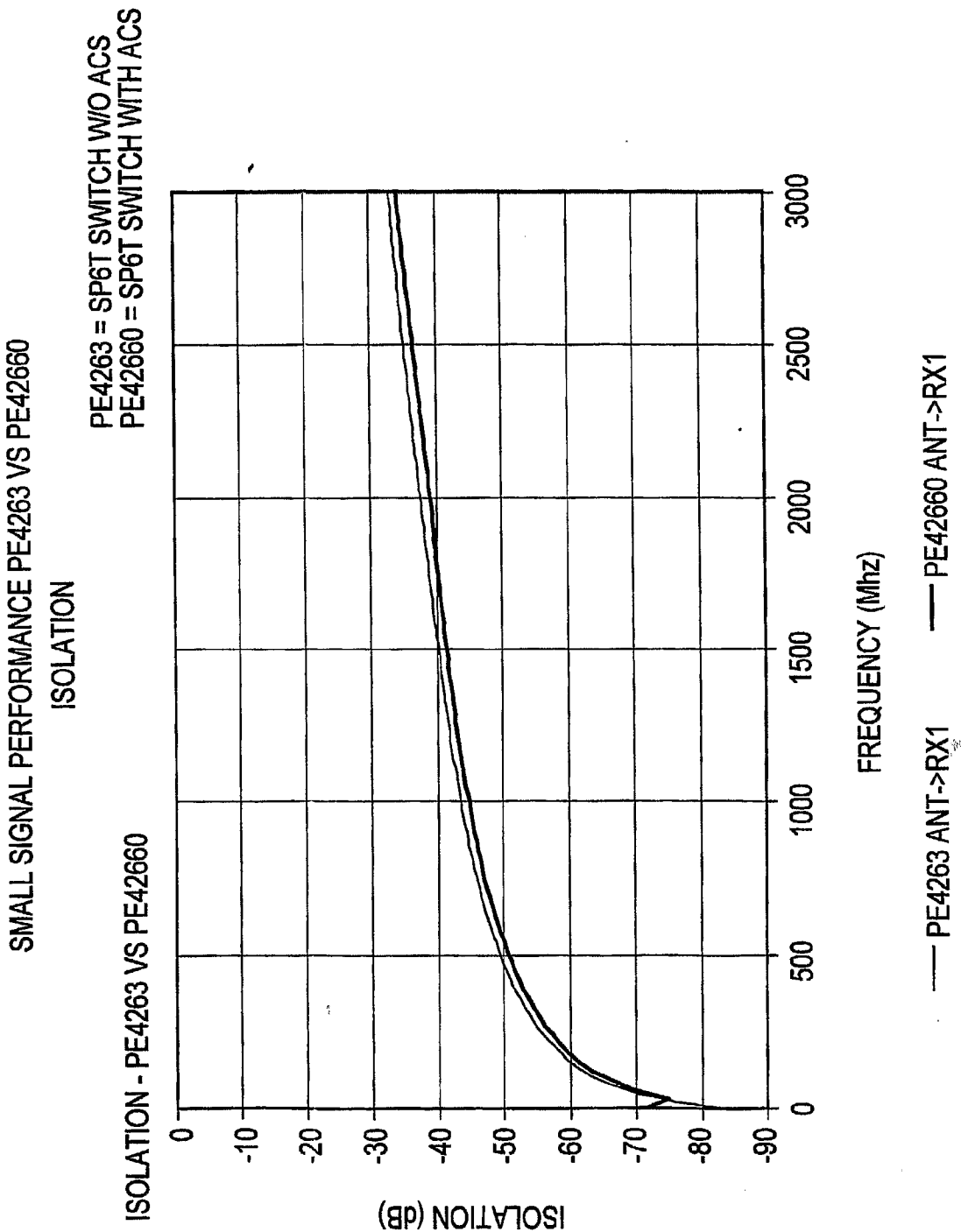


FIG. 17

IM3 PERFORMANCE OF STANDARD PE4263 VS. PE42660
IM3 VS RELATIVE PHASE BETWEEN DUPLEXER AND SWITCH
PTX = +20 dBm, PBL = -15 dBm
PE4263 = SP6T SWITCH W/O ACS
PE42660 = SP6T SWITCH WITH ACS

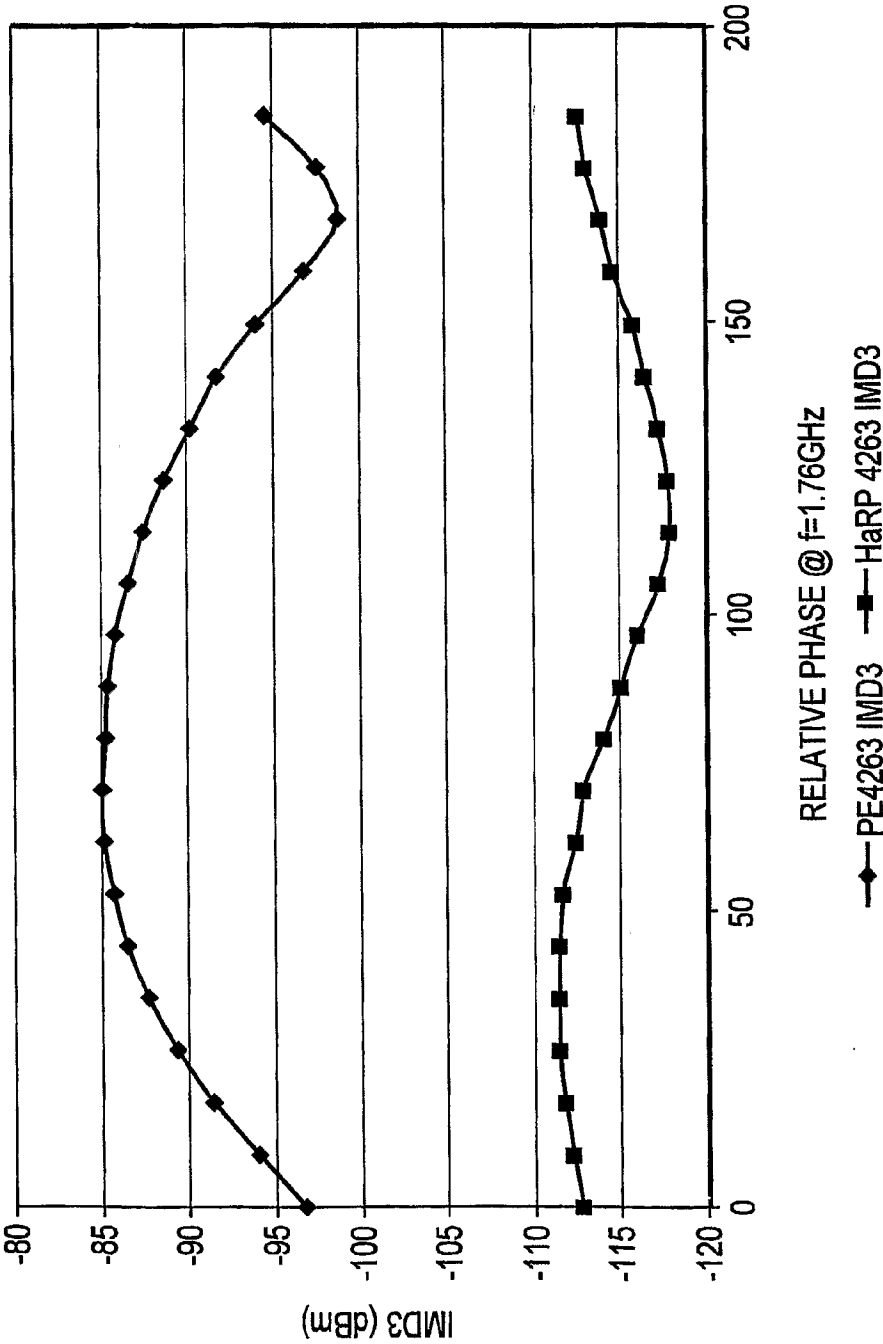


FIG. 18

INTERMODULATION (IM3 AND IM2) COMPARISON TABLE
(WORST CAST PHASE ANGLE)

PE4263 = SP6T SWITCH W/O ACS
PE42660 = SP6T SWITCH WITH ACS

	IMD2 f_{bl} = 190 MHz	IMD3 f_{bl} = 1760 MHz	IMD2 f_{bl} = 4090 MHz
PE4263	-97.0	-85.3	-100.6
HaRP PE4263	-116.7	-111.4	-111.5

- LOWER IS BETTER
- BOTH IMD2 AND IMD3 MEASUREMENTS MEET THE - 103 dBm INDUSTRY REQUEST AT ALL PHASE ANGLES

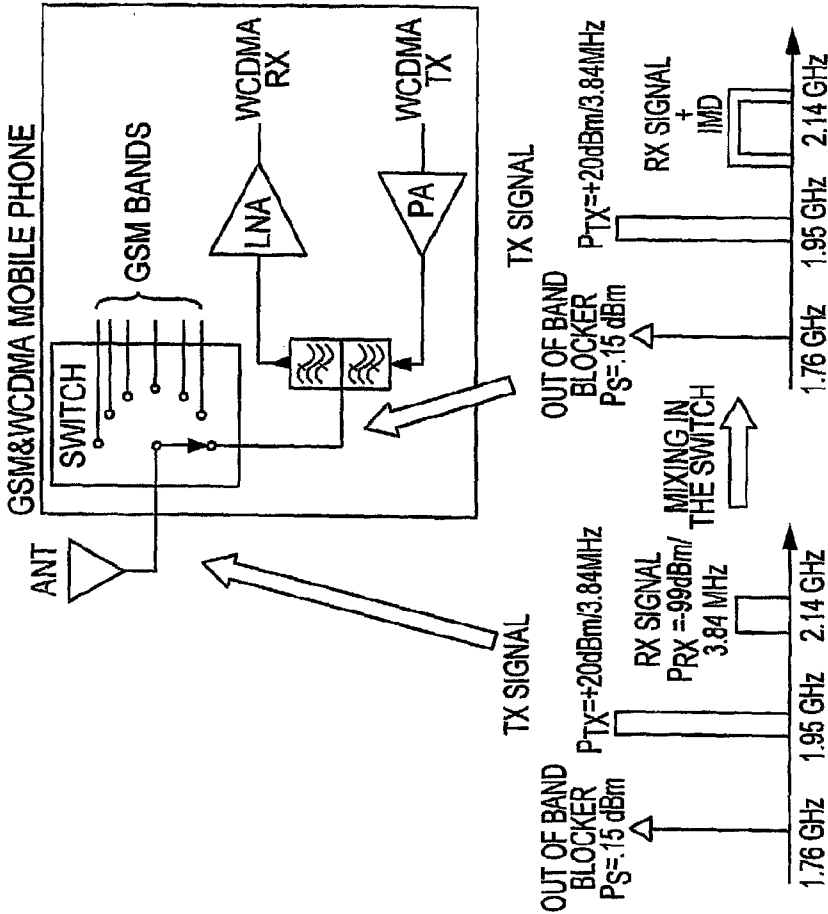


FIG. 19

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2006/026965

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L29/786 H01P1/15

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L H01P

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/015461 A1 (EBINA AKIHIKO [JP]) 23 August 2001 (2001-08-23)	1-49, 52-85, 116-120, 131
Y	the whole document	86-115, 121-130, 132, 133
X	US 2003/205760 A1 (KAWANAKA SHIGERU [JP] ET AL) 6 November 2003 (2003-11-06)	1-28, 30, 32-49, 52-70, 73-85, 116-120, 131
	paragraph [0036] - paragraph [0043]; figures ----- -/--	

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

19 October 2006

Date of mailing of the international search report

07/11/2006

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Hoffmann, Niels

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2006/026965

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 249 027 B1 (BURR JAMES B [US]) 19 June 2001 (2001-06-19) the whole document	1-28,30, 32-49, 52-70, 73-85, 116-120, 131
X	EP 1 006 584 A2 (SHARP KK [JP]) 7 June 2000 (2000-06-07) the whole document	1-28,30, 32-49, 52-70, 73-85, 116-120, 131
Y	US 6 804 502 B2 (BURGENER MARK L [US] ET AL) 12 October 2004 (2004-10-12) the whole document	86-115, 121-130, 132,133
A	US 5 012 123 A (AYASLI YALCIN [US] ET AL) 30 April 1991 (1991-04-30) the whole document	86-115, 121-130, 132,133
A	US 5 818 099 A (BURGHARTZ JOACHIM NORBERT [US]) 6 October 1998 (1998-10-06) the whole document	86-115, 121-130, 132,133
A	US 6 504 212 B1 (ALLEN DAVID HOWARD [US] ET AL) 7 January 2003 (2003-01-07) the whole document	1-49, 52-133
A	J. B. KUO, S.-C. LIN: "Low-Voltage SOI CMOS VLSI Devices and Circuits" 2001, WILEY INTERSCIENCE, NEW YORK, XP001090589 page 57 - page 60 page 349 - page 354	1-49, 52-133

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2006/026965

Box II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☒ Claims Nos.: 50,51
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box II.2

Claims Nos.: 50,51

It is not clear, which features are meant to be implied by the "contact region overlap region", as this region should "ensure that all of the gate oxide layer is completely covered with dopant material that is the same as dopant material used to form the electrical contact region". It is especially not at all clear, how such a region may ensure that the gate oxide layer UNDER the gate electrode (cf. "all of the gate oxide" ; "completely covered") is covered by the dopant material. It is moreover not clear, how the presence of such a region may have any influence on the presence of doping material on the gate oxide layer of the finished device at all and especially not on the type of dopant material. Accordingly, no meaningful search is possible with respect to claims 50 and 51.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2006/026965

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 2001015461	A1	23-08-2001	JP 3608456 B2 JP 2001168340 A	12-01-2005 22-06-2001
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