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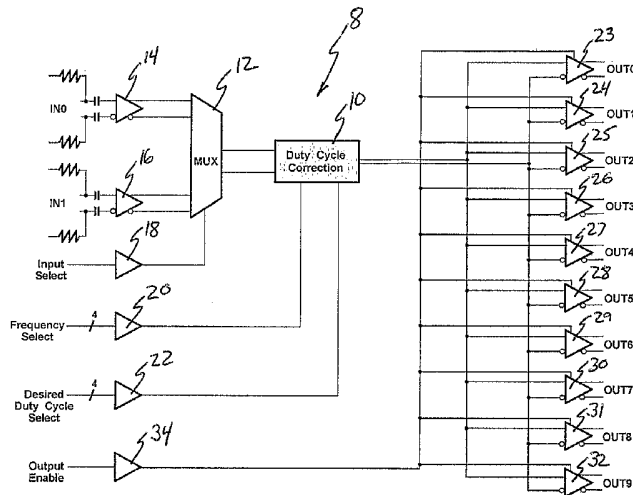
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(54) Title: CLOCK PULSE DUTY CYCLE CONTROL CIRCUIT FOR A CLOCK FANOUT CHIP



(57) Abstract: A clock pulse duty cycle control circuit for receiving an input clock signal and for providing an output clock signal having a desired duty cycle. An error signal generator includes a differential integrator that is connected to receive the output clock signal. The differential integrator integrates the output clock signal to produce a time-varying DC error signal representative of a difference between the output clock signal duty cycle and the desired duty cycle. A duty cycle corrector includes a differential integrator connected to receive the input clock signal and the error signal. The differential integrator integrates the input clock signal to produce a correction stage clock signal. The differential integrator causes the slopes of the input clock signal edges to be adjusted as a function of the error signal. A buffer including a high gain amplifier is connected to receive the correction stage clock signal and squares the edges of the clock signal to produce the output clock signal.

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**INTERNATIONAL SEARCH REPORT**

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**A. CLASSIFICATION OF SUBJECT MATTER**  
 IPC: G06F 1/04( 2006.01);H03K 3/00( 2006.01),3/013( 2006.01);H03B 1/00( 2006.01)  
 USPC: 327/108,112,291,292,293,294,295,296,297,298 T  
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**B. FIELDS SEARCHED** Sc

Minimum documentation searched (classification system followed by classification symbols)  
 U.S. : 327/108, 112, 291, 292, 293, 294, 295, 296, 297, 298 D.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6518809 (Kotra) 11 February 2003 Figures 3,4 and 5	1-6, 9, 12-14 and 16
X	US 6690202(Groen et al.) 10 February 2004 Figure 2-4	1-10 and 12-19

Further documents are listed in the continuation of Box C.  See patent family annex. C

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