



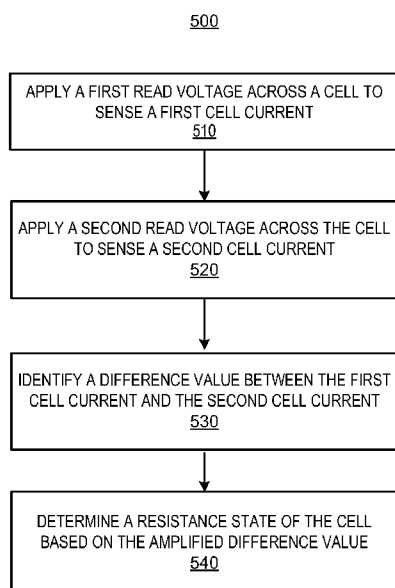
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[Continued on next page]

- (54) **Title:** DETERMINING A RESISTANCE STATE OF A CELL IN A CROSSBAR MEMORY ARRAY



(57) **Abstract:** According to an example, in a method for determining a resistance state of a cell in a crossbar memory array, a first read voltage may be applied across a cell to sense a first cell current. In addition, a second read voltage may be applied across the cell to sense a second cell current. A difference value between the first cell current and the second cell current may be identified and a resistance state of the cell may be determined based on the difference value.

FIG. 5



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— *as to the identity of the inventor (Rule 4.17(i))*

DETERMINING A RESISTANCE STATE OF A CELL IN A CROSSBAR MEMORY ARRAY

BACKGROUND

[0001] Electronic data is typically represented using a binary number system. The binary number system is one in which values may take on one of two states, typically represented by a logical “1” and a “0”. Various types of memory systems have been developed which include small programmable devices that store a single bit as either a logical “1” or a “0”. The ON state may be used to represent a logical “1,” while the OFF state may be used to represent a logical “0”. One type of memory architecture is the crossbar memory architecture. The crossbar memory architecture includes two sets of interconnecting wire segments and memory elements are placed at multiple crosspoints between the interconnecting wire segments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] Features of the present disclosure are illustrated by way of example and not limited in the following figure(s), in which like numerals indicate like elements, in which:

[0003] FIG. 1 shows a schematic view of a data storage apparatus including a crossbar array of memory elements, according to an example of the present disclosure;

[0004] FIG. 2 shows a diagram of a crossbar memory array, according to an example of the present disclosure;

[0005] FIG. 3A shows a cell including a switching element and a selector, according to an example of the present disclosure;

[0006] FIG. 3B shows current-voltage (I-V) curves for selectors, according to an example of the present disclosure;

[0007] FIG. 4 shows I-V curves for a memristor, according to an example of the present disclosure;

[0008] FIG. 5 shows a flow chart of a method for determining a resistance state of a cell in a crossbar memory array, according to an example of the present disclosure; and

[0009] FIG. 6 shows a dual-sensing circuit, according to an example of the present disclosure.

DETAILED DESCRIPTION

[0010] For simplicity and illustrative purposes, the present disclosure is described by referring mainly to an example thereof. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. It will be readily apparent however, that the present disclosure may be practiced without limitation to these specific details. In other instances, some methods and structures have not been described in detail so as not to unnecessarily obscure the present disclosure. As used herein, the terms “a” and “an” are intended to denote at least one of a particular element, the term “includes” means includes but not limited to, the term “including” means including but not limited to, and the term “based on” means based at least in part on.

[0011] Disclosed herein are examples of methods for determining a resistance state of a cell in a crossbar memory array. Particularly, the disclosed examples provide dual-sensing reading methods to improve read margin reliability while determining the resistance state of a cell. In this regard, for instance, the disclosed methods may provide tolerance for variation in selector threshold and parasitic current (e.g., leak current or sneak current). Also disclosed herein are a data storage system and a dual-sensing circuit for implementing the methods.

[0012] According to a disclosed example, a first read voltage is applied across a cell in a crossbar memory array to sense a first current through the cell. In addition, a second read voltage is applied across the cell to sense a second current through the cell. The first read voltage, for instance, may be lower than the second read voltage and the second read voltage may be lower than a write voltage for the cell. A difference value between the first current and the second current may be identified and amplified. In addition, a resistance state of the cell may be determined based on the amplified difference value. For example, a low resistance state (i.e., logical “1” or ON) may be determined for the cell in response to a high amplified difference value and a high

resistance state (i.e., logical “0” or OFF) may be determined for the cell in response to a low amplified difference value.

[0013] According to another disclosed example, the cell may further include a selector in series with the cell. The selector, for instance, may include a threshold voltage (V_{th}) in order to provide non-linearity to the cell and reduce the loss of current across a row of the crossbar memory array due to leakage or sneak current. As used herein, the term “non-linearity” refers generally to a characteristic of a function with the characteristic comprising deviation over a finite domain from the slope of a straight line that most closely approximates the function over that domain. With particular reference to current-voltage (I-V) functions, “nonlinear” functions exhibit marked departures from a linear ohmic function. An exponential I-V function is a particular example of such a function. More specifically, a highly nonlinear I-V function can exhibit substantially adjacent domains of very high resistance and very low resistance. The cell in the crossbar memory array may be a memristor device in series with a non-linear selector, according to an example.

[0014] In a memristor cell, variation in selector threshold and leakage or sneak current may significantly impact the read margin. For instance, when using Niobium Oxide as a selector, which is prone to be thermally sensitive, the variation in selector behavior may lead to high read failures. In addition, a high variation in sneak or leakage current may also lead to high read failures. Accordingly, the disclosed examples provide a low overhead, dual-sensing reading method that may trade-off access time to dramatically improve the read margin to tolerate variations in selector threshold and leakage or sneak current. Generally speaking, the disclosed examples provide a dual-sensing reading method that may improve the read margin for cells in the crossbar memory array and enhance the distribution of ON and OFF current for the cells in the crossbar memory array.

[0015] FIG. 1 illustrates a schematic view of a data storage apparatus 100 that includes a memory control module 103, according to an example. The memory control module 103 may control operations of storing and retrieving

data to and from an $m \times n$ memory array 101 of cells 102, which may be memristor devices, memristors, etc. The apparatus 100 is depicted as including an encoder module 104 that is to encode data and a decoder module 105 that is to decode data. The apparatus 100 is further depicted as including a read/write control module 106 that is to control operations of reading data from the memory array 101 and writing data to the memory array 101. The memory control module 103 may encode input data 107 and store the encoded data into the memory array 101. The memory control module 103 may also read out the encoded data stored in the memory array 101, decode the data to recover the original bits in the input data 107, and transmit the decoded data as output data 108.

[0016] According to an example, the memory array 101 is part of the apparatus 100. In another example, the memory array 101 is separate from the apparatus 100. In any regard, the $m \times n$ memory array 101 may respectively include first and second sets of m and n conductors, e.g., wires. Each of the m conductors in the first set may cross each of the n conductors in the second set to address one of the cells 102 located at the crossing point. In order to facilitate a description of the memory array 101, the conductors in the first and second sets may be respectively referred to as rows (i.e., wordlines) and columns (i.e., bitlines) of the memory array 101. The $m \times n$ memory array 101 may include m row conductors 109 and n column conductors 110 in a circuit plane. The crosspoints of the row conductors 109 and the column conductors 110 may form a total of $m \times n$ cells. The reading and writing of individual bits of data to the cells 102 involves the application of voltages by row drivers 111 and column drivers 112. The conductors 109, 110 and cells 102 may be formed in different circuit planes. Moreover, the conductors 109, 110 may be formed of a variety of shapes as needed or desired, and may likewise form a grid of a variety of shapes.

[0017] FIG. 2 is a diagram showing a crossbar memory array 200 according to an example of the present disclosure. According to an example, the crossbar memory array 200 includes a set of horizontal conductors 202,

which are depicted as being generally in parallel with respect to each other. Additionally, a set of vertical conductors 204 is depicted as being generally perpendicular to, and crossing, the horizontal conductors 202. Programmable cells 102 are further depicted as being placed at the crosspoints 206 between a horizontal conductor 208 and a vertical conductor 210.

[0018] As discussed above, the cells 102 may be memristors or equivalently, memristor devices. Memristors exhibit a “memory” of past electrical conditions. For example, a memristor may include a matrix material that contains mobile dopants that may be moved within the matrix material to dynamically alter the electrical operation of the memristor.

[0019] The motion of dopants may be induced by the application of a programming condition such as an applied electrical voltage across the memristive matrix material. Particularly, the programming voltage generates a relatively high electrical field through the memristive matrix material and alters the distribution of dopants. After removal of the electrical field, the location and characteristics of the dopants remain stable until the application of another programming electrical field. For example, by changing the dopant configurations within the memristive matrix material, the electrical resistance of the memristor may be altered. The state of the memristor may be read by applying a lower reading voltage across the memristive matrix material which allows the internal electrical resistance of the memristor to be sensed but does not generate a sufficiently high electrical field to cause significant dopant motion. Consequently, the state of the memristor may remain stable over long time periods and through multiple read cycles.

[0020] According to an example, the crossbar memory array 200 may be used to form a non-volatile memory array. In this example, each of the cells at the crosspoints 206 may be used to represent a bit of data. Although individual conductors 208, 210 in FIG. 2 are shown with rectangular cross sections, the crossbar memory array 200 may also have square, circular, elliptical, or more complex cross sections. The conductors may also have many different widths, diameters, aspect ratios and/or eccentricities. The crossbars may be

nanowires, sub-microscale wires, microscale wires, or wires with larger dimensions.

[0021] According to various examples, the crossbar memory array 200 may be integrated into a Complimentary Metal-Oxide-Semiconductor (CMOS) circuit or other conventional computer circuitry. Each individual conductor may be connected to the CMOS circuitry by a via 212. The via 212 may be an electrically conductive path through the various substrate materials used in manufacturing the crossbar architecture. This CMOS circuitry may provide additional functionality to the memristor such as input/output functions, buffering, logic, configuration, or other functionality. Multiple crossbar memory arrays may be formed over the CMOS circuitry to create a multilayer circuit.

[0022] As discussed above, a cell 300 may include a switching element, such as a memristor 310, with at least two stable states to store a logical “1” or a logical “0” and a selector 320 in series with the memristor 310 to provide non-linearity to the cell, as shown in Fig. 3A. Ideally, in a crossbar memory array 101, the selector sub-threshold leakage or sneak current (i.e., current through the selector 320 for any voltage drop across a cell less than V_{th} , where V_{th} is the threshold voltage of a selector) is close to zero. Further, ideally V_{th} should be the same for all the selectors in the crossbar memory array.

[0023] However, as shown in example I-V curves 350 for selectors in FIG. 3B, due to process variation in selectors and Niobium Oxide’s sensitivity to temperature, the leakage or sneak current of the cell may vary from 200 nanoamperes (nA) to 2 microamperes (uA), and V_{th} (i.e., the knee of a selector curve) may vary from 1.3 V to 2V. Therefore, as the standard deviation of a cell’s selector threshold voltage in a crossbar increases, the effective read margin available at the sense-amplifier goes down, which eventually leads to a read failure.

[0024] With reference to FIG. 4, there are shown examples of memristor ON and OFF I-V curves 400. In FIG. 4 the solid line represents a high resistance state (i.e., OFF or logical “0”) 410 and dotted line represents a low resistance state (i.e., ON or logical “1”) 420. To perform a read, the read/write

control module 106, for instance, may apply a voltage across the selected row and column conductors to induce approximately 500 millivolts (mV) across the memristor component of a cell and sense the resulting current. To write to a cell, the read/write control module 106, for instance, may apply a voltage across the selected row and column conductors to induce a voltage of approximately 900mV across the memristor component of a cell to alter the state of the cell.

[0025] If the selector V_{th} varies, such as increasing by approximately 400mV, then the effective read voltage across the memristor goes down causing the read margin between the high resistance state and the low resistance state to decrease. In this instance, for example, the read/write control module 106 may sense the cell current at approximately 100mV (as indicated by ellipse 430) across the memristor where the read margin between the high resistance state and the low resistance state is low instead of at approximately 500mV (as indicated by ellipse 440) where the read margin between the high resistance state and the low resistance state is very high. This may result in a read failure. Moreover, the overall read voltage may not simply be increased to solve this problem because, if the selector V_{th} is low for some cells, then having a high read voltage may write to a cell instead, which may cause a read disturbance. As discussed in greater detail herein, the disclosed methods provide a two-level reading method that may trade access time for improved reliability.

[0026] With reference to FIG. 5, there is shown a flow chart of a method 500 for determining a resistance state of a cell in a crossbar memory array, according to an example of the present disclosure. It should be apparent to those of ordinary skill in the art that method 500 represents a generalized illustration and that other operations may be added or existing operations may be removed, modified or rearranged without departing from the scopes of method 500. The method 500 may be implemented, for example, by a dual-sensing circuit 600 as depicted in FIG. 6 below.

[0027] As discussed above, the cell may be a memristor cell that further includes a selector in series with the memristor cell. The selector may include a

threshold voltage (V_{th}) and may be added to provide non-linearity to the cell, which may help reduce leakage or sneak current. For example, for up to a V_{th} of 1.5 V, the selector may be completely off. If, however, the V_{th} is exceeded, significant voltage may drop across the memristor cell.

[0028] As mentioned above with respect to FIG. 4, in an ideal scenario shown by the ellipse 440 (~500 mV), the difference between the low resistance state 420 and the high resistance state 410 current is very high. However, if the read voltage difference across the memristor cell is lower, such as around approximately 100mV, then the low resistance state current 420 is as low as the high resistance state current 410, which may cause a read failure. Moreover, the low resistance state current may fall below a low resistance state decision threshold level, which is set independently of V_{th} . As discussed above, the reason for the decreased read voltage may stem from a variation in the V_{th} of the selector due to process variation and/or sensitivity to temperature and variation in the leakage or sneak current across a row or column of the crossbar memory array.

[0029] In this regard, a rate of increase or slope of the current through a memristor cell is a more reliable metric than the actual current through the memristor cell. That is, the rate at which the current increases may be a more accurate representation of the resistance state of the memristor cell than simply measuring the current at one static point. For example, the rate of increase in the low resistance state 420 current is always greater than the rate of increase for the high resistance state 410 current irrespective of any voltage variation due to the selector or the parasitic current across the row of the crossbar memory array.

[0030] Accordingly, the method 500 provides a dual-sensing reading scheme, which may trade-off access time for improved reliability. In FIG. 5, the read/write control module 106, for instance, may apply a first read voltage across a memristor cell to sense or measure a first cell current, as shown in block 510. According to an example, the read/write control module 106 may apply a first read voltage that is higher than 200mV. For instance, 200mV may

be a selected voltage to apply across the memristor cell. To apply 200mV, however, a larger voltage needs to be applied because some voltage will drop across the selector (V_{th}) and other circuit elements. In other words, to get 200mV across the memristor cell, $V_{th} + 200\text{mV} + V_{parasitic}$ (i.e., parasitic voltage) would need to be applied across the row column conductors. However, V_{th} and $V_{parasitic}$ are varying and unknown. Therefore, according to an example, a reasonably large V_{read} (i.e., read voltage) is selected so that there is a high likelihood that $V_{read} > V_{th} + 200\text{mV} + V_{parasitic}$. On the other hand, V_{read} should be less than $V_{th} + V_{switch}$ (i.e., switching voltage) + $V_{parasitic}$. Otherwise, the memristor cell may switch. According to an example, the first read voltage may be less than a second read voltage as discussed below.

[0031] In block 520, the read/write control module 106, for instance, may apply a second read voltage across the cell to sense a second cell current. According to an example, the read/write control module 106 may apply the second read voltage that is higher than 500 mV. As discussed above, to apply a selected voltage of 500mV so that there is a high likelihood that $V_{read} > V_{th} + 500\text{mV} + V_{parasitic}$. On the other hand, V_{read} should be less than $V_{th} + V_{switch} + V_{parasitic}$, since otherwise the memristor cell may switch. The second read voltage may include a voltage that is more than the first read voltage and below a write voltage.

[0032] The first and second read voltages may be targeted towards a high side of a valid read voltage range. This makes it likely that voltage drops induced across the memristor cell for both the first and second read voltages are above V_{th} , but not so high that the memristor cell is disturbed when its selector has too low of a V_{th} . According to an example, the method 500 may be optimized when the first and second read voltages are relatively close together, such that memristor cell voltage drops for both the first and second read voltages are above V_{th} even when V_{th} is on the high side. For instance, the first read voltage and the second read voltage may be within a close predetermined range, wherein the induced voltage drop range on the memristor cell for the predetermined range is at least above V_{th} with sufficiently high

likelihood, as V_{th} varies from cell to cell. Additionally, the predetermined range should be set so that, the likelihood that the difference between the memristor cell voltage drop induced by the second read voltage and V_{th} exceeds the memristor cell switching voltage is sufficiently small so as to allow an error correcting code with reasonable redundancy to recover the original data, prior to accidental switches or read disturb. According to an example, the first read voltage and the second read voltage are within a close predetermined range of each other and each of the first read voltage and the second read voltage is sufficiently high to induce a voltage drop on the cell that exceeds the selector threshold voltage and is sufficiently low to not cause the cell to switch to a different state.

[0033] In block 530, the read/write control module 106, for instance, may identify a difference value between the first memristor cell current and the second memristor cell current. The difference value may also be amplified by the read/write control module 106, for instance.

[0034] In block 540, the read/write control module 106, for instance, may determine a resistance state of the memristor cell based on the difference value. For example, in response to detecting the amplified difference value being above a predetermined high threshold value, the read/write control module 106 may read a low resistance state for the memristor cell. Alternatively, in response to detecting the difference value being below a predetermined low threshold value, the read/write control module 106 may read a high resistance state for the memristor cell. The predetermined high threshold value is generally higher than the predetermined low threshold value. In addition, the predetermined high threshold value and the predetermined low threshold value may be set to any desired values and may be determined through testing. If the response is found to fall between the low and high threshold values, an error condition may be indicated to higher level control circuits and/or processors.

[0035] The method 500 may effectively measure the rate of change of the current, which may be a better indicator of the resistance state than measuring the current at a single static data point. Since both the reads may be performed

at or below the normal read voltage of a memristor cell, which is below the write voltage for the memristor cell, it is unlikely that the method 500 causes any read disturbance.

[0036] Additionally, the method 500 may not only be effective in tolerating V_{th} variation in a selector. The method 500 may also tolerate high leakage or sneak current and the variation in leakage or sneak current. For example, assume that the sneak current of various memristor cells in the crossbar memory array are four times higher than the specified sneak current value (e.g., 750 nA vs. 190nA). The increase in the sneak current may have a maximum impact on the memristor cell that is farthest from the voltage sources 111 and 112. In $m \times n$ memory array 101, with top left most cell representing the memristor cell (1,1), the memristor cell (m,n) located at the nth column and mth row is most impacted due to a large half-selected row and column. This impact may manifest itself in the form of a reduced voltage drop across the selected memristor cell. However, since method 500 measures the rate of change of the current instead of the actual value of the current, the loss in read voltage due to sneak current may be handled similarly to the loss in read voltage due to V_{th} variation in the selector.

[0037] Accordingly, the method 500 provides a low overhead, dual-sensing reading scheme that trades-off access time to dramatically improve the read margin to tolerate variations in selector threshold and leakage or sneak current. Generally speaking, the method 500 may improve the read margin for memristor cells in the crossbar memory array and enhances the distribution of ON and OFF current for the memristor cells in the crossbar memory array.

[0038] FIG. 6 shows a dual-sensing circuit 600 that may be used to implement the examples described herein. The dual-sensing circuit 600 may receive a first read voltage V_{low} across a cell 602 from row driver 111 to sense a first cell current I_{low} at column driver 112, which is sampled and held at a holding circuit 604. The dual-sensing circuit 600 may then receive a second read voltage V_{high} across the cell 602 from row driver 111 to sense a second cell current I_{high} at column driver 112. The difference value between the second cell

current I_{high} and the first cell current I_{low} may be determined at a current differencing circuit 606. The difference value may then be compared to a predetermined threshold value ΔI_{ref} by a comparator circuit 608 to determine the resistance state for the cell 602. Other known electronic components may be added or substituted in the computer system 600.

[0039] What has been described and illustrated herein are examples of the disclosure along with some variations. The terms, descriptions and figures used herein are set forth by way of illustration only and are not meant as limitations. Many variations are possible within the scope of the disclosure, which is intended to be defined by the following claims -- and their equivalents -- in which all terms are meant in their broadest reasonable sense unless otherwise indicated.

CLAIMS

What is claimed is:

1. A method for determining a resistance state of a cell in a crossbar memory array, said method comprising:

applying, by a dual-sensing circuit, a first read voltage across a cell to sense a first cell current;

applying a second read voltage across the cell to sense a second cell current;

identifying a difference value between the first cell current and the second cell current; and

determining a resistance state of the cell based on the difference value.

2. The method of claim 1, wherein the first read voltage is lower than the second read voltage.

3. The method of claim 2, wherein the second read voltage is lower than a write voltage for the cell.

4. The method of claim 1, wherein the cell further includes a selector in series with the cell, the selector including a threshold voltage (V_{th}) to provide non-linearity to the cell.

5. The method of claim 4, wherein the first read voltage and the second read voltage are within a close predetermined range of each other, and wherein each of the first read voltage and the second read voltage is sufficiently high to induce a voltage drop on the cell that exceeds the selector threshold voltage

and is sufficiently low to not cause the cell to switch to a different state.

6. The method of claim 1, further comprising:

amplifying the difference value; and

wherein determining the resistance state of the cell includes:

reading a low resistance state for the cell in response to the amplified difference value being above a predetermined high threshold value; and

reading a high resistance state for the cell in response to the amplified difference value being below a predetermined low threshold value.

7. The method of claim 1, wherein the cell is a memristor device that is to switch between an ON state with a low resistance and to an OFF state with a high resistance.

8. The method of claim 7, wherein the memristor device includes a matrix material containing mobile dopants that are to be moved within the matrix material to dynamically alter the electrical resistance of the memristor device, wherein locations and characteristics of the mobile dopants remain stable until an application of a programming electrical field.

9. A data storage system to determine a resistance state of a cell in a crossbar memory array, comprising:

a processor;

a memory storing machine readable instructions that are to cause the processor to:

apply a first read voltage across a cell to measure a first cell current;

apply a second read voltage across the cell to measure a second cell

current, wherein the first read voltage is lower than the second read voltage;

identify a difference value between the first cell current and the second cell current; and

determine a resistance state of the cell based on the difference value .

10. The data storage system of claim 9, wherein the machine readable instructions are to cause the processor to amplify the difference value between the first cell current and the second cell current to determine the resistance state of the cell based on the amplified difference value.

11. The data storage system of claim 10, wherein to determine the resistance state of the cell, the machine readable instructions are to cause the processor to

read a low resistance state for the cell in response to the amplified difference value being above a predetermined high threshold value; and

read a high resistance state for the cell in response to the amplified difference value being below a predetermined low threshold value.

12. The data storage system of claim 9, wherein the machine readable instructions are to cause the processor to provide non-linearity to the cell to reduce leakage or sneak current across a conductor of the crossbar memory array.

13. A system, comprising a dual-sensing circuit to:

receive a first read voltage across a cell to measure a first cell current;

receive a second read voltage across the cell to measure a second cell current, wherein the first read voltage is lower than the second read voltage and the second voltage is lower than a write voltage;

determine a difference value between the first cell current and the second cell current;

amplify the difference value; and

determine a resistance state of the cell based on the amplified difference value.

14. The system of claim 13, wherein to determine the resistance state of the cell, the dual-sensing circuit is to:

read a low resistance state for the cell in response to the amplified difference value exceeding a predetermined high threshold value; and

read a high resistance state for the cell in response to the amplified difference value falling below a predetermined low threshold value.

15. The system of claim 13, wherein the cell further includes a selector in series with the cell, the selector including a threshold voltage (V_{th}) to provide non-linearity to the cell.

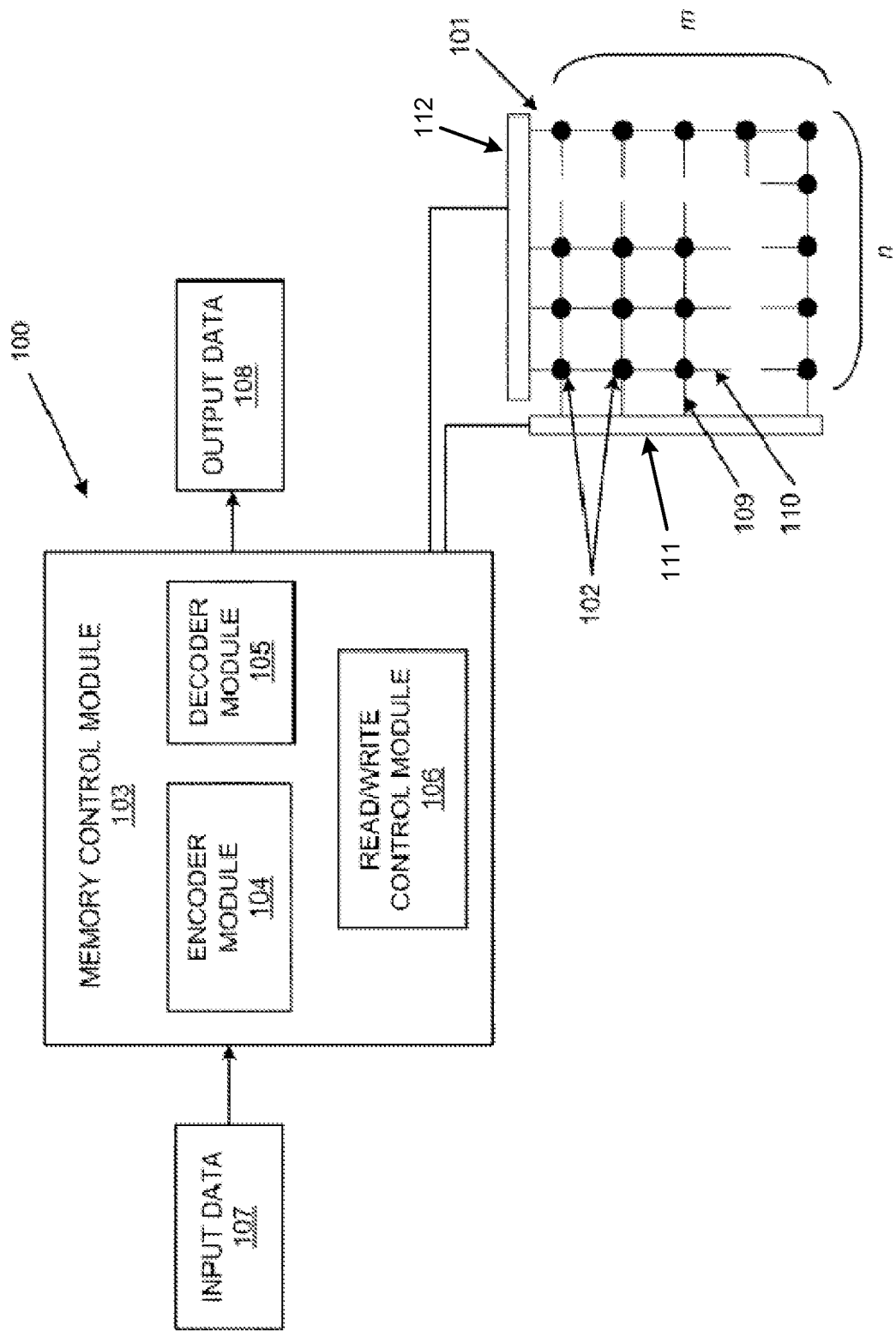


FIG. 1

2 / 6

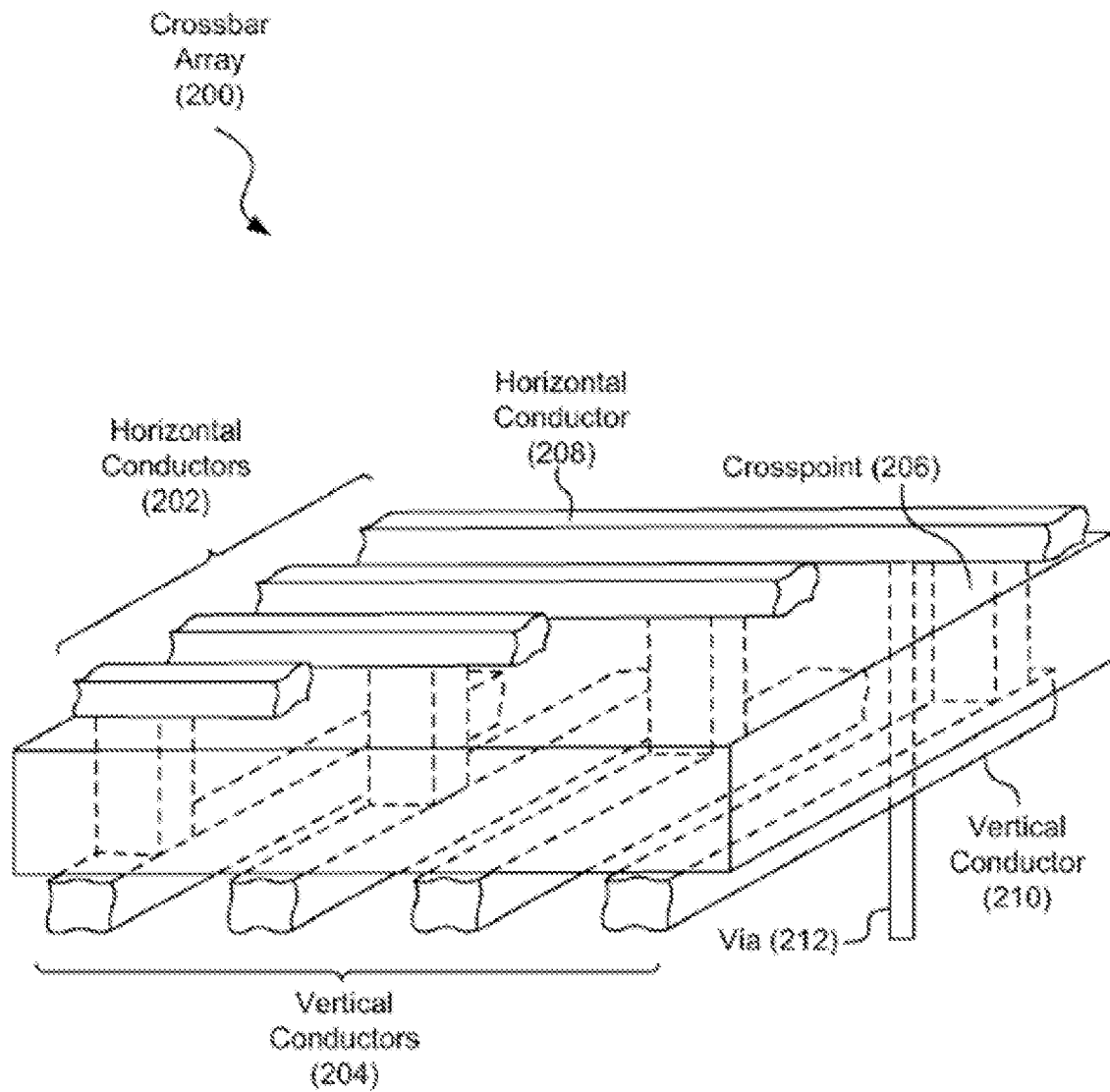


FIG. 2

300

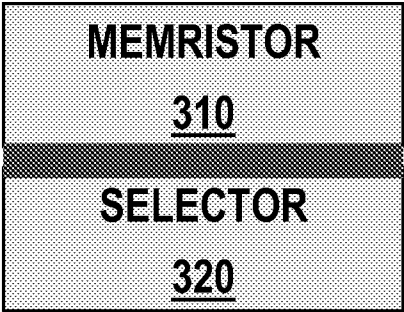


FIG. 3A

350

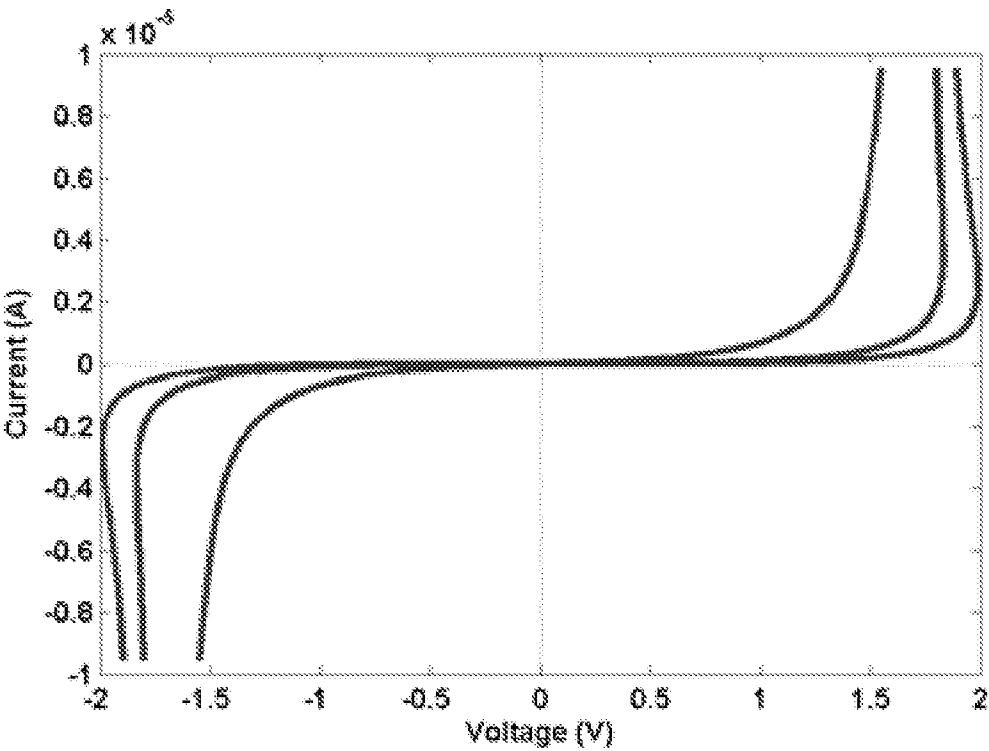


FIG. 3B

400

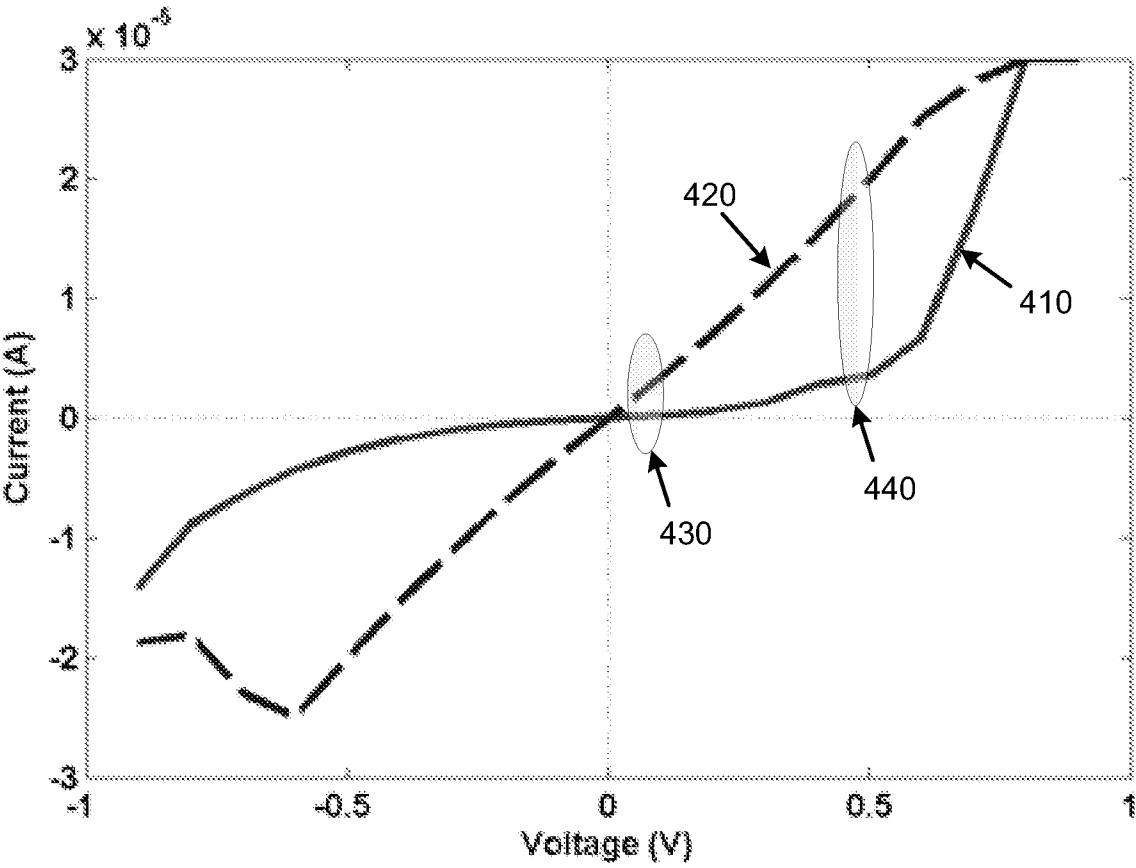
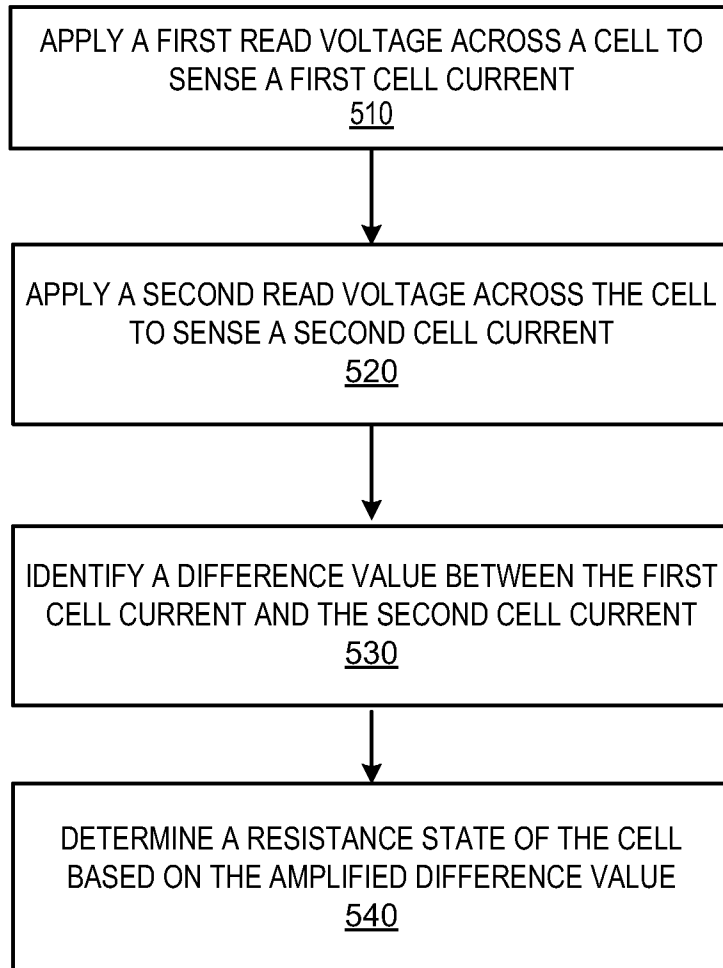
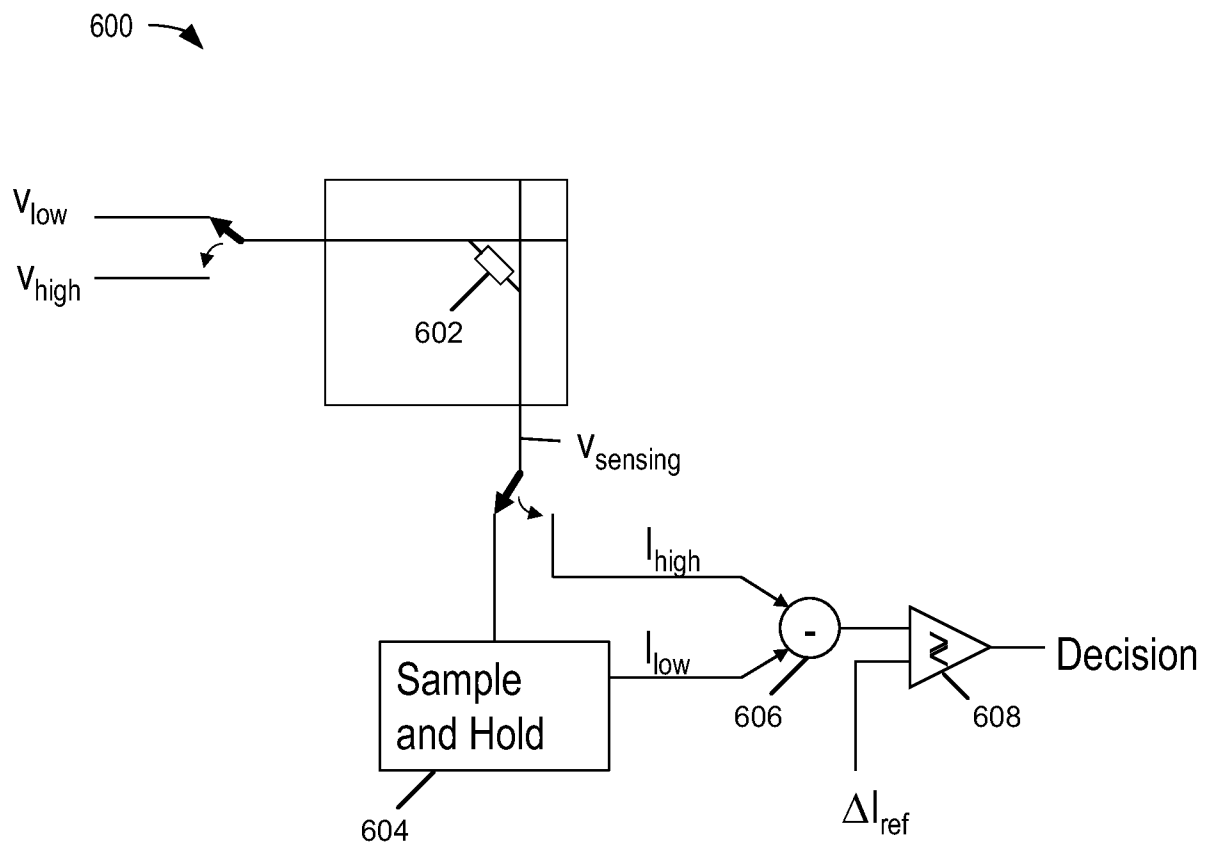


FIG. 4

5 / 6

500**FIG. 5**

6 / 6

**FIG. 6**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/049271**A. CLASSIFICATION OF SUBJECT MATTER****G11C 7/04(2006.01)i, G11C 7/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 7/04; G11C 7/00; G11C 8/00; G11C 11/15; G11C 7/06; G11C 7/02; G11C 11/00; G11C 7/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: crossbar, memory, cell, array, dual-sensing, circuit, read, voltage, memristor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002-0167838 A1 (FREDERICK A. PERNER) 14 November 2002 See paragraphs [0037], [0046]; claim 15; and figures 4, 6-7.	1-3, 9, 13
Y		4, 7-8, 12, 15
A		5-6, 10-11, 14
Y	US 2011-0286259 A1 (FREDERICK PERNER) 24 November 2011 See paragraphs [0002], [0015], [0026], [0037], [0039], [0055]; and figures 1-2, 6.	4, 7-8, 12, 15
A	US 2003-0206473 A1 (LUNG T. TRAN) 06 November 2003 See paragraph [0032]; and figure 6.	1-15
A	US 2004-0170048 A1 (SHENG TENG HSU) 02 September 2004 See paragraph [0026]; and figure 3.	1-15
A	US 2009-0175094 A1 (ROY E. SCHEUERLEIN) 09 July 2009 See paragraph [0033]; and figure 2.	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

13 March 2015 (13.03.2015)

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