

(19) (KR)  
(12) (B1)

(51) 。 Int. Cl.<sup>7</sup>  
H03H 11/40

(45)  
(11)  
(24)

2003 12 18  
10-0410536  
2003 12 01

(21) 10-2001-0005340  
(22) 2001 02 05

(65)  
(43)

2002-0065021  
2002 08 13

(73)

416

(72)

1 212 101 29/3

3 1162 APT10 1502

(74)

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(54)

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5a

, ,

1

2

3a 가 on transition

3b 가 off transition

4a 2a 가 on transition

4b	2b		가	off transition
5a, 5b		/		
5a		-		
5b		-		
6		1		
7	6			
8		2		
9		3		
10		4		
*			*	
10:		20:		
30:		31: -		
33: -		50, 90: -		
60, 100: -		70, 120:		
80, 130:				

[illegible]

3

가

:

가

가

가

2 4

(31)

(33)가

(transmitter) (10) (receiver) (20) (30)가

(30) (31) (33) (Input Buffer) (30)

(on) (off) 가

3a ('00000') ( '11111' ) (glitch) 3b 가

(on transition) , '11111' 'a' 'b' '가' ' ' ' ' 가

(' ' (10) 가 ) off

transition , '00000' 'c' 'd' , , 가

(' ' (10) 가 )

가 (off transition) , 2

2

가 /

가

가

5a, 5b

5a

(10)가 ' ' (10) NR2 I3 가 (30) 5a 5b

(10) R1 I1 , (30) ( NR1)

I2가 , , 'N' 1

(30) 5b , (10)가 ' ' (10) NR11 I21 가

(30) ( NR21) (10) R11 I31 , 가 'N' 1

가 , 가 / 가

3가  
(PIC: Programmable Impedance Controller)  
가 (Setup Time)  
(Hold)

1 6 7  
6 1 6 6 2  
(10) (31), (33), (4  
20)가 (31) VDDQ (31) (4  
(PIUC: Programmable Impedance Up Controller)  
1) (33) (PIDC: Programmabl  
e Impedance Down Controller)  
(31) (41) IA (43) (43)  
IB IA (41) (20) (50) IB Vref (43) (6  
0) (50) (60)

6 1  
DC ; (41) (43) (43) PIUC PI  
가 (41) (43) (31) (33) '가  
가 IA가 '가 가 IB가 (31) 가 (33)  
(50, 60)  
가 (31) (33) (31) (50)  
(33) (60)  
가  
가  
8 2  
8  
(31), (33) (20)가 (31) (61)  
(PIUC: Programmable Impedance Up Controller) (PIDC: Programmable Impedance Down Controll  
(33) (20) (63) (20) (63) (70) (6  
er) Vref (20) (70) Klatch (70) (70) (70)  
1) (80) 2  
8 ; PIUC PID

C (20) (61) (63) Klatch CMOS 가  
 PIUC ( PIDC ( ( (61) (63) 가 (31)  
 - (33) -  
 가 (80) 가 (31)  
 (33) (31) (80) 가  
 (33) (80) 가  
 9 10 3 4  
 9 3  
 9  
 (31), - 2 (33) (20)가 (10) (31) VDDQ  
 (31) (PIUC: Programmable Impedance Up Co  
 ntroller) (91) (33)  
 (PIDC: Programmable Impedance Down Controller) (93) IA IB NAND1  
 IB NAND2 (91) IA NAND1  
 가 (93) NAND2 (20) (91)  
 Vref (90) IB NAND2, (100)  
 (90) (100)  
 9 3 6  
 가  
 NAND (90, 100) (31) (33) 가  
 (31) (90) (33)  
 (100) 가  
 10 4  
 2 (10)  
 (31), - (33) (20)가 (31)  
 (PIUC: Programmable Impedance Up Controller) (111)  
 (33) (PIDC: Programmable Impedance Down Controller)  
 Vref (20) (120) (120) NAND  
 NAND11 (111) AND21 (113)  
 11 가 Klatch (130) (111), (113),  
 AND21 (120) NAND11, AND21 (120) 4  
 10 9 ;

D - AND - / 가 NAN  
 (130) (31) -  
 (33) , 가 (31) (130) 가  
 (33) (130) 가  
 (10) (20) (31) (33) 가 가  
 가 , 가  
 / 가  
 / 가  
 , 가 가  
 가 가  
 / ,  
 .

- (57)
1. , 가 :  
 가 가 , 가 가  
 ;
  2. 1 , 가  
 가
  3. 1 , - -  
 가
  4. 1 ,  
 가
  - 5.

가

$$\begin{array}{ccccc} & & : & & \\ 1 & & & 2 & & 1 \\ & & & 1 & & 2 \\ & & & & 2 & \end{array}$$

2

$$, \quad \text{가} \quad , \quad \text{가} \quad 1 \quad \text{가} \quad - \quad \text{가} \quad 2 \quad \text{가} \quad ;$$

가 1 - 가 -

가 2 가

**6.**

$$5 \quad 1 \quad , \quad : \quad , \quad - \quad , \quad 2 \quad , \quad 2 \quad , \quad 2$$

1

1

1

2

2

2

7.

가

2

1

2

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1. 가 - , 2. 가 -

フ

2

가

8.

1

2

9.

$$\vdots$$

가 / 가

•  
;

가

가

가

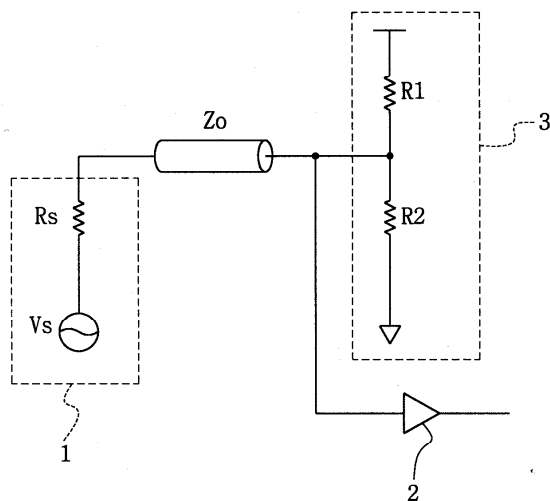
가

10.

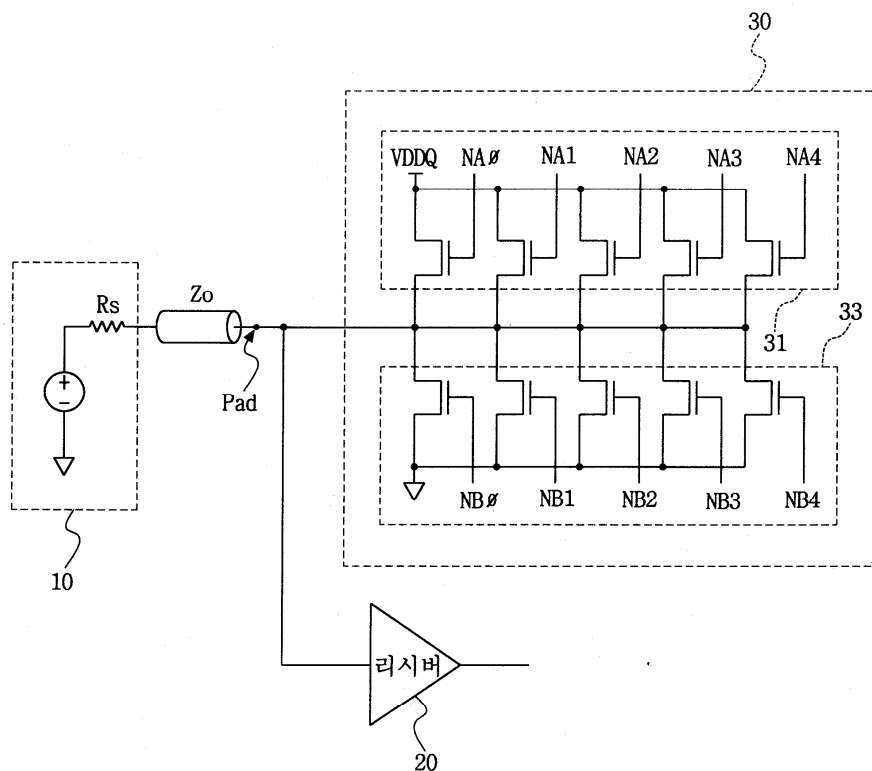
( )

11.  
( )

1

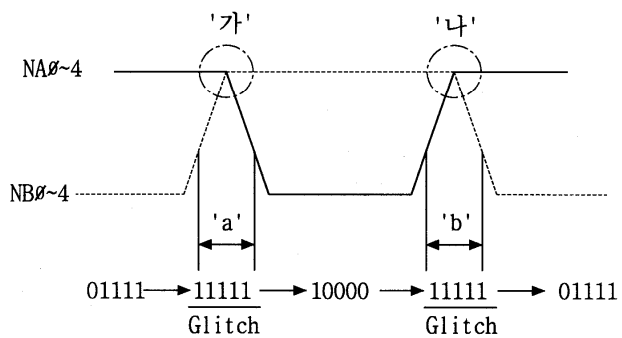


2

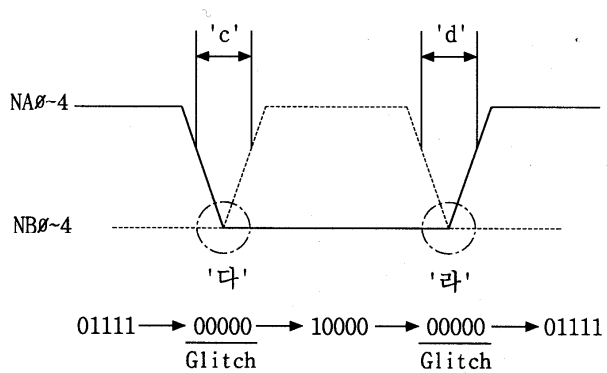




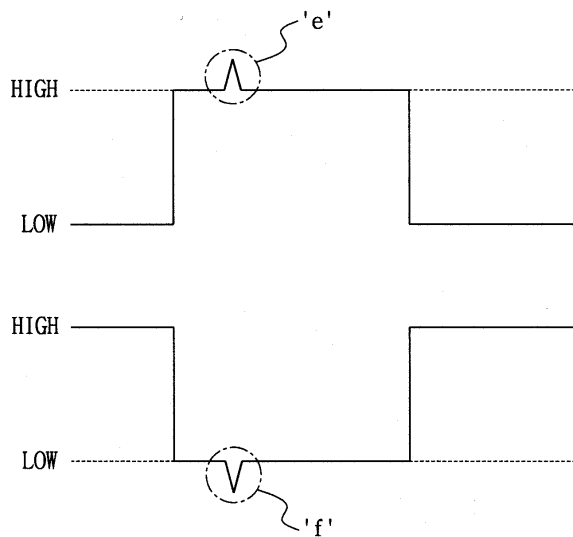
3a



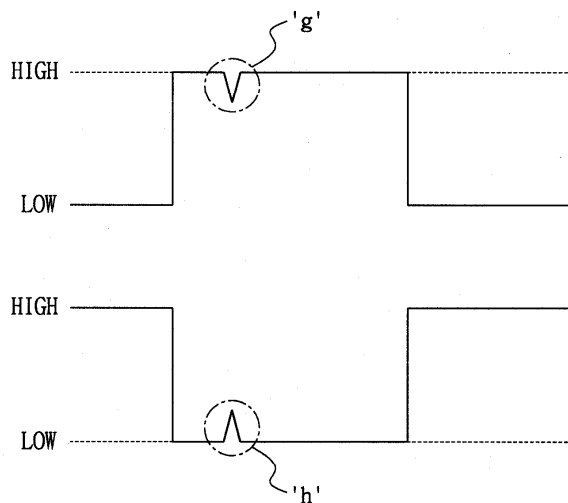
3b



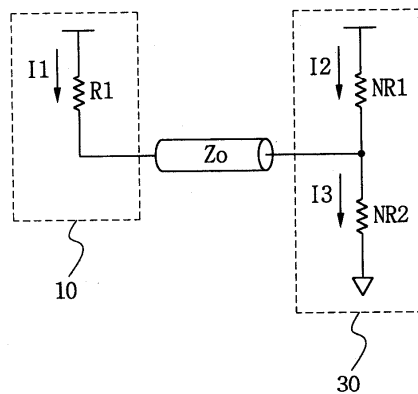
4a



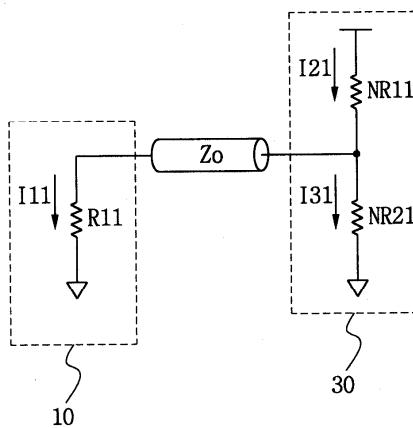
4b



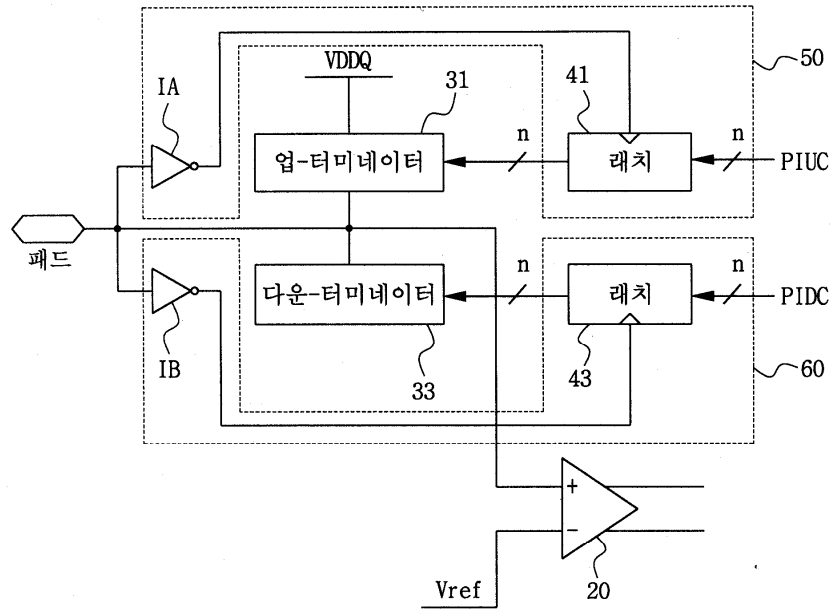
5a



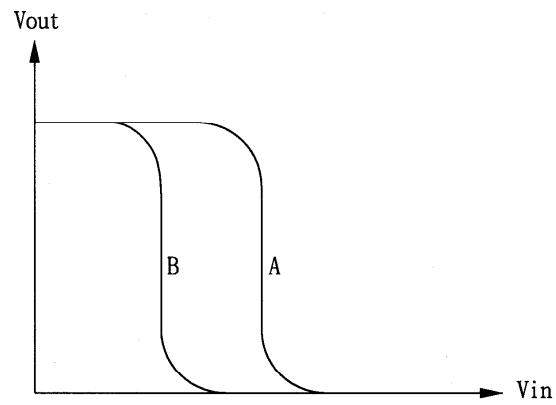
5b



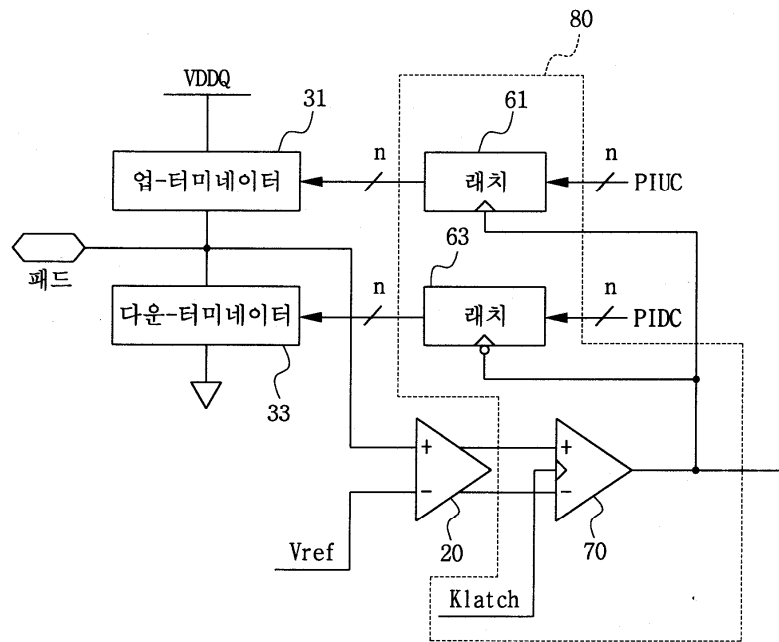
6



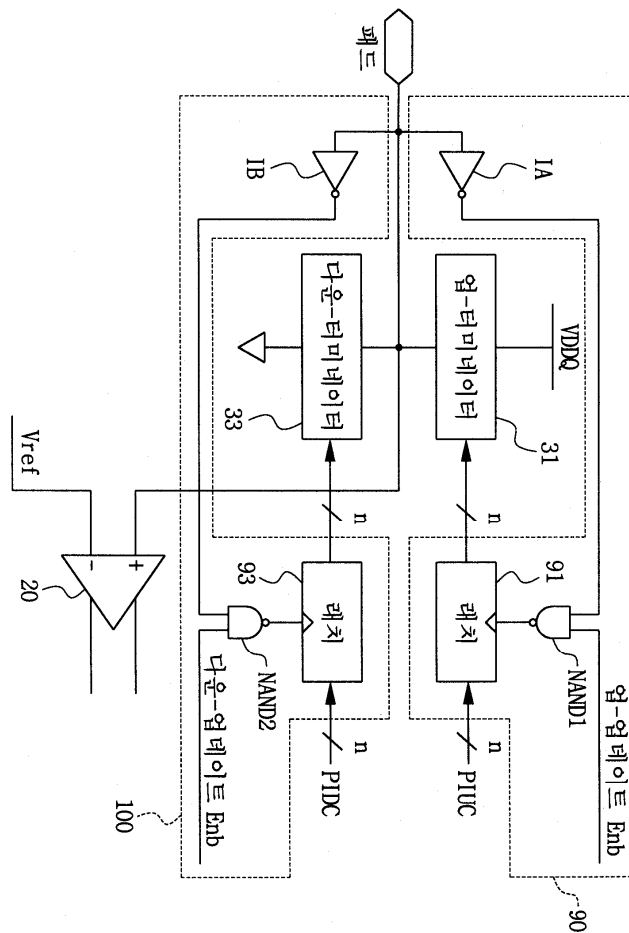
7



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9



10

