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[54] **FAIL TO FLASH INDICATOR CIRCUIT**  
11 Claims, 1 Drawing Fig.

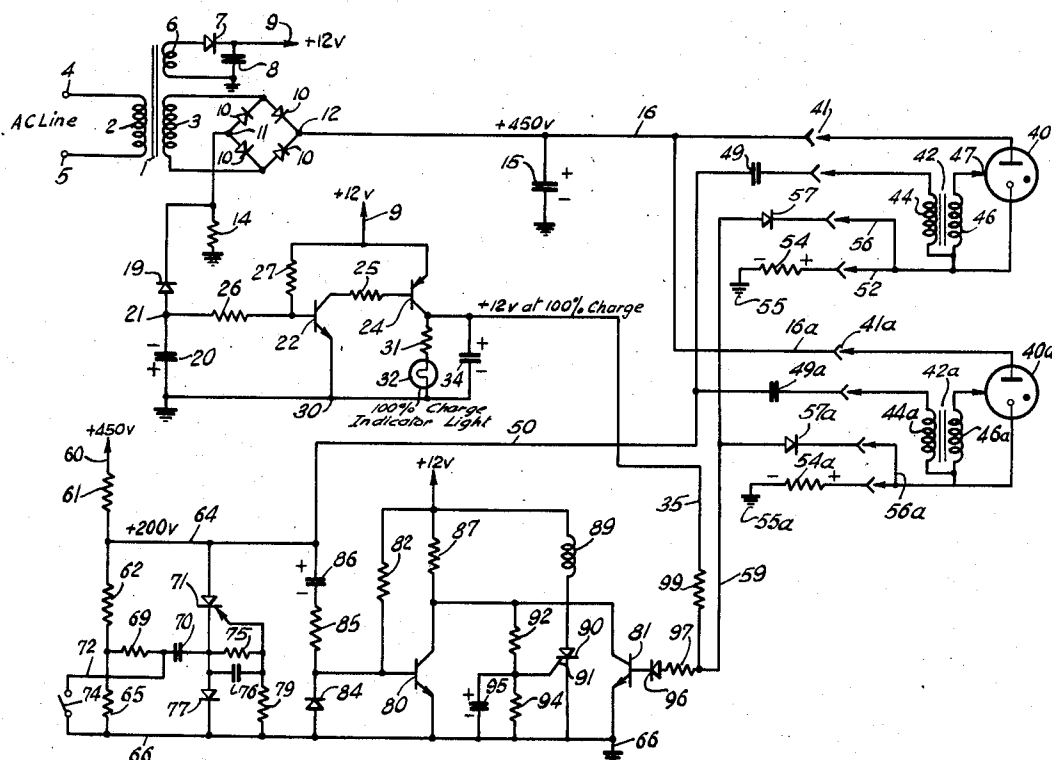
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11.5 A

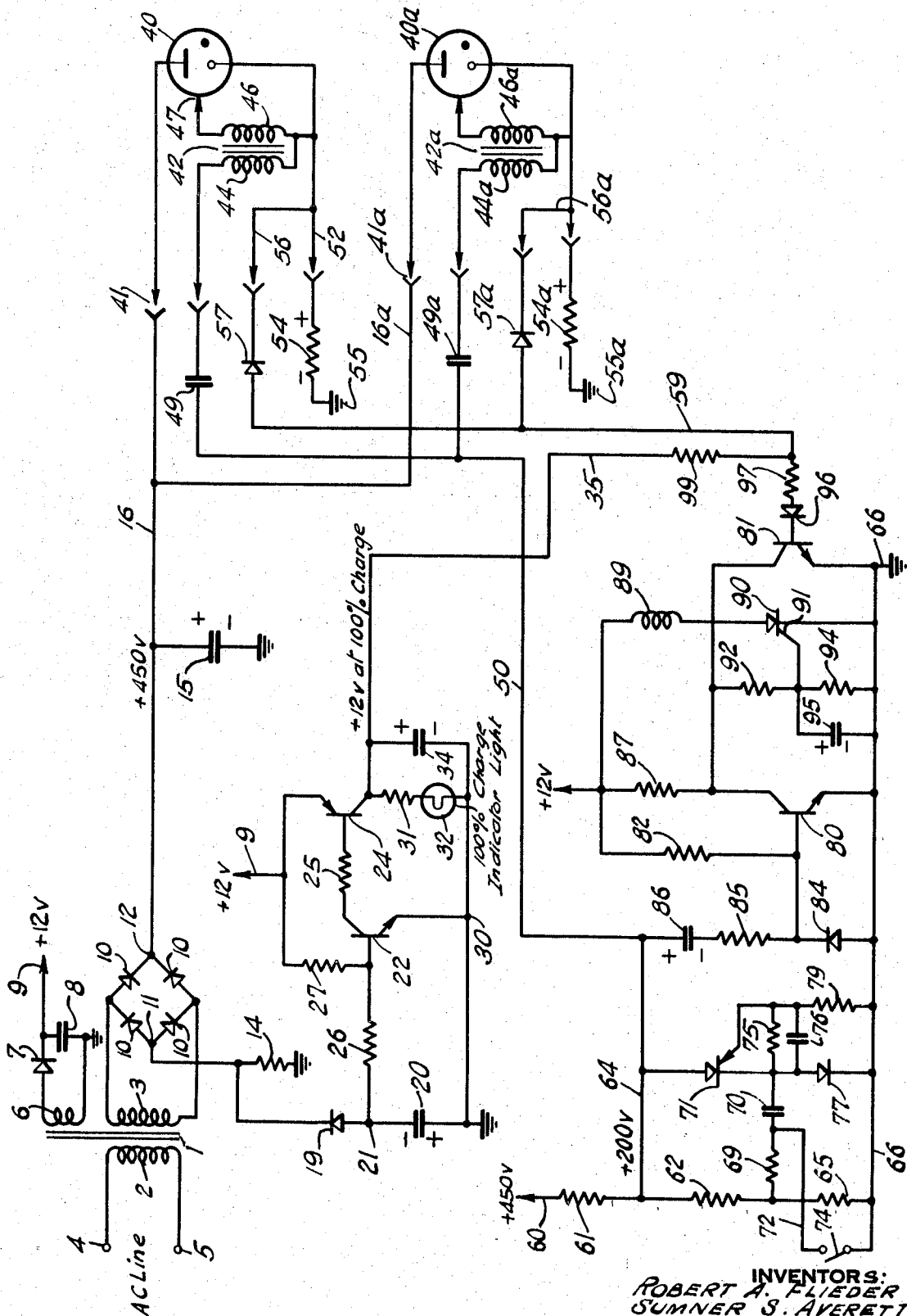
[56] **References Cited**

**UNITED STATES PATENTS**

3,246,201 4/1966 Michalski ..... 340/251 UX  
3,408,625 10/1968 Skinner ..... 340/73 X

**ABSTRACT:** A fail to flash alarm circuit including a main capacitor flash supply means and flash initiating means to discharge the capacitor into a discharge lamp. Control means includes alarm means so arranged as to be responsive to the actuation of the flash initiating means in the absence of current flow to the discharge lamp, this condition being determined by a current sensing resistor which is connected in the circuit to the discharge lamp to actuate switching means to block actuation of the alarm means. Bias means for the switching means may include a supervised charging circuit arranged so that bias means is not available to prevent a fail to flash alarm in the event the main capacitor is not fully charged. The bias means is connected through a voltage dropping resistor for normally dropping the control voltage to the second switching means. The drop in voltage is nullified current passed to the discharge lamp as sensed through the current sensing means and used to back bias the diodes to prevent the voltage drop and block actuation of the alarm. The circuit provides an alarm in the event the discharge lamp fails to be powered by current or in the event the main capacitor is not fully charged.





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**FAIL TO FLASH INDICATOR CIRCUIT**

This application is a streamlined continuation of application 625,519 filed Mar. 23, 1967, now abandoned.

**BACKGROUND OF THE INVENTION****1. Field of the Invention**

The present invention relates to discharge lamp circuits and more particularly to a fail to flash alarm circuit for indicating the failure to flash of one or more discharge lamps supplied through a single main capacitor.

**2. Description of the Prior Art**

The discharge lamps may be of the type used for exposing photographic film or other material sensitive to light. Generally a plurality of discharge lamps are used such as may be positioned in various locations on a scene for photographing a model or the like. Inasmuch as the flash is of short duration it is impossible for the operator to discern if one or more of the lamps have failed to flash resulting in low illumination upon certain parts of the scene.

In such cases it is necessary that the film or other sensitive material be developed and viewed before the failure to flash of one or more of the discharge lamps is discovered. Obviously this is time consuming and wasteful of model and operator's time. It is extremely desirable that indicating means be provided to indicate whether or not any of the lamps have failed to flash. It is also desirable that means be incorporated to indicate to the operator if a flash has taken place before the main capacitor has been fully charged. In some instances of course the operator may desire that the flash be made with a partially charged main capacitor, but in other cases an insufficient light level might result in which event the photographed scene would be underexposed.

Heretofore fail to flash circuits have been provided for electronic discharge lamps. In some cases such systems required isolated energy supply systems if more than one lamp was used.

**SUMMARY OF THE INVENTION**

The present invention aims to overcome the difficulties and disadvantages of prior circuits by providing a fail to flash alarm system operative for a plurality of discharge lamps connected to a single energy source.

In accordance with the invention the fail to flash alarm circuit includes means arranged to be operated by the flash initiating means to provide an alarm in the absence of a blocking control operative by current flow to each of the discharge lamps. Another feature of the invention is the incorporation of means so that said blocking means is inoperative in the event the main capacitor is not fully charged.

The circuit in accordance with the invention is advantageous in that interlocking means can be readily incorporated so that if a discharge lamp is wilfully disconnected the operation of the fail to flash alarm circuit will not be affected with respect to the operation of the other discharge lamps.

Other objects and advantages of the invention will be apparent from the following description and from the accompanying drawing which shows, by way of example, an embodiment of the invention.

**BRIEF DESCRIPTION OF THE DRAWING**

In the drawing the single FIGURE shows a schematic wiring diagram of a circuit in accordance with the invention.

**DESCRIPTION OF THE PREFERRED EMBODIMENT**

Referring to the drawing there is shown a transformer 1 having a primary 2 and a secondary 3. The primary 2 has a pair of terminals 4 and 5 adapted to be connected to a source of alternating current. A second secondary winding 6 is connected in series with a diode 7 to provide an output connected across a capacitor 8 having one terminal grounded and its other terminal providing a source 9 of direct current of a voltage preferably of the magnitude of about 12 volts positive. The

secondary winding 3 is connected across bridge connected diodes 10 to provide a source of direct current across terminals 11 and 12 of the bridge. Terminal 11 is connected to ground through a current sensing resistor 14, terminal 12 is connected to one terminal of a main storage capacitor 15 having connected thereto a lead 16 providing a source of direct current the potential of which may be about 450 volts. The current sensing resistor 14 is incorporated into a circuit which senses the lack of a voltage drop thereacross. This circuit includes a diode 19 connected in series with a capacitor 20 to ground, connection 21 between the diode 19 and capacitor 20 providing a source of negative potential responsive to pulsating current flow through the current sensing resistor 14. A pair of transistors 22 and 24 are connected as a direct connected amplifier, transistor 22 preferably being of the NPN-type, while transistor 24 is of the PNP-type. The collector of transistor 22 is connected to the base of transistor 24 through a resistor 25. The base of transistor 22 is connected to the midpoint of a voltage divider including resistors 26 and 27. Resistor 26 is connected at 21 to the capacitor 20. Resistor 27 is connected to the positive 12 volt supply 9, the power supply being also connected to the emitter of the transistor 24. The emitter of transistor 22 is grounded as indicated at 30 while the collector of transistor 24 is connected to ground through a resistor 31 and indicating means which may be a lamp 32. A filter capacitor 34 is connected from the collector of transistor 24 to ground, the ungrounded terminal of the capacitor providing a source of positive potential and the lamp 32 providing a light signal when the transistor 24 is "on".

The operation of the charge indicating circuit in accordance with the invention is based on the fact that at 100 percent charge on the main capacitor bank the current flow into the capacitor is negligible. Therefore the circuit may be quite simply described as a current flow indicator.

The secondary 3 through the rectifying diodes 10 provides a voltage of about 450 volts to ground. The second secondary 6 through the diode 7 provides a supply of 12 volts direct current. The potential sensed across the resistor 14 is passed through the diode 19 to the capacitor 20, the diode 19 being poled so that the capacitor 20 acquires a negative potential with respect to ground. The constants of the circuit are so arranged that both of the transistors 22 and 24 are saturated or turned "on" in the absence of a negative potential on the capacitor 20.

During the period of charge of the main capacitor 15 there is a pulsating voltage drop across the resistor 14 which is used to charge the capacitor 20 to the desired negative potential. At this time the negative charge on capacitor 20 overcomes the effect of the positive potential on the resistor 27 so as to cause the transistors 22 and 24 to be turned "off". In other words the junction of resistors 26 and 27 changes from a positive potential in the steady state or charged condition of the main capacitor 15 to a negative potential when charging current is flowing to the main capacitor 15. Therefore the transistors 22 and 24 go from an "on" condition in steady state or charged condition of the main capacitor 15 to an "off" condition while the charging current is flowing. Transistor 24 provides a switching action between the plus 12 volt supply 9 and ground for the lamp 32 and for a source of potential on the filter capacitor 34. Upon the absence of the negative potential on the capacitor 20, after the main capacitor 15 has become charged, the bias on the transistors 22 and 24 is from the 12 volt power supply through resistor 27. Both transistors are switched "on" and therefore the indicator lamp 32 is turned "on" providing the 12 volt supply across the capacitor 34. This charge indicator circuit has been described and claimed in our copending U.S. Pat. application, Ser. No. 808,574 filed on even date herewith.

A lead 35 is termed the 12 volt 100 percent charge lead and conducts bias potential to circuitry to be later described.

The main storage capacitor 15 is adapted to supply a discharge lamp 40 through disconnect means 41. The discharge lamp 40 may be provided with the usual starting or

triggering transformer 42 having a primary 44 and a secondary 46. The secondary 46 may be connected to the discharge lamp 40 by means of a third electrode 47 bearing against the surface of the envelope of the discharge lamp 40. The primary of the starting or triggering is connected through a triggering capacitor 49 and a lamp triggering lead 50 to a 200 volt bus.

Ground lead 52 of the discharge lamp 40 is connected through a current sensing resistor 54 to ground as indicated at 55. A lead 56 connected to the lead 52 between the current sensing resistor 54 and the discharge lamp 40 provides means for connecting the current sensing resistor 54 to a diode 57 and a lead 59 which will be termed the blocking circuit lead.

Connected in parallel with the lamp 40 may be connected one or more lamps 40a which may be connected through disconnect members 41a in parallel with the disconnect member 41 for lamp 40 and the associated circuitry. The associated circuitry in connection with lamp 40a is identified by the same indicia as used in connection with lamp 40 with the addition of the letter "a".

A triggering circuit for the discharge lamps 40 and 40a includes means to charge and discharge the triggering capacitor 49, 49a. The triggering circuit used is similar to that described in U.S. Pat. No. 3,375,403 issued to one of the inventors herein on Mar. 26, 1968. The triggering circuit includes a lead 60 adapted to be connected to the 450 volt direct-current supply. To lead 60 is connected voltage divider resistors 61 and 62, the junction having a lead 64 attached thereto providing a 200 volt supply. The resistor 62 is connected in series with a resistor 65 and to ground 66. The junction between resistors 62 and 65 is connected through a resistor 69 and a capacitor 70 to the cathode of an SCR 71. The junction between resistor 69 and capacitor 70 is connected by a lead 72 to a switch 74 connected to ground 66.

The SCR 71 has its anode connected to the 200 volt supply 64 and its cathode is connected to the capacitor 70 and to a resistor 75 and a capacitor 76 connected in parallel, the cathode being also connected through a diode 77 to ground. The other terminals of the resistor 75 and capacitor 76 are connected together and to the gate of SCR 71 and through a resistor 79 to ground 66. This circuitry including the SCR 71 is the triggering means for triggering capacitors 49 and 49a, the triggering thereof being initiated by closing switch 74.

Means for providing an alarm signal includes NPN-transistor 80 having its collector connected to the collector of an NPN-transistor 81, the emitters of both transistors being connected to ground 66. The base of transistor 80 is connected through a resistor 82 to the 12 volt power supply 9. Also connected to the base of the transistor 80 is an isolation diode 84 connected to ground and a resistor 85 connected through capacitor 86 to the 200 volt lead 64. The collectors of both transistors 80 and 81 are connected through a resistor 87 to the 12 volt supply. A buzzer or other suitable alarm producing means 89 is connected between the 12 volt supply and an SCR 90 to ground 66. The gate 91 of the SCR 90 is connected to the junction of resistors 92 and 94, resistor 94 being paralleled by a capacitor 95. The transistor 81 has its base connected through a diode 96 and a resistor 97 to a resistor 99 supplied through the 12 volt charging lead 35. The junction between resistors 97 and 99 is connected to the blocking circuit lead 59.

In the operation of the circuit in accordance with the invention it is incorporated with the charging circuit for a main capacitor 15 and one or more discharge lamps 40. The main supply capacitor 15 for the discharge lamp is charged from the transformer 1 through the diodes 10. A current sensing resistance 14 is incorporated between the rectifiers 10 and the main capacitor 15. The charge indicator circuit incorporating the transistors 22 and 24 operates to energize the lamp 32 when the main supply capacitor is fully charged as evidenced by the absence of an appreciable current through the current sensing resistor 14. At the same time as the indicator lamp 32 is energized the 12 volt 100 percent charge lead 35 is energized thereby providing a 12 volt potential on the top of the

resistor 99. Simultaneously the 200 volt bus 64 is energized from the 450 volt supply and the triggering capacitors 49 and 49a have become charged to ground through the primary of the triggering transformers 42 and 42a.

The circuit so far described is ready for flashing which is achieved by closing the switch 74 so as to switch the SCR 71 into conduction to discharge the triggering capacitor 49 through the triggering transformer 42 to ground and through the diode 77 connected to the cathode of SCR 71. Before the triggering of the SCR 71 the capacitor 70 has been charged to about 30 volts from the divider string incorporating resistors 61, 62, 65, through resistor 69 and diode 77. Condenser 76 is normally at zero voltage due to the resistor 75 connected in shunt across it. Upon the closing of the switch 74 the junction of capacitor 70 and resistor 69 is brought to ground potential which applies a negative 30 volt pulse to the cathode terminal of SCR 71. Diode 77 prevents capacitor 70 from discharging to ground because it is backbiased at that point, but does lower the potential of the cathode to minus 30 volts. Since the potential of the gate of the SCR 71 is held to zero voltage through resistor 79 there is in effect a positive pulse to the gate with respect to the cathode which fires SCR 71. The resistance 75 is used to decrease the sensitivity of the triggering so that SCR 71 is not fired by transients. Capacitor 76 is a filter condenser also used to protect the gate against transients. Resistor 79 limits the current from condenser 70 through the gate. The flash initiating means is used to trigger means normally responsive thereto to produce an alarm. Such means includes the transistor 80 which controls the buzzer 89 by causing the triggering of SCR 90. The transistor 80 is normally "on" by reason of the bias through resistor 82. While the transistor 80 is in a steady state condition the capacitor 86 has been charged to about 200 volts through the emitter of the transistor 80 and the bus 64. When the triggering circuit is operated the bus 64 is brought practically to ground potential thereby causing a negative pulse from capacitor 86 to turn "off" transistor 80. The "off" time of transistor 80 depends upon the time constant of the resistor 85 and the capacitor 86. This time constant must be long enough so that capacitor 95 can acquire a sufficient charge so that its potential is great enough to fire SCR 90.

Upon turning "off" the transistor 80 by the negative pulse from the capacitor 86 its collector rises in voltage. The gate of SCR 90 is connected to the voltage divider 92 and 94. The capacitor 95 gradually becomes charged during the "off" period of the transistor 80 (held off by its base potential from the RC circuit of resistor 85 and the capacitor 86) finally triggering the gate 91 of SCR 90.

In the event one of the lamps 40 or 40a fails to flash, or in the event there is no potential on the lead 35, the actuation of the alarm 89 will now be described. The transistor 81 is connected across the transistor 80 but the transistor 81 is normally "off" and is turned "on" by a positive pulse on its base. By reason of the connection used wherein the 12 volt supply is passed through the voltage dropping resistor 99 and the diode 47 through the current sensing resistor 54 to ground, the voltage is normally lowered at the bottom of resistor 99 to practically ground potential or actually to the approximately one half volt junction voltage of the diode 57. Under this condition of low voltage on its base the transistor 81 is normally "off". Upon the discharge of lamp 40 the current through the current sensing resistor 54 causes a potential to be applied to the cathode of the diode 57 backbiasing it so as to prevent the flow of current therethrough. The reduction in current flow through the resistor 99 causes the positive potential to rise on the base of the transistor 81 thereby turning "on." In the event one or more lamps 40a are connected to the system, in that the disconnect means 41 are engaged, but for some reason one or more of the lamps 40a fail to flash at the same time as lamp 40 is flashed, it will be noted that there is no backbiasing of the diodes 57 and 57a. Therefore, the current continues to flow through the diodes 57 and 57a from lead 35, resulting in the absence of sufficient positive voltage at the base of transistor

81 to turn it "on." thereby allowing capacitor 95 to become charged so as to trigger SCR 90 and thereby causing the alarm signal to operate indicating that one or more of the lamps 40 or 40a have failed to flash. Of course the same situation applies when the capacitor 34 is not fully charged in that transistor 24 is still turned "off" thereby deenergizing the 12 volt lead 35 which results of course in lack of positive potential at the base of transistor 81.

Perhaps the operation of the circuit will be better understood by reviewing the conditions present in the circuit. In the condition under which both lamps flash a voltage drop is produced across the current sensing resistors 54 and 54a in the polarity to backbias diodes 57 and 57a. By blocking the diodes the base of transistor 81 receives a forward bias through resistor 99 which has the effect of turning "on" transistor 81 thereby dropping the collector potential of transistors 80 and 81 to ground. The gate of SCR 90 is connected to the collectors of these transistors through the voltage divider 92 and 94. Since both collectors are at ground potential the gate of SCR 90 is not allowed to rise and therefore there is no alarm signal. This is perhaps better understood by noting that in the steady state before the discharge lamp has been flashed SCR 90 had been kept "off" as transistor 80 had been turned "on" which kept the gate 91 potential down. Upon actuation of the trigger circuit by closing the switch 74 the transistor 80 is momentarily turned "off" and its collector momentarily rises, the turnoff time depending upon the time constant of resistor 85 and capacitor 86. The filter condenser 95 does not cause SCR 90 to fire because of lack of sufficient charge potential. Meanwhile transistor 81 is turned "on" to bring the collector down to zero before capacitor 95 can become sufficiently charged so as to trigger the gate for SCR 90, and the alarm signal is not turned on.

Now assume again the situation whereby one of the lamps 40 or 40a fails to fire. Just prior to the closing of the triggering switch 75 transistor 81 is biased "off" due to conduction through the diodes 57 and 57a to ground resulting in the lowering of the base potential for the transistor 81. If one of the lamps is not discharged there is no backbiasing potential provided by its current sensing resistor 54 or 54a and the flow of current to ground through the current diode 57 or 57a maintains the potential lowered at the base of transistor 81 holding it "off." Meanwhile the transistor 80 is held off for the period of the time constant of the resistor 85 and the capacitor 86 during which period the capacitor 95 has been charged to trigger the SCR 90 into conduction turning on the alarm 89. It should be noted that the back biasing of one or more of the diodes 57 or 57a has no effect on the current flow through any of the other diodes to ground. This is an important feature when considering the interlock feature in that if one or more of the lamps are removed and its lead 56 or 56a opened, the cathode of the corresponding diode 57 or 57a is disconnected from ground thereby preventing the flow of current therethrough which would tend to hold the transistor 81 in the "off" position.

The following circuit components were used in an illustrative exemplification of the invention as set out in the figure and are given by way of example:

|               |                |
|---------------|----------------|
| Diode 7       | 50. PIV diode  |
| Diode 10      | 600 PIV diodes |
| Diode 19      | 50 PIV diode   |
| Transistor 22 | 2N5172         |
| Transistor 24 | 2N3638         |
| Capacitor 20  | 50 mfd.        |
| Capacitor 34  | 50 mfd.        |
| Resistor 14   | 5 ohms         |
| Resistor 25   | 510 ohms       |
| Resistor 26   | 1              |
| Resistor 27   | 4.3 kΩ         |
| Resistor 31   | 30 ohms        |
| Diode 84      | 50 PIV         |
| Diode 96      | 50 PIV         |
| Diode 77      | 50 PIV         |
| Diode 57      | 600 PIV        |
| SCR 71        | C106B2         |
| SCR 90        | C106B2         |
| Transistor 80 | 2N5172         |

|                    |            |
|--------------------|------------|
| Transistor 81      | 2N5172     |
| Capacitor 70       | 0.1 mfd.   |
| 76                 | 1 mfd.     |
| Capacitor 86       | 0.1 mfd.   |
| Capacitor 95       | 1 mfd.     |
| Resistor 61        | 150 kΩ     |
| Resistor 62        | 110 kΩ     |
| Resistor 65        | 27 kΩ      |
| Resistor 69        | 100 kΩ     |
| Resistor 75        | 100 ohms   |
| Resistor 79        | 100 ohms   |
| Resistor 85        | 22 kΩ      |
| Resistor 82        | 4.3 kΩ     |
| Resistor 87 2.2 kΩ |            |
| Resistor 92        | 680 kΩ     |
| Resistor 94        | 330 kΩ     |
| Resistor 54        | 0.05 ohms  |
| Resistor 97        | 1 kΩ       |
| Resistor 99        | 22 kΩ ohms |

While the invention has been described and illustrated with reference to a specific embodiment thereof, it will be understood that other embodiments may be resorted to without departing from the invention. Therefore, the form of the invention set out above should be considered as illustrative and not as limiting the scope of the following claims.

We claim:

1. A fail to flash alarm circuit for a discharge lamp circuit including flash supply means incorporating a main capacitor and flash initiating means to discharge the flash supply means to the discharge lamp, the fail to flash circuit comprising alarm means responsive to the actuation of said flash initiating means, and alarm override means responsive to the current flowing in said discharge lamp and coupled to said alarm means for preventing actuation of said alarm means when current flows from said flash supply means to said discharge lamp and for allowing actuation of said alarm means when current fails to flow from said flash supply means to said discharge lamp, whereby said alarm circuit signals a fail to flash condition by the absence of current flow to the discharge lamp upon the actuation of said flash initiating means.
2. A fail to flash circuit according to claim 1 in which said alarm means normally responsive to the actuation of said flash initiating means includes transistor switching means, control means for said transistor responsive to said flash initiating means, and time delay means holding off actuation of said alarm means for a predetermined time.
3. A fail to flash circuit according to claim 2 in which said time delay means is a RC circuit.
4. A fail to flash alarm circuit for a discharge lamp circuit including flash supply means incorporating a main capacitor and flash initiating means to discharge the flash supply means to the discharge lamp, said fail to flash circuit comprising alarm means normally responsive to the actuation of said flash initiating means, and means responsive to current flow from said flash supply means to the discharge lamp for preventing actuation of said alarm means whereby said alarm circuit signals a fail to flash condition by the absence of current flow to the discharge lamp upon the actuation of said flash initiating means, said means responsive to current flow from said flash supply means to said discharge lamp including a current sensing resistor adapted to be connected in series with said discharge lamp.
5. A fail to flash circuit according to claim 4 in which said means responsive to current flow from said flash supply means includes switching means, circuit means connected to said switching means so that actuation of said switching means blocks normal operation of said alarm means, bias means for said switching means, means normally causing current flow in one direction to said current sensing resistor thereby reducing said bias means, said circuit so arranged that current flow from said current sensing means responsive to current flow from said flash supply means to said discharge lamp is in the opposite direction from said one direction so that the effect on said bias means is nullified when discharge current flows to said lamp, said unreduced bias means effective to control said switching means to block normal operation of said alarm means.

6. A fail to flash alarm circuit for a discharge lamp circuit including flash supply means incorporating a main capacitor and flash initiating means to discharge the flash supply means to the discharge lamp, the fail to flash circuit comprising alarm means normally responsive to the actuation of said flash initiating means, and means responsive to current flow from said flash supply means to the discharge lamp for preventing actuation of said alarm means whereby said alarm circuit signals a fail to flash condition by the absence of current flow to the discharge lamp upon the actuation of said flash initiating means, said means responsive to current flow from said flash supply means to said discharge lamp including a current sensing resistor adapted to be connected in series with said discharge lamp, transistor switching means, means connecting said transistor switching means in a circuit with said alarm means normally responsive to the actuation of said flash initiating means so that normal alarm operation is blocked by operation of said switching means, bias means normally effective to actuate said switching means, voltage dropping means connected to said bias means, said current sensing resistor adapted to produce a voltage responsive to said current flow, circuit means to apply said voltage in opposition to the voltage of said bias means whereby upon a failure to flash of said discharge lamp said switching means is inoperative and said alarm is actuated.

7. A fail to flash circuit according to claim 6 in which said bias means includes a source of current, a voltage dropping resistor and a diode connected in series to said voltage sensing resistor, said switching means controlled through said voltage dropping resistor, so that normally the bias on the switching means is the junction voltage of the diode, the voltage dropping resistor so connected that potential therefrom is in opposition to the junction voltage of the diode so that the diode is back biased whereby the bias voltage on the switching means rises causing actuation thereof and the blocking of said fail to flash alarm.

8. A fail to flash circuit according to claim 7 in which said source of current includes means responsive to current flow from said charging circuit to said capacitor below a predetermined amount, and switching means for said source of current controlled by said last mentioned means so that said source of current is not available until the desired amount of charge is on the capacitor bank, whereby a fail to flash signal is provided in the absence of potential from said source upon the actuation of said flash initiating means.

9. A fail to flash circuit according to claim 7 in which said source of current includes a main current sensing resistor

adapted to be connected in series with the main capacitor for sensing current flow thereto, a capacitor and a diode connected in series across said current sensing resistor, a pair of transistors connected as a direct coupled amplifier and controlled by the potential on said capacitor to provide closed switching means in the absence of a potential on said capacitor so that the source of current is not connected to said voltage dropping resistor until current flow has ceased to said main capacitor whereby an actuation of the flash initiating means will produce a fail to flash alarm.

10. A fail to flash alarm circuit for a discharge lamp circuit including flash supply means incorporating a main capacitor and flash initiating means to discharge the flash supply means to the discharge lamp, the fail to circuit comprising alarm means normally responsive to the actuation of said flash initiating means, and means responsive to current flow from said flash supply means to the discharge lamp for preventing actuation of said alarm means whereby said alarm circuit signals a fail to flash condition by the absence of current flow to the discharge lamp upon the actuation of said flash initiating means, said alarm means normally responsive to the actuation of said flash initiating means including first transistor means control means for said first transistor responsive to said flash initiating means, and time delay means, a current sensing resistor adapted to be connected in series with said discharge lamp, second transistor switching means connected in opposition to said first transistor switching means and blocking operation of said alarm means, bias means effective to operate said second switching means, voltage dropping means for said bias means, diode means connected between said voltage dropping means and said current sensing means, said bias means poled with respect to said current sensing means so that current flow through said diode is blocked by current from said current sensing means whereby upon the usual operation of said discharge by said flash initiating means the failure to flash alarm is not given but is given in the event of the absence of current flow in said current sensing means.

11. A fail to flash circuit according to claim 10 in which said bias means includes a main current sensing resistor adapted to be connected in series with the main capacitor for sensing current flow thereto, a capacitor and a diode connected in series across said current sensing resistor, a pair of transistors connected as a direct current amplifier and controlled by the potential on said capacitor to provide closed switching means in the absence of a potential on said capacitor so that the source of current is not connected to said voltage dropping resistor until current flow has ceased to said main capacitor.

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