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**Asplund**

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[45] **Aug. 14, 1973**


[54] **ELECTRONIC IGNITION TIMING SYSTEM FOR INTERNAL COMBUSTION ENGINES**


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[73] Assignee: **GTE Sylvania Incorporated,** Seneca Falls, N.Y.



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[52] **U.S. Cl.** ... **123/146.5 A,** 123/148 E, 123/117 R

[51] **Int. Cl.** ..... **F02p 3/02,** F02p 5/00

[58] **Field of Search** ..... 123/148 E, 146.5 A, 123/117 A, 117 R



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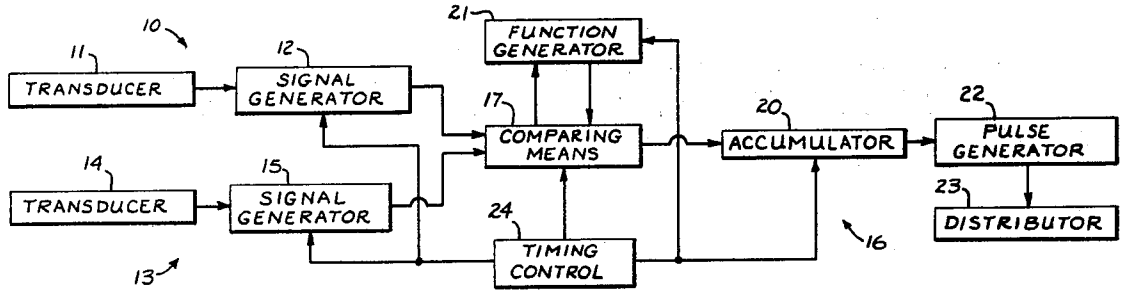
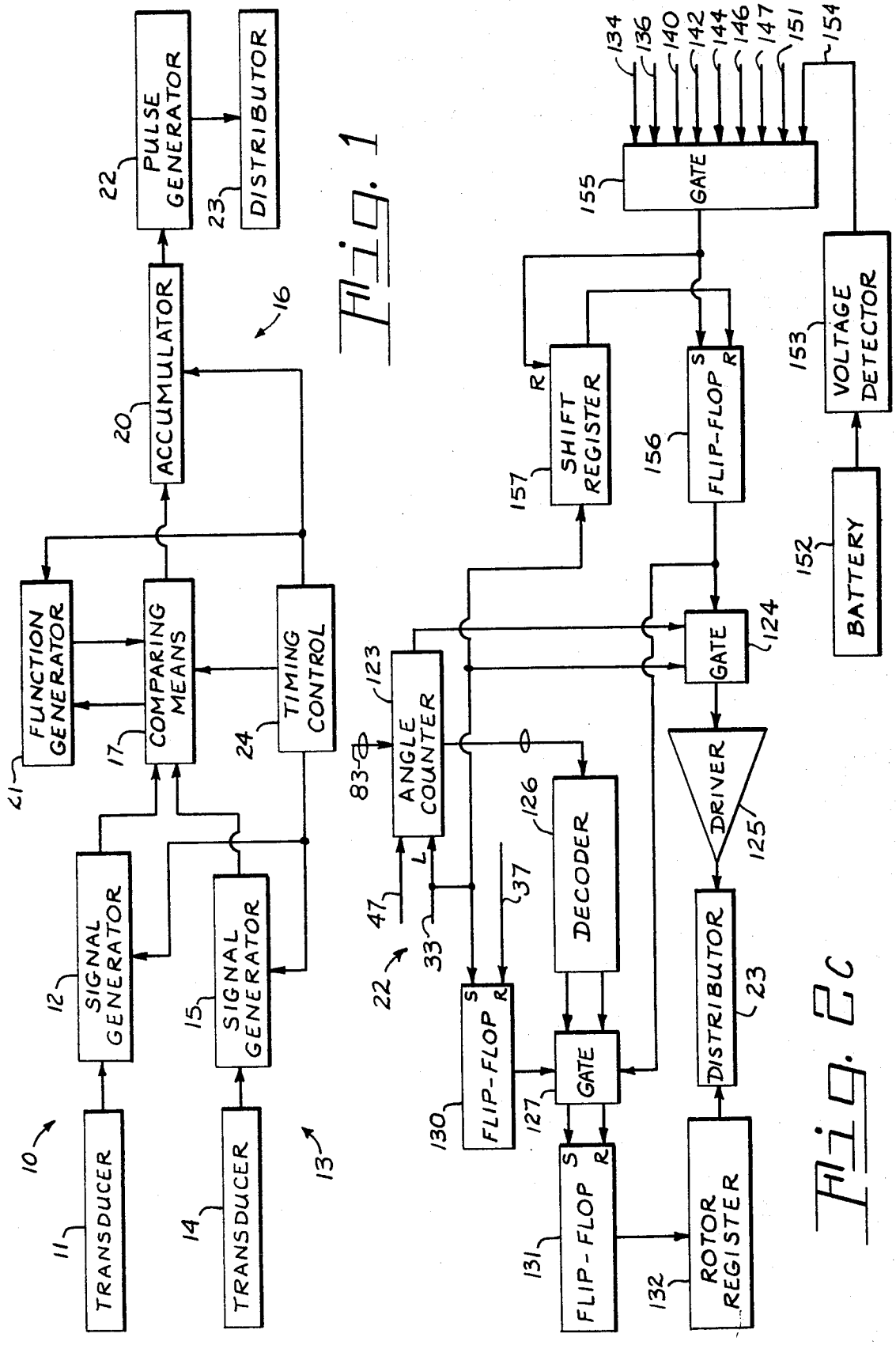
[57] **ABSTRACT**

An electronic ignition timing system for internal combustion engines is disclosed which utilizes electronic circuitry to vary the timing of ignition pulses in response to engine speed and vacuum to provide optimum or improved performance by the engine. Preferably the electrical circuitry utilizes digital signals for high accuracy.


**15 Claims, 6 Drawing Figures**




10
11
TRANSDUCER
12
SIGNAL GENERATOR
13
14
TRANSDUCER
15
SIGNAL GENERATOR
16
17
COMPARING MEANS
20
ACCUMULATOR
21
FUNCTION GENERATOR
22
PULSE GENERATOR
23
DISTRIBUTOR
24
TIMING CONTROL
Fig. 1
22
47
33
37
83
123
ANGLE COUNTER
L
126
DECODER
130
FLIP-FLOP
S
R
127
GATE
131
FLIP-FLOP
S
R
132
ROTOR REGISTER
124
GATE
125
DRIVER
23
DISTRIBUTOR
155
GATE
134
136
140
142
144
146
147
151
154
157
SHIFT REGISTER
156
FLIP-FLOP
S
R
153
VOLTAGE DETECTOR
152
BATTERY
Fig. 2c

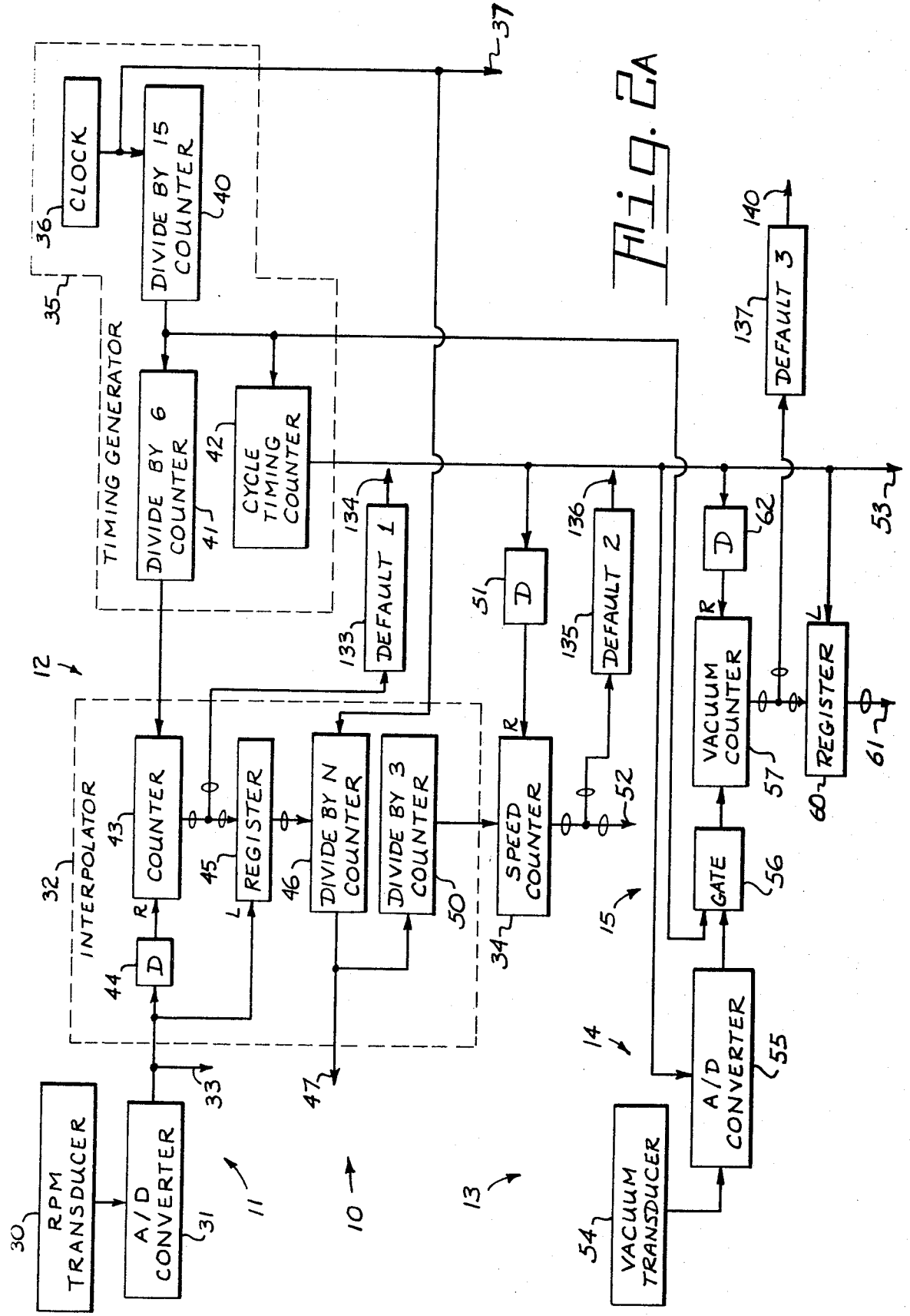

RPM TRANSDUCER
30
A/D CONVERTER
31
33
11
10
13
INTERPOLATOR
32
COUNTER
43
D
44
R
REGISTER
45
L
DIVIDE BY N COUNTER
46
47
DIVIDE BY 3 COUNTER
50
SPEED COUNTER
34
R
51
D
TIMING GENERATOR
35
CLOCK
36
37
DIVIDE BY 15 COUNTER
40
DIVIDE BY 6 COUNTER
41
CYCLE TIMING COUNTER
42
DEFAULT 1
133
134
DEFAULT 2
135
136
52
15
14
VACUUM TRANSDUCER
54
A/D CONVERTER
55
GATE
56
VACUUM COUNTER
57
R
D
62
L
REGISTER
60
61
DEFAULT 3
137
140
53

Fig. 2A

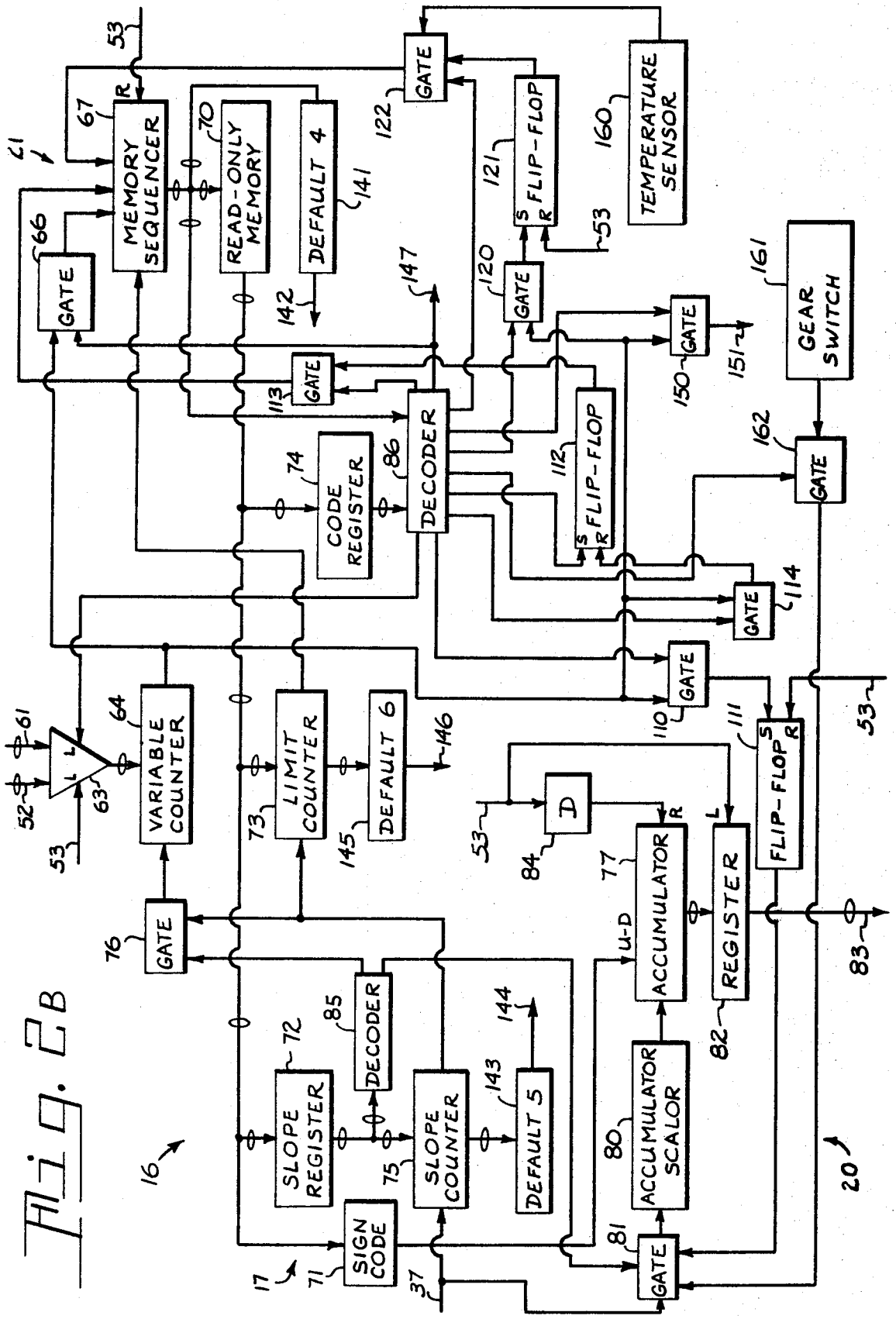

MEMORY SEQUENCER
READ-ONLY MEMORY
DEFAULT 4
GATE
FLIP-FLOP
TEMPERATURE SENSOR
GEAR SWITCH
DECODER
CODE REGISTER
VARIABLE COUNTER
LIMIT COUNTER
DEFAULT 6
SLOPE REGISTER
SLOPE COUNTER
DEFAULT 5
SIGN CODE
ACCUMULATOR SCALOR
ACCUMULATOR
REGISTER
U-D
D

Fig. 2B

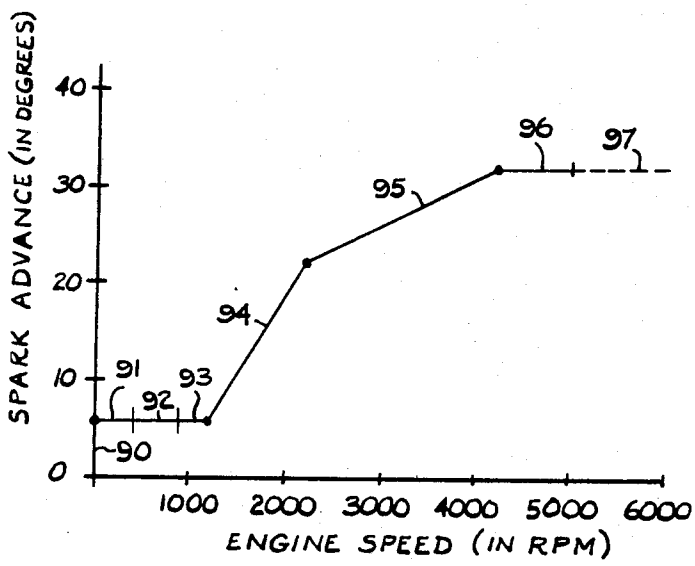

SPARK ADVANCE (IN DEGREES)
40
30
20
10
0
90
91
92
93
94
95
96
97
1000
2000
3000
4000
5000
6000
ENGINE SPEED (IN RPM)

Fig. 3

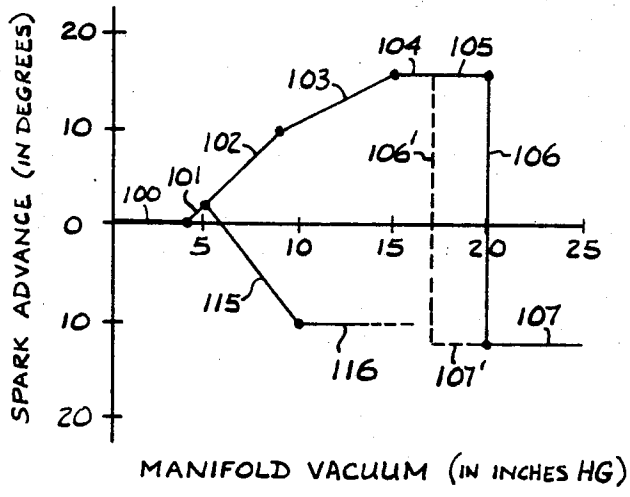

SPARK ADVANCE (IN DEGREES)
20
10
0
10
20
100
101
102
103
104
105
106
106'
107
107'
115
116
5
10
15
20
25
MANIFOLD VACUUM (IN INCHES HG)

Fig. 4

# ELECTRONIC IGNITION TIMING SYSTEM FOR INTERNAL COMBUSTION ENGINES

## CROSS-REFERENCE TO RELATED APPLICATION

The copending application of Robert W. Asplund, Ser. No. 201,362, filed Nov. 23,1971 entitled "Electronic Ignition Timing System for Internal Combustion Engines," and assigned to the same assignee as this application, discloses a system related to the system disclosed herein.

## BACKGROUND OF THE INVENTION

This invention relates to ignition timing for internal combustion engines and more specifically to the timing of ignition pulses in response to engine characteristics for providing improved performance by such engines.

Prior art ignition timing systems for internal combustion engines generally utilize mechanical devices to control spark advance. Such systems may utilize engine speed (RPM) and vacuum inputs to mechanically vary the spark advance. Such mechanical devices, however, suffer from several serious limitations. First, the mechanical complexity required to generate optimum transfer functions dictates the use of only simple transfer functions thereby providing less than satisfactory results. Second, accurate generation of even simple transfer functions with mechanical devices is difficult and expensive. Third, repeatability or accuracy within acceptable limits from device to device is difficult and expensive to achieve and in high volume production becomes virtually impossible to achieve. Fourth, mechanical wear and maladjustment limit the usefulness of such devices. These and other disadvantages of mechanical devices present problems which are exceedingly difficult, if not impossible, to overcome.

Attempts to provide electronic ignition timing systems have generally suffered from many of the same disadvantages, particularly inaccuracy, undue expense to achieve sufficient complexity of transfer functions, difficulty of adjustments and tuning, and other disadvantages.

With regard to exhaust emissions, various solutions for reducing such emissions have been proposed. Such solutions include various control devices such as catalytic burners, control valves, fuel injection, etc. These various devices or systems all suffer from numerous disadvantages. In general, they may be unduly expensive, require substantial maintenance or periodic replacement, and decrease performance and horsepower of the engine among other disadvantages, while providing less than satisfactory emission control.

The various prior art devices accordingly do not provide optimum engine performance under varying conditions. They are inaccurate, do not provide long term stability, decrease the reliability of the engine, provide poor engine response, decrease the economy of the engine, waste power, increase maintenance costs, and provide poor control of exhaust emissions among numerous other disadvantages.

## OBJECTS AND SUMMARY OF THE INVENTION

Accordingly, it is a primary object of this invention to provide an ignition timing system which obviates the above-noted and other disadvantages of the prior art.

It is a further object of this invention to provide an electronic ignition timing system that exhibits numerous advantages over the prior art.



It is a further object of this invention to provide an electronic ignition timing system which is highly accurate and stable over long periods of time to improve the performance and reliability of internal combustion engines.

It is a further object of this invention to provide an electronic ignition timing system for reducing engine emissions by internal combustion engines while enhancing the reliability and performance of such engines.

It is a further object of this invention to provide an electronic ignition timing system which varies the timing of ignition pulses in response to at least two characteristics related to the amount of emission by and the performance of an internal combustion engine.

It is a yet further object of this invention to provide an electronic ignition timing system which is highly accurate and reliable but relatively inexpensive while providing sufficient complexity of timing ignition pulses to significantly reduce engine emissions.

It is a still further object of this invention to provide an electronic ignition timing system which utilizes digital signals and pulse signals for increased accuracy.

It is a still further object of this invention to provide an electronic ignition timing system which varies the timing of ignition pulses in response to the speed and vacuum of an internal combustion engine.

These and other objects and advantages are achieved in one aspect of this invention in a system for controlling ignition timing of an internal combustion engine by varying the timing of ignition pulses in response to first and second characteristics of the engine. The system includes first and second signal generating means, function generating means, comparing means, accumulating means, and pulse generating means. The first and second signal generating means provide first and second electrical signals, respectively, which are representative of the first and second characteristics, respectively, of the engine. The function generating means provides third electrical signals representative of the relationship of the timing of ignition pulses to the first and second characteristics of the engine. The comparing means compares the first and second electrical signals to the third electrical signals while the accumulating means accumulates timing values responsive to the results of the comparisons. The pulse generating means generates ignition pulses at times responsive to the timing values.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating one embodiment of the invention;

FIGS. 2A, 2B, and 2C are a more detailed block diagram of the preferred embodiment of the invention; and

FIGS. 3 and 4 are graphs of transfer functions to aid in explaining the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

For a better understanding of the present invention, together with other and further objects, advantages, and capabilities thereof, reference is made to the following disclosure and appended claims in connection with the above-described drawings.

In FIG. 1 a block diagram of a system for controlling the ignition timing of an internal combustion engine by

varying the timing of ignition pulses in response to first and second characteristics of the engine is shown. The system includes a signal generating means **10** which provides electrical signals representative of the first characteristic of the engine. Preferably signal generating means **10** includes a transducer **11** and a signal generator **13** connected thereto. Transducer **11** provides a signal representative of the first characteristic such as engine speed (RPM) while signal generator **12** generates electrical signals corresponding thereto. A signal generating means **13** provides electrical signals representative of the second characteristic of the engine. Preferably signal generating means **13** includes a transducer **14** and a signal generator **15** connected thereto. Transducer **14** provides a signal representative of the second characteristic such as engine vacuum while signal generator **15** generates electrical signals corresponding thereto.

The output signals from signal generators **12** and **15** are coupled to a signal processing means **16** which preferably includes a comparing means **17** and an accumulating means or accumulator **20.** A function generating means **21** is connected to comparing means **17** which also receives the output signals from signal generators **12** and **15** and provides an output signal to accumulator **20.** Function generator **21** provides electrical signals representative of the relationship of the timing of ignition pulses to the first and second characteristics of the engine for controlling emissions of the engine. Comparing means **17** compares the signals from signal generators **12** and **15** to the signals from function generator **21** while accumulator **20** computes or accumulates timing values responsive to the results of the comparisons.

A pulse generating means **22** is connected to the output of accumulator **20** and generates ignition pulses at times responsive to the timing values accumulated in accumulator **20.** The ignition pulses are applied to a distributor **23** which distributes them to the proper spark plugs associated with the engine. A timing control means **24** provides timing signals to signal generators **12** and **15,** function generator **21,** comparing means **17,** and accumulator **20.**

FIGS. 2A, 2B, and 2C are detailed block diagrams of an electronic system for controlling the ignition timing of an internal combustion engine in accordance with the preferred embodiment of the invention. In FIG. 2A signal generating means **10** and **13** together with part of timing control means **24** are illustrated. FIG. 2B illustrates the signal processing means **16** together with function generator **21** and additional control circuitry. FIG. 2C illustrates pulse generator **22** and further control circuitry. The detailed block diagram will be explained with reference to FIGS. **3** and **4** which are piece-wise linear graphs of typical transfer functions based on experimental data. These transfer functions will vary depending upon the particular engine with which this invention is to be used. Also the number of linear segments can vary depending upon the desired accuracy. In describing the preferred embodiment reference will be made to particular frequencies, time periods, and other values. Those skilled in the art will realize, however, that these values may be varied as desired.

In FIG. 2A signal generating means **10** includes transducer means **11** and signal generator **12.** Transducer means **11** includes a speed (RPM) transducer **30** and an analog-to-digital (A/D) converter **31** connected thereto. The output of A/D converter **31** is connected to an interpolator means **32** and to an output lead **33.** Signal generator **12** includes interpolator **32** and a counter means or speed counter **34.** Timing control means **24** includes a timing generator **35.** Timing generator **35** includes a system clock **36** which provides clock pulses to an output lead **37** and to a divide-by-15 counter **40.** Counter **40** divides the clock pulses by 15 and provides an output to a divide-by-six counter **41** and to a cycle timing counter **42** which further divides the clock pulses to provide the basic timing cycle for the system operation. The output signal of counter **41** is the clock pulse rate scaled or divided by a predetermined factor such as ninety. The output of counter **41** is connected to an input of interpolator **32.**

Interpolator **32** includes a counter means **43** having an input connected to the output of counter **41.** The output of A/D converter **31** is connected via a delay device **44** to a reset input of counter **43** and to a load input of a register **45.** An output of counter **43** is connected in parallel to an input of register **45** which has an output connected in parallel to a counter means or divide-by-N counter **46.** Counter **46** also has an input connected to the output of clock **36** and an output connected to an output lead **47.** The output of counter **46** is also connected to an input of a divide-by-three counter **50** which has an output connected to an input of speed counter **34.** Counter **34** also receives a reset input from cycle timing counter **42** via a delay device **51.** An output of counter **34** is provided in parallel via a set of output leads **52.** The output of cycle timing counter **42** is also connected to an output lead **53.**

The purpose of signal generating means **10** is to generate electrical signals representative of the first characteristic of the engine. In the preferred embodiment speed counter **34** provides digital signals proportional to the speed (RPM) of the engine crankshaft. RPM transducer **30** is preferably a simple and inexpensive device for providing one output pulse for each 90° of crankshaft rotation. For example, a disk with four equally-spaced slots connected to rotate with the crankshaft and a magnetic pickup to sense the slots can be used. In this case A/D converter **31** is a pulse forming circuit which provides suitable timing reference pulses at 90° intervals of crankshaft rotation. Preferably the slotted disk is positioned such that the output pulses from converter **31** are at a predetermined 6° spark advance and can be used as ignition or firing pulses when a standard 6° spark advance is desired.

The object of interpolator **32** is to provide a predetermined number of pulses, for example, ninety, between successive ones of the pulses from A/D converter **31.** Thus, interpolator **32** will provide pulses at 1° intervals of crankshaft rotation. As an example, assume the frequency of clock **36** is 300 kHz. Counter **40** will provide pulses with a frequency of 20 kHz while counter **41** will provide pulses at a frequency of 3.3 kHz. As examples, also assume a typical low engine speed of 600 RPM and a typical high speed of 6,000 RPM. Between these engine speeds the reference pulses from A/D converter vary from 40 Hz to 400 Hz or a spacing from 25 millisecond (ms) to 2.5 ms. Counter **43** thus counts 3.3 kHz pulses for periods varying from 2.5 to 25 ms to generate a number N which varies from about eight to 83. Each pulse from A/D coverter **31** causes register **45** to load the number N and resets counter **43** to zero to start the next cycle. The purpose of delay device **44** is to prevent

the reset of counter 43 until the number N is loaded into register 45.

Counter 46 is a down counter which loads the number N from register 45 and counts clock pulse down to zero. When counter 46 reaches zero, it provides an output pulse to lead 47 and counter 50 and reloads the number N. Thus, counter 46 counts clock pulses in groups of N clock pulses in each group. Since the frequency of the output pulses from clock 36 is 90 times the frequency of the pulses from counter 41, counter 46 provides approximately 90 equally spaced output pulses for each cycle or one pulse for each degree of crankshaft rotation. The 1° pulses are provided at frequencies that vary from 3.6 kHz to 36 kHz as engine speed varies from 600 to 6,000 RPM. The 1° pulses are scaled by counter 50 which, for example, divides the 1° pulse train by three to provide 3° pulses to counter 34.

Timing cycle counter 42 establishes the basic cycle time for the system. For example, assume a computing cycle of 10 ms is desired. Counter 42 is then a divide-by-two hundred counter to further divide the 20 kHz pulse train from the counter by 200 thereby providing 10 ms gating pulses. These gating pulses are coupled to speed counter 34 via delay device 51. Between successive 10 ms gating pulses counter 34 counts 3° pulses to obtain a speed or RPM count that varies from 12 to 120 as engine speed varies from 600 to 6,000 RPM or one count for each 50 RPM. Delay device 51 delays the reset of counter 34 to permit transfer of the RPM count via leads 52 to the circuitry of FIG. 2B before counter 34 resets.

As will be evident to those skilled in the art, various other techniques and/or circuit values can be used to obtain the RPM signal. For example, a shaft angle encoder can be used or a tachometer and A/D converter. Also the timing periods and frequencies can be varied depending upon the desired accuracy. Also the number of RPM/count can be other than 50 and the range of engine speeds is not restricted to 600–6,000 RPM.

Signal generating means 13 includes transducer means 14 and signal generator 15. Transducer means 14 includes a vacuum transducer 54 and an A/D converter 55 connected thereto. An output of A/D converter 55 is connected to a gate 56 which also receives an input from counter 40. An output of gate 56 is connected to a counter means or vacuum counter 57 in signal generator 15. An output signal from counter 57 is coupled in parallel to an input of a register 60 which has an output connected in parallel to output leads 61. The output of counter 42 is connected to an input of A/D converter 55, to a load input of register 60, and via a delay device 62 to a reset input of counter 57.

Vacuum transducer 54 is, for example, a strain gage that senses the second characteristic or manifold vacuum of the engine and provides an analog signal to A/D converter 55. A/D converter 55 is enabled or triggered by gating pulses from counter 42 to provide a width or duration modulated output signal to gate 56 wherein the duration of the output signal from A/D converter is proportional to the analog signal from vacuum transducer 54. The duration modulated signal enables gate 56 to couple pulses from counter 40 to the input of counter 57, the number of pulses coupled through gate 56 being proportional to the manifold vacuum. These pulses are counted by counter 57. The next 10 ms gate pulse causes register 60 to load the vacuum count from counter 57 and resets counter 57 via delay device 62.

Thus, at the end of each cycle period counter 34 contains an RPM count and provides a digital signal representative of engine speed while register 60 contains a vacuum count and provides a digital signal representative of manifold vacuum.

In FIG. 2B leads 52 and 61 are connected in parallel to a gating array 63 which also receives a load input signal from lead 53 (10 ms gating pulses). The output of gating array 63 is connected in parallel to a counting means or variable counter 64. The 10 ms gating pulse that starts each computing cycle causes counter 64 to load the RPM count from counter 34 of FIG. 2A via leads 52 and gating array 63. The 10 ms gating pulses also reset counter 34 via delay device 51. Thus, at the start of a computing cycle the RPM count obtained during the previous cycle is loaded in counter 64 and the vacuum count from register 60 is available at the second input of gating array 63.

The output signal of counter 64 is a pulse $V_o$ which is coupled to an input of a gate 66. An output of gate 66 is connected to an input of a memory sequencing means or sequencer 67. Memory sequencer 67 also receives the 10 ms gating pulses via lead 53 which reset memory sequencer 67 to a starting point. Memory sequencer 67 can be a ring counter or shift register, or other suitable circuit for sequentially providing output signals.

An output of memory sequencer 67 is connected in parallel to an input of a memory device or read-only memory 70. Memory 70 provides digital output signals in parallel to a sign code register 71, a slope register 72, a counting means or limit counter 73, and a code register 74. Register 72 is part of a counting means that includes a slope counter 75, an input of which is connected in parallel to an output of register 72. Counter 75 also receives a clock pulse input via lead 37 and provides an output to limit counter 73 and to a gate 76 which has an output connected to an input of counter 64. An output of counter 73 provides $L_o$ pulses to an input of memory sequencer 67. The components described thus far essentially comprise comparing means 17 and function generating means 21.

Accumulating means 20 includes an accumulator 77 and an accumulator scalor 80. Clock pulses are coupled via lead 37 and a gate 81 to an input of accumulator scalor 80 which has an output connected to an input of accumulator 77. Accumulator 77 is basically an up-down counter which receives an up-down control signal from sign code register 71. An output of accumulator 77 is connected in parallel to a register 82 which provides an output in parallel via leads 83. Register 82 acts as a buffer between accumulator 77 and pulse generating means 22 of FIG. 2C. Register 82 receives a load signal via lead 53 which is also connected via a delay device 84 to a reset input of accumulator 77. Thus, at the start of a computing cycle the 10 ms gating pulse loads register 82 and resets accumulator 77.

In the preferred embodiment of this invention signal processing means 16 is a sequential processor which sequentially compares the digital signals from signal generators 12 and 15 to the digital signals from function generator 21. Memory sequencer 67 and memory 70 of function generator 21 sequentially provide digital signals or memory words corresponding to the transfer functions of FIGS. 3 and 4. These memory words are, first, sequentially compared to the RPM count and, second, sequentially compared to the vacuum count.

Accumulator 77 accumulates digital timing values by counting clock pulses in synchronism with slope counter 75 of comparing means 17.

FIG. 3 is a piece-wise linear plot of a transfer function relating the timing of ignition pulses as determined by degrees of spark advance to the speed of the engine. FIG. 4 is a piece-wise linear plot of a transfer function relating the timing of ignition pulse as determined by degrees of spark advance to the manifold vacuum of the engine. The curve of FIG. 3 consists of linear segments 90–97, while the curve of FIG. 4 consists of linear segments 100–107 and certain "branches" which will be described below. The transfer curves are approximations based on experimental data related to enhanced or optimum engine performance considering such factors as minimum exhaust emissions, engine response, power, economy, etc. Since the curves are related to a particular engine, the general shape, number of linear segments, and numerical values of each curve will depend in part on the particular engine and the desired accuracy.

Memory 70 is programmed in accordance with the slopes and limits of the various linear segments of FIGS. 3 and 4. The first memory word is an RPM word that corresponds to the slope and limit of segment 90, and the second memory word corresponds to the slope and limit of segment 91, and so forth. Following the memory word corresponding to segment 97, the next memory word is a vacuum word that corresponds to the slope and limit of segment 100, and so forth through the vacuum words.

When memory sequencer 67 is reset by a 10 ms gating pulse, it proivdes a signal to memory 70 which causes memory 70 to provide the first speed or RPM word. The memory words can have the following format: a one-bit sign code which is loaded into sign code register 71, a seven-bit slope word which is loaded into slope register 72, a seven-bit limit word which is loaded into counter 73, and a four-bit code word which is loaded into code register 74.

Slope counter 75 is a down counter that loads the slope word from register 72 and counts clock pulses down to zero. Each time zero is reached an output pulse is provided to counter 73 and gate 76, and counter 75 reloads the slope word. Thus, slope counter 75 divides (scales) the clock pulses by the number in slope register 72. Variable counter 64 and limit counter 73 are also down counters. Accumulator scale 80 divides the clock pulses by a suitable factor such that accumulator 77 preferably accumulates timing values directly in degrees. With the specific example of frequencies and magnitudes used above, scalor 80 is a divide-by-twenty counter.

The first word provided by memory 70 corresponds to segment 90 of the transfer curve. Segment 90 corresponds to an initial spark advance for low engine speeds, for example, 6°. Thus, segment 90 has infinite slope. The first word from memory 70 accordingly includes a sign bit to cause accumulator 77 to count up, a slope word of 20, a limit word of six corresponding to 6° of spark advance, and a code word indicative of segment 90. Thus, slope counter 75 and accumulator scalor 80 divide the clock pulses by the same factor twenty so that their output pulses are provided at the same rate. After 120 clock pulses counter 75 has provided six pulses to counter 73 and gate 76. At the same time accumulator scalor 80 provides six pulses to accumulator 77 which counts to six corresponding to the initial 6° of spark advance.

Since the RPM is not changing during segment 90, counter 64 is inhibited so that it does not count the pulses from counter 75. The output from register 72 is connected in parallel to a decoder 85 which decodes the slope word. If the slope word indicates that a segment with infinite slope is being computed, decoder 85 provides an inhibit signal to gate 76 to prevent pulses from counter 75 from reaching counter 64. Counter 73 however counts the six output pulses from counter 75 down to zero and thereupon provides an $L_o$ pulse to memory sequencer 67.

As a specific example to aid in explaining the operation, assume that the engine speed is 3,000 RPM so that the number in counter 64 is 60. The $L_o$ pulse from counter 73 causes memory sequencer 67 to step one position to cause memory 70 to provide the next memory word corresponding to segment 91 of the transfer curve. Segment 91 is zero slope segment so that the slope word is one and the limit word is 400/50 = 8 corresponding to a limit of 400 RPM. The sign bit is immaterial, while the code word is indicative of segment 91. Since the slope is zero, the degrees of spark advance is constant during segment 91. Decoder 85 thus provides an output signal to gate 81 to inhibit gate 81 in response to the slope word indicative of zero slope. Gate 76 is enabled so that output pulses from counter 75 are coupled to counter 64 as well as counter 73. Counters 64 and 73 count down for eight pulses after which counter 64 has a count therein of 60−8 = 52 and counter 73 provides an $L_o$ pulse to step memory sequencer 67.

Memory 70 then provides the next word corresponding to segment 92. Segment 92 also has zero slope and a limit word of (900−400)/50 = 10 corresponding to a limit of 900 RPM. Gate 81 remains inhibited while counter 64 counts down from 52 to 42. The count in counter 64 is similarly reduced to 36 during the computation based on segment 93 which corresponds to a 1,200 RPM limit. During the computation of segments 91–93 the count in accumulator 77 remains at six. The significance of the limits between segments 91, 92, and 93 will be explained below.

The $L_o$ pulse at the end of segment 93 causes memory sequencer 67 to step and memory 70 to provide the word corresponding to segment 94. During this segment both the degrees of spark advance and the RPM are changing so that decoder 85 provides signals that enable gates 76 and 81 and the sign bit causes accumulator 77 to count up. The limit word for segment 94 is (2,200−1,200)/50 = 20 and the slope word is 20×16/20 = 16. Thus, every 16 clock pulses, counter 75 provides an output pulse until 20 such output pulses have occurred or a total of 320 clock pulses. The count in counter 64 is reduced to 36−20 = 16 and accumulator 77 receives 16 pulses. Thus, the count in accumulator 77 is 22 when the $L_o$ pulse from counter 73 occurs at the end of segment 94.

The next memory word corresponding to segment 95 has a limit word of 40 and a slope word of 20×8/40 = 4. Thus, counter 75 divides the clock pulses by four and counter 64 counts sixteen such pulses until it reaches zero thereby providing a $V_o$ output pulse. Prior to the $V_o$ pulse, accumulator 77 receives three pulses so that when the $V_o$ pulse from counter 64 occurs, the timing value count in accumulator 77 is 25 corresponding to

the degrees of spark advance for an engine speed of 3,000 RPM.

If the engine speed is less than 3,000 RPM, the $V_o$ pulse from counter **64** indicating that counter **64** has counted down to zero will occur earlier so that the count in accmulator **77** will be less. If the engine speed is greater than 3,000 RPM the count in accumulator **77** will be greater. The maximum count that accumulator **77** will accumulate during RPM processing is 32 corresponding to speeds in excess of 4,200 RPM where segments **96** and **97** are processed. During the processing of segments **96** and **97**, the count in accumulator **77** does not change.

The $V_o$ pulse at the end of RPM processing is coupled from counter **64** through gate **66** to memory sequencer **67** and causes memory sequencer **67** to skip to the start of the vacuum words. Memory **70** then provides the first vacuum word which in format is similar to the RPM words. The outputs of memory sequencer **67** and code register **74** are each connected in parallel to a decoder **86** which decodes the input words to provide several output signals. When the code for the first vacuum word is loaded in register **74**, decoder **86** provides an output signal to a load input of gating array **63** to cause the vacuum signal or count from register **60** to be loaded via leads **61** and gating array **63** into counter **64**. Either the output of code register **74** or the output of memory sequencer **67** or both can be decoded to cause gating array **63** to load the vacuum count.

The operation of the circuitry during vacuum processing is essentially the same as was explained for RPM processing. The count in counter **64** is compared to the successive signals from memory **70** corresponding to the segments of the curve of FIG. **4**. The transfer function of FIG. **4** includes segments **100–107** which are processed sequentially. Segments **100, 104, 105** and **107** are zero slope segments and during the processing of these segments, gate **81** is inhibited so that accumulator **77** does not count. The vacuum processing is an additive function, that is, the count corresponding to degrees of spark advance for vacuum is added to the count accumulated during RPM processing to produce the final timing value in accumulator **77**.

When the $V_o$ pulse at the end of vacuum processing occurs, the computation is ended. The output of counter **64** is connected to a gate **110** which also receives an output of decoder **86**. An output of gate **110** is connected to a set input of a flip-flop **111** which has an output connected to gate **81**. Lead **53** is connected to a reset input of flip-flop **111**. The $V_o$ pulse at the end of vacuum processing is coupled through gate **110** to set flip-flop **111** which provides an inhibit signal to gate **81** to prevent clock pulses from being coupled therethrough. Decoder **86** enables gate **110** only during vacuum processing so that the $V_o$ pulse at the end of RPM processing does not reach flip-flop **111**. Flip-flop **111** is reset by the 10 ms gating pulses. The $V_o$ pulse at the end of vacuum processing can also step memory sequencer **67** to an inactive state if desired, where it will remain until reset by a **10** ms gating pulse.

Segments **106** and **107** of the vacuum transfer function cause a spark retard (negative spark advance) if the vacuum becomes very large. This condition can occur, for example, during deceleration. If a $V_o$ pulse ending vacuum processing by setting flip-flop **111** does not occur before the processing reaches the end of segment **105**, the $L_o$ pulse at the end of the processing of segment **105** causes memory sequencer **67** and memory **70** to provide the memory word corresponding to segment **106**. This memory word carries a sign bit that causes accumulator **77** to count down. Since segment **106** is an infinite slope segment decoder **85** inhibits gate **76** so that the count in counter **64** does not change during the processing of segment **106**. The next segment, **107**, is processed in the usual manner until the $V_o$ pulse occurs.

Since there is a substantial difference in spark advance depending upon whether segment **106** is reached or not, and since oscillation between the spark advance for segments **105** and **107** may deleteriously affect the engine operation, a provision is made to ensure against such oscillation. The circuitry for providing this function includes a flip-flop **112** which has a set input connected to an output of decoder **86**. An output of flip-flop **112** is connected to a gate **113** which has an output connected to an input of memory sequencer **67**. Another output of decoder **86** is connected to an input of gate **113**. The output of counter **64** and an output of decoder **86** are connected to inputs of a gate **114** which has an output connected to a reset input of flip-flop **112**.

If, during a first computing cycle, memory **70** provides the memory word corresponding to segment **106**, decoder **86** provides an output signal that sets flip-flop **112**. On the next computing cycle if the $V_o$ pulse ending vacuum processing does not occur during or before segment **104**, that is, the limit between segments **104** and **105** is reached without a $V_o$ pulse occurring, the circuitry skips segment **105** and proceeds directly to segment **106**. The output of flip-flop **112** is gated with the output of decoder **86** indicative of segment **104** by gate **113** to provide a signal to memory sequencer **67** which causes memory sequencer **67** to skip or advance two steps when the $L_o$ pulse from limit counter **73** occurs ending the processing of segment **104**. The processing then follows dashed line segments **106'** and **107'** which are processed until a $V_o$ pulse occurs ending vacuum processing. Gate **114** is enabled by decoder **86** during the processing of segments **100–104** so that if a $V_o$ pulse occurs during processing of any of these segments, it is coupled through gate **114** to reset flip-flop **112**. When flip-flop **112** is reset, gate **113** is inhibited.

When the engine is idling, it has been found that it is desirable to modify the transfer function for vacuum processing to obtain reduced emissions. The idle limit in FIG. **3** is the limit between segments **92** and **93**, for example, 900 RPM. Thus, if the engine speed is less than 900 RPM, the vacuum processing follows curve segments **115** and **116** rather than segments **102–107** of FIG. **4**. In FIG. **2B** the output of counter **64** is connected to a gate **120** which has an output connected to a set input of a flip-flop **121**. An output of decoder **86** is connected to an input of gate **120**, while another output of decoder **86** is connected to an input of a gate **122**. An output of flip-flop **121** is connected to another input of gate **122** which has an output connected to memory sequencer **67**. The 10 ms gating pulses are coupled via lead **53** to a reset input of flip-flop **121**.

When the code word in register **74** and/or the output of memory sequencer indicates that segment **92** (and segment **91** if desired) is being processed, **86** provides an output to enable gate **120**. If a $V_o$ pulse from counter **64** occurs during the time that gate **120** is enabled, the

$V_o$ pulse is coupled through gate **120** to set flip-flop **121**. Then when the vacuum processing is being performed, decoder **86** provides an output indicative of segment **101** when that segment is being processed. This output of decoder **86** and the output of flip-flop **121** are gated in gate **122** to provide a signal to memory sequencer **67**. If the $V_o$ pulse ending vacuum processing does not occur before the processing based on segment **101** is completed, the signal from gate **122** causes memory sequencer **67** to skip to the address of the memory word corresponding to segment **115** when the $L_o$ pulse from counter **73** occurs ending the processing of segment **101**.

Segment **115** has a negative slope so that the sign bit of the memory word associated therewith causes accumulator **77** to count down. If the $V_o$ pulse ending vacuum processing does not occur before the processing of segment **115** is completed, the $L_o$ pulse from counter **73** causes memory sequencer **67** and memory **70** to provide the memory word corresponding to segment **116** which controls the processing until a $V_o$ pulse occurs. Flip-flop **121** is reset by the **10** ms gating pulse at the start of the next cycle.

Referring next to FIG. **2C**, there is shown therein pulse generating means **22**. The function of pulse generating means **22** is to convert the digital timing values accumulated by accumulator **77** to timing pulses which control the ignition of firing. Leads **83** are connected in parallel to an input of a firing angle. counter **123** which is also connected to lead **47** to receive the 1° pulses and to lead **33** to receive the reference or 90° pulses at a load input. An output of counter **123** is connected to an input of a gate **124** which has an output connected via a driver **125** to distributor **23**. Gate **124** is also connected to lead **33** to receive the 90° pulses. Another output of counter **123** is connected in parallel to a decoder **126** which has first and second outputs connected to corresponding inputs of a gate **127**. Lead **33** is also connected to a set input of a flip-flop **130** which has an output connected to another input of gate **127**. Clock pulses are coupled to a reset input of flip-flop **130** via lead **37**. First and second outputs of gate **127** are connected to set and reset inputs of a flip-flop **131** which has an output connected to a rotor register means **132**. An output of rotor register **132** is connected to distributor **23**.

Each reference or 90° pulse applied via lead **33** causes counter **123** to load the digital timing value from register **82**. Counter **123** counts 1° pulses applied via lead **47** downward to zero whereupon counter **123** provides an output timing pulse. This output pulse is coupled via gate **124** to driver **125** which provides an output pulse suitable for application to distributor **23**. Thus, counter **123** provides ignition or firing pulses at firing angles or times which vary from reference times by a number of degrees determined by the digital timing values.

The number of degrees of spark advance can vary greatly and may cause an ambiguity within distributor **23** as to which spark plug receives a particular pulse. Rotor register **132** provides a step or gross adjustment of the distributor rotor to eliminate the ambiguity. The 90° pulses are coupled via lead **33** to the set input of flip-flop **130** which is reset by the next succeeding clock pulse. The output pulse of flip-flop **130** is applied to gate **127**. Decoder **126** decodes the digital timing values loaded into counter **123**. If the digital timing value is greater than a predetermined magnitude, decoder **126** provides an output signal to gate **127** which directs the pulse from flip-flop **130** via gate **127** to the set input of flip-flop **131**. When flip-flop **131** is set, it provides a signal to rotor register **132** which causes the rotor to be retarded. If the digital timing value is less than the predetermined magnitude representing a large spark advance, decoder **126** causes gate **127** to direct the pulse from flip-flop **130** to the reset input of flip-flop **131** to adance the rotor. Flip-flop **130** provides a delay for the 90° pulses to permit counter **123** to load the digital timing value before flip-flop **131** is set or reset. Other suitable devices for providing a delay can also be used. Rotor register **132** can be, for example, a solenoid which pulls the rotor to an advanced or retarded position.

As was explained above, the cycle time of the processor is 10 ms so that a new digital timing value is computed every 10 ms. When the engine is operating at high speeds, more than one 90° pulse will occur during each 10 ms cycle. Thus, at high engine speeds one computation will be used to time more than one ignition pulse. When the engine is operating at low speeds, however, more than one computation will occur between successive 90° pulses. In this case only the last digital timing value will be utilized with earlier computations being ignored.

In the described embodiment pulse generator **22** generates ignition timing pulses at times varied from 90° reference pulses. When the 90° pulses are provided at a standard 6° advance, it may be necessary to provide the ignition pulses both before and after the 90° pulses. If this timing arrangement is not desired, a different set of reference pulses can be provided at times which are between the maximum retard and maximum advance. In this interval ignition pulses will not occur. Note that this alternative will shift the zero references of the curves in FIGS. **3** and **4**.

Another alternative is to utilize a "dummy" or delayed reference pulse. Counter **123** can include two counters. The first counter receives the digital timing value from register **82** and counts down a predetermined number of counts after which the number therein is transferred to the second counter which completes the counting. The 90° reference pulse can be delayed (for example, in a shift register or counter) for a number of degrees equal to the predetermined number of counts. The delayed reference pulse is used to transfer the number from the first counter to the second counter. As a still further alternative, accumulator **77** can be preset to a number other than zero to accomplish the same result. In this case the reference pulses would also be delayed by a number of degrees equal to the preset count.

Under some conditions of the engine different operation than that described above may be desired. Also under some conditions the circuitry may operate improperly. In the system means are provided for modifying the operation when such conditions or defaults occur. For example, a predetermined spark advance can be provided which will permit the engine to operate even if the system operates improperly. In one system constructed in accordance with the invention, the predetermined spark advance used was 6°. For convenience the position of RPM transducer **30** was adjusted so that the 90° pulses were advanced a predetermined 6° and thereby could be used as ignition pulses.

In FIG. 2A the output of counter 43 is connected in parallel to a first default circuit 133 which provides an output signal via a lead 134. The output of counter 34 is connected in parallel to a second default circuit 135 which provides an output signal via a lead 136. The output of counter 57 is connected in parallel to a third default circuit 137 which provides an output signal via a lead 140. In FIG. 2B the output of memory sequencer 67 is connected in parallel to a fourth default circuit 141 which provides an output signal via a lead 142. The output of counter 75 is connected in parallel to a fifth default circuit 143 which provides an output signal via a lead 144. The output of counter 73 is connected in parallel to a sixth default circuit 145 which provides an output signal via a lead 146.

Default circuits 133, 135, 137, 141, 143, and 145 detect erroneous operation of the circuit to which they are connected. For example, a default circuit can detect when the counter or circuit connected thereto is in an illegal state or otherwise is not operating properly and provide an output indication thereof. Other forms of default circuits can also be used and error detection circuitry can be used at places in the system other than those illustrated.

Other default conditions that can be detected are engine overspeed, engine underspeed, high engine temperature, gear shift, high or low input voltage and the like. Circuitry is provided to detect each of these default conditions in the preferred embodiment.

If the engine overspeeds, it may be desirable to provide a standard 6° spark advance that, while not necessarily providing optimum engine performance, will tend to limit the engine speed to prevent damage. For example, assume that the maximum permissible engine speed is 5,000 RPM. Accordingly, in FIG. 3 a limit is provided between segments 96 and 97. If the $V_o$ pulse from counter 64 of FIG. 2B does not occur before the $L_o$ pulse ending the computation of segment 96 is provided by counter 73, the $L_o$ pulse steps memory sequencer 67 to the memory word for segment 97. However, the occurrence of this word means that the engine is overspeeding. Thus, decoder 86 decodes its inputs and provides an output via a lead 147 indicating that an overspeed condition has occurred. This output signal can be coupled via gate 66 to memory sequencer 67 to serve as the $V_o$ pulse ending RPM processing if desired to prevent "hang-up" of the circuitry. However, further computation during that cycle is immaterial since the computed digital timing value will not be used anyway.

If an underspeed condition occurs, a standard 6° spark advance is also desirable. Assume that the low speed limit is 400 RPM so that a default occurs at speeds below the limit. In FIG. 3 the low speed limit is between segments 91 and 92. Thus, if the $V_o$ pulse from counter 64 occurs while segment 91 is being processed, an underspeed condition exists. This condition is detected by gate 150 which receives as inputs the $V_o$ pulse from counter 64 and an output of decoder 86. This output of decoder 86 enables gate 150 so that if a $V_o$ pulse occurs during the processing of segment 91, the $V_o$ pulse is coupled through gate 150 to lead 151 indicating that an underspeed condition exists.

Another default condition wherein it may be desired to use a standard 6° spark advance is high or low input voltage. For example, the voltage of the battery associated with the engine may be so low that improper circuit operation may result or so high that damage to the circuitry could occur. In FIG. 2C battery 152 has an output connected to a voltage detector 153 which detects high or low voltage and provides an output signal indicative thereof on lead 154.

Leads 134, 136, 140, 142, 144, 146, 147, 151, and 154 are connected to inputs of a gate 155 which has an output connected to a set input of a flip-flop 156 and to a reset input of a shift register 157. The 90° pulses are coupled to shift register 157 via lead 33. An output of shift register 157 is connected to a reset input of flip-flop 156 which has an output connected to an input of gate 124 and to an input of gate 127.

If one of the various defaults occur, the corresponding signal on one of the leads connected to gate 155 will be coupled through gate 155 to set flip-flop 156 and reset shift register 157. The output of flip-flop 156 causes gate 124 to couple the reference or 90° pulse therethrough to serve as an ignition pulse while inhibiting the output of counter 123. The output signal from flip-flop 156 also inhibits gate 127 to ensure that rotor register 132 adjusts the rotor for a 6° spark advance.

Shift register 157 ensures against oscillation between default/no default conditions. When a default occurs shift register 157 is reset. The 90° pulses shift shift register 157 until a predetermined number of shifts, for example, eight shifts, have occurred. If during this time another default signal occurs, shift register 157 is again reset. Thus, eight successive ignition pulses without a default must be provided before shift register 157 clears. After the predetermined number of shifts of shift register 157 have occurred, shift register 157 provides an output signal to reset flip-flop 156 thereby causing gate 124 to inhibit the 90° pulses and couple therethrough the output pulses from counter 123.

Certain other default conditions may occur where it is not desired to use a 6° spark advance. For example, during idle the engine may overheat due to spark retard. Under these conditions spark retard can be prevented by preventing the circuitry from processing segments 115 and 116 of FIG. 4. In FIG. 2B temperature sensor 160 provides an output signal to inhibit gate 122 if the temperature exceeds a predetermined limit. Since gate 122 provides the signal that causes memory sequencer 67 to skip to the addresses of memory words corresponding to segments 115 and 116, inhibiting gate 122 permits the circuitry to process segment 102 and the following segments rather than segments 115 and 116 thereby preventing spark retard due to those segments.

Another feature that may be desired is to inhibit a spark advance due to vacuum when a vehicle in which the invention may be used is operating in a gear other than high gear. This function is provided by a gear switch 161 which provides an output signal to a gate 162. Gate 162 also receives an input signal from decoder 86 and provides an output signal to gate 81. During vacuum processing, decoder 86 provides an output signal to gate 162 during the processing of segments 101–107. Gear switch 161 provides an output signal when the vehicle is in any gear except high gear. When both output signals are present, gate 162 provides a signal to inhibit gate 81. Thus, although the vacuum processing occurs normally, accumulator 77 is inhibited from counting if advance due to vacuum processing is to occur. Other arrangements to provide similar functions can also be used, if desired.

The above-described system can be implemented with any desired circuitry. One practical embodiment of the invention was implemented with commercially available bipolar logic and digital circuit components, while another embodiment was implemented with commercially available MOS components. It is also possible to implement the system with custom designed circuits, for example LSI/MOS circuitry.

The signal processing technique described above utilizes a 10 ms cycle time to perform the processing of the RPM and vacuum counts. A "real-time" processing system as is described in the above-identified copending application can also be utilized. In a real-time processor, for example, the signal processing can be performed between successive reference or 90° pulses. Since the processing must be performed between 90° pulses which occur at relatively high frequencies at high engine speeds, the clock frequency must be correspondingly high to complete the processing and to provide satisfactory accuracy in a real-time system. In a system implemented with MOS components or circuitry, sufficiently high clock frequencies may be difficult to achieve. In such cases, and in other situations as well, the technique of using a fixed cycle time is desirable. The duration of the timing cycle can be selected as convenient for processing the signals. It should be noted, however, that the accuracy of the system increases with increasing clock frequency. The embodiment described is the embodiment preferred at present, however, there are many alternations and variations that can be made. For example, inputs other than or in addition to RPM and vacuum can be provided. Many special features and operating modes have been described which may not be needed or desired in some systems while still other features may be desired. Also, the specific numbers, values, frequencies, etc., are not to be taken as limiting. Also various circuit changes and modes of operation will be evident to those skilled in the art.

The above-described embodiment of the invention exhibits numerous advantages over the prior art. A system in accordance with the invention can provide enhanced or optimum engine performance under varying conditions unobtainable in the prior art. A primary advantage of the system is to provide the capability of controlling and reducing exhaust emissions without degrading or while actually enhancing the performance of the engine. The system provides high accuracy and long term stability thereby increasing the reliability of the engine and decreasing maintenance costs. The system also provides other advantages such as improved engine response, increased economy, and increased horsepower, among other similar advantages. Another major advantage is the flexibility provided by a system in accordance with the invention. The same basic system can accommodate many transfer functions merely by reprogramming the memory thereby requiring minimal changes to the system for various engines.

While there has been shown and described what is at present considered the preferred embodiment of the invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

What is claimed is:

1. A system for controlling ignition timing of an internal combustion engine by electrically varying the timing of ignition pulses in response to first and second characteristics of said engine comprising:

first signal generating means for providing first digital signals representative of said first characteristic of said engine;

second signal generating means for providing second digital signals representative of said second characteristic of said engine;

function generating means for providing third digital signals representative of the relationship of the timing of ignition pulses to said first and second characteristics of said engine;

comparing means connected to said first and second signal generating means and to said function generating means for comparing said first and second digital signals to said third digital signals;

accumulating means connected to said comparing means for accumulating timing values responsive to the results of comparisions by said comparing means; and

pulse generating means connected to said accumulating means for generating ignition pulses at times responsive to said timing values.

2. A system as defined in claim 1 wherein said first and second characteristics of said engine are crankshaft speed and manifold vacuum, respectively.

3. A system as defined in claim 1 wherein said function generating means includes a memory device programmed in accordance with the relationship of the timing of ignition pulses to said first and second characteristics of said engine.

4. A system as defined in claim 3 wherein said memory device is programmed in accordance with the slope and limit of a piece-wise linear approximation of the relationship of the timing of ignition pulses to said first and second characteristics of said engine, and said function generating means includes memory sequencing means connected to said comparing means and to said memory device for causing said memory device to provide said third digital signals sequentially, said third digital signals being representative of the slopes and limits of sequential segments of the relationship of the timing of ignition pulses to said first and second characteristics of said engine.

5. A system as defined in claim 4 wherein said comparing means includes first counter means connected to said first and second signal generating means for successively receiving said first and second digital signals, second counter means connected to said memory device and to said memory sequencing means for receiving the portions of said third digital signals representative of the limits of said sequential segments and for providing sequencing signals to said memory sequencing means when said second counter means has counted through a number of states representative of the limits of said sequential segments, and third counter means connected to said memory device and to said first and second counter means for providing pulses to said first and second counter means at rates proportional to the slopes of said sequential segments, said first counter means providing output signals indicative of the results of the comparisons.

6. A system as defined in claim 5 wherein said accumulating means includes a counter for counting clock pulses in synchronism with third counting means.

7. A system as defined in claim 1 wherein said first signal generating means includes a transducer means

for providing pulse signals representative of engine speed, and a signal generator connected to said transducer means for converting the signals therefrom to said first digital signals.

8. A system as defined in claim 7 wherein said transducer means provides pulse signals at predetermined intervals of crankshaft rotation of said engine, and said signal generator includes a first counter for counting clock pulses scaled by a predetermined factor between successive ones of the pulses from said transducer means for generating a number N and a second counter including a register connected to said first counter to which the number N is transferred, said second counter for counting clock pulses in groups of N clock pulses each and for providing output pulses after each group of N pulses has been counted whereby a predetermined number of output pulses of said second counter are provided equally spaced between successive ones of the pulses from said transducer means.

9. A system as defined in claim 7 wherein said pulse generating means is connected to said transducer means and to said signal generator for counting a number of pulses from said signal generator equal to one of said timing values after each pulse signal from said transducer means.

10. An electronic system for controlling exhaust emissions of an internal combustion engine by varying the timing of ignition pulses in response to the speed and vacuum of said engine comprising:

first signal generating means for providing first digital signals representative of the speed of said engine;

second signal generating means for providing second digital signals representative of the vacuum of said engine;

function generating means for sequentially providing third digital signals representative of the slopes and limits of piece-wise linear segments of the relationship of the timing of ignition pulses to the speed and vacuum of said engine for controlling exhaust emissions of said engine;

comparing means, including counter means, connected to said first and second signal generating means and to said function generating means for comparing said first and second digital signals to said third digital signals by counting in said counting means in response to said third digital signals;

accumulating means connected to said comparing means for counting in synchronism with said counting means for accumulating timing values responsive to the results of comparisons between said first and second digital signals and said third digital signals; and

pulse generating means connected to said accumulating means for generating ignition pulses at times responsive to said timing values.

11. An electronic system as defined in claim 10 wherein said first signal generating means includes transducer means for providing pulses at predetermined intervals of crankshaft rotation of said engine, interpolator means connected thereto for providing a predetermined number of equally spaced pulses between successive ones of the pulses from said transducer means, and second counter means connected to said interpolator means for providing said first digital signals.

12. An electronic system as defined in claim 11 wherein said interpolator means includes a first counter for counting clock pulses scaled by said predetermined number between successive pulses from said transducer means, a register connected to said first counter for retaining digital signals provided by said first counter, and a second counter connected to said register for counting clock pulses in groups determined by the digital signals retained by said register and for providing an output signal after each of the groups of clock pulses counter thereby.

13. An electronic sysem as defined in claim 11 wherein said pulse generating means is connected to said transducer means and to said interpolator means for counting a number of pulses from said interpolator means equal to one of said timing values after each pulse from said transducer means.

14. An electronic system as defined in claim 10 wherein said counter means of said comparing means includes a first counter connected to said function generating means for providing output pulses corresponding to clock pulses scaled by portions of said third digital signals representative of said slopes of said segments, a second counter connected to said first counter and to said function generating means for counting output pulses from said first counter and for sequencing said function generating means when the numbers of output pulses from said first counter equal portions of said third digital signals representative of said limits of said segments to provide the next successive ones of said third digital signals, and a third counter connected to said first counter for determining when the numbers of pulses from said first counter equal said first and second digital signals.

15. An electronic system as defined in claim 14 wherein said function generating means includes a memory device for providing said third digital signals, and a memory sequencer connected to said memory device and to said second counter for sequencing said memory device in response to output pulses from said second counter.

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