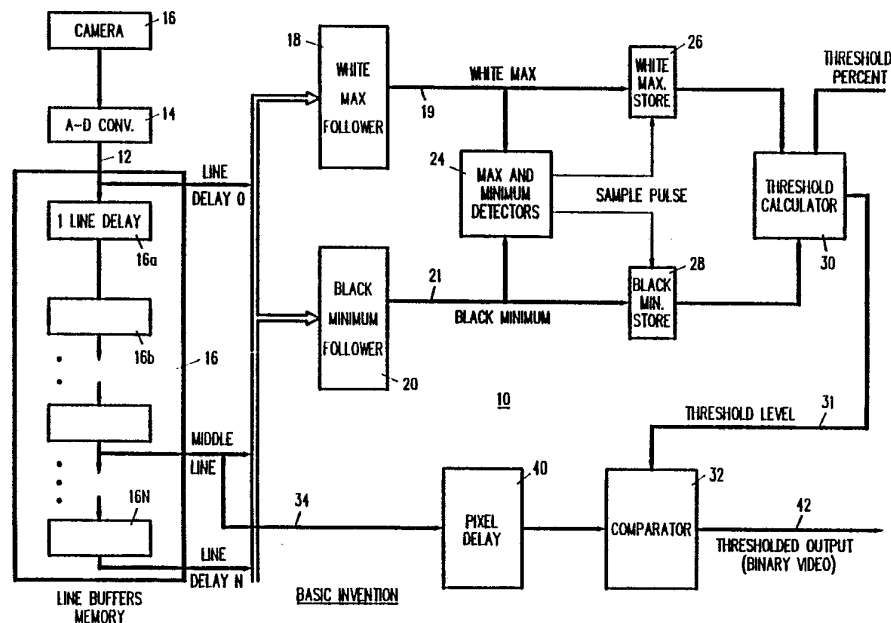




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<p>(51) International Patent Classification ⁵ : G06K 9/48</p>	<p>A1</p>	<p>(11) International Publication Number: WO 92/05518</p> <p>(43) International Publication Date: 2 April 1992 (02.04.92)</p>
<p>(21) International Application Number: PCT/US91/06688</p> <p>(22) International Filing Date: 16 September 1991 (16.09.91)</p> <p>(30) Priority data: 583,444 17 September 1990 (17.09.90) US</p> <p>(71) Applicant: TEKNEKRON COMMUNICATIONS SYSTEMS, INC. [US/US]; 2121 Allston Way, Berkeley, CA 94704 (US).</p> <p>(72) Inventor: HOLT, Kenneth, Cooper ; 1822 Berkeley Way, Berkeley, CA 94703 (US).</p> <p>(74) Agents: YIN, Ronald, L. et al.; Limbach, Limbach & Sutton, 2001 Ferry Building, San Francisco, CA 94111 (US).</p>		<p>(81) Designated States: AT (European patent), AU, BE (European patent), CA, CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).</p> <p>Published <i>With international search report.</i></p>

(54) Title: A METHOD AND AN APPARATUS FOR GENERATING A VIDEO BINARY SIGNAL FOR A VIDEO IMAGE HAVING A MATRIX OF PIXELS



(57) Abstract

A method and an apparatus for dynamically setting a discrimination threshold for the processing of an image is disclosed. The image is composed of a matrix of pixels (12) with each pixel having a grey scale value. The plurality of pixels are supplied to a line buffers memory (16). From the line buffers memory, the white peak line and the black minimum line are supplied to a peak and minimum detectors (24) which determine the white peak value and the black minimum value associated with an edge. The white peak value and the black minimum values are stored and are supplied to a threshold calculator (30) to which a user selectable input is also supplied. The output of a threshold calculator is a threshold level which is used by comparator (32). Another input to the comparator is the grey scale value of the pixel from the image. The output of the comparator is a binary video signal.

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A METHOD AND AN APPARATUS FOR GENERATING
A VIDEO BINARY SIGNAL FOR A
VIDEO IMAGE HAVING A MATRIX OF PIXELS

Technical Field

5 The present invention relates to a method and an
apparatus for dynamically setting a discrimination
threshold for the processing of an image which is
composed of a matrix of pixels with each having a
grey value. More particularly, in the present
10 invention, the method and apparatus relates to the
setting of a discrimination threshold for background
processing based upon the detection of an edge and
based upon a user input.

Background of the Invention

15 Methods and apparatuses for generating a video
binary signal for a video image having a matrix of
pixels with each pixel having a grey scale value are
well known in the art. See, for example, U.S. Patent
No. 4,817,174; 4,791,676; 4,789,933; 4,760,5541;
20 4,672,463; 4,517,607; 4,630,307; and 4,498,104.

 There are two prior art techniques for setting
the discrimination threshold, based upon background
processing and foreground processing. In background
processing, where the pixel of interest is not near
25 an area of the image having great contrast, such as
an edge, the setting of the threshold has been based
upon the threshold being a fixed value. In
foreground processing, where the edge of an image can
be clearly found, the threshold is set dependent upon
30 the grey scale value of the pixels surrounding the

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pixel of interest. This is called a high frequency operator and is typified by U.S. Patent 4,501,016.

In foreground processing, the threshold is dynamically set and is dependent upon the grey scale value of the pixels surrounding the pixel of interest. In the device disclosed in U.S. Patent 4,501,016, a pixel of interest is compared to a threshold value which is defined as the average of highest and the darkest of the pixels in an array of pixels immediately surrounding the pixel of interest. See, for example, column 5, lines 33-36.

Necessarily, this means that the threshold is calculated for each pixel of interest. Furthermore, if the calculator is unable to discern the highest and the lowest values, i.e. the pixels are of an imaging area which is essentially constant grey values, the threshold cannot be used because it is too "noisy". Thus, it can be used only in foreground processing applications.

Thus, there is a need in the prior art wherein for background processing, the threshold can be dynamically set yet, yet does not require an extensive amount of computation.

Summary of the Invention

In the present invention, an apparatus for setting dynamically the discrimination threshold for the processing of an image which is composed of a plurality of pixels is disclosed. Each pixel has a grey scale value. The apparatus has means to receive a plurality of the pixels. The apparatus has means for determining the grey value of the pixels having the maximum grey value among the plurality of pixels

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received. Means for storing the maximum grey value
determined is also provided. Means for determining
the grey value of the pixel having the minimum grey
value among the plurality of pixels received is also
5 provided. Means for storing the minimum grey value
determined is also disclosed. The apparatus also
comprises means for setting a grey scale threshold
based upon the stored minimum grey value and the
stored maximum grey value. Finally, the apparatus
10 provides a means for comparing the grey value of each
pixel of the image to the grey scale threshold to
produce a video binary signal.

A method for generating a video binary signal
for a video image having a matrix of pixels is also
15 disclosed.

Brief Description of the Drawings

Figure 1 is a schematic diagram of one
embodiment of the apparatus of the present invention.

Figure 2 is a schematic diagram of a portion of
20 another embodiment which is an improvement to the
apparatus of the present invention.

Figure 3 is a detailed schematic diagram of the
high frequency edge operator shown in Figure 2.

Figure 4 is a schematic diagram of a portion of
25 yet another embodiment of the apparatus of the
present invention.

Figure 5(a-c) are detailed schematic diagrams of
one embodiment of the White Maximum Follower Circuit,
Black Minimum Follower Circuit, and Maximum and
30 Minimum Detector Circuits, respectively shown in
Figure 1.

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Fig 5(d) (1-2) are two embodiments of the Threshold Calculator Circuit, shown in Fig. 1.

Fig. 5(e) is an embodiment of the Threshold Calculator Circuit with dither capability.

5 Fig. 6 is an example of an image digitized with the present invention.

Detailed Description of the Drawings

Referring to Figure 1 there is shown a block diagram of the apparatus 10 of the present invention. The apparatus 10 receives a plurality of pixels from an input line 12. Each of the pixels is a digitized signal having a grey value. The plurality of pixels are arranged in a plurality of lines with each line containing a plurality pixels. The pixels can be from an A to D converter 14 which digitizes an analog signal from a camera 16. Although the apparatus 10 in Fig. 1 is shown as receiving the pixels from a camera 16, as will be seen, the apparatus 10 of the present invention can be used with any source of digitized image data with grey scale value.

The pixel data from the incoming line 12 is stored a line at a time in a line buffers memory 16. The line buffers memory 16 comprises a plurality of storage sites for storing a plurality of lines of pixel data. As shown in Fig. 1, the line buffers memory 16 comprises N lines of storage. As each pixel of data is received by the line buffers memory 16, it is stored first in the first line delay 16a. The pixel is then propagated through the first line delay 16a and is stored in the first position of the second line delay 16b, through which it propagates, and so forth. Thus, the output of every line buffers

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16x, is the grey value of the line of pixels immediately preceding it. In one embodiment, each of the lines of delay 16x in the line buffers memory 16 can be a shift register.

5 The real-time output of the A to D converter 14 is also supplied to a white maximum follower circuit 18 (shown in greater detail in Figure 5a) and simultaneously to a black minimum follower circuit 20 (shown in greater detail in Figure 5b).

10 The white maximum follower circuit 18 receives each pixel from the A to D converter 14 and produces the maximum or the highest grey scale value. At each horizontal position, the white maximum follower circuit 18 finds the highest white grey scale value
15 among the input pixels, and produces this at its output. The white maximum value so determined is supplied on the output 19.

 Similarly, the black minimum follower circuit 20 produces the lowest grey scale value. The black
20 minimum value so determined is supplied on the output 21.

 The instantaneous white maximum value and the instantaneous black minimum value are supplied to the maximum and minimum detector circuit 24 and to the
25 white maximum store 26 and black minimum store 28, respectively.

 The maximum detector portion of the maximum and minimum detectors circuit 24 reads each pixel of the white maximum value and determines if the maximum
30 value located on that line is associated with a light/dark boundary (or an edge). In one embodiment, the maximum and minimum detectors 24 reads each pixel value to determine if a plurality of successive

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pixels have white maximum values which become successively more white. At the end of such a succession, a sample pulse is generated to store that white maximum value in the white maximum store 26.

5 Thus, the white maximum value is defined as the white maximum value on one side of an edge. In this manner, noise and other unimportant variations do not cause incorrect white maximum values to be detected.

10 Similarly, the black minimum value is supplied to the maximum and minimum detectors circuit 24. The minimum detector portion of the maximum and minimum detectors circuit 24 reads the black minimum value and determines the black minimum value when a plurality of successive black minimum pixels are
15 determined with a subsequent decrease in the pixel value denoting the crossover of an edge. Thus, the black minimum value is on the "black side" of an edge. The black value determined in this matter is then stored in a black minimum storage 28.

20 In an improvement to the apparatus 10, the white maximum store 26 and the black minimum store 28, averages the newly received value with the previously stored value and stores that as the new value.

25 The threshold calculator circuit 30 (shown in greater detail in Figure 5(d)(1) or Figure 5(d)(2) receives the output of the white maximum storage 26 and the black minimum storage 28. In addition, the threshold calculator circuit 30 receives a user
30 selectable threshold input which is expressed as a percentage of the difference between the white maximum storage 26 and the black minimum storage 28. The output of the threshold calculator circuit 30 is a threshold level 31, which is supplied to a

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comparator 32. The threshold calculator 30 will be described in greater detail hereinafter.

After the first pixel of the first line has shifted through the line buffers memory 16 by a
5 preset number of lines of delay, it is then supplied to the middle line 34 and is outputted from the line buffers memory 16. The middle line 34 is supplied to a pixel delay 40. The pixel delay 40 is a storage
10 area which delays a fixed number of pixels in order to permit the apparatus 10 of the present invention to "look ahead" from the pixel that is being currently the subject of the threshold by the comparator 32. This is to permit the threshold level for a place on the image to be set, before the pixels
15 in that place are supplied to the comparator 32. From the pixel delay 40, the grey scale value of the pixel is then supplied to the comparator 32. The grey scale value of a pixel supplied to a comparator 32 is compared to the threshold level 31 from the
20 threshold calculator circuit 30. In the event the grey scale value exceeds the threshold level 31, a binary "one" representing white is the output. In the event the grey scale value is less than the threshold level 31, the comparator 32 outputs a
25 binary "zero" representing black. Thus, the output of the comparator 32 is a binary video signal 42.

Referring to Fig. 2, there is shown a portion of a circuit which, when used in the apparatus 10 shown in Figure 1, is an improvement to the apparatus 10.
30 Figure 2 shows the middle line 34 being supplied to a pixel delay 40 which supplies the grey scale value of the pixel to the comparator 32. The threshold level 31 from the threshold calculator circuit 30 is also

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supplied to the comparator 32. The output of the comparator 32 is the video binary signal 42. In the embodiment shown in Fig. 2, the video binary signal 42 from the comparator 32 shall be called the

5 "background binary video signal 42".

The middle line 34 is also supplied to a high frequency pixel delay circuit 42. The high frequency pixel delay circuit 42, like the pixel delay 40 delays the pixels by a fixed length. The output of

10 the high frequency pixel delay 42 is supplied to a high frequency convolution operator 44 and a high frequency edge operator 48. In fact, the output of the pixel delay 40 can be supplied to the high frequency convolution operator 44 and to the high

15 frequency edge operator 48.

The high frequency convolution operator 44 is a foreground processor, which helps to correct for the blurring of the optics and electronics in the camera 16 and helps to exactly determine the proper position

20 of a black/white transition. The output of the high frequency operator 44 is a video binary signal which is usually termed "foreground signal".

The high frequency convolution operator 44 is for small, sharp features, and is used generally in

25 areas where relatively sharp edges can be easily found. The high frequency convolution operator 44 is used to maximize the contrast in a small area around the pixel in question. In contrast, the background areas of the image as processed by the apparatus 10

30 of the present invention, produces a background video signal 42 which is in areas where no sharp edges exist or none can be easily found. Thus, a threshold

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different from the threshold for foreground processing is usually used.

5 The circuit shown in Figure 2 is a "one dimensional" high frequency convolver, since only the middle line 34 is supplied as a source. Therefore, the "surround" pixels are only the pixels to the left and to the right of the center pixel. Most high frequency convolvers use multiple lines as input (2-dimensional) and therefore can use the pixels in the vertical dimension as well, for the comparison
10 "surround" value.

In the embodiment shown in Figure 2, The high frequency convolution operator 44 does not have any threshold value 31 supplied thereto. It uses the
15 pixel values of the surrounding pixels to determine the threshold value. The output of the high frequency convolution operator 44 is a high frequency binary video signal 46 which is continually changing, showing as black or white output with a slightest
20 change in level from pixel to pixel. Because it is such a sensitive and noisy signal, it cannot be used as the only output because it is continually switching between black and white, even in areas that the eye perceives as uniform.

25 The high frequency binary video signal 46 is supplied to a combiner switch 52. The background binary video signal 42 is also supplied to the combiner switch 52. The combiner switch 52 outputs either the background binary video signal 42 or the
30 high frequency binary video signal 46. The switch between the background binary video signal 42 and the high frequency binary video 46 is made by the high

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frequency edge operator 48 generating a switch signal 50.

When the high frequency edge operator 48 determines that the pixel of interest is sufficiently close to a well defined edge, or that an edge has been detected, then the output of the high frequency convolution operator 44, the high frequency binary video signal 46 can safely be used as the output of the apparatus 10 of the present invention. In the event no edge is detected by the high frequency edge operator 48, the switch signal 50 is not present and the output of the combiner switch 52 is the background binary video signal 42.

There are many examples of the high frequency convolution operator 44. One example is shown in U.S. Patent 4,501,016. Another example is a Laplacian operator, which compares the pixel of interest to an average or waited average of the close neighboring pixels. The method of generating the high frequency binary video signal 46 from a high frequency operator 44 is well known in the art.

The high frequency edge operator 48 simply detects the presence of an edge in the image near the pixel of interest and serves to switch the combiner switch 52. There are many well known prior art circuits which can perform this function.

One prior art high frequency edge operator 48 determines the slope, or the "first derivative" of the video signal in one or more axis. Although this type of operator 48 can be used in the apparatus 10 of the present invention, it has the disadvantage of being too sensitive to signals the eye considers

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noise and not sensitive enough to features that the eye considers to be true edges.

Referring to Figure 3, there is shown in greater detail one embodiment of a high frequency edge operator 48, for use in the apparatus 10. A plurality of lines 34 from the line buffers memory 16 are supplied to a buffer of pixel registers 54, thereby storing a two-dimensional array of pixels in the pixel registers 54. The data from the pixel array registers 54 is then supplied simultaneously to a plurality of edge detectors such as a horizontal edge detector 56, a vertical edge detector 58, a diagonal edge detector 60 and a texture detector 62. The outputs of the horizontal edge detector 56, vertical edge detector 58, diagonal edge detector 60, and the texture detector 62 are supplied to an edge calculator 64. Each of the edge detectors 56, 58, and 60 supplies an edge detection signal 66(a-d), respectively when the edge detector (56, 58, or 60) has detected an edge in the pixel array stored in the pixel registers 54.

Thus, the horizontal edge detector 56 would output an edge detection signal 66a if it detects a horizontal edge in any of the lines within the pixel registers 54. Similarly, a vertical edge detector 58 would output an edge detection signal 66b if it detects a vertical edge in the pixel array stored in pixel registers 54. Similarly, a diagonal edge detector 60 would an output an edge detection signal 66c if within the pixel array stored in the pixel registers 54, the diagonal edge detector detects an edge in the diagonal direction. Finally, the texture

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detector 62 outputs a signal 66d which serves to inhibit a false edge generation.

The plurality of edge detection signals 66(a...d) are supplied to the edge calculator 64.

5 The edge calculator 64 also receives a user selectable input 68 for the edge function which the user selects. In response to the edge function select input 68, the edge calculator 64 outputs the appropriate edge detection signal 50, which is
10 supplied to the combiner switch 52.

Thus, for example, if within the image, the user is interested in only horizontal edge detections then the user edge function selection is set to horizontal edge detection. The edge calculator 64 supplies an
15 edge operator output signal 50 only if the horizontal edge detector 56 detects a horizontal edge crossing within the pixel registers 54. A horizontal edge detection would be useful to find edges of text in an image.

20 Referring to Figure 4, there is a shown a portion of another embodiment of the apparatus 10 of the present invention. Each line from the line buffers memory 16 is averaged with an adjacent line. Thus, as shown in Figure 4, the output of the first
25 line delay 16a and the second line delay 16b are both supplied to an average circuit 70 which produces an average line 72. Within the average line 72, adjacent pixels are averaged by average circuit 76 which averages the delayed pixel from the pixel delay
30 74 and current pixel. Similar operations are carried out for successive pairs of lines of delay such as line 3 and line 4, line 5 and line 6, etc.

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The filtering of lines from the line buffers memory 16 serves to average the image in one or two dimensions before the pixel values are used to find the white peak maximum value and the black minimum value.

5

Although the circuit shown in Figure 4 averages a pixel with its vertical neighbor (average circuit 70) and with its horizontal neighbor (average circuit 76), the invention can be practiced by averaging a pixel only with its vertical neighbor, or only with its horizontal neighbor, or any other type of spatial low pass filtering, of which the circuit in Figure 4 is one example.

10

Referring to Fig. 5(a), there is shown a schematic diagram of the White Max Follower circuit 18. In the example shown in Fig. 5(a), the White Max Follower circuit 18 receives three lines of pixels from the line buffers memory 16: The first line (L1) from the real time output of the A-to-D converter 14, the middle line (L2), and line delay N (L3). Each line has a plurality of pixels with each pixel having a different grey scale value. Thus, at any one point in time, three pixels, representing three different grey scale values, are supplied to the white max follower circuit 18. At each point in time, the pixel from L1 is compared to the pixel from L2 by the first compare-and-pass larger value circuit 80. The first compare-and-pass larger value circuit 80 outputs the grey scale value which is the larger of the two from the lines L1 and L2. The output of the first compare-and-pass larger value circuit 80 is supplied to a second compare-and-pass larger value circuit 82, which receives at its other input the

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pixel from line L3. The output of the second
compare-and-pass larger value circuit 82 produces the
pixel value which is the largest of the three pixels
from the lines L1, L2 and L3. Thus, the white max
5 follower circuit 18 outputs a line of grey values,
such that each grey value is the maximum at each
horizontal point along the scanning line.

In like manner, the black minimum follower
circuit 20 receives the plurality of pixel values
10 from the lines L1, L2 and L3 and produces a line of
grey scale values which is the local vertical minimum
at each horizontal point along the scanning line.
This is accomplished by the circuit shown in Fig.
5(b), wherein the pixels from lines L1 and L2 are
15 supplied to a first compare-and-pass smaller value
circuit 84, whose output is supplied to a second
compare-and-pass smaller value circuit 86. The pixel
values from line L3 is also supplied to the second
compare-and-pass smaller value circuit 86 with the
20 output thereof being the output of the black minimum
follower circuit 20.

It should be appreciated that the white max
follower circuit 18 and/or the black minimum follower
circuit 20 can receive more than three lines and
25 produce the maximum and minimum grey values
accordingly.

Referring to Fig.5(c), there is shown a
schematic diagram of the max and minimum detectors
circuit 24. In the embodiment shown in Fig. 5(c),
30 the white max values 19 from the white max follower
circuit 18 are first supplied to a low-pass filter 90
which removes noise and also broadens an edge with
usually the larger or higher edges becoming broader.

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This allows the width of the edge (the number of pixels increasing or decreasing) to be a rough measure of the size of the edge. From the low-pass filter 90, the white max values 19 are then supplied to a horizontal edge detector 92 which comprises a positive derivative detector 94 and an end of sequence detector 96. The positive derivative detector 94 detects when the white max values 19 are increasing. The end of sequence detector circuit 96 detects when the sequence of white max values 19 have stopped increasing (i.e., the end of the sequence represents an edge). Upon the detection of a horizontal edge, the end of sequence detector circuit 96 generates a sample pulse which causes the particular white max value 19 to be stored in the white max stored store 26.

Similarly, the plurality of black minimum values 21 are first passed through a low-pass filter 100 and are then supplied to a second horizontal edge detector 102. The second horizontal edge detector 102 comprises a negative derivative detector 104 with an end of sequence detector 106. In like manner, the low-pass filter 100 serves to remove noise and also broaden an edge from the black minimum values 21. The negative, derivative detector 104 detects when the black minimum values 21 decreases. The end of sequence detector 106 detects when the sequence of decreasing black minimum values 21 have ceased to decrease. At that point, the end of sequence detector 106 generates a sample pulse which causes the particular black minimum value 21 to be stored in the black minimum store 28.

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The white max value 19 and the black minimum value 21 are also supplied to a vertical edge detector 110. The vertical edge detector 110 comprises a subtractor 112, a comparator 114, and a count N pixel sequence circuit 116. A difference between the white max value 19 and the black minimum value 21 is first made by the subtractor 112. The output of the subtractor 112 is supplied to the comparator 114 to which a constant is also supplied as the input thereof. If the difference lasts for a number of pixels, as determined by the count N pixel sequence circuit 116, then a sample pulse is generated by the count N pixel sequence 116 which causes both the white max value 19 and the black minimum value 21 to be stored in the white max store 26 and the black minimum store 28, respectively.

Referring to Fig. 5(d), there is shown a schematic block diagram of one embodiment of the threshold calculator 30. The values stored in the white max store 26 and the black minimum store 28 are both supplied to a subtractor 120. From the subtractor 120, the result is passed to a multiplier 122 to which the user selectable threshold percentage value is also supplied. The output of the multiplier 122 is supplied to an adder 124 to which the black value from the black minimum store 28 is also supplied. The output of the adder 124 is the threshold level 31. Thus, the threshold level 31 is calculated as follows:

Threshold level =
(white max - black min) *thres percentage +
black min.

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In one embodiment the user selectable threshold input is constant during a scan. Of course, that user selectable threshold input can be changed during the scan affording dynamic adjustment of the threshold percentage 31.

Referring to Fig. 5(d-2), there is shown a block diagram of a more generalized threshold calculator 30 which allows the threshold value 31 to be any function of the white max value stored in the white max store 26 and the black min value stored in the black min store 28. A particular function is selected by the user by the threshold function select. All of the functions of the simpler threshold calculator 30 are a subset of the functions possible in this implementation. A typical function might be one that produces a threshold value 31 that was close to the black min value when both white max and black min are low and close to white max when both are high. The threshold value 31 could remain equally distant between the two values for all other values. The effect of such a type of setting would be to produce a threshold image that was lighter in the darker areas and darker in the lighter areas of the scanned image. This type of calculator can be implemented by means of a Read-Only Memory (ROM) look-up table, wherein the threshold level 31 can be specified for every possible combination of input values from the white max store 26, black min store 28 and threshold function select.

Referring to Fig. 5(e), there is shown another variation of the threshold calculator 30, with dither or half-tone capability. In general the use of

dither or half-tone patterns to represent grey images is well-known in the art. The threshold calculator 30 receives the white max value, the black min value, the threshold functions select and, in addition, the pixel address and the line address. In almost all applications of dither or half-tone, the pattern of threshold values stays fixed for the whole image. By using the white max and black min values as inputs to a dither threshold calculator 30, a more efficient use of the dither values can be made, for example, by spreading them between the white max and the black min values dynamically.

Referring to Fig. 6, there is shown an example of an image having nine lines (L0 - L8) with each line having twenty pixels, with the image having a blurred dark line approximately five pixels wide spanning lines L0 to L8. The result of the direction of scan produces the three line delays having the following grey scale values between the values 0 to 10 where 10 is white and 0 is black.

	Values																			
L8	10	10	10	8	5	2	2	2	2	4	9	10	10	10	10	10	10	10	10	10
L4	10	10	10	10	10	8	5	2	2	2	4	9	10	10	10	10	10	10	10	10
L0	10	10	10	10	10	10	10	8	5	2	2	2	4	9	10	10	10	10	10	10

The output of the white max follower circuit 18 (WM) and the black minimum follower circuit 20 (BM) would be the following pixel values:

	Values																			
WM	10	10	10	10	10	10	10	8	5	9	10	10	10	10	10	10	10	10	10	10
BM	10	10	10	10	5	2	2	2	2	2	2	2	4	9	10	10	10	10	10	10

The max and minimum detectors 24 receives the output of the white max follower circuit 18 and the black minimum follower circuit 20 and generates a

sample pulse causing the following indicated values to be stored in the white max store 26 (WS) and the black min store 28 (BS), respectively.

		<u>Values</u>																		
5	WS	X	X	X	X	X	X	X	X	X	X	X	10	10	10	10	10	10	10	10
	BS	X	X	X	X	X	X	2	2	2	2	2	2	2	2	2	2	2	2	2

where X is the value previously stored in store 26 and 28, respectively.

If we assume the threshold percentage is set at fifty percent (50%), then the result of the threshold calculator 30, the threshold level 31 (TV) would have the following value:

TV	X	X	X	X	X	X	X	X	X	X	X	6	6	6	6	6	6	6	6	6
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

where X is the prior stored value.

The middle line 34 is delayed by eight pixels by the pixel of delay 40 resulting in the following values:

L4	X	X	X	X	X	X	X	X	10	10	10	10	10	8	5	2	2	2	4	9
----	---	---	---	---	---	---	---	---	----	----	----	----	----	---	---	---	---	---	---	---

where X is the prior value.

The binary video signal 42, (BV) which is the output of the comparator 32 would then have the following values:

BV	X	X	X	X	X	X	X	X	X	X	W	W	W	B	B	B	B	B	B	W
----	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

where B is black and W is white.

As can be seen from the foregoing, the method and apparatus of the present invention has many advantages. First and foremost is that the determination of the threshold level is based upon detection of maximum white peak value and minimum black value, associated with an edge or edges. Further, these values may not necessarily be proximate to the pixel of interest. Finally, by having the threshold as a user selectable input, the

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threshold can be dynamically changed and yet be
insensitive to noise and slightest pixel value change
as in a high frequency operator.

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WHAT IS CLAIMED IS:

1. An apparatus for dynamically setting a discrimination threshold for the processing of an image which is composed of a plurality of pixels, each having a grey value, said apparatus comprising:
 - 5 means for receiving a plurality of pixels;
 - means for determining the grey value of the pixel having the maximum grey value among the plurality of pixels received;
 - 10 means for storing said maximum grey value determined;
 - means for determining the grey value of the pixel having the minimum grey value among the plurality of pixels received;
 - 15 means for storing said minimum grey value determined;
 - means for setting a grey scale threshold based upon the stored minimum grey value and the stored maximum grey value; and
 - 20 means for comparing the grey value of each pixel of said image to said grey scale threshold to produce a first binary output for each pixel.
2. The apparatus of Claim 1 wherein said setting means is responsive to a user selectable input to set the grey scale threshold between the stored minimum grey value and the stored maximum grey value based upon said user selectable input.
- 25 3. The apparatus of Claim 2 wherein said setting means further comprises:

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means for subtracting the stored minimum grey value from the stored maximum grey value to produce a difference value;

5 means for multiplying said difference value by said user selectable input expressed as a percentage to produce an intermediate value; and

means for summing said intermediate value to said stored minimum grey value to produce said grey scale threshold.

10 4. The apparatus of Claim 1 further comprising means for delaying said pixels prior to being supplied to said comparing means.

15 5. The apparatus of Claim 1 further comprising means for filtering said pixels prior to being supplied to the determining means.

6. The apparatus of Claim 1 wherein each of said determining means determines the grey value of the pixel associated with an edge in the image.

20 7. The apparatus of Claim 1 further comprising:

means for generating a high frequency binary output for each pixel;

25 means for receiving said first binary output and said high frequency binary output; and

means for detecting an edge and for switching the output of said apparatus between said first binary output and said high frequency

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binary output, in response to said edge detected.

8. The apparatus of Claim 7 wherein said means for detecting an edge further comprises:

5 a plurality of different types of edge detecting means, each for generating an output upon the detecting of an edge different from the other;

10 means for receiving the plurality of outputs from the different types of edge detecting means; said receiving means also responsive to a user selectable input for switching the output of said apparatus in response to said user selectable input selecting
15 one of said type of edge detecting means.

9. The apparatus of Claim 1 wherein said plurality of pixels are arranged in a plurality of lines with each line containing a plurality of pixels, and

20 said receiving means receives a plurality of lines of pixels.

10. A method of generating a video binary signal for a video image having a plurality of pixels with each pixel having a grey scale value, said
25 method comprising:

receiving a plurality of pixels;
determining the grey value of the pixel having the maximum grey value among the plurality of pixels received;
30 storing the maximum grey value determined;

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determining the grey value of the pixel having the minimum grey value among the plurality of pixels received;

storing the minimum grey value determined;

5 setting a grey scale threshold based upon the stored minimum grey value and the stored maximum grey value; and

10 comparing the grey value of each pixel of said video image to said grey scale threshold to produce said video binary signal.

11. The method of Claim 10 wherein said setting step further comprises the steps of:

receiving a user input; and

15 generating the grey scale threshold between the stored minimum grey value and the stored maximum grey value based upon the user input.

12. The method of Claim 11 wherein said generating step further comprising:

20 subtracting the stored minimum grey value from the stored maximum grey value to produce a difference value;

 multiplying said difference value by said user selectable input expressed as a percentage to produce an intermediate value; and

25 summing said intermediate value to said stored minimum grey value to produce said grey scale threshold.

13. The method of Claim 10 further comprising:

30 delaying the pixels of the image prior to the comparing step.

- 25 -

14. The method of Claim 10 further comprising:
filtering the pixels prior to the
determining step.

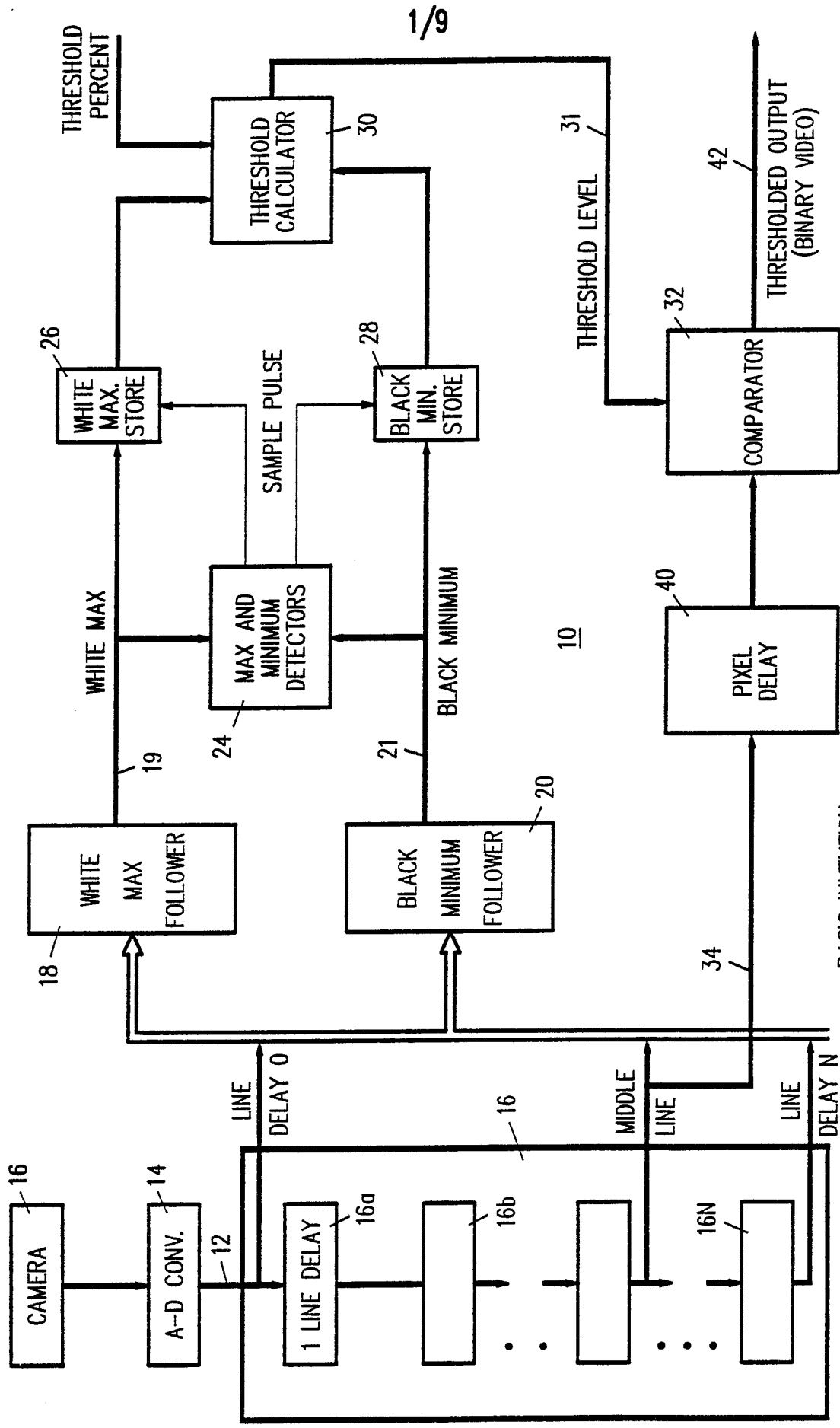
5 15. The method of Claim 10 further comprising:
generating a high frequency binary output
signal for each pixel;
receiving the video binary signal and the
high frequency binary output signal by a
combiner;
10 detecting an edge in said image; and
switching the output of the combiner
between the video binary signal and the high
frequency binary output signal in response to
the edge detected in the image.

15 16. The method of Claim 10 wherein said step
for determining the grey value of the pixel having
the maximum grey value among the plurality of pixels
further comprises:

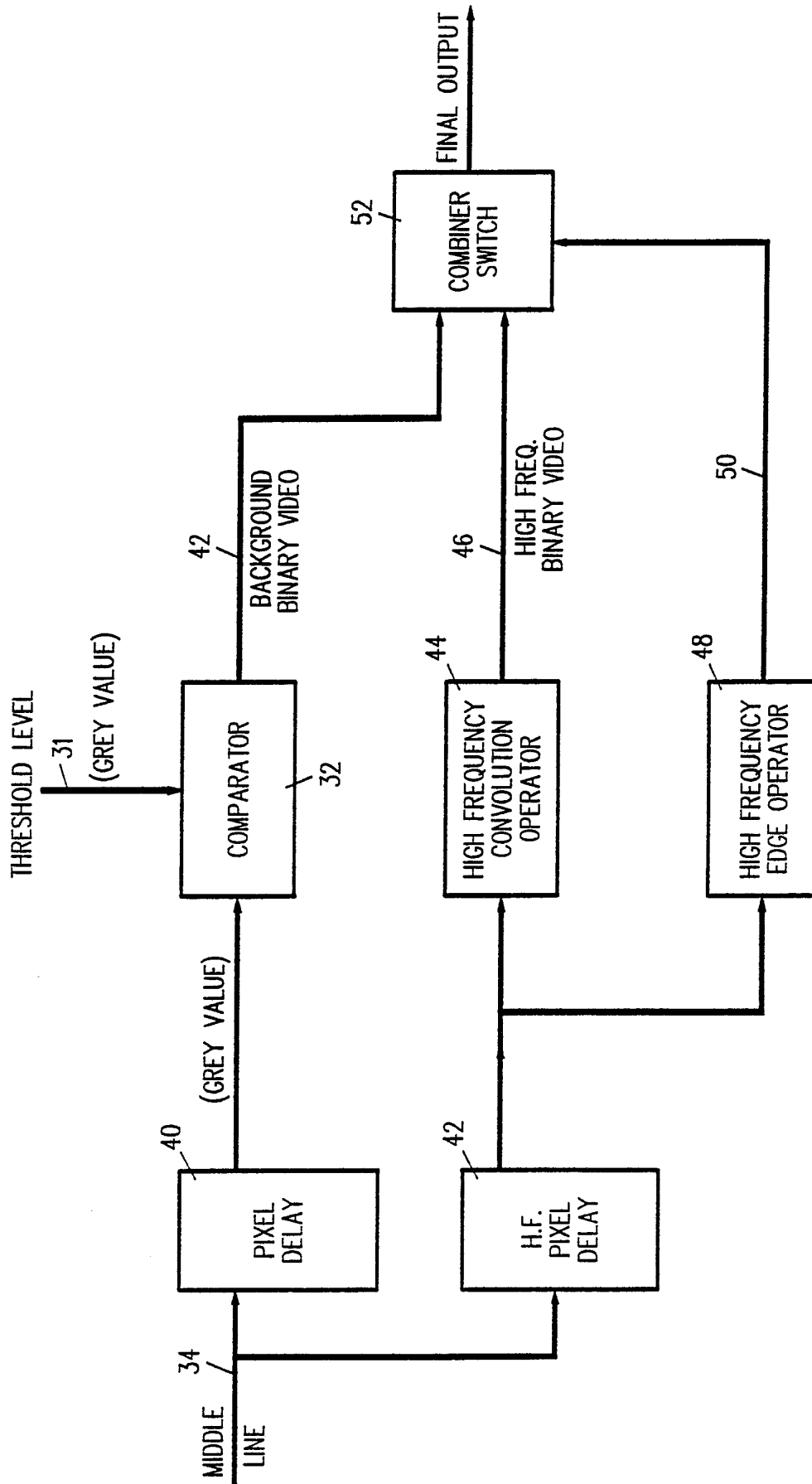
20 analyzing said maximum grey value to
determine if said maximum grey value is
associated with an edge.

25 17. The method of Claim 10 wherein said step
for determining the grey value of the pixel having
the minimum grey value among the plurality of pixels
further comprises:

analyzing said minimum grey value to
determine if said minimum grey value is
associated with an edge.

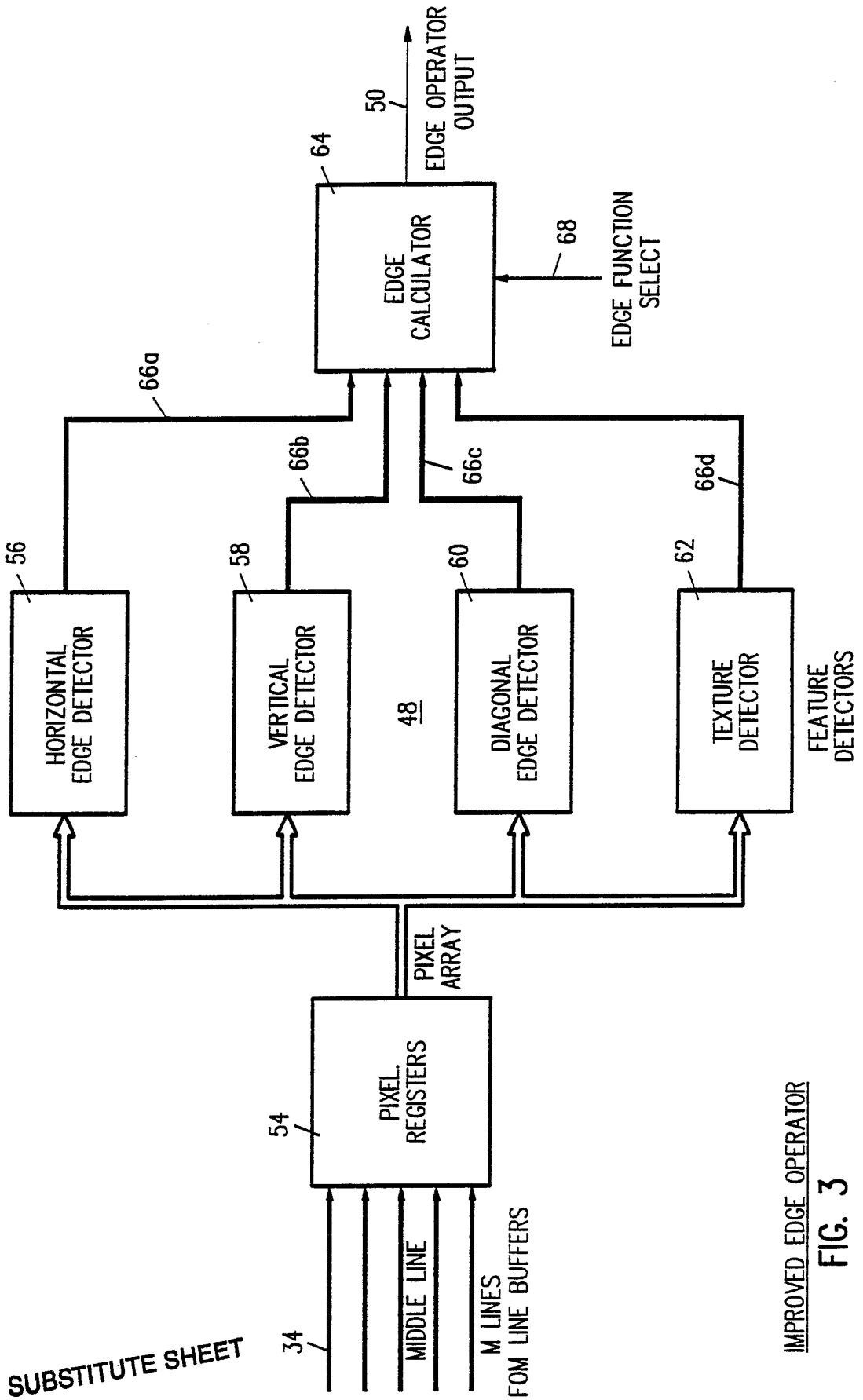


BASIC INVENTION
FIG. 1



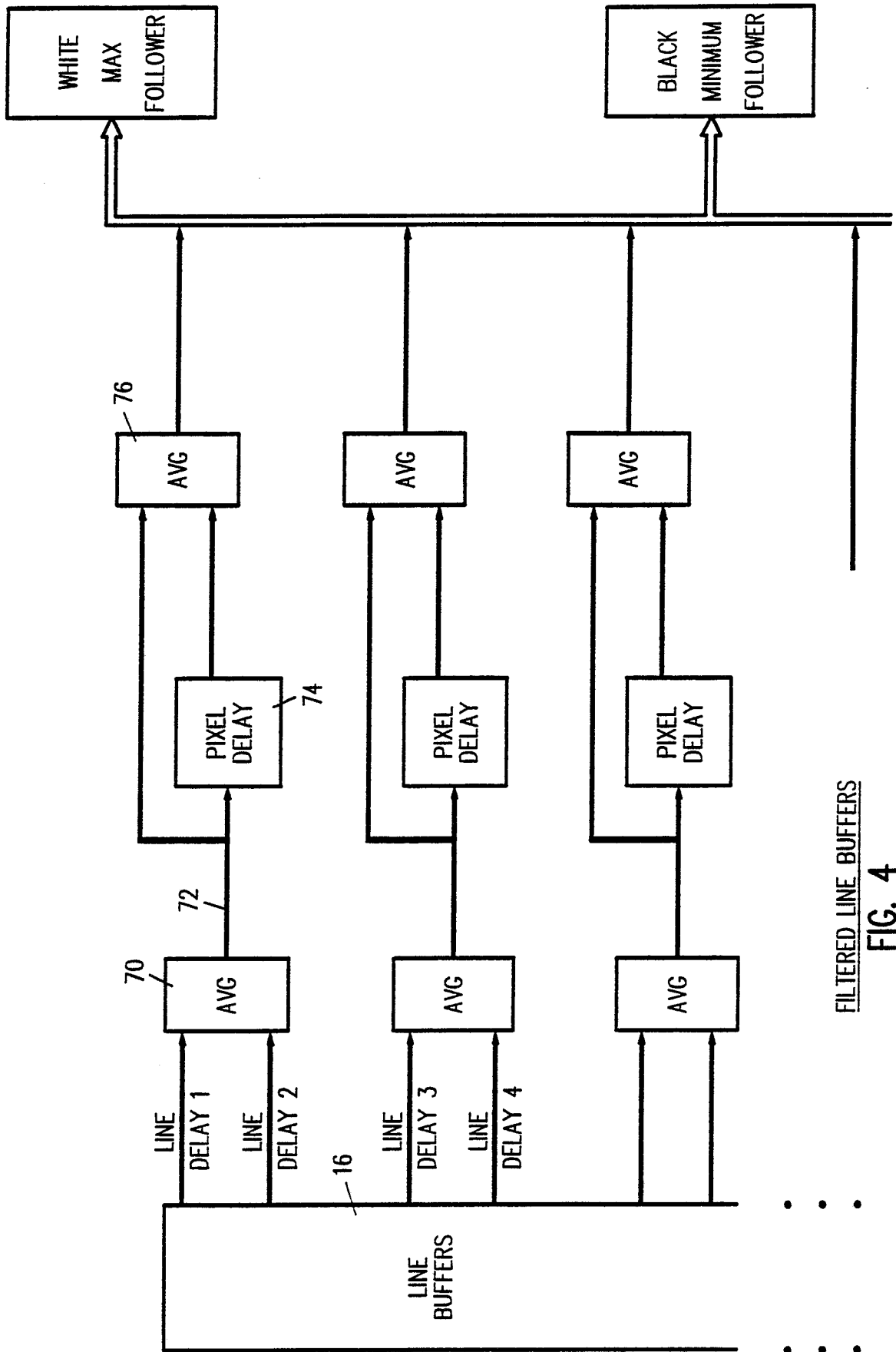
HIGH FREQ. ENHANCEMENT

FIG. 2



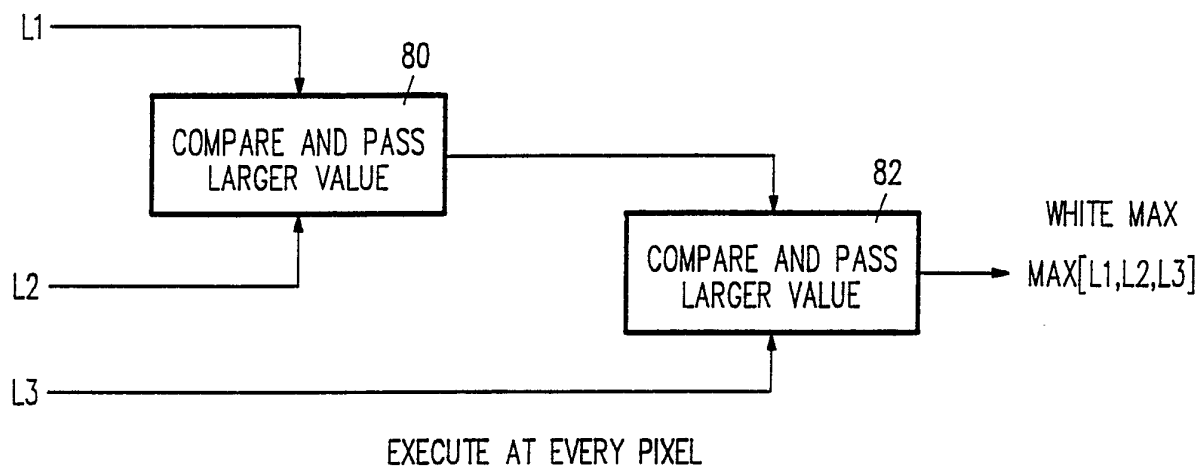
IMPROVED EDGE OPERATOR

FIG. 3

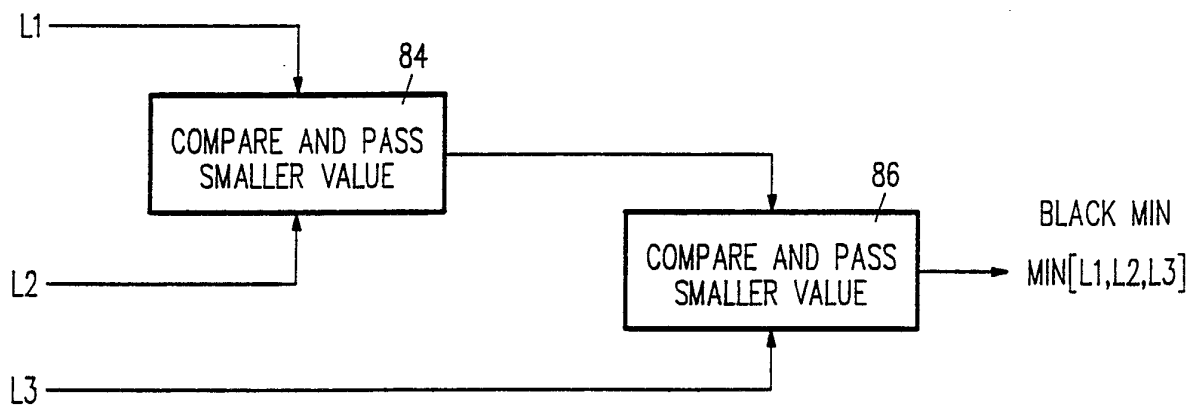


FILTERED LINE BUFFERS

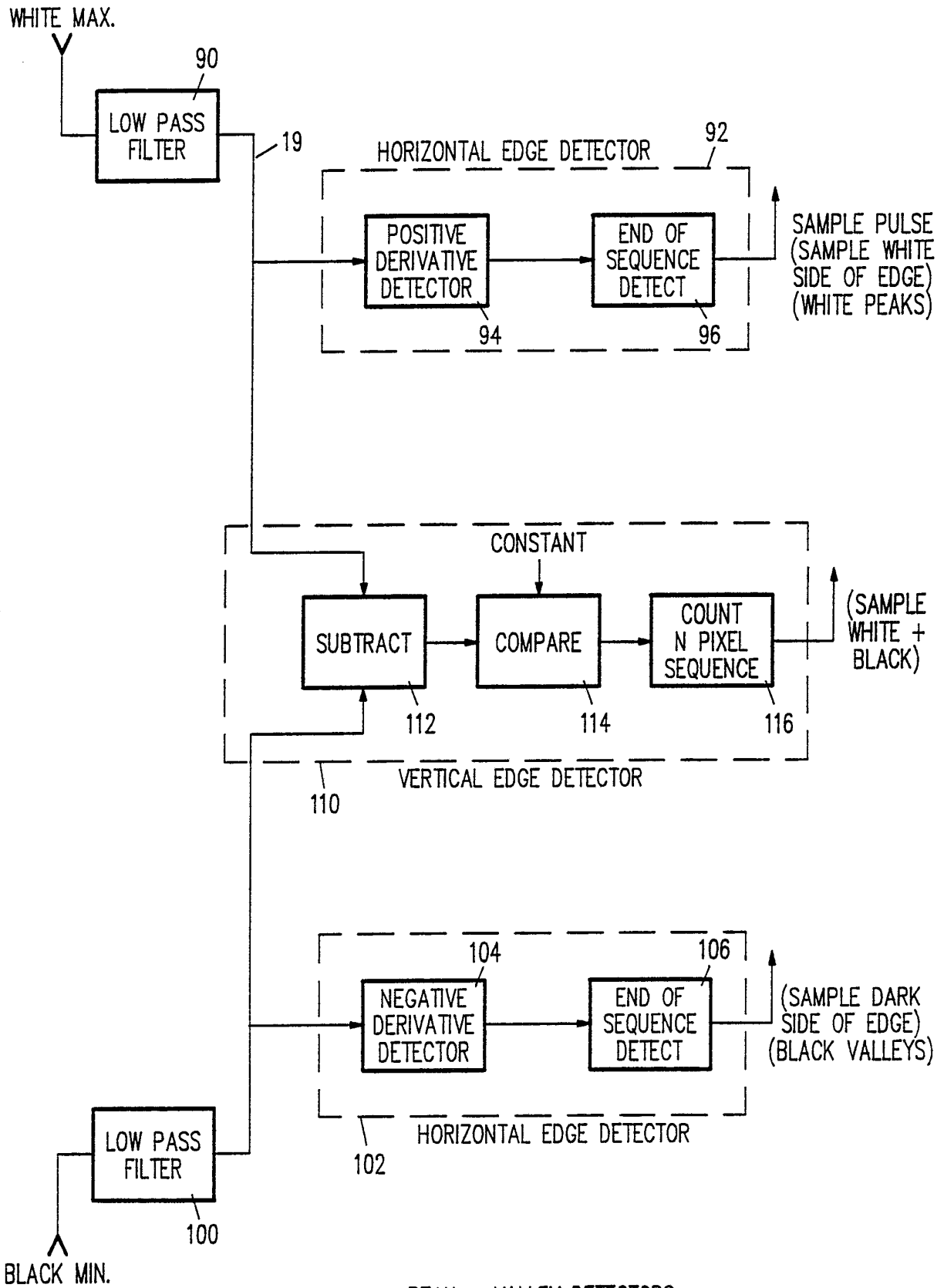
FIG. 4



3 LINE EXAMPLE
FIG. 5a



3 LINE EXAMPLE
FIG. 5b

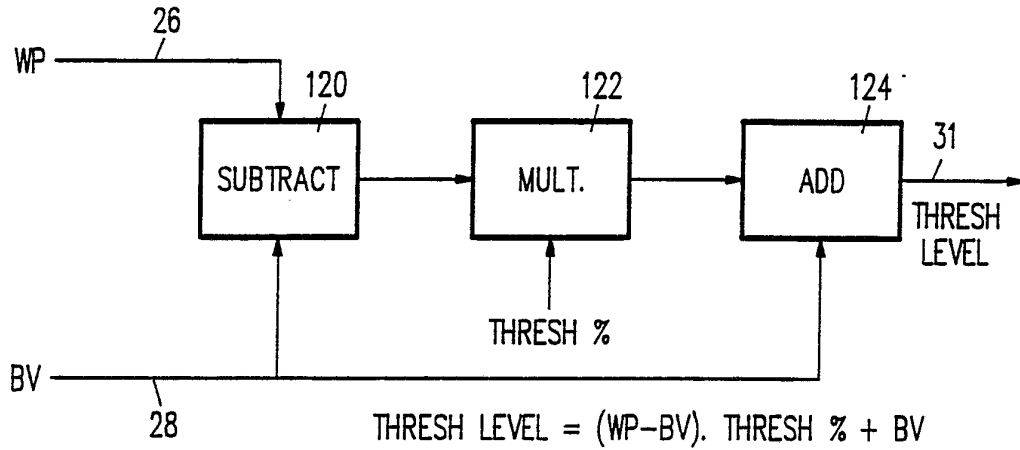


PEAK + VALLEY DETECTORS
ONE IMPLEMENTATION

SUBSTITUTE SHEET

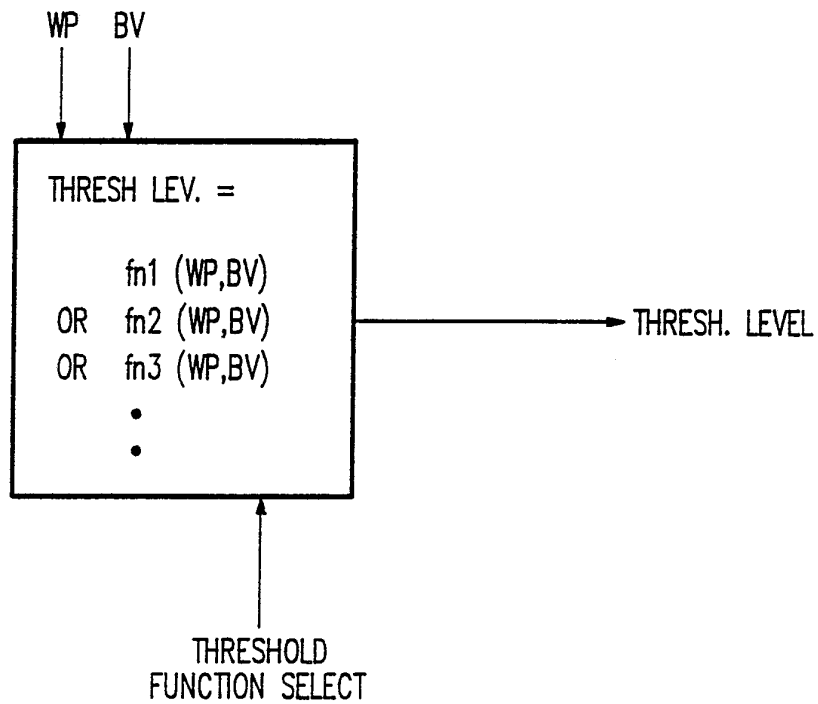
FIG. 5c

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THRESHOLD CALCULATOR
TWO IMPLEMENTATIONS

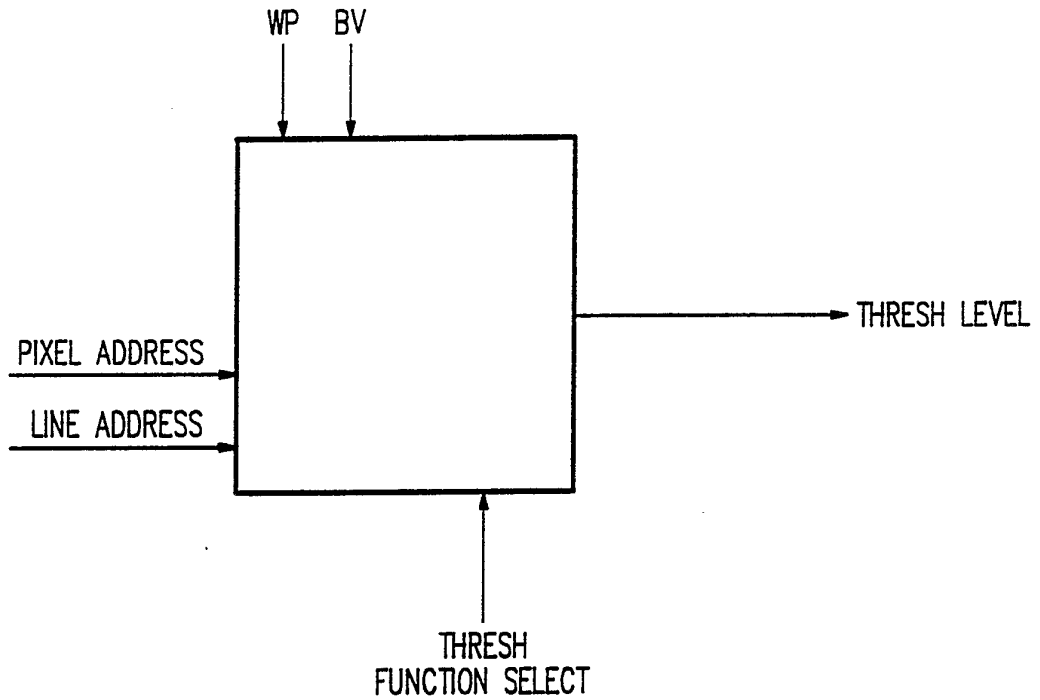
FIG. 5d-1



THRESHOLD CALCULATOR
TWO IMPLEMENTATIONS

FIG. 5d-2

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THRESHOLD CALCULATOR WITH DITHER/HALFTONE

FIG. 5e-1

EX.

WP = 80 % OF F.S.

BV = 30



75	45	65
50	60	35
55	40	70

THRESHOLD CALCULATOR WITH DITHER/HALFTONE

FIG. 5e-2

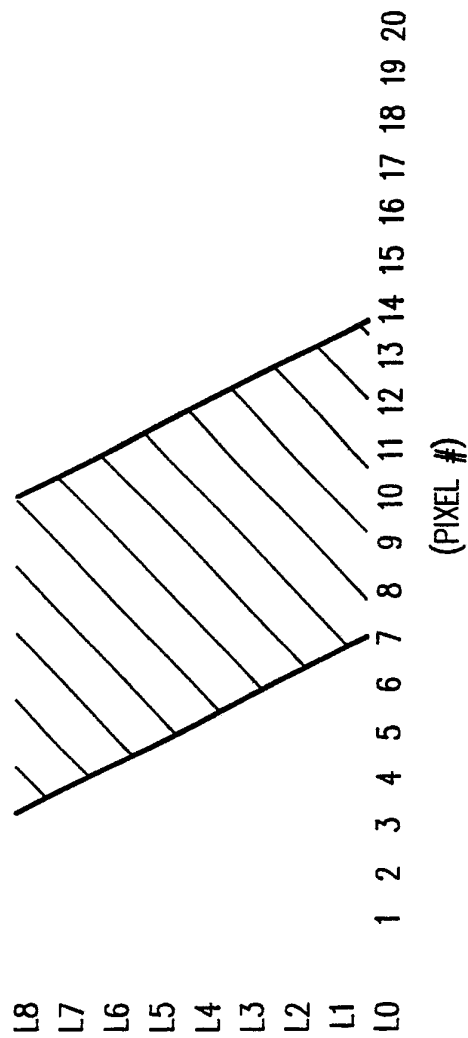
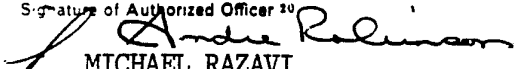


FIG. 6

INTERNATIONAL SEARCH REPORT

International Application No **PCT/US91/06688**

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC IPC(5): G06K 9/48 US.CL: 382/22,50,52; 378/99		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
US	382/22,50,52 378/99	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ^{1,2}		
Category ⁶	Citation of Document, ^{1,2} with indication, where appropriate, of the relevant passages ^{1,2}	Relevant to Claim No. ^{1,2}
X	US, A, 4,501,016 (PERSON ET. AL.) 19 FEBRUARY 1985, See Column 6, lines 22-44 Column 7, lines 10-12, 16-21, Column 11, lines 6-39 and Fig. 2B.	1,4-7,9,10, 13-17
Y	US, A, 4,688,175 (KANEKO ET. AL.) 18 AUGUST 1987 See Column 8, lines 8-21, and Fig. 1	2,3,8,11,12
A	US, A, 4,550,435 (HAYMAN) 29 OCTOBER 1985 See abstract	1-17
A	US, A, 4,910,786 (EICHEL) 20 MARCH 1990 See abstract	1-17
A,P	US, A, 4,969,202 (GROEZINGER) 06 NOVEMBER 1990 See Figs. 1-4	1-17
<p>⁶ Special categories of cited documents: ^{1,2}</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>Δ" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ²	Date of Mailing of this International Search Report ²	
12 DECEMBER 1991	10 JAN 1992	
International Searching Authority ¹	Signature of Authorized Officer ²⁰	
ISA/US	 MICHAEL RAZAVI	