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(71) **Applicant**: **HEWLETT PACKARD ENTERPRISE DEVELOPMENT LP** [US/US]; 11445 Compaq Center Drive West, Houston, TX 77070 (US).

(72) **Inventors**: **BUCHANAN, Brent**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **LAM, Sity**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US). **ZHENG, Le**; 1501 Page Mill Rd., Palo Alto, California 94304-1100 (US).

(74) **Agents**: **PAGAR, Preetam B.** et al.; Hewlett Packard Enterprise, 3404 E. Harmony Road, Mail Stop 79 , Fort Collins, CO 80528 (US).

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(54) **Title**: MEMORY ARRAY WITH BIT-CELLS TO ACCOMMODATE DIFFERENT NUMBERS AND TYPES OF MEMORY ELEMENTS

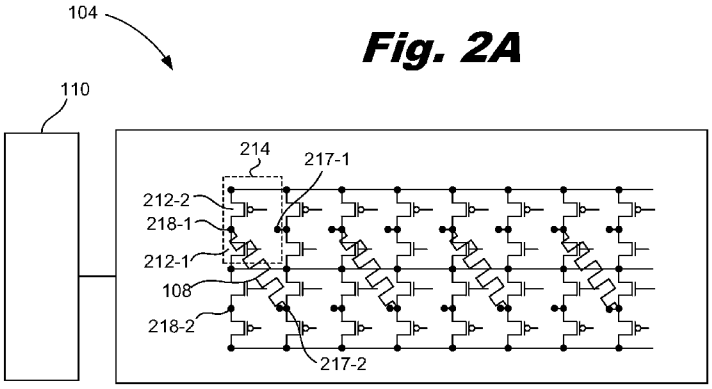

Fig. 2A

(57) **Abstract**: In one example in accordance with the present disclosure a device is described. The device includes a switching array having a number of bit-cells. Each bit-cell has a first node and a second node. The array also includes a number of memory elements, each memory element communicatively coupled to a first node and a second node. The number of memory elements is less than or equal to the number of bit-cells in the switching array. The device also includes an addressing circuit for addressing any number of memory elements. The switching array accommodates different numbers and different types of memory elements and different types of addressing circuits.

MEMORY ARRAY WITH BIT-CELLS TO ACCOMMODATE DIFFERENT NUMBERS AND TYPES OF MEMORY ELEMENTS

BACKGROUND

[0001] Memory arrays may be made up of memory elements of various sizes and shapes. A switching array that includes transistors, logic gates, electrical circuit components and the like is used to read information from the memory elements of the memory array and to write information to the memory elements of the memory array.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The accompanying drawings illustrate various examples of the principles described herein and are a part of the specification. The illustrated examples are given merely for illustration, and do not limit the scope of the claims.

[0003] Fig. 1 is a diagram of an electronic device including a switching array to accommodate different numbers and types of memory elements, according to one example of the principles described herein.

[0004] Figs. 2A and 2B are diagrams of a switching array with two switching elements per bit-cell to accommodate different numbers and types of memory elements, according to one example of the principles described herein.

[0005] Fig. 3 is a flowchart of a method for establishing a switching array to accommodate different numbers and types of memory elements, according to one example of the principles described herein.

[0006] Figs. 4A and 4B are diagrams of a set path and reset path for a switching array with two switching elements per bit-cell, according to one example of the principles described herein.

[0007] Throughout the drawings, identical reference numbers designate similar, but not necessarily identical, elements.

DETAILED DESCRIPTION

[0008] A variety of memory elements are used in everyday computing devices. The different memory elements serve different purposes. Some are intended to operate on low power while others are intended to be used with higher voltage levels. The different memory elements may be of differing quality based on the processes used to form the memory element. For example, more reliable memory elements may incorporate more complex and costly manufacturing operations while other memory elements may be formed of cheaper raw materials and less-costly procedures, which may result in a less reliable memory element. Which memory element is used for a particular application may be based on the characteristics of the application. For example, one application may utilize a highly reliable memory element and the application may justify the additional cost of such a highly reliable memory element. By comparison, a different application may not justify the cost and a less reliable memory element may suffice.

[0009] The different memory elements have different physical and operational characteristics. For example, different sized memory elements may have different read/write latencies as well as different voltage operation levels. As a specific example large memory elements operate at a higher voltage level as compared to smaller memory elements, but these larger memory elements may have a larger read/write latency. The different memory elements also differ in cost and time to produce with smaller, quicker, and more efficient memory elements costing more and taking more time to produce. In yet another example of a characteristic that may differ among memory elements is a failure

rate, with a memory element having a lower failure rate being more expensive and potentially more advantageously marketed.

[0010] To use an array of memory elements, a switching array that includes switching elements such as logic gates, transistors, or other electronic circuitry is used to address and access the memory elements. Specifically, the memory elements are coupled to sensory signal control lines that pass currents or voltages to the memory elements to either read information from the memory elements or write information to the memory elements.

[0011] While such memory arrays are beneficial for storing information, some characteristics impede their more widespread use. For example, a switching array for a memory array may be specific to the type of memory element and addressing circuit used in the application. Accordingly, a specialized switching array and addressing circuit is formed for each type of memory array. Such a customized switching array adds to the overall cost of production of a memory array.

[0012] The systems and methods of the present specification and appended claims address this and other issues. Specifically, the present application describes a memory array that includes a switching array that accommodates different numbers and different types of memory elements. The memory array also includes an addressing circuit that addresses a number of memory elements that is less than the number of bit-cells in the memory array.

[0013] The present specification describes a memory array. The memory array includes a switching array including a number of bit-cells. Each bit-cell has a first node and a second node. The memory array also includes a number of memory elements. The memory elements are coupled to a first node and a second node of the switching array. In the memory array, the number of memory elements is less than or equal to the number of bit-cells in the switching array. The memory array also includes an addressing circuit for addressing any number of memory elements. In the memory array, the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits.

[0014] The present specification describes a method. According to the method, a switching array that includes a number of bit-cells is provided. Each bit-cell has a first node and a second node and the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits. According to the method, a number of memory elements are provided. The number of memory elements in the memory array is less than the number of bit-cells in the switching array. The memory elements are coupled to a first node and a second node of the switching array. At least one memory element is addressed by identifying a location of a first node or a second node corresponding to the at least one memory element and nodes that do not have a corresponding memory element are not addressed.

[0015] The present specification describes a device that includes a processor and a memory array coupled to the processor. The memory array includes a switching array with a number of bit-cells. Each bit-cell has a first node and a second node. A number of memory elements of the device are coupled to a first node and a second node. The number of memory elements in the device is less than or equal to the number of bit-cells in the switching array and the number of memory elements are cross bit-cell memory elements. The device also includes an addressing circuit selected based on the switching array and the number of memory elements. In the device, the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits.

[0016] The array and device of the present specification allow for a single switching array to be formed to accommodate the different sizes and types of memory elements present. In accommodating different sizes and types of memory elements, the device and array include an addressing circuit that addresses the memory elements, regardless of how many memory elements are placed on the switching array. In a specific example, the addressing circuit may accommodate any sub-population scheme of the memory array. Such a multi-configurable switching array may reduce the cost of memory array

fabrication as one switching array can be used in different applications with different numbers and different types of memory elements.

[0017] Certain examples of the present disclosure are directed to a system and method for forming memory arrays that provides a number of advantages not previously offered including 1) providing a switching array that can be used with different configurations of different numbers and different types of memory elements; 2) reduce cost and waste of memory array manufacture; and 3) remove limitation of bit-cell size in selection of memory element usage; 4) increase volume production of switching arrays; and 5) reduce cost of memory array testing. However, it is contemplated that the devices and methods disclosed herein may prove useful in addressing other deficiencies in a number of technical areas. Therefore the systems and devices disclosed herein should not be construed as addressing just the particular elements or deficiencies discussed herein.

[0018] As used in the present specification and in the appended claims, the term "type" of memory element may refer to a memory element's size, shape, functionality, or a variety of the memory element. For example, one type of memory element may be larger than another. In another example, a memristor may be one variety of a memory element and an erasable programmable read-only memory (EPROM) may be another variety of memory element.

[0019] Still further, as used in the present specification and in the appended claims, the term "type" of addressing circuit may refer to an addressing circuit that corresponds to a type and number of memory element. For example one type of addressing circuit may accommodate a certain number of memristor memory elements and another type of addressing circuit may accommodate a different number of memristor memory elements. Still further, another type of addressing circuit may correspond to a certain number of EPROM memory elements.

[0020] Even further, as used in the present specification and in the appended claims, the term "a number of" or similar language is meant to be

understood broadly as any positive number including 1 to infinity; zero not being a number, but the absence of a number.

[0021] In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present systems and methods. It will be apparent, however, to one skilled in the art that the present apparatus, systems, and methods may be practiced without these specific details. Reference in the specification to "an example" or similar language indicates that a particular feature, structure, or characteristic described in connection with that example is included as described, but may not be included in other examples.

[0022] Fig. 1 is a diagram of an electronic device (100) including a switching array (106) to accommodate different numbers and types of memory elements (108), according to one example of the principles described herein. An electronic device (100) may be any device that is capable of executing data processing operations. Examples of electronic devices (100) include laptop computers, personal digital assistants (PDAs), mobile devices, notebooks, tablets, gaming systems, smartphones, mobile devices, printers such as laser printers, copiers, scanners, fax machines and other electronic devices.

[0023] To achieve its desired functionality, the electronic device (100) includes various hardware components. Specifically, the electronic device (100) includes a processor (102) and a memory array (104) coupled to the processor (102). Although the following description refers to a single processor (102) and a single memory array (104), the descriptions may also apply to an electronic device (100) with multiple processors and multiple memory arrays.

[0024] The processor (102) may include the hardware architecture to retrieve executable code from a machine-readable storage medium and execute the executable code. For example, the processor (102) may be a number of central processing units (CPUs), microprocessors, and/or other hardware devices suitable for retrieval and execution of instructions stored in machine-readable storage medium. The executable code may, when executed by the processor (102), cause the processor (102) to implement at least the functionality of managing the memory array (104), such as reading information from and writing

information to the memory array (104). In the course of executing code, the processor (102) may receive input from and provide output to a number of the remaining hardware units.

[0025] In the electronic device (100), the processor (102) may fetch, decode, and execute instructions to execute any one of the operations in the methods described in Fig. 3. As an alternative or in addition to retrieving and executing instructions, the processor (102) may include a number of electronic circuits including a number of electronic components for performing the functionality of a number of the instructions in the machine-readable storage medium.

[0026] The electronic device (100) may include a memory array (104) to store information. For example, the memory array (104) includes a number of memory elements (108) which individually store information. For example the memory elements may be binary in that they can represent either a logical “0” or a logical “1” value. The memory elements (108) may be of any variety that responds to voltages and/or currents. For example, different voltages and currents may be passed to the memory elements (108) to change a characteristic of the memory element (108) such that it indicates a different logic value.

[0027] For example, the memory element (108) may be a resistive memory element (108) such as a memristor that indicates a logic value based on its resistance. A resistance of a memristor may change as an applied voltage or current greater than a threshold value is passed to the memristor. In some examples, the memory elements (108) may be polarized meaning that a memory element (108) may receive a signal (i.e., voltage or current) in two directions, which different directions of signal may either set the memory element (108) to a low-resistance state or a high-resistance state.

[0028] While specific reference is made to a memristor memory element (108), the memory element (108) may be of any variety, such as phase change random-access memory (PCRAM), resistive random-access memory (RRAM), magnetoresistive random-access memory (MRAM), erasable programmable read-only memory (EPROM), and electrically erasable programmable read-only

memory (EEPROM), among other types of memory that are writable and readable with a controllable voltage and/or current. As the memory element (108) may be of different varieties and manufactured using different processes, the characteristics such as the size and shape of the memory element (108) may also vary. As will be described below, the switching array (106) of the memory array (104) may accommodate various sizes, as well as numbers, of memory elements (108).

[0029] The memory array (104) also includes a switching array (106). The switching array (106) may be used to access a desired memory element (108). In other words, the switching array (106) may include elements that selectively pass an electrical signal (i.e., a current or a voltage). Examples of such elements include transistors, logic gates, diodes, capacitors, relays, and combinations thereof among other signal-passing elements. In passing the electrical signals, the elements of the switching array (106) may be turned on or off by the processor (102) to provide a voltage difference across a memory element (108). In one example, the voltage difference may be greater than a threshold voltage for the memory element (108) and may accordingly change the logical value indicated by the memory element (108). Such processes may be referred to as setting a memory element (108) and resetting a memory element (108).

[0030] The switching elements of the switching array (106) may also be used for reading and writing information to the memory elements (108). For example, the switching array (106) includes control lines that are coupled to the processor (102). To read information from, and write information to, the memory elements (108) a sensing signal is passed along these control lines and the switching elements are turned on or off to allow the sensing signal to pass to a corresponding memory element (108). As the sensing signal passes through the memory elements (108) an output signal may be detected, which output signal is indicative of the state of the particular memory element (108). Another example of an operation that may be carried out on the memory elements (108) by the switching array (106) is memory element (108) formation. During

formation a large sensing signal is passed to set the memory element (108) permanently in a particular state.

[0031] The memory array (104) also includes an addressing circuit (110) that is used to identify the different memory elements (108) within the memory array (104). The addressing circuit (110) may include hardware components that receive a signal from the processor (102) and identify and isolate the desired memory element (108). In some examples, the addressing circuit (110) may accommodate different numbers and types of memory elements (108) disposed in the memory array (104).

[0032] Figs. 2A and 2B are diagrams of a memory array (Fig. 1, 106) with two switching elements (212-1, 212-2) per bit-cell (214) to accommodate different numbers and types of memory elements (108), according to one example of the principles described herein. In the examples of Figs. 2A and 2B the memory element (108) is depicted as a memristor, however as described above, the memory element (108) may be any variety of memory element (108) such as PRAM, MRAM, RRAM, EPROM, or EEPROM. Moreover, while Figs. 2A and 2B depict switching elements (212-1, 212-2) as transistors, the switching elements (212-1, 212-2) may be capacitors, diodes, logic gates or other control circuitry.

[0033] The switching array may include a number of bit-cells (214), each bit-cell (214) having a first node (218) and a second node (217). As used in the present specification reference numbers with a "-*" indicate a specific instance of an element. For example, (217-1) and (218-1) reference specific instances of nodes. By comparison, reference numbers without the "-*" refer to the element generically. For example, (217) and (218) refer to generic nodes and not specific nodes. The nodes (217, 218) are places where a memory element (108) may attach. Some nodes (217, 218) may be populated, meaning there is a corresponding memory element (108) coupled thereto. Other nodes (217, 218) may be unpopulated, meaning there is not a corresponding memory element (108) coupled thereto. In other words, the switching array (Fig. 1, 106) and the memory array (104) may be sub-populated.

[0034] For simplicity a few instances of a bit-cell (214), switching elements (212), memory element (108), first node (218), and second node (217) are referenced with a reference numeral. The first node (218) and second node (217) may be referred to as a top electrode and a bottom electrode. In Fig. 2A and the other figures a "-*" indicates another instance of a similar element. For example, 217-1 is an example of a second node in a first bit-cell and 217-2 is an example of a second node in a second bit cell. Similarly, 218-1 is a first node in a first bit-cell and 218-2 is an example of a first node in a second bit-cell. The memory elements (108) of the memory array (104) are coupled to a first node (218) and a second node (217). For example, as depicted in Fig. 2A, a memory element (108) may be coupled to a first node (218-1) in one bit-cell (214) and coupled to a second node (217-2) of a different bit-cell. While Figs. 2A and 2B depict a memory array (108) with a certain number of these elements, a memory array (104) may include any number of these components.

[0035] As described above, in some examples each bit-cell (214) may include two switching elements (212-1, 212-2), such as two transistors. Such a switching array (Fig. 1, 106) architecture may be referred to as a 2-transistor 1-resistor (2T1R) architecture. Figs. 2A and 2B depict a generally linear arrangement of the bit-cells (214), however any number of rows or any number of arrangement of the bit-cells (214) may be implemented in accordance with the principles described herein.

[0036] In the memory array (104), the number of memory elements (108), i.e., memristors in the memory array (104) may be less than the number of bit-cells (214) in the memory array (104). In other words, the switching array (Fig 1, 106) may be sub-populated with memory elements (108). While Figs. 2A and 2B describe a particular sub-population of the memory array (104), any sub-population scheme may be employed in accordance with the principles described herein. The sub-population scheme may be selected based on the types and characteristics of the memory elements (108). For example, larger memristors may prevent the full population of the memory array (104). Accordingly, memristors may be placed on the array in a grid-like pattern, with every other bit-cell (214) being unpopulated as shown in a first row of Figs. 2A

and 2B. Note however, that the switching array (106) may still allow for fully populating, or sub-populating, the switching array (106) in any fashion. In other words, the switching array (Fig. 1, 106) used in the sub-populated memory array (Fig. 1, 104) may be the same switching array (Fig. 1, 106) as used in a fully-populated memory array (Fig. 1, 104).

[0037] Accommodating both a fully-populated and sub-populated memory array (104) may be beneficial as the switching array (Fig. 1, 106) can accommodate memory elements (108) of different sizes without tying the type of memory element (108) used to the size of the corresponding bit-cell (214). In other words, the switching array (Fig. 1, 106) accommodates different numbers and different types of memory elements (108). For example, the switching array (Fig. 1, 106) may allow for smaller memristors to be placed at one density and the placement of larger memristors (216) at a lighter density. As shown in Fig. 2B, the use of larger memristors may also rely on larger straps (220). Doing so may allow for a base switching array (Fig. 1, 106) to be formed and used in different memory applications.

[0038] To accommodate the sub-populated memory array (104) and a single switching array (Fig. 1, 106) that supports various memory elements (108), the memory array (104) includes an addressing circuit (110) for addressing the number of memory elements (108) and avoiding addressing spaces in the switching array (Fig. 1, 106) that do not contain memory elements (108).

[0039] As will be described in connection with Figs. 4A and 4B, the addressing circuit (110) may accommodate any configuration and any number of memristors in a memristor array (104). For example, while Fig. 2A depicts memristors in every other column, the addressing circuit (110) may accommodate memristors spaced 2 columns away from one another.

[0040] As depicted in Figs. 2A and 2B, one memristor end, may be coupled to two switching elements (212-1, 212-2) of a first bit-cell (214) at a node (218-1) and at the other end, may be coupled to two switching elements (212-1, 212-2) of a second bit-cell (214) at a node (217-2).

[0041] Each of the switching elements (212-1, 212-2) of a bit-cell (214) may be coupled to different control lines (not shown) such that each switching element (212-1, 212-2) is individually-controlled and individually turned on or off. Specifically, as depicted in Fig. 2A, the second switching element (212-2) is depicted as a positive-channel field-effect transistor (PFET) and the first switching component (212-1) is depicted as a negative-channel field-effect transistor (NFET), although other types/polarity of switching elements (212) may be used (e.g., including the use of first and second switching elements (212-1, 212-2) having the same polarity or no polarity). The first switching element (212-1) may be switched on and off by an input to the gate of the first switching element (212-1). Similarly, the second switching element (212-2) may be switched on and off by an input to the gate of the second switching element (212-2). Such inputs may be controlled by the addressing circuit (110) that also provides the various voltages and/or current signals through the switching elements (212) and the memory element (108). As depicted in Fig. 2A and 2B, the first bit-cell (214), to which the first node (218-1) is connected is in a different row than the second bit-cell (214) to which the second node (217-2) is connected. Such a configuration where a memory element (108) is coupled to a first node (218-1) in a first bit-cell (214) and to a second node (217-2) in a second bit-cell (214) in another row may be referred to as a cross bit-cell memory element (108).

[0042] Using a cross bit-cell memory element (108) as depicted in Figs. 2A and 2B may allow for a sub-populated 2T1R switching array (Fig. 1, 106). The sub-populated 2T1R architecture may allow for larger memristors, or memristors with different characteristics to be used with a switching array (Fig. 1, 106) that may also be fully populated with memory elements (108). In other words, the switching array (Fig. 1, 106) of Figs 2A and 2B may be sub-populated or may be fully-populated. Even though sub-populated, the switching array (Fig. 1, 106) may still be used due to an addressing circuit (110) that accommodates the number and type of memory elements (108).

[0043] As depicted in Fig. 2B, at least one node of adjacent bit-cells (214) are communicatively coupled to one another. For example, a first node (218-1)

may be shared by adjacent bit-cells as indicated by the line (222-2). In another example, a second node (217-2) may be shared by adjacent bit-cells as indicated by the line (222-1). In this example, as adjacent bit-cells (214) share nodes, i.e., a first bit-cell shares a second node with an adjacent second bit-cell, the corresponding memory elements of the first bit-cell and second bit-cell may be of alternating polarity.

[0044] Fig. 3 is a flowchart of a method (300) for establishing a switching array (Fig. 1, 106) to accommodate different numbers and types of memory elements (Fig. 1, 108), according to one example of the principles described herein. The method includes providing (block 301) a switching array (Fig. 1, 106) that includes a number of bit-cells (Fig. 2, 214). The switching array (Fig. 1, 106) may include one, two or other number of switching elements (Fig. 2, 212). For example, the switching array (Fig. 1, 106) may include one switching transistor or two switching transistors. The provided switching array (Fig. 1, 106) may accommodate different types and number of memory elements (Fig. 1, 108) and may accommodate different types of addressing circuits (Fig. 1, 110). For example, in one product, the switching array (Fig. 1, 106) may be partially populated with memory elements (Fig. 1, 108) as indicated in Fig. 2A and in another product may be fully populated with memory elements (Fig. 1, 108).

[0045] Each bit-cell (Fig. 2, 214) in the switching array (Fig. 1, 106) includes a first node (Fig. 2, 218) and a second node (Fig. 2, 217) and in the method (300) a number of memory elements (Fig. 1, 108) are provided (block 302) and coupled to first nodes (Fig. 2, 218) and second nodes (Fig. 2, 218). In some examples, a memory element (Fig. 1, 108) is coupled to a first node (Fig. 2, 218) and a second node (Fig. 2, 217) of the same bit-cell (Fig. 2, 214) and in other examples the memory element (Fig. 1, 108) is coupled to a first node (Fig. 2, 218-1) of one bit-cell (Fig. 2, 214) and a second node (Fig. 2, 217-2) of another bit-cell (Fig. 2, 214). The number of memory elements (Fig. 1, 108) that are provided (block 302) is less than or equal to the number of bit-cells (Fig. 2, 214) in the provided (block 301) switching array (Fig. 1, 106) such that the switching array (Fig. 1, 106) is sub-populated or fully-populated. As used in the

present specification and in the appended claims, a sub-populated switching array (Fig. 1, 106) may be an array where less than all of the first nodes (Fig. 2, 218) and second nodes (Fig. 2, 217) are coupled to memory elements (Fig. 1, 108).

[0046] A target memory element (Fig. 1, 108) of the memory array (Fig. 1, 104) is addressed (block 303) by identifying a location of a first node (Fig. 2, 218) or a second node (Fig. 2, 217) corresponding to the at least one memory element (Fig. 1, 108) and nodes (Fig. 2, 217, 218) that do not have a corresponding memory element (Fig. 1, 108) are avoided being addressed (block 304). For example, as will be described in Figs. 4A and 4B, an address of a first node (Fig. 2, 218) may be used during a set operation and an address of a second node (Fig. 2, 217) may be used during a reset operation. The method of Fig. 3 may allow for sub-populated memory arrays (Fig. 1, 104) to be formed using the same switching arrays (Fig. 1, 106) as used in a fully-populated memory array (Fig. 1, 104). Using the addressing circuit (Fig. 1, 110) described herein, populated bit-cells (Fig. 2, 214) are addressed while unpopulated bit-cells (Fig. 2, 214) are avoided being addressed. Such addressing of sub-populated memory arrays (Fig. 1, 104) is not known in the field.

[0047] Figs. 4A and 4B are diagrams of a set path (424-1) and reset path (424-2) for a switching array (Fig. 1, 106) with two switching elements (Fig. 2, 212) per bit-cell (Fig. 2, 214), according to one example of the principles described herein. Specifically, Fig. 4A illustrates a setting of a memory element (108). In this example, the first switching elements (Fig. 2, 212-1) of the different bit-cells (Fig. 2, 214) may be of a different type from the second switching elements (Fig. 2, 212-2) of the same bit-cells (Fig. 2, 214). For example, a second switching element (Fig. 2, 212-2) may be a PFET and the first switching element (Fig. 2, 212-1) may be an NFET. In setting the particular memory element (108), a set voltage is applied to a first control line (426-1) and a second control line (426-2) is set to ground. In this example, a third control line (426-3) is inactive. At the same time all of the second switching elements (Fig. 2, 212-2) (PFET) for the first column are activated and the first switching

elements (Fig. 2, 212-1) (NFET) of the second column are activated such that the current path is through the second switching element (Fig. 2, 212-2) of a bit-cell (Fig. 2, 214) in the first column through the memory element (108), and through the first switching element (Fig. 2, 212-2) of a bit-cell (Fig. 2, 214) in the second column to the second control line (426-2).

[0048] Fig. 4A also indicates an addressing (428-1) used during a set operation. Specifically, Fig. 4A depicts a row addressing from a processor (Fig. 1, 102) to the memory array (Fig. 1, 104). During an operation one row is active or 'hot' at a given time. Accordingly, an 8-bit binary bus from the processor (Fig. 1, 102) may pass into a one-hot to one-hot line mapper as indicated in Fig. 4A. Note that for a column address each input may activate two output lines.

[0049] By comparison, during a reset operation, a reset voltage is applied to the third control line (426-3) and the second control line (426-2) is set to ground. In this example, the first control line (426-1) is inactive. At the same time, all of the second switching elements (Fig. 2, 212-2) (PFET) of the second column are turned on and all of the first switching elements (Fig. 2, 212-1) (NFET) in the first column are activated such that the current path is through the second switching element (Fig. 2, 212-2) of a bit-cell (Fig. 2, 214) in the second column through the memory element (108), and through the first switching element (Fig. 2, 212-1) of a bit-cell (Fig. 2, 214) in the first column to the second control line (426-2). In other words, in this example, the cross-bit-cell memory element has a set address and a reset address that are distinct from one another. While specific reference is made to particular set and reset paths, the different paths may be established relative to the orientation of the polarity of the memory element. Moreover, while specific reference is made to set and reset current paths. Other paths may be established for other operations such as read and write operations.

[0050] Fig. 4B also indicates an addressing (428-2) used during a reset operation. Specifically, Fig. 4B depicts a row addressing from a processor (Fig. 1, 102) to the memory array (Fig. 1, 104). During an operation one row is active or 'hot' at a given time. Accordingly, an 8-bit binary bus from the processor (Fig.

1, 102) may pass into a one-hot to one-hot line mapper as indicated in Fig. 4B. Note that for a column address each input may activate two output lines.

[0051] As described above, the addressing as depicted in Fig. 4A and 4B may be used with any number of sub-population schemes.

[0052] Certain examples of the present disclosure are directed to a system and method for managing power of an electronic device that provides a number of advantages not previously offered including 1) providing a switching array that can be used with different configurations of different numbers and different types of memory elements; 2) reduce cost and waste of memory array manufacture; and 3) remove limitation of bit-cell size in selection of memory element usage; 4) increase volume production of switching arrays; and 5) reduce cost of memory array testing. However, it is contemplated that the devices and methods disclosed herein may prove useful in addressing other deficiencies in a number of technical areas. Therefore the systems and devices disclosed herein should not be construed as addressing just the particular elements or deficiencies discussed herein.

[0053] The preceding description has been presented to illustrate and describe examples of the principles described. This description is not intended to be exhaustive or to limit these principles to any precise form disclosed. Many modifications and variations are possible in light of the above teaching.

CLAIMS

WHAT IS CLAIMED IS:

1. A device comprising:

a switching array comprising a number of bit-cells, each bit-cell having a first node and a second node;

a number of memory elements, each memory element communicatively coupled to a first node and a second node, wherein the number of memory elements is less than or equal to the number of bit-cells in the switching array; and

an addressing circuit for addressing any number of memory elements;

wherein the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits.

2. The device of claim 1, wherein the number of memory elements are polarized.

3. The device of claim 1, wherein a bit-cell comprises two switching elements.

4. The device of claim 1, wherein a memory element is coupled to a first node and a second node of a same bit-cell.

5. The device of claim 1, wherein a memory element is:

coupled to a first node of a first bit-cell; and

coupled to a second node of a second bit-cell.

6. The device of claim 5, wherein the first bit-cell and the second bit-cell are in different rows of the switching array.

7. A method comprising:

providing a switching array comprising a number of bit-cells, each bit-cell having a first node and a second node, wherein the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits;

providing a number of memory elements coupled to first nodes and second nodes of the switching array, wherein the number of memory elements is less than the number of bit-cells;

addressing a memory element by identifying a location of a first node or a second node corresponding to the memory element; and

avoiding addressing nodes that do not have a corresponding memory element.

8. The method of claim 7, further comprising identifying which bit-cells do not have corresponding memory elements.

9. The method of claim 7, further comprising dropping a least significant bit from an address of a memory element.

10. The method of claim 7, wherein addressing the memory element further comprises addressing the memory element during a set operation using a bit-cell address of a corresponding first node and addressing the memory element during a reset operation using a bit-cell address of a corresponding second node.

11. A device comprising:

a processor; and

a memory array coupled to the processor, the memory array comprising:

a switching array comprising a number of bit-cells, each bit-cell having a first node and a second node;

a number of memory elements coupled to a first node and a second node, wherein:

the number of memory elements is less than or equal to the number of bit-cells in the switching array; and

the number of memory elements are cross bit cell memory elements; and

an addressing circuit selected based on the switching array and the number of memory elements;

wherein the switching array accommodates different numbers and different types of memory elements and different types of addressing circuits.

12. The computing device of claim 11, wherein a first bit-cell and a second bit-cell to which the cross bit-cell memory element is coupled are in different rows of the switching array.

13. The computing device of claim 11, wherein:

the cross-bit-cell memory element has a set address and a reset address; and

the reset address is distinct from the set address.

14. The device of claim 11, wherein the bit-cells comprise two switching elements.

15. The computing device of claim 11, wherein one node of adjacent bit-cells are communicatively coupled to one another.

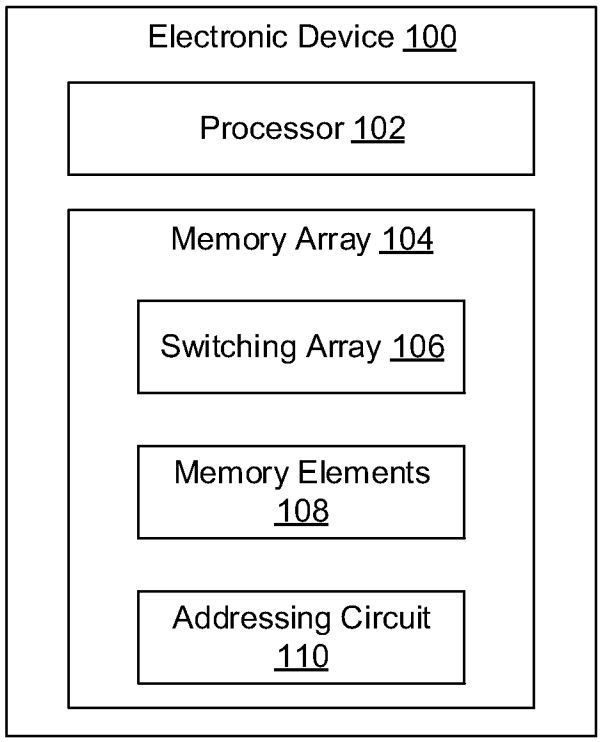
Electronic Device 100
Processor 102
Memory Array 104
Switching Array 106
Memory Elements 108
Addressing Circuit 110

Fig. 1

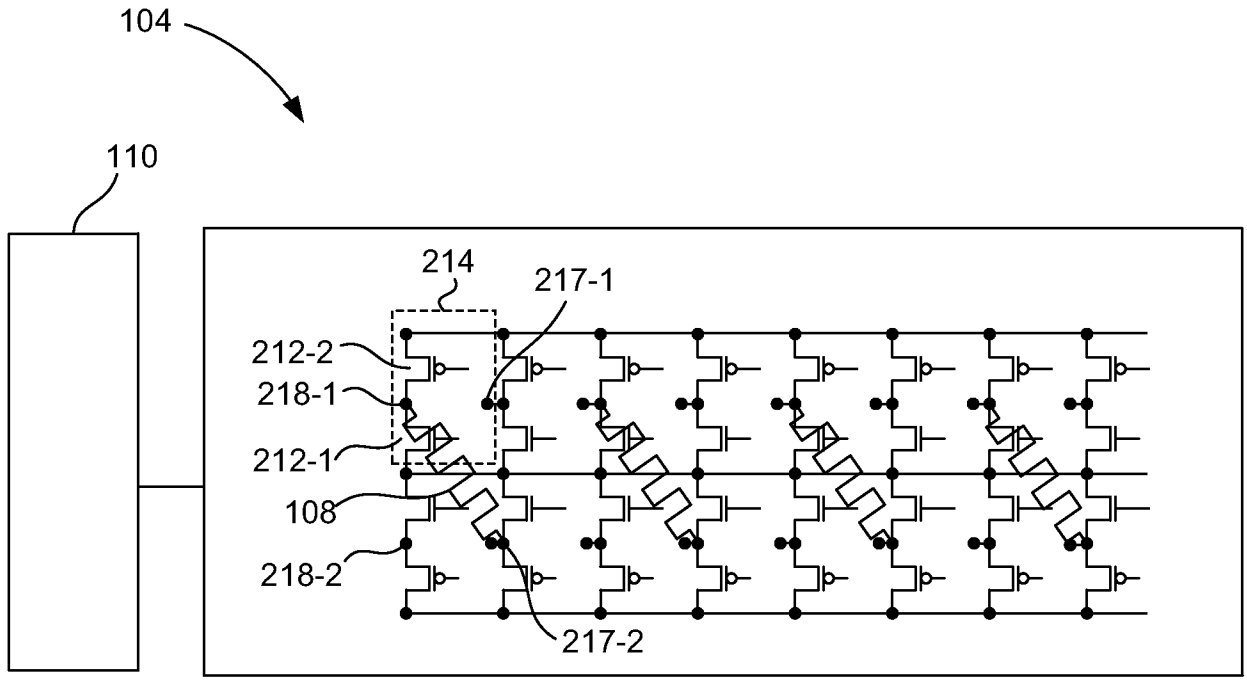
104
110
214
217-1
212-2
218-1
212-1
108
218-2
217-2

Fig. 2A

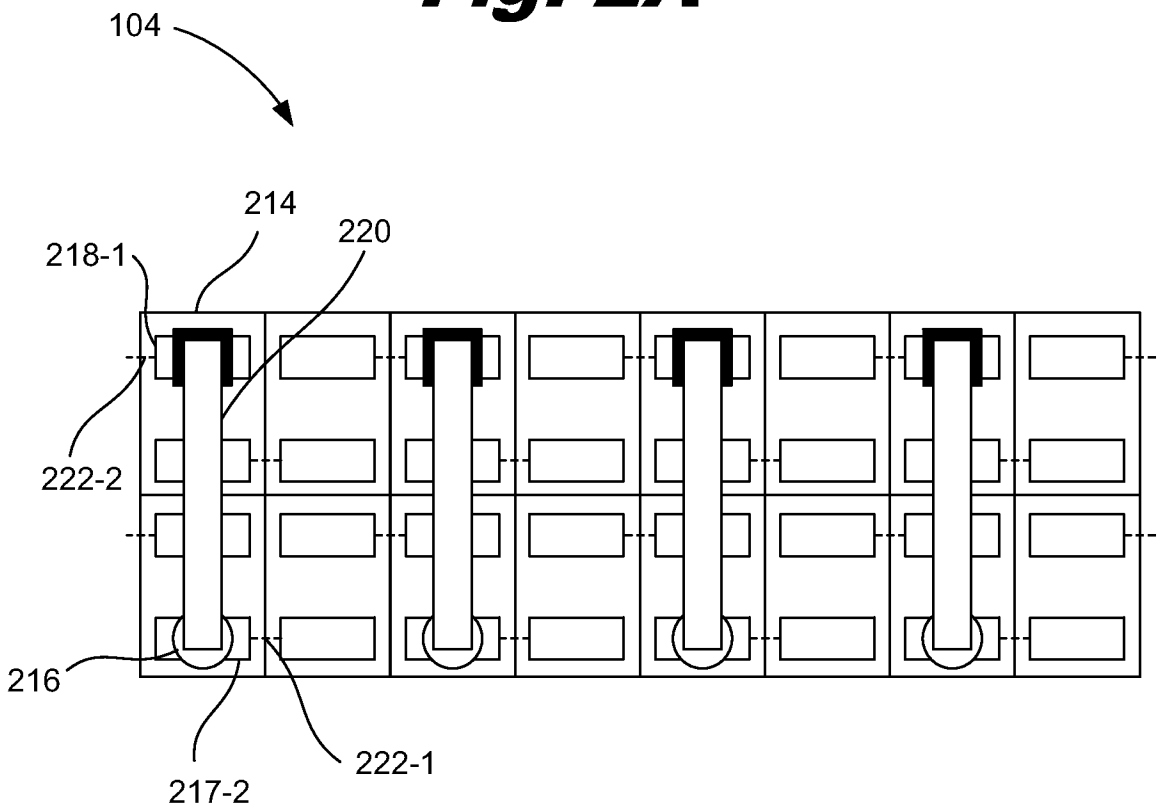
104
214
220
218-1
222-2
216
217-2
222-1

Fig. 2B

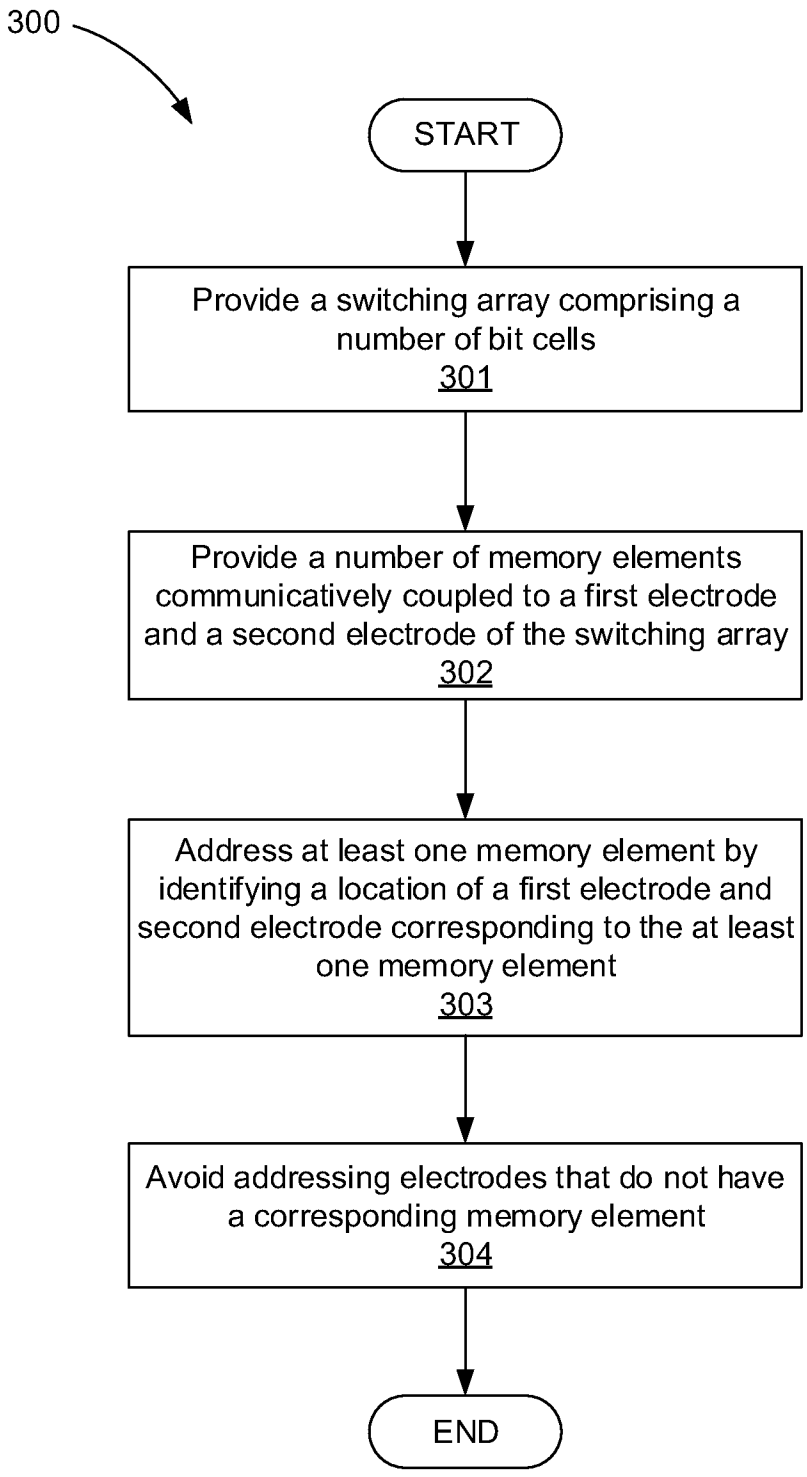
300
START
Provide a switching array comprising a number of bit cells
301
Provide a number of memory elements communicatively coupled to a first electrode and a second electrode of the switching array
302
Address at least one memory element by identifying a location of a first electrode and second electrode corresponding to the at least one memory element
303
Avoid addressing electrodes that do not have a corresponding memory element
304
END

Fig. 3

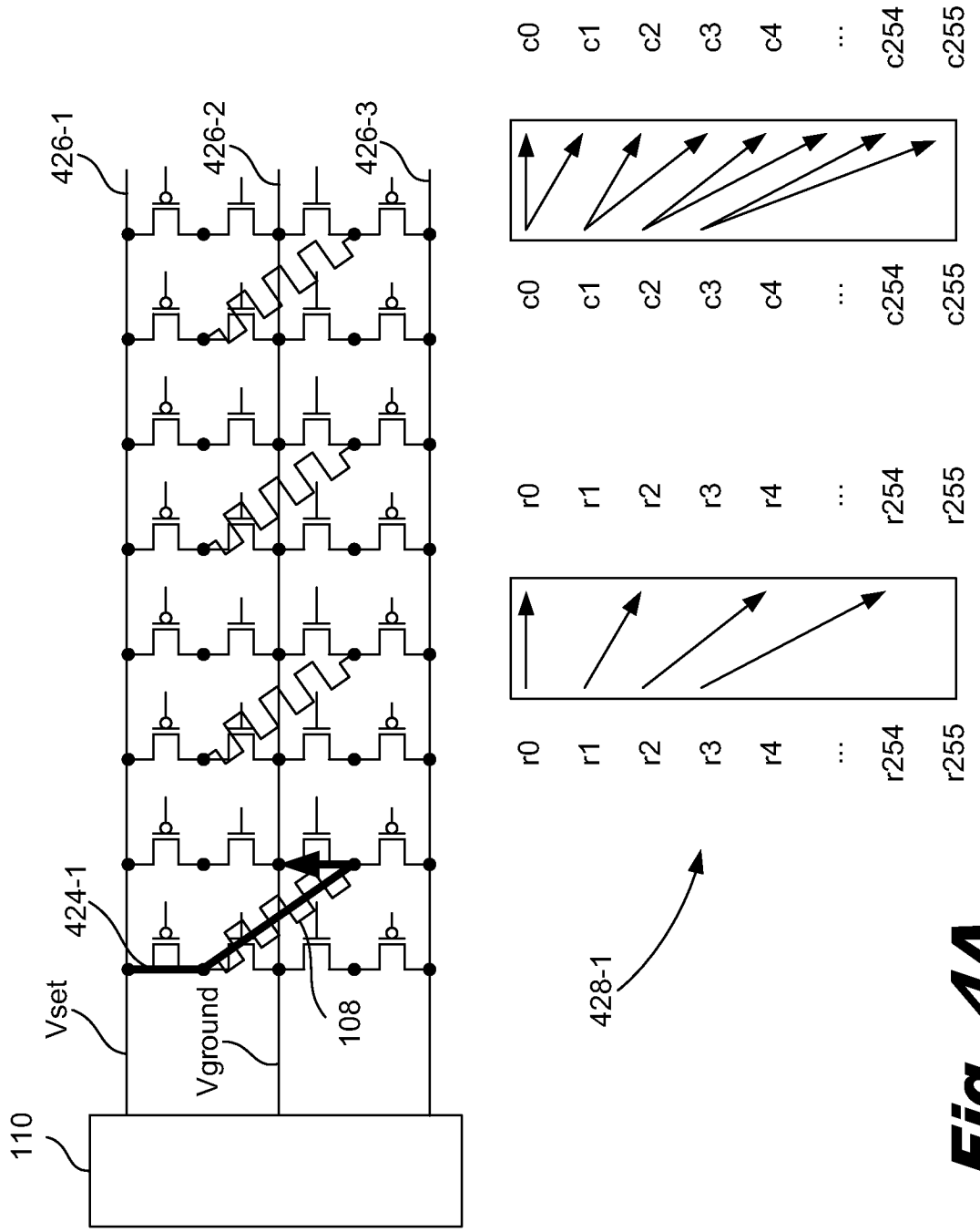
426-1
426-2
426-3
424-1
Vset
Vground
108
110
428-1
r0
r1
r2
r3
r4
...
r254
r255
c0
c1
c2
c3
c4
...
c254
c255

Fig. 4A

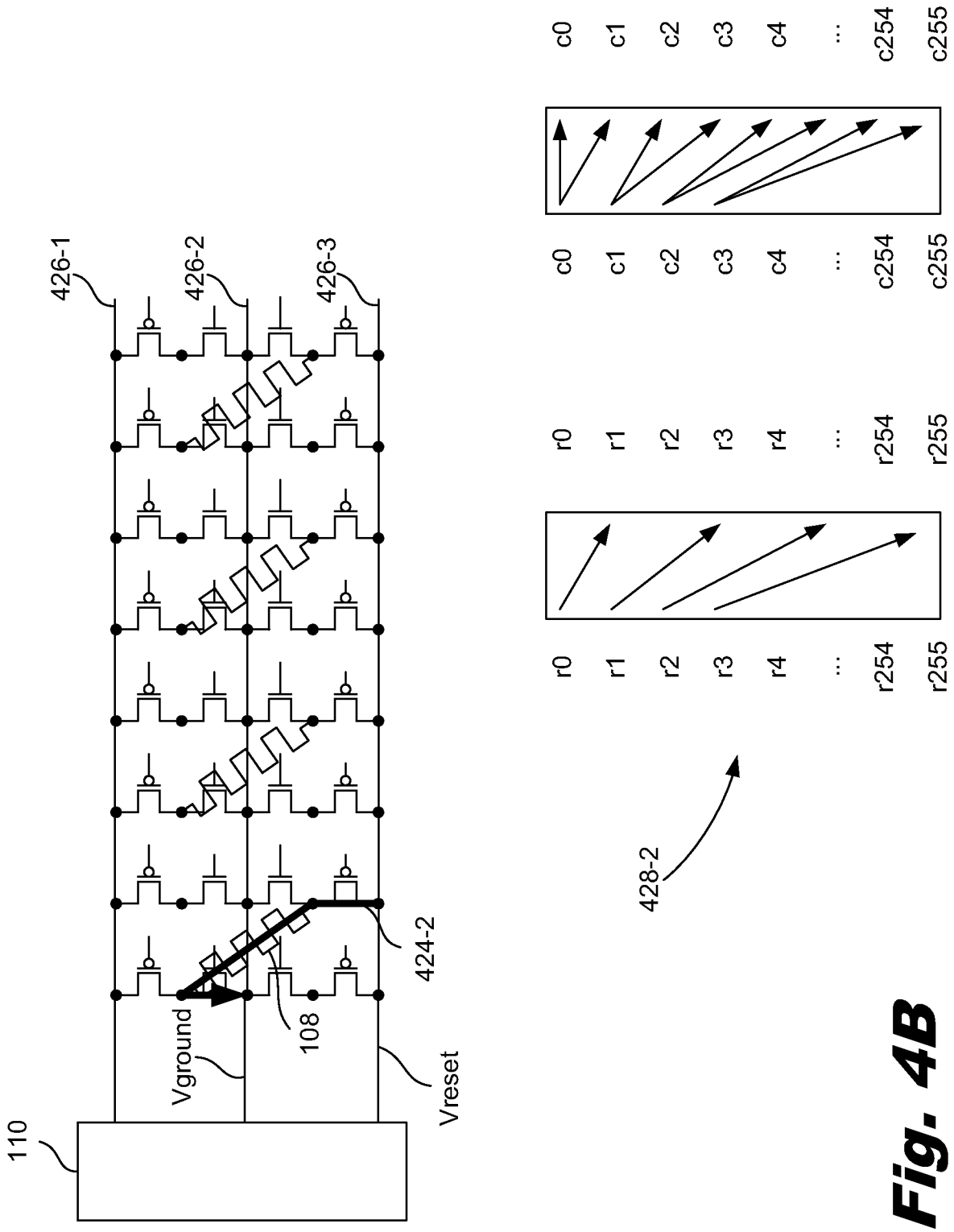
426-1
426-2
426-3
424-2
108
Vground
Vreset
110
428-2
r0
r1
r2
r3
r4
...
r254
r255
c0
c1
c2
c3
c4
...
c254
c255

Fig. 4B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/039711

A. CLASSIFICATION OF SUBJECT MATTER

G11C 7/10(2006.01)i, G11C 8/06(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G11C 7/10; G11C 5/06; H01L 29/82; G11C 11/15; G11C 11/00; G11C 13/00; G11C 8/06

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: switching, array, cross, bit-cell, first, second, node, element, coupled, addressing, circuit, memory

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0069534 A1 (TSUNEO INABA) 24 March 2011 See paragraphs [0075], [0112]-[0115]; and figures 1, 20.	1-6
A		7-15
Y	US 2010-0072530 A1 (RYOUSUKE TAKIZAWA et al.) 25 March 2010 See paragraphs [0037], [0076], [0078]; and figures 1, 13.	1-6
A	US 2014-0241051 A1 (SATORU HANZAWA et al.) 28 August 2014 See paragraph [0099]; and figure 26.	1-15
A	US 2004-0257868 A1 (DENNY DUAN-LEE TANG et al.) 23 December 2004 See paragraph [0054]; and figure 10.	1-15
A	US 6606263 B1 (DENNY TANG) 12 August 2003 See column 4, lines 63-67; column 5, lines 1-8; and figure 4.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
02 May 2016 (02.05.2016)	**03 May 2016 (03.05.2016)**

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
BYUN, Sung Cheal
Telephone No. +82-42-481-8262

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/039711

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		US 6885577 B2	26/04/2005
US 6606263 B1	12/08/2003	None	